Optocoupler Isolation Circuits
for Intelligent Power Modules (IPM) and Gate Drivers

Application Note 5401

Introduction

An IPM (*smart, intelligent* or *integrated* power module) combines power IGBTs (insulated gate bipolar transistors) and gate drivers into a single compact package. Most IPMs also incorporate functions such as over-temperature detection and over-current sensing to provide fault signal feedback to the microcontroller. In a three-phase switching power conversion application (Fig. 1), a typical IPM incorporates seven gate drivers to drive six IGBTs (three high-side and three low-side) switching the three-phase power, and an additional IGBT for the braking function, to protect phase running from over- or under-voltage on the DC bus. Each gate driver requires a 10 V to 30 V power supply. The emitters of the low-side IGBTs are connected to the DC bus (HV-) as a common reference ground, which allows all low-side gate drivers to share the same power supply, V_{CC_L} - GND1.

Power Supply

In the case of a conventional IPM circuit, the emitter of one high-side IGBT and the collector of one low-side IGBT are connected to form one leg of a three-phase switching circuit. By turning the high-side and low-side IGBTs ON and OFF alternately, the HV DC bus voltage is switched and supplied to the load on the U, V or W phase (each phase vector having a 120-degree difference). With ground connected to the collectors of the low-side IGBTs, the ground of each high-side gate-driver circuit will swing between HV- and HV+. Thus, the ground of each power supply for the high-side IGBT gate-driver circuit must be floating and separated from each of the others.

A more robust solution is to provide three isolated power supplies, each supplying one of the high-side gate-driver circuits. A lower-cost alternative is to use bootstrapping power supplies with individual floating grounds. A bootstrapping power supply can be derived from either the DC bus voltage or from the low-side power supply V_{CC_L}. For a conventional IPM, the input logic and gate driving circuits are integrated in a monolithic IC, the power supply voltage generally ranging from 15 V to 20 V.

Design considerations for IPM power conversion are different than for either small-signal or low voltage digital circuit design, since the IPM's switching power conversion calls for high voltage insulation and common-mode transient rejection.

Safety Insulation

High voltage inverters or power supplies must be compliant with equipment regulatory safety standards such as IEC 60950 for IT (information technology) equipment and IEC 60335 for household appliances. Optocouplers can be used to interface between an MCU (microcontroller) and the IPM, to isolate the MCU from the high voltages within the IPM.

In testing to qualify to these safety standards, a high voltage is usually applied between the low- and high-voltage interfaces of a piece of equipment. Most commonly optocouplers provide the isolation across the low-to-high voltage boundary to meet the safety insulation requirements. Common semiconductor component electrical safety standards applicable to optocouplers include IEC 60747-5-2 and UL 1577. Appropriate optocouplers can be selected based on the equipment safety requirements.

Some of the key parameters of the equipment safety ratings that are required for the selection of optocouplers are working voltage, installation class and insulation level. A reinforced insulation level is usually required for electrical equipment powered from AC line voltage by safety standards for industrial, home, office and IT equipment. In addition to insulation voltage rating, basic insulation parameters including external clearance, creepage and distance-through-insulation (DTI, also referred-to as internal clearance) and comparative tracking index (CTI) are specified by some equipment safety standards. Avago offers a broad range of IPM interface optocouplers in various packages, capable of meeting different insulation requirements.

Table 1. Safety Standard Specifications for Avago IPM optocouplers

Part Number	IEC/EN/DIN EN60747-5-2, V_{IORM} (Vpeak)	UL1577, V_{ISO} (VAC/1 minute)	CSA, V_{ISO} (VAC/1 minute)	Package	Clearance, min. (mm)	Creepage, min. (mm)	DTI, min. (mm)	CTI, min. (Volt)
ACPL-P480	891	3750	3750	Stretched SO6	7	8	0.08	175
ACPL-W456	1140	3750	3750	Stretched SO6	8	8	0.08	175
HCPL-J454-600E	891	3750	3750	Wide lead DIP8	8	8	0.5	175
HCNW4506	1414	5000	5000	Widebody DIP8	9.6	10	1.0	200

Interfacing a Conventional IPM Circuit

Figure 1 shows a diagram of a motor drive circuit between an MCU and IPM. Seven Avago ACPL-W456 digital optocouplers isolate the IPM's seven gate driver inputs (six for the upper and lower IGBTs used in each of the three phases, and one for the brake function). Two Avago HCPL-7840 isolated amplifiers isolate the linear signals that are proportional to two motor phase currents, derived from sampling the voltages across two shunt resistors, which are fed back to the MCU. Four Avago HCPL-817 general-purpose phototransistor optocouplers isolate the fault feedback signals developed by the IPM. All of these optocouplers are compliant to reinforced safety insulation levels, and provide a galvanic isolation boundary between low- and high-voltage circuits.

This conventional IPM uses inverted logic: when the input voltage is high, the IGBT turns off; when the input voltage is low, the IGBT turns on. The ACPL-W456 optocoupler has an open-collector transistor output, which means that prior to the MCU and input side of the IPM being powered up, the optocoupler output logic level is high, which keeps all IGBTs off. Typically both the three high-side floating power supplies V_{CC_UH} / V_{CC_VH} / V_{CC_WH} and low side power supply V_{CC_L} supply 15 V. The IPM driver input is able to operate at 15 V as logic high.

The output-high voltage of the ACPL-W456 can be calculated from:

$$V_{OH} = V_{CC} - I_{OH} \times R_L$$

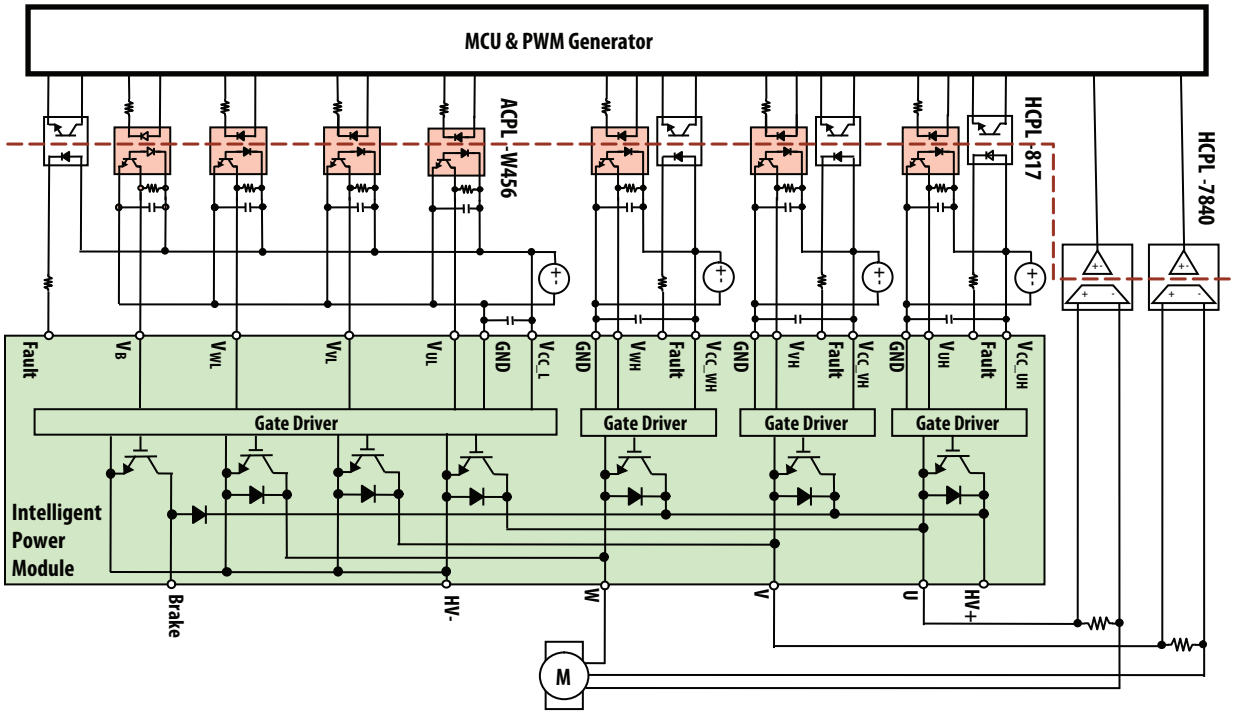

Figure 1. Optocouplers Interfacing IPM in a Motor Drive

Where V_{CC} is the power supply voltage, I_{OH} is the transistor leakage current when output is high, and R_L is the value of the output transistor pull-up resistor.

A moderate pull-up resistor value can be selected to give a sufficiently high V_{OH}, with the capability of driving the IGBT on and off without error in the PWM logic. For example at a maximum 50 μA leakage current, a 20 kΩ pull-up resistor would be appropriate for a 15 V power supply and a 3 kΩ resistor for a 5 V power supply. If the voltage of V_{CC} fluctuates in operation, the *minimum* value of V_{CC} should be used in this calculation.

Interface Gate Drivers

If gate drivers are not integrated into a power module, optocouplers will interface gate drivers as shown in Figure 2. Stand-alone gate drivers have standard digital logic input and high output current, for example 30A a are able to drive very high power motors, up to thousand kilo watts.

When driving a low current IGBT, an economical solution uses a pair of transistors as a buffer instead of an integrated gate driver as shown in Figure 3. The transistor pair could be formed by N-channel and P-channel MOSFETs, or by PNP and NPN transistors. The buffer's current gain should be calculated so that it can amplify the optocoupler output current to drive the IGBT.

Interfacing an IPM Circuit That Incorporates HVICs

IPM development is moving toward integrating HVICs (high-voltage integrated circuits) into gate drive circuits. HVIC technology enables a low-voltage circuit to control high-voltage power devices through a level shifting fabrication process.

As shown in Figure 4, in a HVIC-based IPM, the high-side gate driver output circuits are floating with respect to the IGBTs, hence they are powered by separate bootstrapping power supply V_B. From low to high side, all gate driver input circuits can connect to one power supply V_{CC}, and input logic is compatible with a range of 5 V to 20 V DC. Optocouplers are still required to interface between the MCU and IPM, primarily to provide electrical safety isolation between the low voltage and high voltage circuits. Optocouplers are tested and certified to electrical safety regulations between their input and output pins, while HVICs and IPMs are tested between the molding base and circuit, not from the low voltage to high voltage circuits. This means that if a high voltage punctures the HVIC's level-shifting dielectric layer or junctions, the result is a short circuit between the output and input.

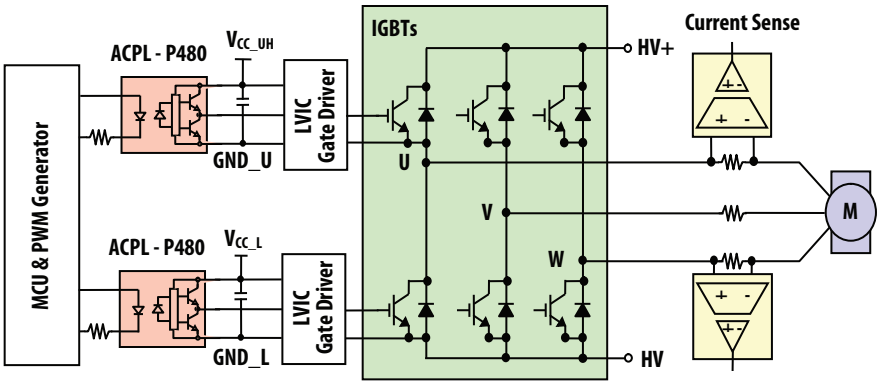

Figure 2. Optocouplers Interfacing LVIC Gate Drivers

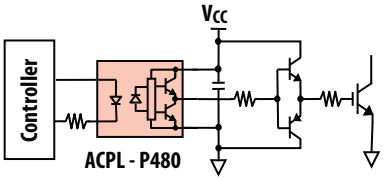

Figure 3. Driving IGBT through Transistor Buffer

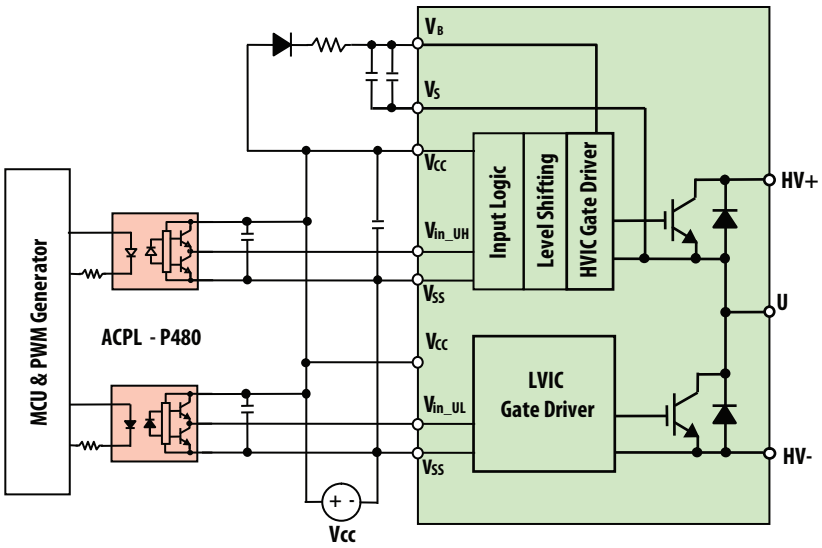

Figure 4. Optocouplers Interface with New Type IPM (Illustrated for one leg connection only)

Optocouplers also prevent transient noise from interfering with the low voltage control circuits during IGBT switching. Looking at the voltage potential at the high side IGBT emitter (point U in Fig. 4), it is swinging between DC bus HV- and HV+ which is usually several hundred or even thousand of volts. The HVIC gate driver power supply V_S is at the same electrical potential as U, and is also swinging on the high voltage bus. Assuming an 800 V DC bus with IGBT V_{CE} rise/fall time of 0.1 μs, this swing will generate a transient voltage of:

$dV/dt = 800V/0.1\mu s = 8\ kV/\mu s$

This transient spike can flood through the gate driver to the MCU controller and disturb the PWM switching signal or damage the microcontroller or IGBT if electrical isolation is not provided.

There is another type of transient noise in a motor drive, as represented by EFT (electrical fast transient) testing. In one procedure for EMC testing according to IEC 60801-4 or IEC 61000-4-4, a high-voltage burst is applied to the motor drive through a capacitive coupling clamp, using a voltage amplitude of up to 2 kV when coupling to signal lines or 4 kV when coupling to power cables. The EFT dV/dt rating is up to hundreds of kV/μs because the pulse rise/fall time is as short as 5 ns, which means that the EFT dV/dt will generate high levels of transient noise into the signal or power lines. If the low voltage signal and high voltage power circuits are not isolated, the transients can interfere with each other and potentially cause a motor drive to fail EFT testing.

Common-mode rejection (CMR) is the maximum slew rate of common-mode voltage (V_{CM}) which can be sustained, while the output remains in the correct logic state. CMR failure results in a glitch on the output as either a positive or negative pulse. This key specification guarantees the reliable transfer of drive information at very high DC-link voltages and fast switching operations. CMR performance is tested on a common-mode voltage V_{CM} between the input and output circuit grounds during a designated V_{CM} rise/fall time Δt. When the output voltage is not disturbed by this transient voltage, then CMR is calculated by CMR = $V_{CM}/\Delta t$. The CMR rating is always related to the amplitude of the voltage difference of V_{CM}: when V_{CM} is increasing, CMR may drastically drop. The Avago ACPL-P480 is specified for a minimum CMR of 20 kV/μs with V_{CM} =1000 V.

The output stage of the ACPL-P480 is a totem-pole transistor pair, which does not require a pull-up resistor and provides very low output impedance between V_{CC} and V_{OUT}, when operating at level high. In the case of an optocoupler with an open-collector transistor output, the impedance between V_{CC} and V_{OUT} is constrained by the pull-up resistor. A totem-pole output provides a good impedance margin interfacing with an IPM if the IPM's input impedance is not excessively high. The ACPL-4800's positive logic can match with positive logic IPMs, which means that when the control-side power supply is not turned on, the IGBTs are kept off.

Figure 5 shows an alternative solution driving IGBTs with stand-alone HVIC gate drivers. The design considerations of optocoupler interface are the same as the circuit of Figure 4, this solution provides a designer a wider selection of IGBT power ratings.

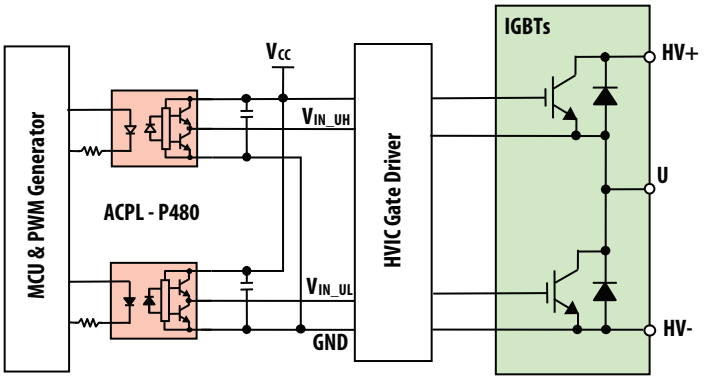

Figure 5. An Optocoupler Interface to HVIC Gate Drivers

Dead Time Control

Pulse-width modulation operates at a constant frequency with the width of the pulse varying. In industrial applications, assuming that the IPM switching frequency is selectable from 5 kHz to 20 kHz, we need to know what is required to ensure that the pulse train will be transmitted without logic errors. To determine the requirements, first we convert the 20 kHz switching speed to its inverse, which is a 50 µs cycle period. If the PWM duty cycle varies from 1 percent to 99 percent, the narrowest pulse, either high or low, represents 1 percent of the cycle period:

t_{MIN} = (1/20 kHz) x 0.01 = 500 ns

The basic rule in accurately transmitting the shortest-possible pulse is that the optocoupler's maximum propagation delay time must be less than t_{MIN} across the operating temperature range. Typically, 2 MBd optocouplers, such as the ACPL-W456, are appropriate.

Since the delay times of optocouplers can be different between channels, any overlap between the ON conditions of the high- and low-channel IGBTs will result in large currents flowing through the devices. To prevent half-bridge IGBTs from shorting through, dead time control is programmed into the MCU. Dead time is the time period during which MCU PWM signals command both the high and low side IGBTs off.

Minimizing dead time in the PWM signals increases the operating efficiency of the motor. This means that the designer must consider the propagation delay characteristics of the optocoupler as well as the characteristics of the IPM IGBT gate-driver circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the IPM IGBT gate-driver circuit can be analyzed in the same way) it is important to know the minimum and maximum turn-on and turn-off propagation delay specifications t_{PLH} / t_{PHL} (as shown in Fig. 4 for the ACPL-P480), preferably over the desired operating temperature range.

The limiting case of zero dead time occurs when the input to the high IGBT turns off at precisely the same time that the input to the low IGBT turns on. This case determines the minimum delay between high channel LED turn-off and low channel LED turn-on, which is related to the worst case optocoupler propagation delay difference. In Fig. 4 both the ACPL-P480 and IPM use positive logic, which means that a minimum dead time of zero is achieved when the signal to turn on the low-channel LED in the optocoupler is delayed by (t_{PHL}[max] - t_{PLH}[min]) from the point where the high-channel LED turns off. Note that in most designs the optocouplers are mounted in close proximity to each other, so it is reasonable to assume that the propagation delays used to calculate PDD are at equal temperatures. Thus the *actual* propagation delays in operation are *not* the same as the t_{PLH} (max) and t_{PHL} (min) specified in the data sheet, since these are the maximum values over the full operating temperature range.

PDD is defined as Propagation Delay Difference (t_{PHL} - t_{PLH}) between any two parts or channels at same operating environment; for example in Figure 4, t_{PHL} is high-channel ACPL-P480 output high-to-low propagation delay and t_{PLH} is low-channel ACPL-P480 output low-to-high propagation delay. The minimum and maximum value of t_{PHL}/t_{PLH} is derived from the spread *at* any discrete temperature within the operating range, so PDD_{MAX} = t_{PHL}(max) - t_{PLH}(min) and PDD_{MIN} = t_{PHL}(min) - t_{PLH}(max). In the case of the ACPL-P480, PDD_{MAX} is specified at 250 ns, PDD_{MIN} is specified at -100 ns at any discrete temperature within the -40° C to +100° C range.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the *maximum* dead time will be. The maximum dead time occurs in the highly unlikely case where the high-channel optocoupler with the fastest t_{PHL} and the low-channel one with the slowest t_{PLH} are in the same inverter leg. In this case the maximum dead time in is represented by the sum of the spread in the t_{PHL} and t_{PLH} propagation delays. The maximum dead time is also equivalent to the difference between the maximum and minimum propagation delay difference PDD specifications.

$$\text{Dead Time}_{MAX} = \text{PDD}_{MAX} - \text{PDD}_{MIN}$$

The maximum dead time (due to the optocouplers) for the ACPL-P480 is 350 ns (= 250 ns – [-100 ns]) over an operating temperature range of -40° C to 100° C.

Summary

To build reliable and robust power conversion circuits, IPM and gate driver interface optocouplers provide electrical safety insulation voltage up to 5000 Vac and common mode noise rejection up to 30 kV/μs, such performance is not available with other isolation circuits. To assure error-free PWM signal transmission, an optocoupler which has a propagation delay time longer than the minimum pulse width of the PWM signal must be used, and the dead time is calculated from the optocoupler's PDD range. Depending on the PWM switching frequency, a data rate from 1 MBd to 5 MBd is required.

Note:
A similar article was first published in June 2008 Power Electronics Technology, written by HE Junhua.

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