BROADCOM®

Data Sheet

ACPL-P480, ACPL-W480, ACPL-4800

High CMR Intelligent Power Module and Gate Drive Interface Optocoupler

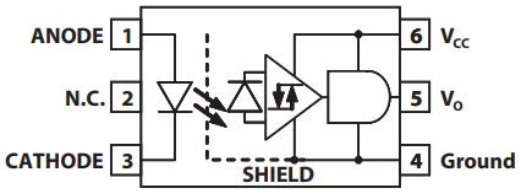
Description

The Broadcom® high-speed ACPL-P480/W480/4800 optocoupler contains an AlGaAs LED, a photo detector, and a Schmitt trigger that eliminates the requirement for external waveform conditioning circuits and the need for a pull-up resistor, which allows for a direct-drive Intelligent Power Module or gate drive. Propagation delay difference between devices has been minimized to maximize inverter efficiency through reduced switching dead time.

Applications

- IPM interface isolation
- Isolated IGBT/MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters
- General digital isolation

Functional Diagram



NOTE: A 0.1-µF bypass capacitor must be connected between pins 4 and 6.

Truth Table (Non-Inverting Logic)

LED	V_O
ON	HIGH
OFF	LOW

Features

- Performance specified for common IPM applications over industrial temperature range
- Short maximum propagation delays
- Minimized pulse width distortion (PWD)
- Very high common mode rejection (CMR)
- Hysteresis
- CMOS output (no pull-up resistor required)
- Available in stretched SO-6 package
- Safety approvals:
  - UL recognized 3750V_{rms} for 1 minute per UL1577
  - CSA approved
  - IEC/EN/DIN EN 60747-5-5 approved with V_{IORM} = 891V_{peak}

Specifications

- Wide operating temperature range: –40°C to 100°C
- Maximum propagation delay t_{PHL}/t_{PLH} = 350 ns
- Maximum pulse width distortion (PWD) = 250 ns
- Propagation delay difference:
  - Minimum: –100 ns
  - Maximum: +250 ns
- Wide operating V_{CC} range: 4.5V to 20V
- 20 kV/µs minimum common mode rejection (CMR) at V_{CM} = 1000V

CAUTION! It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Ordering Information

ACPL-P480, ACPL-W480, and ACPL-4800 are UL Recognized with 5000V_{rms} for 1 minute per UL1577. All part numbers are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option RoHS Compliant	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-P480	-000E	7-mm Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per reel
	-020E		X			100 per tube
	-520E		X	X		1000 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per tube
ACPL-W480	-000E	8-mm Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per reel
	-020E		X			100 per tube
	-520E		X	X		1000 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per tube
ACPL-4800	-000E	300-mil DIP-8				50 per tube
	-300E		X			50 per tube
	-500E		X		X	1000 per tube
	-060E					50 per tube
	-360E		X		X	50 per tube
	-560E		X	X	X	1000 per tube

To order, choose a part number and select the desired options as indicated by the X.

Solder Reflow Profile

The recommended reflow profile is per JEDEC Standard, J-STD-020 (latest revision). Use non-halide flux.

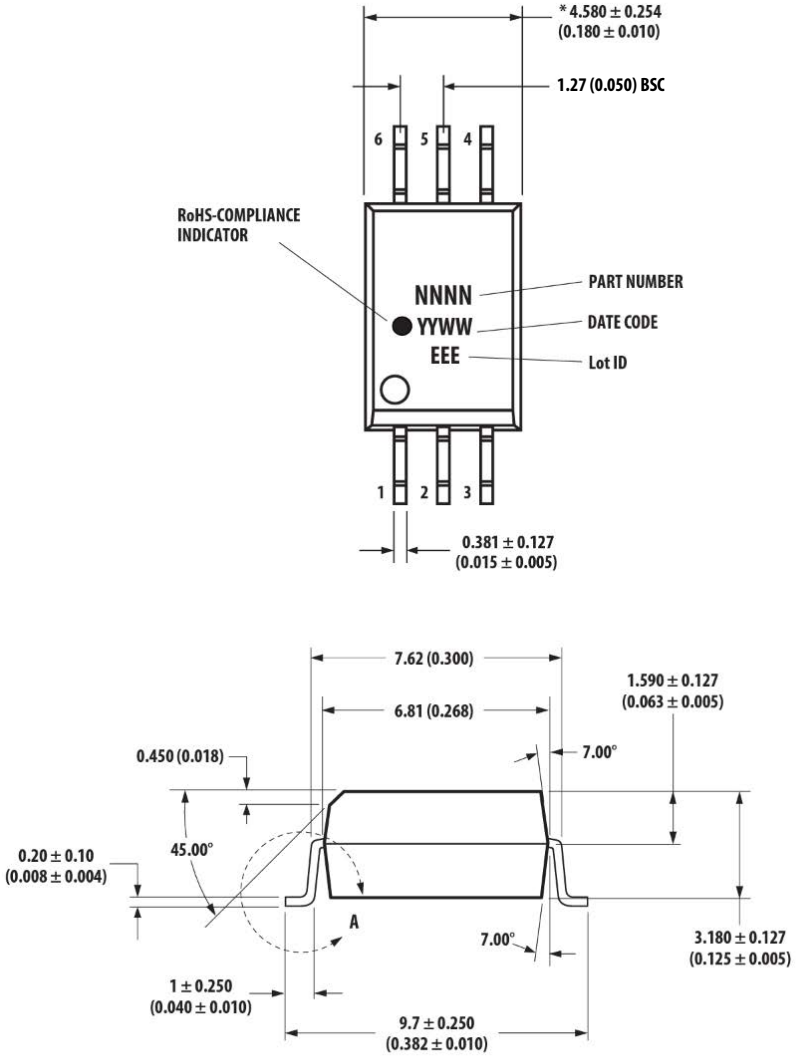
Regulatory Information

The ACPL-P480, ACPL-W480, and ACPL-4800 are approved by the following organizations:

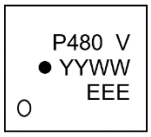
- IEC/EN/DIN EN 60747-5-5 (Option 060 only):
  - IEC 60747-5-5: 2007
  - EN 60747-5-5: 2011
  - DIN EN 60747-5-5 (VDE 0884-5): 2011-11
- UL:
  - Approval under UL 1577, component recognition program up to V_{ISO} = 3750V_{rms}. File E55361.
- CSA: Approval under CSA Component Acceptance Notice #5, File CA 88324.

Package Outline Drawings

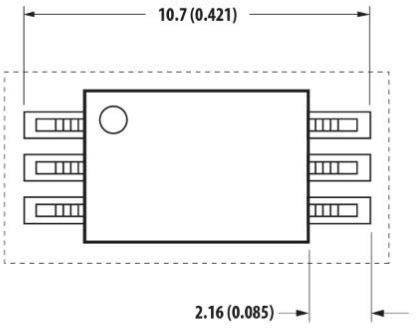
ACPL-P480 Stretched SO-6 Package (7-mm Clearance)

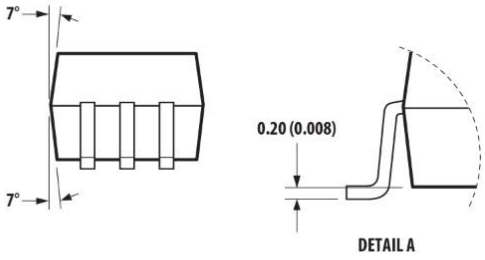


For Option 560E and 060E



LAND PATTERN RECOMMENDATION

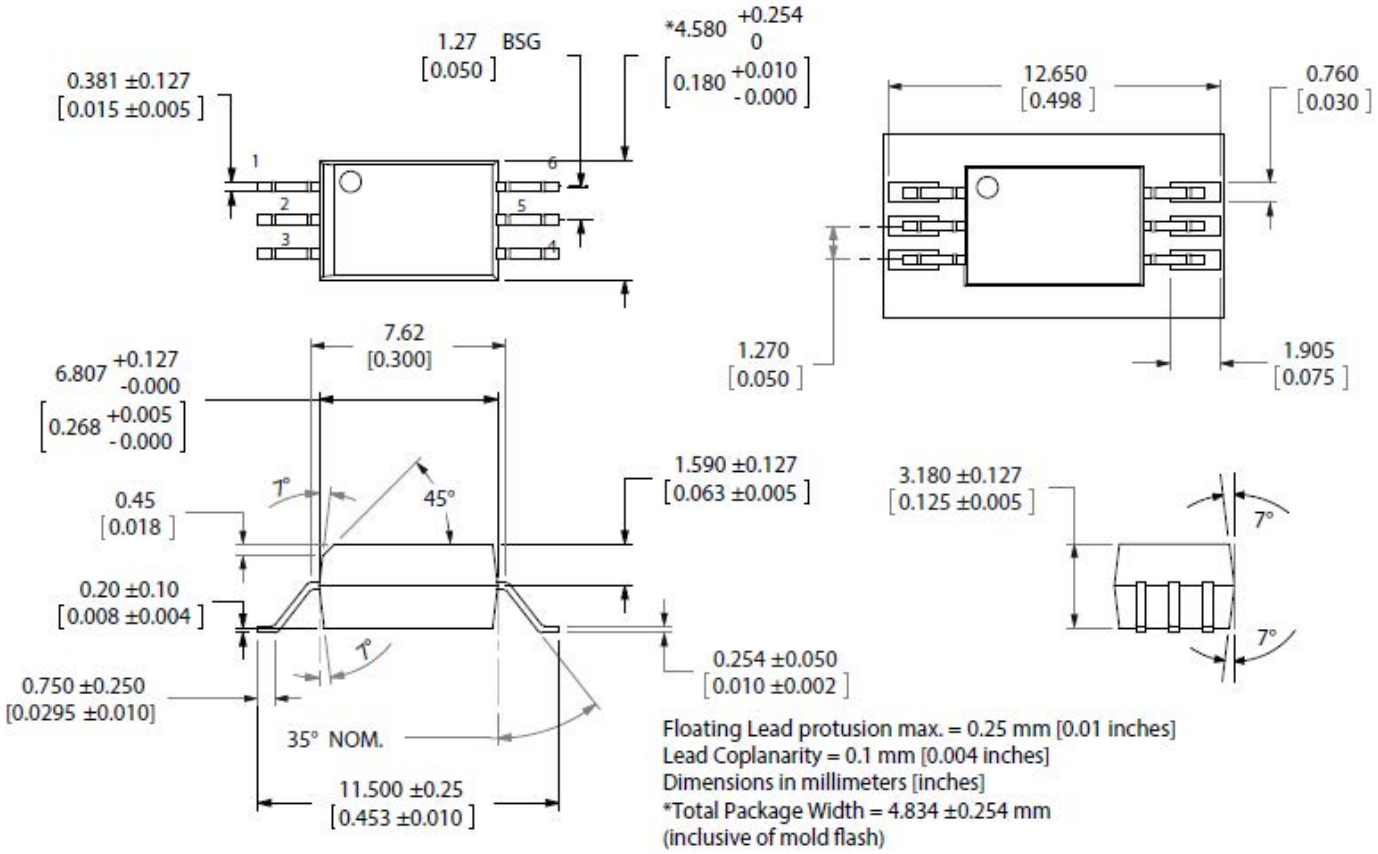




* Total package width (inclusive of mold flash)
4.834 ± 0.254 mm

DIMENSIONS IN MILLIMETERS AND (INCHES).
COPLANARITY = 0.10 mm (0.004 INCHES).

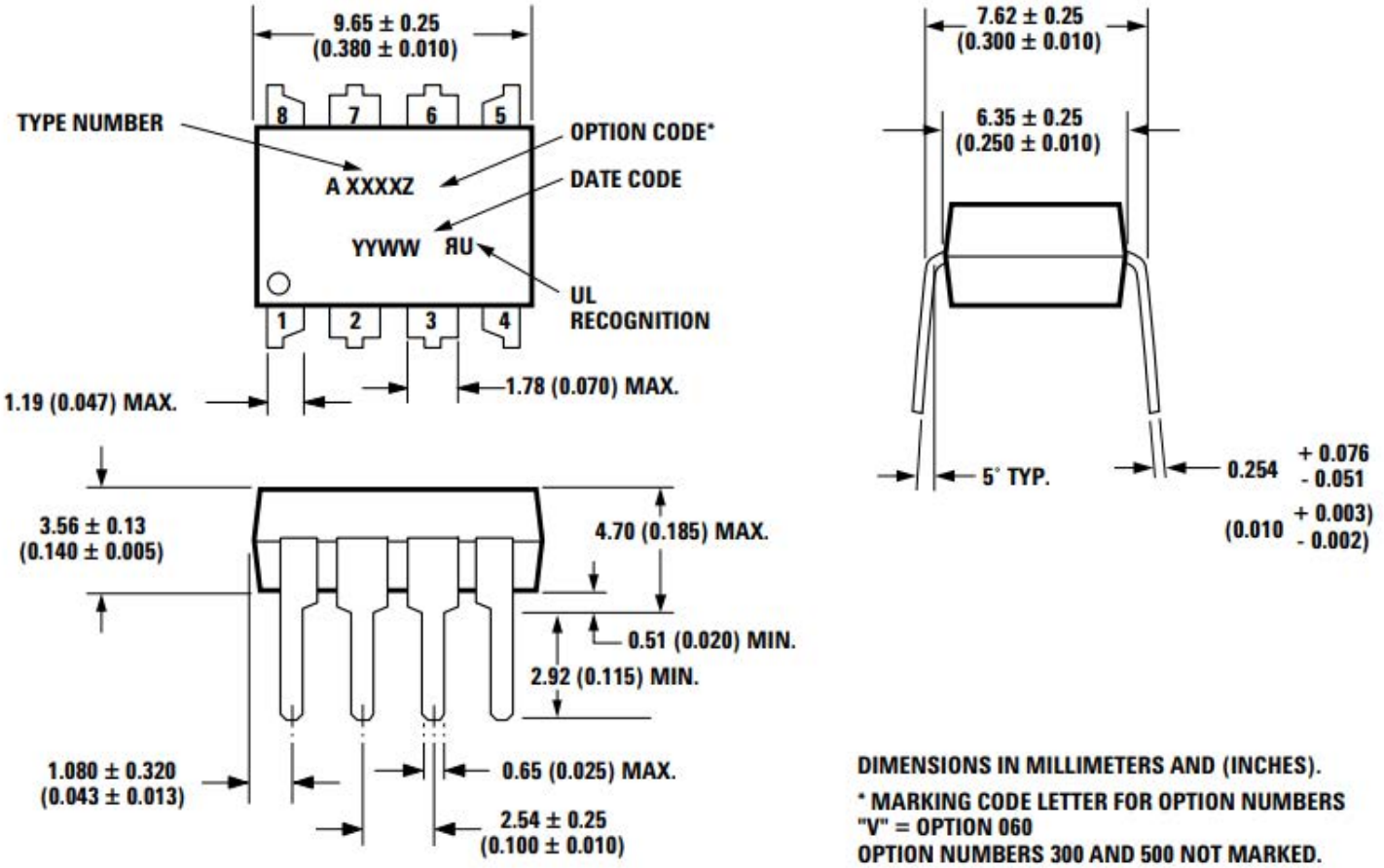
ACPL-W480 Stretched SO-6 Package (8-mm Clearance)



Floating Lead protusion max. = 0.25 mm [0.01 inches]
Lead Coplanarity = 0.1 mm [0.004 inches]
Dimensions in millimeters [inches]
*Total Package Width = 4.834 ±0.254 mm
(inclusive of mold flash)

ACPL-4800 DIP-8

DIP-8 Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060)

Description	Symbol	ACPL-P480	ACPL-W480	ACPL-4800	Units
Installation Classification per DIN VDE 0110/39, Table 1					
For rated mains voltage ≤ 150V_{rms}		I – IV	I – IV	—	
For rated mains voltage ≤ 300V_{rms}		I – IV	I – IV	I – IV	
For rated mains voltage ≤ 450V_{rms}		—	—	I – III	
For rated mains voltage ≤ 600V_{rms}		I – III	I – IV	—	
Climatic Classification		55/100/21		55/85/21	
Pollution Degree (DIN VDE 0110/39)		2			
Maximum Working Insulation Voltage	V_{IORM}	891	1140	630	V_{peak}
Input to Output Test Voltage, Method b[a] V_{IORM} × 1.875 = V_{PR}, 100% Production Test, t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	1670	2137	1181	V_{peak}
Input to Output Test Voltage, Method a[a] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	1426	1824	945	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 seconds)	V_{IOTM}	6000	8000	6000	V_{peak}
Safety-Limiting Values: Maximum values allowed in the event of a failure					
Case Temperature	T_S	175			°C
Input Current	$I_{S, INPUT}$	230			mA
Output Power	$P_{S, OUTPUT}$	600			mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$			Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under the Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5), for a detailed description of Method a and Method b partial discharge test profiles.

Insulation-Related and Safety-Related Specifications

Parameter	Symbol	ACPL-P480	ACPL-W480	ACPL-4800	Unit	Condition
Minimum External Air Gap (External Clearance)	L(101)	7.0	8.0	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	8.0	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.08			mm	Through insulation distance, conductor to conductor, usually the straight-line distance between the photo emitter and photo detector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	>175		200	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group	—	IIIa			—	Material Group (DIN VDE 0110, 1/89, Table 1).

UL 1577 Specification Sheet

Model	Package Type	Current, mA		Power, mW		Isolation Voltage 1 min, V_{rms}	Maximum Operating Temperature, °C	Maximum Junction Temperature, °C	Maximum Storage Temperature, °C
		Emitter	Sensor	Emitter	Sensor				
P480	3	10	25	15	560	5000	110	125	125

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	+125	°C
Operating Temperature	T_A	–40	+100	°C
Average Input Current	$I_{F(AVG)}$	—	10	mA
Peak Transient Input Current	$I_{F(TRAN)}$			
(<1-µs pulse width, 300 pps)		—	1.0	A
(<200-µs pulse width, <1% duty cycle)		—	40	mA
Reverse Input Voltage	V_R	—	5	V
Average Output Current	I_O	—	25	mA
Supply Voltage	V_{CC}	0	25	V
Output Voltage	V_O	–0.5	+25	V
Total Package Power Dissipation[a]	P_T	—	210	mW

a. Derate total package power dissipation, PT, linearly above 70°C free-air temperature at a rate of 4.5 mW/°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	V
Forward Input Current (ON)	$I_{F(ON)}$	6	10	mA
Forward Input Voltage (OFF)	$V_{F(OFF)}$	—	0.8	V
Operating Temperature	T_A	–40	+100	°C

Electrical Specifications

Unless otherwise noted, all typical values are at T_A = 25°C. All minimum and maximum specifications are at recommended operating conditions: T_A = –40°C to +100°C, V_{CC} = +4.5V to 20V, $I_{F(ON)}$ = 6 mA to 10 mA, $V_{F(OFF)}$ = 0V to 0.8V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Logic Low Output Voltage	V_{OL}	—	—	0.5	V	I_{OL} = 6.5 mA	1, 3, 8	
Logic High Output Voltage	V_{OH}	V_{CC} – 0.3	—	—	V	I_{OH} = –3.5 mA, V_{CC} = 4.5V	2, 3, 6, 9	
		V_{CC} – 0.5				I_{OH} = –6.5 mA, V_{CC} = 4.5V		
Threshold Input Current Low to High		—	2.2	5.5	mA			
Logic Low Supply Current	I_{CCL}	—	1.9	3.0	mA	V_{CC} = 5.5V, V_F = 0V, I_O = Open		
		—	2.0	3.0	mA	V_{CC} = 20V, V_F = 0V, I_O = Open		
Logic High Supply Current	I_{CCH}	—	1.5	2.5	mA	V_{CC} = 5.5V, I_F = 10 mA, I_O = Open		
		—	1.6	2.5	mA	V_{CC} = 20V, I_F = 10 mA, I_O = Open		
Logic Low Short Circuit Output Current	I_{OSL}	25	—	—	mA	V_O = V_{CC} = 5.5V, V_F = 0V		a
		50	—	—	mA	V_O = V_{CC} = 20V, V_F = 0V		
Logic High Short Circuit Output Current	I_{OSH}	—	—	–25	mA	V_{CC} = 5.5V, I_F = 10 mA, I_O = Open		a
		—	—	–50	mA	V_{CC} = 20V, I_F = 10 mA, I_O = Open		
Input Forward Voltage	V_F	—	1.5	1.7	V	T_A = 25°C, I_F = 6 mA	4	
		—	—	1.85	V	I_F = 6 mA		
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	I_R = 10 µA		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	—	1.7	—	mV/°C	I_F = 6 mA		
Input Capacitance	C_{IN}	—	60	—	pF	f = 1 MHz, V_F = 0V		b

a. Duration of output short circuit time should not exceed 10 ms.

b. Input capacitance is measured between pin 1 and pin 3.

Switching Specifications

Unless otherwise noted, all typical values are at T_A = 25°C. All minimum and maximum specifications are at recommended operating conditions: T_A = –40°C to +100°C, V_{CC} = +4.5V to 20V, $I_{F(ON)}$ = 6 mA to 10 mA, $V_{F(OFF)}$ = 0V to 0.8V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}	—	150	350	ns	with peaking capacitor	5, 10	a
Propagation Delay Time to Logic High Output Level	t_{PLH}	—	110	350	ns	with peaking capacitor	5, 10	a
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\| = PWD$	—	—	250	ns			b
Propagation Delay Difference Between Any Two Parts	PDD	–100	—	+250	ns			c
Output Rise Time (10% to 90%)	t_r	—	16	—	ns		7, 10	
Output Fall Time (90% to 10%)	t_f	—	20	—	ns		7, 10	
Logic High Common Mode Transient Immunity	$\|CM_H\|$	20	—	—	kV/µs	$\|V_{CM}\|$ = 1000V, I_F = 6.0 mA V_{CC} = 5V, T_A = 25°C	11	d
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	20	—	—	kV/µs	$\|V_{CM}\|$ = 1000V, V_F = 0V, V_{CC} = 5V, T_A = 25°C	11	d

a. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.

b. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.

c. The difference between t_{PLH} and t_{PHL} between any two devices under the same test condition.

d. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state, V_O > 2.0V. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state, V_O < 0.8V.

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	3750	—	—	V_{rms}	RH < 50%, t = 1 minute, T_A = 25°C	b, c
Input-Output Resistance	R_{I-O}	—	10^{12}	—	—	V_{I-O} = 500V_{DC}	b
Input-Output Capacitance	C_{I-O}	—	0.6	—	—	f = 1 MHz, V_{I-O} = 0V_{DC}	b, d

a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable).

b. The device is considered a two-terminal device: pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together.

c. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage 4500V_{rms} for one second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060), if applicable.

d. Use of a 0.1 µF bypass capacitor connected between pins 4 and 6 is recommended.

Figure 1: Typical Logic Low Output Voltage vs. Temperature

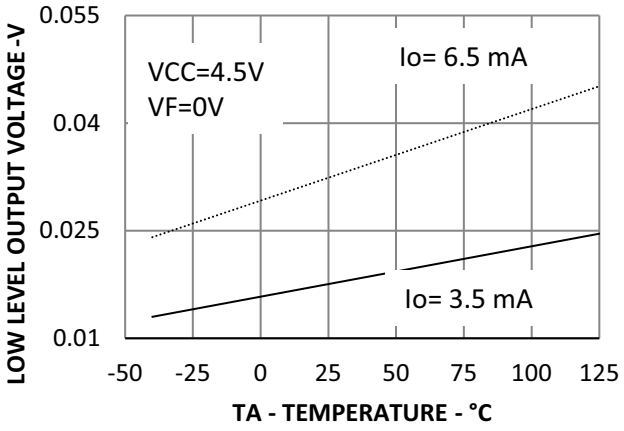


Figure 2: Typical Logic High Output Current vs. Temperature

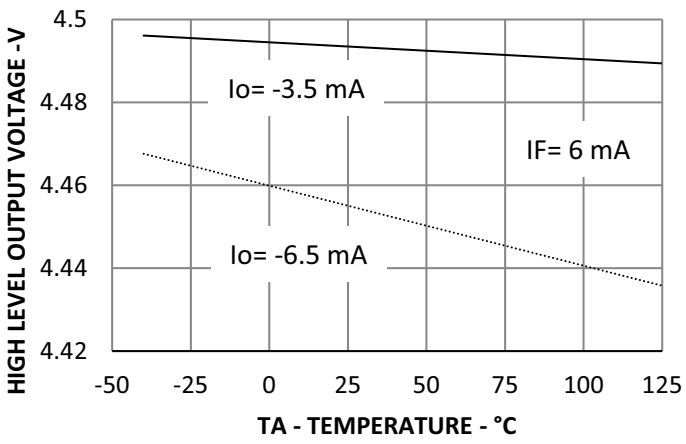


Figure 3: Typical Threshold Current vs. Temperature

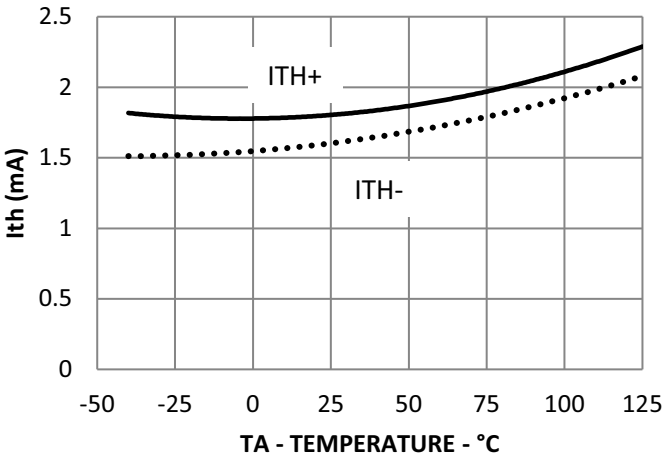


Figure 4: Typical Input Diode Forward Characteristic

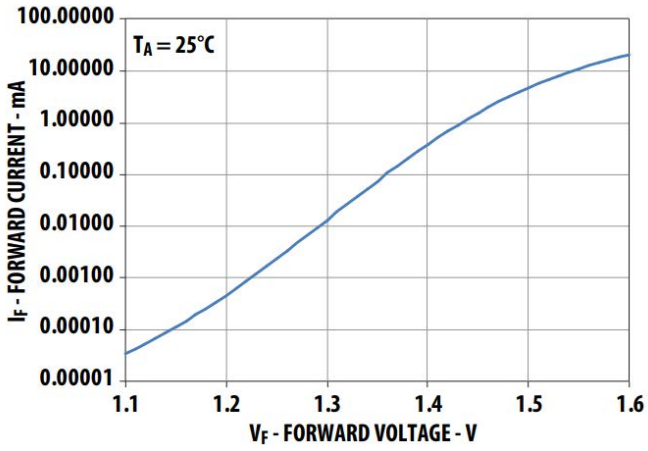


Figure 5: Typical Propagation Delays vs. Temperature

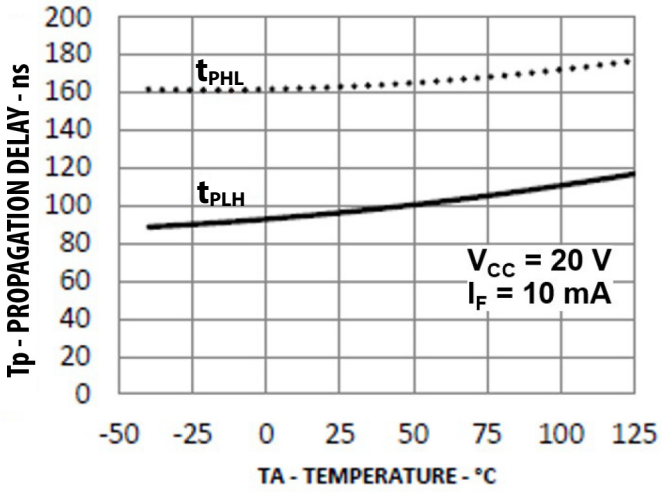


Figure 6: Typical Logic High Output Voltage vs. Supply Voltage

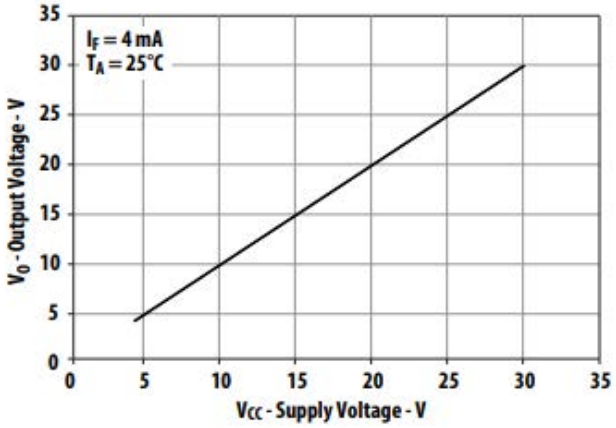


Figure 7: Typical Propagation Delay vs. Supply Voltage

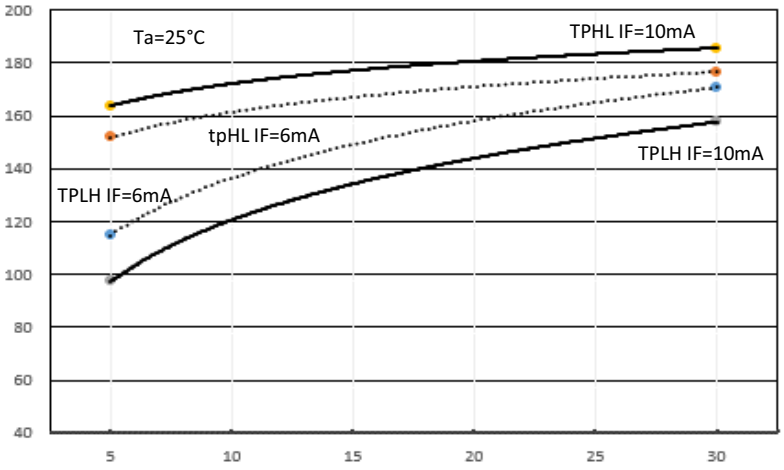


Figure 8: V_{OH} vs. I_{OH} Across Temperatures

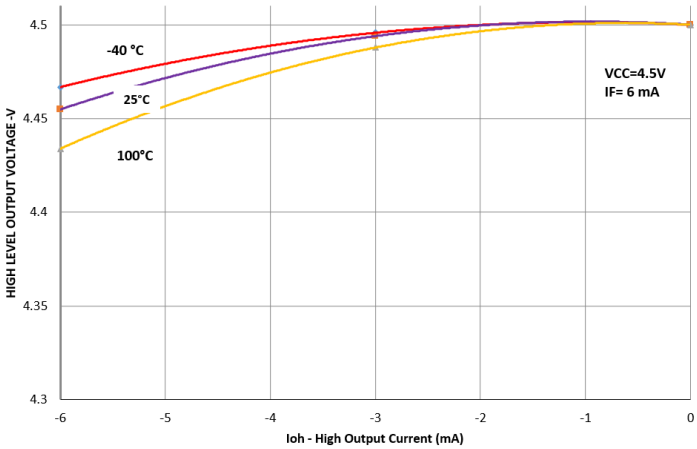


Figure 9: V_{OL} vs. I_{OL} Across Temperatures

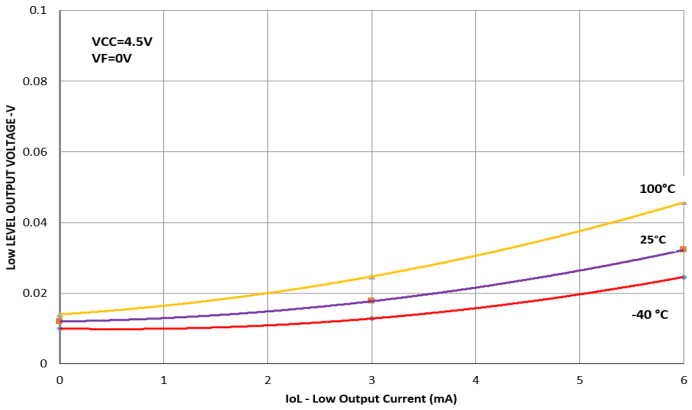
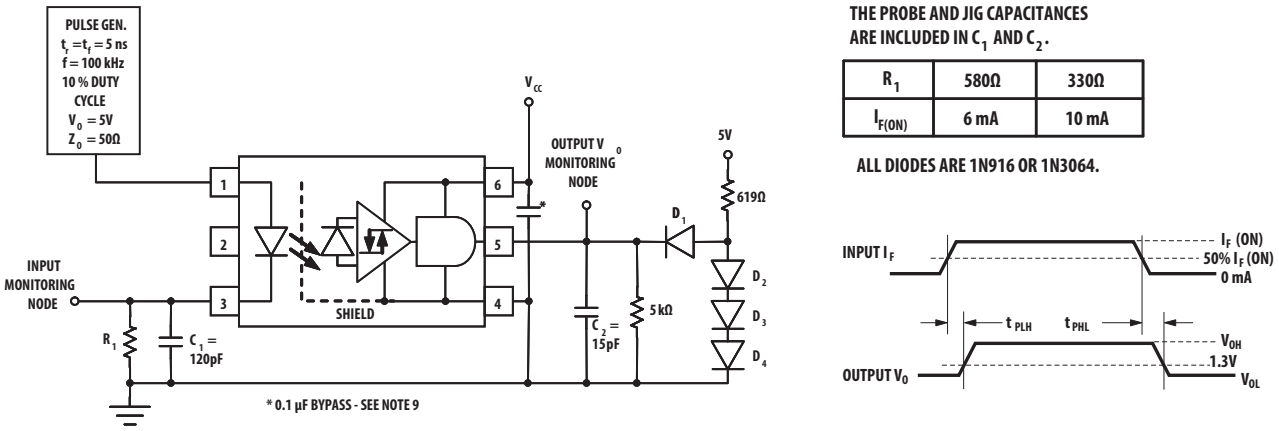
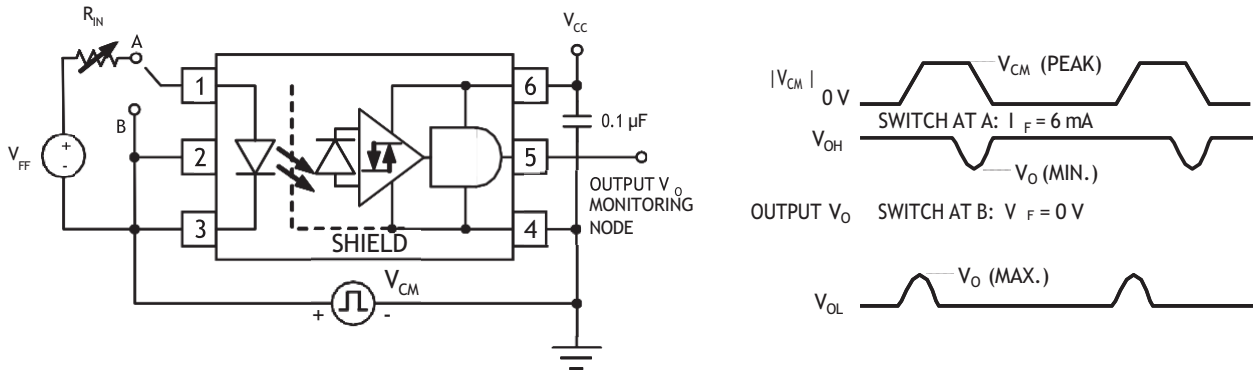


Figure 10: Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f



R_1	580Ω	330Ω
$I_{F(ON)}$	6 mA	10 mA

Figure 11: Test Circuit for Common Mode Transient Immunity and Typical Waveforms



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