Generic Printed Circuit Layout Rules
for Avago Technologies' Low-Cost
Fiberoptic Components

AVAGO TECHNOLOGIES

Application Note 1137

Introduction

Avago Technologies' discrete fiberoptic components have been used to construct high-performance optical transmitters and receivers for numerous cost-sensitive LAN, telecom, industrial, and proprietary point-to-point data communication applications. When using discrete fiberoptic components the layout of the printed circuit board will have a significant impact upon the performance of the optical transmitter and receiver. A printed circuit board layout for inexpensive, high-performance fiberoptic transceivers can usually be developed in one design cycle, using the generic rules described in this publication.

What are discrete fiberoptic components?

Avago Technologies manufactures a broad range of discrete transmitter, receiver, and transceiver components suited for use with a wide variety of fiberoptic cables and connectors. Discrete transmitter components have integral LED or LASER optical emitters, lens assemblies, and housings that mate with industry-standard fiberoptic connectors. This publication will focus upon discrete transmitters implemented with planar- and edge-emitting LEDs. Discrete LED transmitters have been successfully designed into a wide range of data communication applications. This technology is popular because discrete LEDs can meet tough performance, reliability, and cost targets when used in conjunction with very simple, inexpensive circuitry. Discussions regarding the use of discrete LASER transmitters are beyond the scope of this application note.

Receiver components also have integral lens assemblies and housings that are compatible with various industry-standard fiberoptic connectors. At data rates less than 10 MBd, receiver components can be manufactured using monolithic optical detectors that integrate all of the functions needed to provide TTL-compatible outputs. Digital fiberoptic receivers are usually highly integrated at data rates less than 10 MBd, but these integrated receiver components are often classified as discretes because they are commonly used with discrete LED transmitters that require the use of simple external circuitry.

At data rates greater than 10 MBd the receiver is typically a simple hybrid component that contains an optical detector and a transimpedance amplifier. These hybrid receiver components are commonly known as PIN pre-amplifiers, since they include both the PIN diode detector and the transimpedance amplifier needed to convert detector current to voltage. Hybrid PIN pre-amps are classified as discrete components because they require external passive and active circuitry to digitize the PIN pre-amp's analog output signal. Techniques for using discrete fiberoptic components in low-speed digital applications at data rates less than 10 MBd are described in Avago Technologies Application Notes 1035 and 1080. This publication focuses upon the printed circuit design methodologies needed for using LED transmitter components and PIN pre-amp components in higher-speed applications at data rates between 10 and 160 MBd.

Differences between discrete fiberoptic components and fiberoptic modules

Avago Technologies manufactures both discrete fiberoptic components and integrated fiberoptic modules. A fiberoptic module normally includes the LED emitter, PIN pre-amp, lenses and the external housing needed to mate with various types of fiberoptic cables and connectors. In addition, fiberoptic modules typically include the LED driver and receiver digitizing circuits needed to provide logic-compatible inputs and outputs. Fiberoptic modules are usually designed to address specific standards-based applications, whereas fiberoptic components are very flexible since they can be combined with simple external circuits to address a much wider range of proprietary applications. Because they require less external circuitry, fiberoptic modules have commonly been used to reduce design-in costs and shorten product development cycle time.

Table 1. Avago Technologies' Application Notes for Discrete Fiberoptic Components

Application Note Number	Application
AN-1123	20 to 160 MBd with +5V ECL I/O
AN-1122	2 to 70 MBd with TTL I/O
AN-1121	dc to 32 MBd with TTL I/O
AN-1082	Ethernet with single mode fiber
AN-1073	Testing +5V ECL F.O. transceivers
AN-1066	1 to 155 MBd with plastic fibers
AN-1065	Token Ring LANs at 8 or 32 MBd
AN-1038	Ethernet LANs at 20 MBd
AB-78	1-155 MBd with glass fibers

Implementing digital transceivers with fiberoptic components

Avago Technologies fiberoptic components are easy to use in digital data communication applications. Inexpensive, off-the-shelf, advanced CMOS logic gates are commonly used to current modulate (drive) the LED transmitter components. Low-cost ECL line receiver integrated circuits or off-the-shelf high-speed comparators can be used to digitize (quantize) the analog output voltage of the PIN pre-amp front-end. Integrated quantizers can also be used with PIN pre-amp components to lower the receiver's parts count and provide more functions. One of the objectives of this publication is to simplify the design process for discrete fiberoptic components so that they can be used to address cost-sensitive applications that would normally be implemented with copper wires. For more details about proven circuits recommended for use with inexpensive fiberoptic components in digital data communication applications, please refer to the Avago Technologies application notes listed in Table 1.

Where do the generic design rules for fiberoptic components apply?

The generic design rules in this publication have been proven to work with Avago Technologies 650 nm, 820 nm and 1300 nm discrete fiberoptic components. These generic printed circuit design rules can be applied to all of the Avago Technologies components and Application Notes listed in Table 2.

Design rules for surface-mount technology

The following rules should be followed if you desire to use surface-mount technology and a four-layer printed circuit board to construct inexpensive fiberoptic transceivers.

1. Design the PC board with different ground and power planes for the transmitter and receiver. Providing two individual ground planes is the critical technique for minimizing crosstalk between the transmitter and receiver circuits. Use wide power distribution traces when power planes are not possible. These techniques reduce the inductance of the ground and power leads, minimize crosstalk between the transmitter and receiver circuits, and maximize the receiver circuit's damping and sensitivity.
2. Minimize the size of cuts or openings in the ground and power planes. This minimizes the parasitic inductance and improves the dampening of both the transmitter and receiver circuits. Route connections between components on the top and bottom planes; locate the ground and power planes on inner layers of the printed circuit. ***Do not*** make long rectangular openings in the power planes if you have several vias in a row. Allow planes to connect between adjacent vias, this assures that there are no long rectangular cuts in the ground or power planes.
3. The two circuit traces that connect the PIN pre-amp to the differential input of the receiver's quantizer should be of equal length and the components in both traces should be placed to achieve symmetry. This minimizes the cross talk between the fiberoptic transmitter and receiver and improves the receiver's immunity to environmental noise. When viewed from the optical inputs and outputs (looking toward the lenses) the LED transmitter should be on the right and the PIN pre-amp should be on the left to minimize crosstalk between the transmitter and receiver.

Table 2. Components and Application Notes where Generic Layout Rules Apply

Avago Technologies Publications	Applications	Data Rate (symbols/sec)	Transmitter Part Number	Receiver Part Number	Wavelengths
AB-78	Telecom & Proprietary	10 to 155 MBd	HFBR-14X4Z HFBR-1312TZ	HFBR-24X6Z HFBR-2316TZ	820 nm 1300 nm
AN-1038	Ethernet	20 MBd	HFBR-14X4Z	HFBR-24X6Z	820 nm
AN-1065	Token Ring	8 & 32 MBd	HFBR-14X4Z	HFBR-24X6Z	820 nm
AN-1066	Telecom & Proprietary	10 to 155 MBd	HFBR-15X7Z	HFBR-25X6Z	650 nm
AN-1121	Industrial, Medical, Telecom & Proprietary	DC to 32 MBd	HFBR-1312TZ HFBR-14X2Z HFBR-14X4Z HFBR-15X7Z	HFBR-2316TZ HFBR-24X6Z HFBR-24X6Z HFBR-25X6Z	1300 nm 820 nm 820 nm 650 nm
AN-1122	Industrial, Medical, Telecom & Proprietary	2 to 70 MBd	HFBR-1312TZ HFBR-14X2Z HFBR-14X4Z HFBR-15X7Z	HFBR-2316TZ HFBR-24X6Z HFBR-24X6Z HFBR-25X6Z	1300 nm 820 nm 820 nm 650 nm
AN-1123	Industrial, Medical, Telecom & Proprietary	20 to 160 MBd	HFBR-1312TZ HFBR-14X2Z HFBR-14X4Z HFBR-15X7Z	HFBR-2316TZ HFBR-24X6Z HFBR-24X6Z HFBR-25X6Z	1300 nm 820 nm 820 nm 650 nm

4. Connections between the drive circuit and the LED should be of minimum length. This minimizes the noise emitted by the transmitter circuit and improves the optical rise/fall time of the LED.
5. A large, 10 µF, electrolytic capacitor and a 0.1 µF monolithic ceramic capacitor should be located as close as possible to the circuit that drives (current modulates) the LED. This minimizes the noise emitted by the transmitter and improves the optical response time of the LED.
6. A ferrite EMI suppressor should be used to isolate the transmitter circuit's 5 V supply from the host system's 5 V supply.
7. Low-pass filters must be used to protect the fiberoptic receiver from noise present in the host system's 5 V power supply. The required power supply filtering can be quickly and easily incorporated by adhering to the recommended schematics published in Avago Technologies application notes.
8. Inductors or a common-mode choke should be used in series with the receiver's V_{CC} and V_{EE} connections (V_{CC} = +5 V and V_{EE} = 0 V). The receiver should be referenced to V_{CC} and V_{EE} islands that are isolated from the remainder of the host system's power planes. A differential electrical interface at the receiver's output is required if inductors are used in series with V_{CC} and V_{EE}. Figure 1 in Avago Technologies Application Note 1122 shows that this differential interface has been embedded in the quantizer's integrated circuit when using Micro Linear's ML-4624.
9. Use monolithic ceramic chip capacitors. This type of capacitor minimizes parasitic coupling between the receiver's output and input stages. Minimizing the parasitic coupling between the receiver's outputs and inputs assures that the receiver will not oscillate. Monolithic chip capacitors have small geometries that minimize their ability to function as undesirable radiating or receiving antennas. In addition to the features already discussed, monolithic ceramic capacitors have low parasitic inductance and a high self-resonant frequency that make them an excellent choice for radio frequency applications such as fiberoptic transceivers.
10. For capacitances greater than 1.0 µF, tantalum chip capacitors are recommended. Tantalum capacitors are well suited for high-speed fiberoptic transceivers because they have small geometries and are capable of providing a low impedance at high frequencies.
11. The filter network for the +5 V power supply connection to the receiver's PIN pre-amp should be as far as possible from the +5 V bypass capacitors for the driver circuit that current modulates the LED transmitter. The filter network connected to the power pin of the receiver's PIN pre-amp should be physically separated from the LED driver's bypass caps to minimize crosstalk between the fiberoptic transmitter and receiver.

12. Do not fold the receiver layout in an attempt to save board space. The receiver should be constructed in the straightest possible line beginning at the PIN pre-amp and ending at the receiver's logic output. Fiberoptic receivers normally have sufficient gain and phase shift to meet the criteria for oscillation. To achieve stability the receiver's input and output stages must be sufficiently isolated from one another to assure that loop gain is less than one. Receiver stability is easily attained when the printed circuit design rules in this publication are used with the fiberoptic transceiver circuits recommended in Avago Technologies application notes.
13. The receiver's power supply filtering is just as important as good printed circuit layout. Undesirable feedback between the receiver's output and the PIN pre-amp input can occur if the receiver's power bus is improperly bypassed. To assure receiver stability the power supply filter circuits recommended in Avago Technologies application notes should be used to prevent undesirable conductive feedback through the receiver's +5 V power connections.

Design rules for through-hole technology

The following rules should be followed if you desire to use through-hole technology and four-layer printed circuit boards to construct inexpensive fiberoptic transceivers. The design rules for surface-mount and through-hole technology are nearly identical so only the rules that have significant differences are described in detail.

1. Use the techniques described for surface-mount technology.
2. Minimize the size of cuts or openings in the ground and power planes. This minimizes the parasitic inductance and improves the dampening of both the transmitter and receiver circuits. Route connections between components on the top and bottom planes; locate the ground and power planes on inner layers of the printed circuit. ***Do not*** make long rectangular openings in the ground and power planes where IC leads or rows of passive component leads penetrate the printed circuit board. Allow the planes to connect between each component lead and allow the plane to connect between every lead of an integrated circuit.
3. Use the techniques described for surface-mount technology.
4. Use the techniques described for surface-mount technology.
5. Use the techniques described for surface-mount technology.
6. Use the techniques described for surface-mount technology.
7. Use the techniques described for surface-mount technology.
8. Use the techniques described for surface-mount technology.
9. Use monolithic ceramic radial lead capacitors. This type of capacitor minimizes parasitic coupling between the receiver's output and input stages. Minimizing the parasitic coupling between the receiver's outputs and inputs assures that the receiver will not oscillate. Monolithic ceramic radial lead capacitors have small geometries which minimize their ability to function as undesirable radiating or receiving antennas. In addition to the features already discussed, monolithic ceramic capacitors have low parasitic inductance and a high self resonant frequency that make them an excellent choice for radio frequency applications such as fiberoptic transceivers.
10. For capacitances greater than 0.47 μF, tantalum capacitors are recommended. Tantalum capacitors are well suited for high speed fiberoptic transceivers because they are physically small, have low ESR, and are capable of providing a low impedance at high frequencies.
11. Use the techniques described for surface-mount technology.
12. Use the techniques described for surface-mount technology.
13. Use the techniques described for surface-mount technology.

Conclusions

The generic design rules in this publication have been applied to every currently available Avago Technologies application note regarding the use of fiberoptic components. These rules were used to design the printed circuits shown in nine Avago Technologies' fiberoptic application notes published over a six year period. Designers interested in using inexpensive fiberoptic components are encouraged to imbed the circuits and printed circuit layouts shown in Avago Technologies' application notes.

If the existing artworks shown in Avago Technologies' application notes are not compatible with your manufacturing process or form factor requirements, then the generic rules in this publication are useful for quickly designing your own unique printed circuit with a minimal amount of engineering effort.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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