

## Application Note 5241

### Introduction

The ADJD-J823 controls the proportion of light from three color light sources. These three color light sources come from a: red LED, green LED and blue LED. Each color can be a single LED or an array of LEDs. These light sources are thoroughly mixed to produce a resultant color. The mixing is done using optical components such as light guides or light panels. There is optical feedback from the integrated color sensors. The optical feedback allows the ADJD-J823 controller to produce color accurately. The color is maintained by adjusting each of the pulse width modulation signals, PWMR, PWMG, and PWMB, of the light sources.

### Serial Interface Protocol

The programming is done through the serial interface. The serial interface protocol details are described in the data-sheet. The device address consists of the most significant 7-bit slave device address and a R/W bit. The 7-bit slave device address is 58H or decimal 88. Thus, the device address for writing is B0H and for reading is B1H. The dataflow diagram for the serial communication is as follows.

For Write, S [Dw] a [R] a [Vw] a P

For Read, S [Dw] a [R] a Sr [Dr] a [Vr] n P

| KEY  | Description   |
|------|---|
| S    | Start transition from host controller                       |
| a    | Acknowledge bit from device                                 |
| n    | Not acknowledge bit sent by host controller to device       |
| Sr   | Repeat start transition                                     |
| P    | Stop transition from host controller                        |
| [Dw] | ADJD-J823 device write address byte = B0H                   |
| [Dr] | ADJD-J823 device read address byte = B1H                    |
| [R]  | Device register address byte in the write or read operation |
| [Vw] | Value to write to device register address 'R'               |
| [Vr] | Value to read from device register address 'R'              |

Example:

- a) To write a value of 01H to CTRL2 register (address 02H), the datagram is

S [B0] a [02] a [01] a [P]

- b) To read CTRL2 register (address 02H), the datagram is

S [B0] a [02] a S<sub>r</sub> [B1] a [V<sub>r</sub>] n P

Key:

S - Start transition

a - Acknowledge bit receive from device

n - Not acknowledge bit send to device

S<sub>r</sub> - Repeat start transition

P - Stop transition

[B0] - ADJD-J823 device write address byte = B0H

[B1] - ADJD-J823 device read address byte = B1H

[02] - CTRL2 register address = 02H

[01] - Value 01H to write to CTRL2 register

[V<sub>r</sub>] - Byte value read from device

## Operating Modes

There are two operating modes:

- a) Open Loop mode. This mode is for calibration or open loop control of the LED light sources.
- b) Close Loop mode. This mode is also known as normal operating mode with optical feedback.

## Implementation Method

There are three types of implementation. They are dedicated EEPROM in a stand-alone system, dedicated EEPROM in interactive mode and independent EEPROM or a system without a dedicated EEPROM.

### Dedicated EEPROM System

A system with dedicated EEPROM is highly recommended to simplify the programming effort. The dedicated EEPROM must have an I2C bus interface. The EEPROM I2C 7-bit device address is not user configurable and is fixed to 50H. The EEPROM device write address is A0H and the read address is A1H.

### Programming

Before the ADJD-J823 can be used to control color and brightness, a one time calibration is generally required to obtain setup and calibration data values. These values, including offset and frequency data, need to be saved in non-volatile memory, as they need to be read back during normal operation. The method to perform calibration is described in the calibration procedure section.

After calibration, users need to read back the saved offset, frequency, setup and calibration data from non-volatile memory. The offset, frequency, setup and calibration data from non-volatile memory are loaded to the ADJD-J823 for normal operation with optical feedback. A color set point is selected to display the color and brightness desired. This method is described in the basic operating procedure. For systems, with dedicated EEPROM, the AUTO LOAD operating procedure can be used after the set up for auto-load is done.

## Calibration Procedure

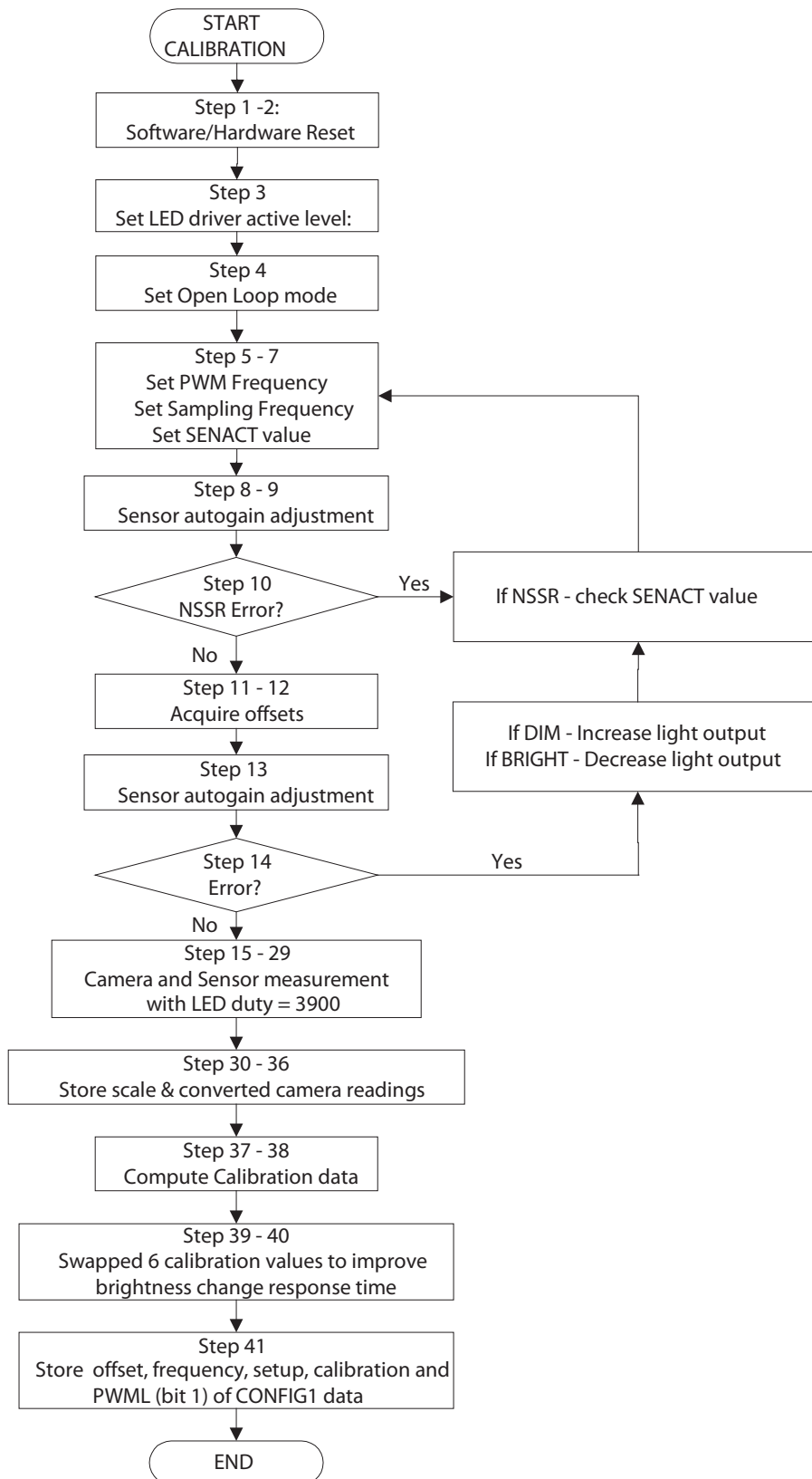


Figure 1. Calibration flow chart

The detail flow chart for sensor and camera measurement with LED duty values = 3900 is shown in Figure 2.

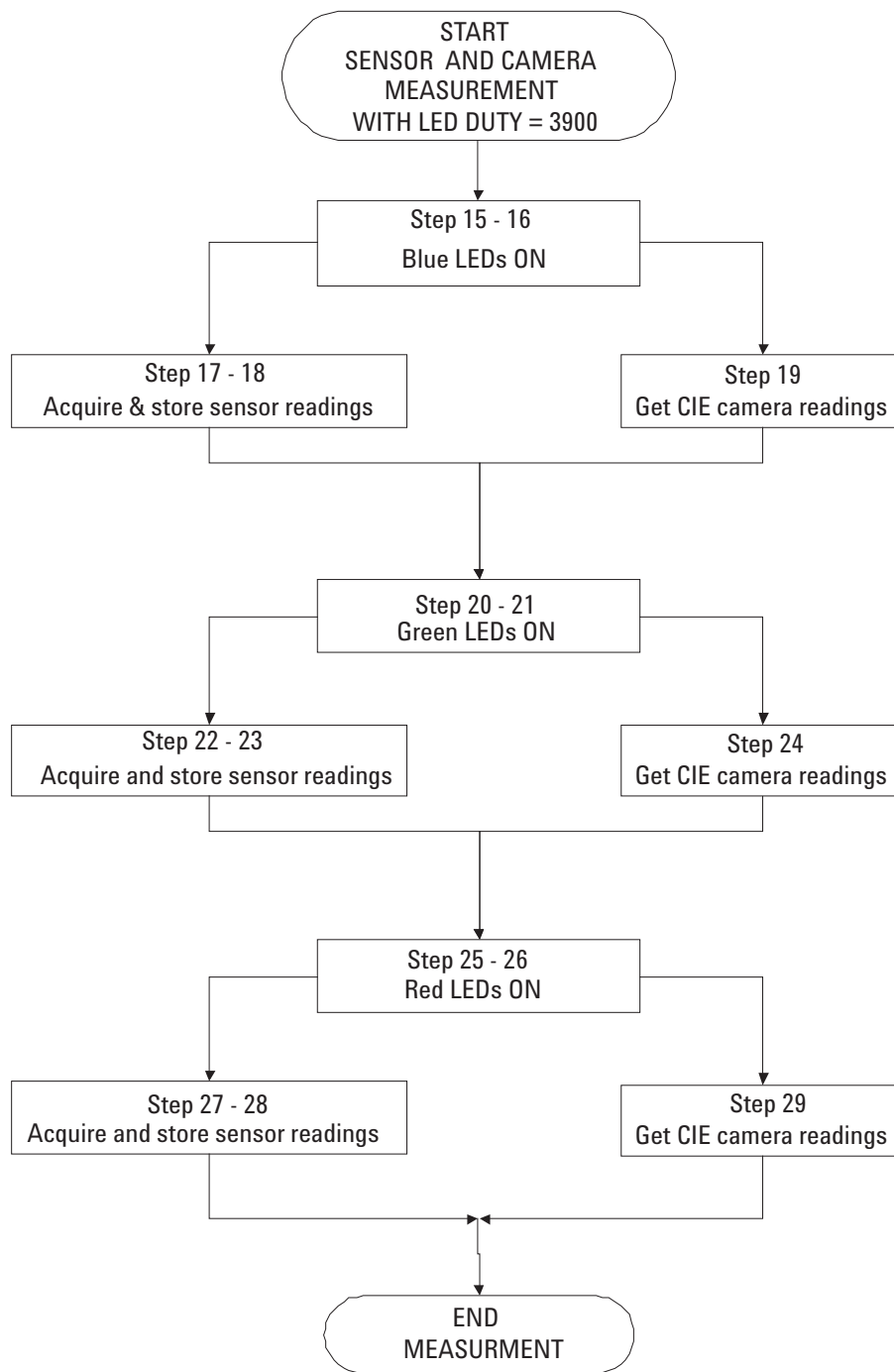


Figure 2. Sensor and camera measurement flow chart

## Calibration Procedure

The procedure for calibration is as follows.

- 1) First perform an external power on reset or software reset by writing CTRL1 register with 01H.

| Bit      | 7   | 6 | 5       | 4       | 3       | 2      | 1     | 0   |
|----------|-----|---|---------|---------|---------|--------|-------|-----|
| Mnemonic | RSV |   | DWL_CAL | UPL_ALL | DWL_ALL | UPL_CP | UD_CP | RSW |
| Value    | 0   | 0 | 0       | 0       | 0       | 0      | 0     | 1   |

**Figure 3. CTRL1 bit format. Address 01H**

- 2) Wait for the reset sequence to be completed. The status register (address 22H) can be read to verify that the INIT (bit 0) is set to "0" before proceeding.

| Bit      | 7   | 6 | 5 | 4 | 3 | 2     | 1    | 0    |
|----------|-----|---|---|---|---|-------|------|------|
| Mnemonic | RSV |   |   |   |   | OPENL | NORM | INIT |
| Value    | 0   | 0 | 0 | 0 | 0 | 0     | 1    | 0    |

**Figure 4. STATUS register. Address 22H**

After power-on reset or software reset, the DUTYR\_LO, DUTYR\_HI, DUTYG\_LO, DUTYG\_HI, DUTYB\_LO and DUTYB\_HI registers are zero. The PWME bit of CONFIG1 register is also set to '0'. This should turn off all the red, green and blue LEDs for an active high LED driver design.

However, for an active low LED driver design, all the red, green and blue LEDs will turn on after power or software reset.

- 3) Write CONFIG1 register to set up the PWML bit depending on the LED driver used.

| Bit      | 7   | 6 | 5 | 4 | 3 | 2     | 1      | 0    |
|----------|-----|---|---|---|---|-------|--------|------|
| Mnemonic | RSV |   |   |   |   | AUTOL | PWML   | PWME |
| Value    | 0   | 0 | 0 | 0 | 0 | 0     | Note a | 0    |

**Figure 5. CONFIG1 format. Address 03H**

Note a: Set PWML bit: '0' for PWM active high, '1' for PWM active low.

- 4) Write CONFIG2 register with 01H to set the device to open loop mode so that the calibration can be done.

| Bit      | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0    |
|----------|-----|---|---|---|---|---|---|------|
| Mnemonic | RSV |   |   |   |   |   |   | OPMD |
| Value    | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 1    |

**Figure 6. CONFIG2 format. Address 04H**

The status register (address 22H) can be read to verify that the OPENL (bit 2) is set to "1" before proceeding with the calibration.

- 5) Determine the PWM frequency.

Usually, the selection of the PWM frequency is not critical. Selection of the PWM frequency depends on the frequency response and the rise and fall time of the LED drivers.

The power on or reset value for the PWMFREQ register value is zero. At the nominal clock frequency of 26 MHz, the PWM frequency is 6.35 kHz. The PWM frequency is related to the PWMFREQ register by the following formula.

$$\text{PWM Frequency} = \frac{\text{Clock Frequency}}{(\text{PWMFREQ} + 1) \times 4096}$$

For example, if the operating PWM frequency is 907 Hz, the PWMFREQ register value is six. Write the PWMFREQ register with 06H.

| Bit      | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|---|---|---|---|---|---|---|
| Mnemonic | PWMFREQ |   |   |   |   |   |   |   |
| Value    | 0       | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Figure 7. PWMFREQ format. Address 05H**

- 6) Determine the sensor sampling frequency. The selected sampling frequency must ensure that the PWM frequency divided by the sampling frequency is at least four. The PWM frequency must be at least four times the sampling frequency.

The power on or reset value for the SAMPFREQ register (address 06H – 07H) is 7530H or decimal 30000. At the nominal clock frequency of 26 MHz, the sensor sampling frequency is 108 Hz. The sampling frequency is related to SAMPFREQ by the following equation.

$$\text{Sampling Frequency} = \frac{\text{Clock Frequency}}{\text{SAMPFREQ} \times 8}$$

For example, if the sensor sampling frequency required is 86.6 Hz, the SAMPFREQ register value is 37500 or 927CH. Write SAMPFREQ\_LO with 7CH and SAMPFREQ\_HI with 92H.

| Bit      | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-------------|---|---|---|---|---|---|---|
| Mnemonic | SAMPFREQ_LO |   |   |   |   |   |   |   |
| Value    | 0           | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

**Figure 8. SAMPFREQ\_LO format. Address 06H**

| Bit      | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-------------|---|---|---|---|---|---|---|
| Mnemonic | SAMPFREQ_HI |   |   |   |   |   |   |   |
| Value    | 1           | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

**Figure 9. SAMPFREQ\_HI format. Address 07H**

- 7) Determine the SENACT value. **The SENACT value must be an integer value from 0 to 9.**

The sensor acquisition constant, SENACT value is given by:

$$\text{SENACT} = 1/3 * \left\{ \frac{\text{SAMPFREQ}}{512(\text{PWMFREQ} + 1)} - 1 \right\} - 1$$

This value must be rounded down to the nearest integer. **If the value is less than 0, the PWM frequency and the sampling frequency must be changed so that the PWM frequency to sampling frequency ratio is at least 4. Use a value of 9, if the calculated SENACT value is greater than 9.**

For example, given that PWMFREQ = 4 and SAMPFREQ = 37500, SENACT = 3.549 or 3 (rounded down to nearest integer). Write the SENACT register with 03H.

| Bit      | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|--------|---|---|---|---|---|---|---|
| Mnemonic | SENACT |   |   |   |   |   |   |   |
| Value    | 0      | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

**Figure 10. SENACT format. Address A9H**

- 8) Write the CONFIG1 register to set the PWME (bit 0) to '1' to turn on the PWM generator.

| Bit      | 7   | 6 | 5 | 4 | 3 | 2     | 1      | 0    |
|----------|-----|---|---|---|---|-------|--------|------|
| Mnemonic | RSV |   |   |   |   | AUTOL | PWML   | PWME |
| Value    | 0   | 0 | 0 | 0 | 0 | 0     | Note a | 1    |

**Figure 11. CONFIG1 format. Address 03H**

Note a: Set PWML bit: '0' for PWM active high, '1' for PWM active low.

- 9) Write CTRL2 register with 08H to set the SAGA (bit 3) to '1'.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Value    | 0       | 0   | 0 | 0       | 1    | 0    | 0    | 0    |

**Figure 12. CTRL2 bit format. Address 02H**

The sensor automatic gain adjustment is performed.

Wait for the sensor automatic gain adjustment to be completed. Alternatively, read the CTRL2 register to verify that SAGA (bit 3) is '0' before proceeding to next step.

- 10) Read the ERROR register (address 23H). Verify that NSSR (bit 7) is '0' before proceeding to next step.

| Bit      | 7    | 6   | 5    | 4   | 3      | 2   | 1     | 0     |
|----------|------|-----|------|-----|--------|-----|-------|-------|
| Mnemonic | NSSR | RSV | NACK | DIM | BRIGHT | RSV | NLOCK | RANGE |
| Value    | 0    | X   | X    | X   | X      | X   | X     | X     |

**Figure 13. ERROR bit format. Address 23H**

If NSSR (bit 7) is '1', check the SENACT register value by reviewing steps 5, 6 and 7.

- 11) Offsets are sensor channel values when all LEDs are off. Write CTRL2 register with 04H to acquire the offset.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Value    | 0       | 0   | 0 | 0       | 0    | 1    | 0    | 0    |

**Figure 14. CTRL2 bit format. Address 02H**

- 12) Read the CTRL2 register. When GOFS (bit 2) goes '0', offsets are stored in the OFFSET\_X, OFFSET\_Y and OFFSET\_Z registers.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Value    | 0       | 0   | 0 | 0       | 0    | 0    | 0    | 0    |

**Figure 15. CTRL2 bit format. Address 02H**

- 13) Write CTRL2 register with 08H to set the SAGA (bit 3) to '1'.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Value    | 0       | 0   | 0 | 0       | 1    | 0    | 0    | 0    |

**Figure 16. CTRL2 bit format. Address 02H**

The sensor automatic gain adjustment is performed.

Wait for the sensor automatic gain adjustment to be completed. Alternatively, read the CTRL2 register to verify that SAGA (bit 3) is '0' before proceeding to next step.

- 14) Read the ERROR register (address 23H). Verify that NSSR (bit 7), BRIGHT (bit 3) and DIM (bit 4) are '0' before proceeding to the next step.

| Bit      | 7    | 6   | 5    | 4   | 3      | 2   | 1     | 0     |
|----------|------|-----|------|-----|--------|-----|-------|-------|
| Mnemonic | NSSR | RSV | NACK | DIM | BRIGHT | RSV | NLOCK | RANGE |
| Value    | 0    | X   | X    | 0   | 0      | X   | X     | X     |

**Figure 17. ERROR bit format. Address 23H**

If BRIGHT (bit 3) is '1', the following actions can be taken

- Decrease the peak current of the saturated channel.
- Review the sensor placement or increase the distance between the sensing area and the sensor. Ensure that there is no external ambient light interference if this is done.
- Review the filter design or insert neutral density gray filter.

If DIM (bit 4) is '1', the following actions can be taken

- Increase the peak current of the dim channel.
- Review the sensor placement or decrease the distance between the sensing area and the sensor.
- Review the filter design.
- Add more LEDs to the dim channel.
- Review frequency selection so that the SENACT value is higher and not more than 9.

If NSSR (bit 7) is '1' check the SENACT value.

Go to step 5 after these actions are done.

- 15) Write DUTYB\_LO with 3CH and DUTYB\_HI with 0FH. Write DUTYR\_HI, DUTYR\_LO, DUTYG\_HI and DUTYG\_LO with 00H. This will only turn on the blue LEDs. Red and green LEDs are turned off.

| Bit            | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---|---|---|---|---|
| DUTYB_LO Value | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| DUTYB_HI Value | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| DUTYG_LO Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DUTYG_HI Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DUTYR_LO Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DUTYR_HI Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 18. DUTY registers. Address 24H to 29H**

- 16) Write CTRL2 register with 80H to set UD\_DUTY to '1'.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Value    | 1       | 0   | 0 | 0       | 0    | 0    | 0    | 0    |

**Figure 19. CTRL2 format. Address 02H**

When UD\_DUTY (bit 7) of the CTRL2 register goes to '0', the duty values are updated.

- 17) Write CTRL2 register with 02H to set GSSR to '1'.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Value    | 0       | 0   | 0 | 0       | 0    | 0    | 1    | 0    |

**Figure 20. CTRL2 format. Address 02H**

- 18) When GSSR (bit 1) of the CTRL2 register goes to '0', read SENSOR\_ADCZ\_LO, SENSOR\_ADCZ\_HI, SENSOR\_ADCY\_LO, SENSOR\_ADCY\_HI, SENSOR\_ADCX\_LO, and SENSOR\_ADCX\_HI. These values are obtained when the blue LEDs are on.

These sensor values need to be written to the input registers in Table 1 before calibration data processing.

**Table 1. Sensor measurement and register storage before calibration data processing when the blue LEDs are on**

| SENSOR measurement | Input register to store before processing |
|--------------------|---|
| SENSOR_ADCZ_LO     | CAL_SMZB_LO                               |
| SENSOR_ADCZ_HI     | CAL_SMZB_HI                               |
| SENSOR_ADCY_LO     | CAL_SMYB_LO                               |
| SENSOR_ADCY_HI     | CAL_SMYB_HI                               |
| SENSOR_ADCX_LO     | CAL_SMXB_LO                               |
| SENSOR_ADCX_HI     | CAL_SMXB_HI                               |

- 19) Obtain the CIE camera measurement in CIE Y, x, y or X, Y, Z. If the measurement is in Y, x, y, it should be converted to X, Y, Z, using the equations below.

$$X = (Y/y) * x$$

$$Z = (Y/y) * (1 - x - y)$$

$$Y = Y$$

- 20) Write DUTYG\_LO with 3CH. Write DUTYG\_HI with 0FH. Write DUTYR\_HI, DUTYR\_LO, DUTYB\_HI and DUTYB\_LO with 00H. This will only turn on the green LEDs. Red and blue LEDs are turned off.

| Bit            | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---|---|---|---|---|
| DUTYB_LO Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DUTYB_HI Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DUTYG_LO Value | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| DUTYG_HI Value | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| DUTYR_LO Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DUTYR_HI Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 21. DUTY registers. Address 24H to 29H**

- 21) Write the CTRL2 register with 80H to set UD\_DUTY to '1'.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Value    | 0       | 0   | 0 | 0       | 0    | 0    | 1    | 0    |

**Figure 22. CTRL2 format. Address 02H**

When UD\_DUTY (bit 7) of the CTRL2 register goes to '0', the duty values are updated.

- 22) Write CTRL2 register with 02H to set GSSR to '1'.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Value    | 0       | 0   | 0 | 0       | 0    | 0    | 1    | 0    |

**Figure 23. CTRL2 format. Address 02H**

- 23) When GSSR (bit 1) of CTRL2 register goes to '0', read SENSOR\_ADCZ\_LO, SENSOR\_ADCZ\_HI, SENSOR\_ADCY\_LO, SENSOR\_ADCY\_HI, SENSOR\_ADCX\_LO, and SENSOR\_ADCX\_HI. These values are obtained when the green LEDs are on.

These sensor values need to be written to the input registers in Table 2 before calibration data processing.

**Table 2. Sensor measurement and register storage before calibration data processing when green LEDs are on**

| SENSOR measurement | Input register to store before processing |
|--------------------|---|
| SENSOR_ADCZ_LO     | CAL_SMZG_LO                               |
| SENSOR_ADCZ_HI     | CAL_SMZG_HI                               |
| SENSOR_ADCY_LO     | CAL_SMYG_LO                               |
| SENSOR_ADCY_HI     | CAL_SMYG_HI                               |
| SENSOR_ADCX_LO     | CAL_SMXG_LO                               |
| SENSOR_ADCX_HI     | CAL_SMXG_HI                               |

- 24) Obtain the CIE camera measurement in CIE Y, x, y or X, Y, Z. If the measurement is in Y, x, y, it should be converted to X, Y, Z.
- 25) Write DUTYR\_LO with 3CH. Write DUTYR\_HI with 0FH. Write DUTYG\_HI, DUTYG\_LO, DUTYB\_HI and DUTYB\_LO with 00H. This will only turn on the red LEDs. Green and blue LEDs are turned off.

| Bit            | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---|---|---|---|---|
| DUTYB_LO Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DUTYB_HI Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DUTYG_LO Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DUTYG_HI Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DUTYR_LO Value | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| DUTYR_HI Value | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Figure 24. DUTY registers. Address 24H to 29H**

- 26) Write the CTRL2 register with 80H to set UD\_DUTY to '1'.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Value    | 1       | 0   | 0 | 0       | 0    | 0    | 0    | 0    |

**Figure 25. CTRL2 format. Address 02H**

When UD\_DUTY (bit 7) of CTRL2 register goes to '0', the duty values are updated.

- 27) Write CTRL2 register with 02H to set GSSR to '1'.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Value    | 0       | 0   | 0 | 0       | 0    | 0    | 1    | 0    |

**Figure 26. CTRL2 format. Address 02H**

- 28) When GSSR (bit 1) of CTRL2 register goes to '0', read SENSOR\_ADCZ\_LO, SENSOR\_ADCZ\_HI, SENSOR\_ADCY\_LO, SENSOR\_ADCY\_HI, SENSOR\_ADCX\_LO, and SENSOR\_ADCX\_HI. These values are obtained when red LEDs are on.

These sensor values need to be written to the input registers in Table 3 before calibration data processing.

**Table 3. Sensor measurement and register storage before calibration data processing when red LEDs are on**

| SENSOR measurement | Register to store for processing |
|--------------------|----------------------------------|
| SENSOR_ADCZ_LO     | CAL_SMZR_LO                      |
| SENSOR_ADCZ_HI     | CAL_SMZR_HI                      |
| SENSOR_ADCY_LO     | CAL_SMYR_LO                      |
| SENSOR_ADCY_HI     | CAL_SMYR_HI                      |
| SENSOR_ADCX_LO     | CAL_SMXR_LO                      |
| SENSOR_ADCX_HI     | CAL_SMXR_HI                      |

- 29) Obtain the CIE camera measurement in CIE Y, x, y or X, Y, Z. If the measurement is in Y, x, y, it should be converted to X, Y, Z.
- 30) The X, Y, Z values obtained in step 19 for the blue LED, step 24 for the green LED and step 29 for the red LED are tabulated in Table 4.

The subscript represents the LED color that was turned on during measurement.

**Table 4. Tabulated camera measurements**

| Red LED on (step 29) | Green LED on (step 24) | Blue LED on (step 19) |
|----------------------|------------------------|-----------------------|
| X <sub>R</sub>       | X <sub>G</sub>         | X <sub>B</sub>        |
| Y <sub>R</sub>       | Y <sub>G</sub>         | Y <sub>B</sub>        |
| Z <sub>R</sub>       | Z <sub>G</sub>         | Z <sub>B</sub>        |

- 31) The maximum value of the set {X<sub>R</sub>, Y<sub>R</sub>, Z<sub>R</sub>, X<sub>G</sub>, Y<sub>G</sub>, Z<sub>G</sub>, X<sub>B</sub>, Y<sub>B</sub>, Z<sub>B</sub>} is determined. Assume that the maximum value is V<sub>M</sub>.
- 32) The Scale1 ratio is obtained by the equation below:

$$\text{Scale Value} = \frac{1000}{V_M}$$

- 33) All the elements of the set {X<sub>R</sub>, Y<sub>R</sub>, Z<sub>R</sub>, X<sub>G</sub>, Y<sub>G</sub>, Z<sub>G</sub>, X<sub>B</sub>, Y<sub>B</sub>, Z<sub>B</sub>} are multiplied by this Scale1 value. Let the scaled value be the set {X<sub>RR</sub>, Y<sub>RR</sub>, Z<sub>RR</sub>, X<sub>GG</sub>, Y<sub>GG</sub>, Z<sub>GG</sub>, X<sub>BB</sub>, Y<sub>BB</sub>, Z<sub>BB</sub>}.
- 34) If Y<sub>RR</sub> + Y<sub>GG</sub> + Y<sub>BB</sub> > 1000, then Scale2 ratio is obtained by the equation below:

$$\text{Scale2} = \frac{1000}{(Y_{RR} + Y_{GG} + Y_{BB})}$$

otherwise

$$\text{Scale2} = 1$$

- 35) All the elements of the set {X<sub>RR</sub>, Y<sub>RR</sub>, Z<sub>RR</sub>, X<sub>GG</sub>, Y<sub>GG</sub>, Z<sub>GG</sub>, X<sub>BB</sub>, Y<sub>BB</sub>, Z<sub>BB</sub>} are multiplied by this Scale2 value and converted to hexadecimal. Let the scaled and converter hexadecimal value be the set {X<sub>RRH</sub>, Y<sub>RRH</sub>, Z<sub>RRH</sub>, X<sub>GGH</sub>, Y<sub>GGH</sub>, Z<sub>GGH</sub>, X<sub>BBH</sub>, Y<sub>BBH</sub>, Z<sub>BBH</sub>}.
- 36) These values are stored to the input registers in Table 5, prior to calibration data processing.

**Table 5. Camera measurements and register storage before calibration data processing**

| Camera value(step 30) | Scale and converted hexadecimal value(step 35) | Input register to store |              |
|-----------------------|--|-------------------------|--------------|
|                       |  | Upper 2 bits            | Lower 8 bits |
| X <sub>R</sub>        | X <sub>RRH</sub>                               | CAL_CMXR_HI             | CAL_CMXR_LO  |
| Y <sub>R</sub>        | Y <sub>RRH</sub>                               | CAL_CMYR_HI             | CAL_CMYR_LO  |
| Z <sub>R</sub>        | Z <sub>RRH</sub>                               | CAL_CMZR_HI             | CAL_CMZR_LO  |
| X <sub>G</sub>        | X <sub>GGH</sub>                               | CAL_CMXG_HI             | CAL_CMXG_LO  |
| Y <sub>G</sub>        | Y <sub>GGH</sub>                               | CAL_CMYG_HI             | CAL_CMYG_LO  |
| Z <sub>G</sub>        | Z <sub>GGH</sub>                               | CAL_CMZG_HI             | CAL_CMZG_LO  |
| X <sub>B</sub>        | X <sub>BBH</sub>                               | CAL_CMXB_HI             | CAL_CMXB_LO  |
| Y <sub>B</sub>        | Y <sub>BBH</sub>                               | CAL_CMYB_HI             | CAL_CMYB_LO  |
| Z <sub>B</sub>        | Z <sub>BBH</sub>                               | CAL_CMZB_HI             | CAL_CMZB_LO  |

- 37) The measured sensor values obtained in steps 18, 23 and 28 and the scaled and converted hexadecimal camera values in step 36 are written to the ADJD-J823 registers listed in Table 12 of Appendix 2. Table 12 consists of input data from Tables 1, 2, 3, and 5 grouped together.
- 38) Write CTRL2 register with a value of 01H to set RCAL bit 0 to '1'. This will start processing of the calibration data.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Value    | 0       | 0   | 0 | 0       | 0    | 0    | 0    | 1    |

**Figure 27. CTRL2 format. Address 02H**

When RCAL bit 0 goes to '0', the calibration data processing is completed.

Note:

1. This step can only be done once.
2. If the calibration data processing is to be repeated, do step 36 before setting RCAL bit to '1'.

- 39) Write the CONFIG1 register to reset the PWME bit to '0' before saving the data to non-volatile memory.

| Bit      | 7   | 6 | 5 | 4 | 3 | 2     | 1      | 0    |
|----------|-----|---|---|---|---|-------|--------|------|
| Mnemonic | RSV |   |   |   |   | AUTOL | PWML   | PWME |
| Value    | 0   | 0 | 0 | 0 | 0 | 0     | Note a | 0    |

**Figure 28. CONFIG1 format. Address 03H**

Note a: Set PWML bit: '0' for PWM active high, '1' for PWM active low .

- 40) This step is recommended to improve the brightness change response of the ADJD-J823. To do this, the six calibration registers need to be swapped. The brightness change response time will be better if the following registers values are swapped before saving to dedicated EEPROM or external EEPROM.

CALDATA19 swapped with CALDATA21

CALDATA20 swapped with CALDATA24

CALDATA23 swapped with CALDATA25

The swapping of these registers can be accomplished by the use of two temporary registers TEMP1 at address DAH and TEMP2 at address DBH as follows:

Transfer register CALDATA19 (9Dh) to register TEMP1 (DAh).

Transfer register CALDATA21 (9Fh) to register TEMP2 (DBh).

Transfer register TEMP1 (DAh) to register CALDATA21 (9Fh).

Transfer register TEMP2 (DBh) to register CALDATA19 (9Dh).

Transfer register CALDATA20 (9Eh) to register TEMP1 (DAh).

Transfer register CALDATA24 (A2h) to register TEMP2 (DBh).

Transfer register TEMP1 (DAh) to register CALDATA24 (A2h).

Transfer register TEMP2 (DBh) to register CALDATA20 (9Eh).

Transfer register CALDATA23 (A1h) to register TEMP1 (DAh).

Transfer register CALDATA25 (A3h) to register TEMP2 (DBh).

Transfer register TEMP1 (DAh) to register CALDATA25 (A3h).

Transfer register TEMP2 (DBh) to register CALDATA23 (A1h).

These transfers are done using the I2C interface.

- 41) The data to be saved consists of 50 bytes of data and the PWML (bit 1) of CONFIG1 register. They must be entered back in normal operating mode to overwrite the default value after power on reset or software reset. These 50 bytes of data consist of offset, frequency, setup and calibration data listed in Tables 14, 15, 16 and 17.

For a system with dedicated EEPROM, write CTRL2 with 10H to set UPL\_CAL to '1'.

| Bit      | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|----------|---------|-----|---|---------|------|------|------|------|
| Mnemonic | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOF5 | GSSR | RCAL |
| Value    | 0       | 0   | 0 | 1       | 0    | 0    | 0    | 0    |

**Figure 29. CTRL2 format. Address 02H**

When UPL\_CAL bit 4 goes to '0', read the ERROR register. These data are saved to EEPROM if the NACK (bit 5) of the ERROR register is '0'.

- 42) The color gamut provided by the red, green and blue LEDs are given by the three points obtained in steps 19, 24 and 29.

## Normal Operating Procedure

All ADJD-J823 systems should follow the flow provided in the basic operating procedure. For a system with a dedicated EEPROM, the programming is simplified and AUTO LOAD is allowed. Refer to set up for auto-load operation, AUTO LOAD operating procedure or the stand alone procedure for more information.

### Color Set Point setting

The color set point or color point must be selected first. The color point is in the CIE 1931 Yxy color space. The inputs consist of the brightness and the color coordinates. The color coordinates is specified by the CIE\_X (CIE\_X\_HI and CIE\_X\_LO), and the CIE\_Y (CIE\_Y\_HI and CIE\_Y\_LO) registers. The value to be entered is the coordinate value multiplied by 1000.

i.e. CIE\_X = CIE 1931 x-coordinate \* 1000

CIE\_Y = CIE 1931 y-coordinate \* 1000

Example. The chosen color coordinates is a D65 white point with x = 0.313 and y = 0.329.

Enter 313 or 0139H to the CIE\_X register. For example, CIE\_X\_HI = 01H, and CIE\_X\_LO = 39H. Enter 329 or 0149H to the CIE\_Y register. For example, CIE\_Y\_HI = 01H, and CIE\_Y\_LO = 49H.

### Brightness

The brightness of the system depends on the following:

- BRIGHT value
- DEVICE\_L value

To avoid confusion, the DEVICE\_L must be programmed with 03E8H, (or decimal 1000). Thus, the system brightness depends solely on the BRIGHT value. With the BRIGHT value

set at the default maximum 0E79H (or decimal 3705), the system will display – the brightness at maximum output. This maximum is the system capability limit to produce the brightness at the color coordinates.

The maximum brightness depends on the chosen color coordinates and will change if the color coordinates change. For this reason, to correlate actual brightness with the BRIGHT register value, the system's actual brightness is measured when the BRIGHT value is at maximum or 0E79H and the DEVICE\_L fixed to 03E8H at the required color coordinates. Thus, for any arbitrary BRIGHT value, the actual brightness is given by

$$\frac{\text{BRIGHT Value}}{3705} \times \text{MML}$$

where MML is the measured brightness with the BRIGHT register set to 0E79H (or decimal 3705) and DEVICE\_L register set to 03E8H or (decimal 1000), at the required color coordinates.

### Response time

The response time of the color controller system can be improved at power on using methods described in application note 5254. Note the registers to be saved before power down are duty registers at address locations (24H - 29H), Table 1 and backup methodology registers at address locations (CAH to E1H and E6H to E7H) for the ADJD-J823. Users can use this technique in independent NVPR0M mode only.

To have better response time when brightness is changed, it is recommended that the programmed brightness (i.e. BRIGHT register) value should not be changed by more than 10% in less than 300 ms.

## Basic Operating Procedure

Figure 30 shows the flow chart for basic operating procedure.

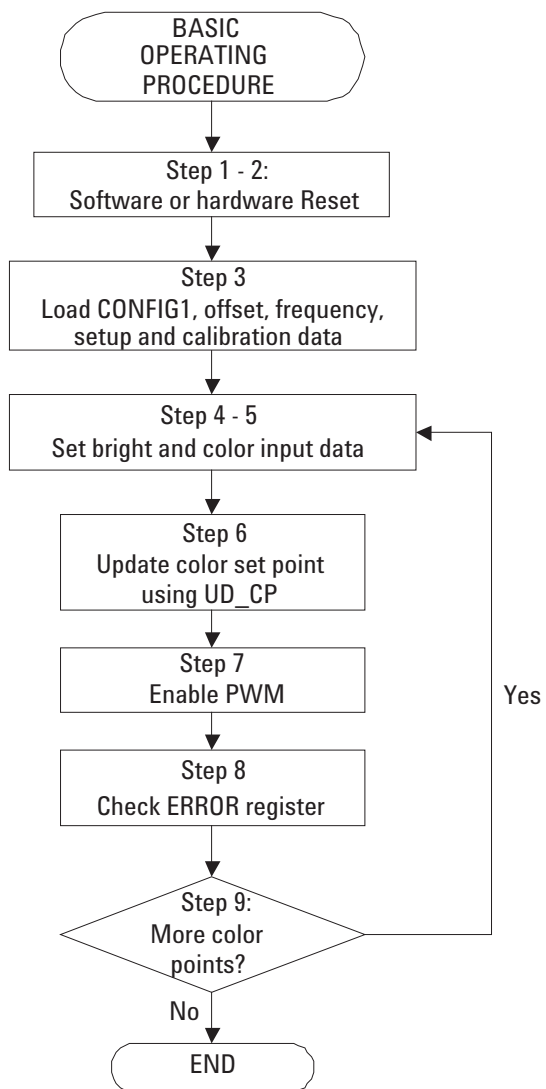


Figure 30. Basic operating flowchart

The procedure for the basic operating mode is as follows.

- 1) Do an external power on reset or perform a software reset. Software reset is done by writing CTRL1 with 01H to set RSW to '1'.

| Bit      | 7   | 6 | 5       | 4       | 3       | 2      | 1     | 0   |
|----------|-----|---|---------|---------|---------|--------|-------|-----|
| Mnemonic | RSV |   | DWL_CAL | UPL_ALL | DWL_ALL | UPL_CP | UD_CP | RSW |
| Value    | 0   | 0 | 0       | 0       | 0       | 0      | 0     | 1   |

**Figure 31. CTRL1 format. Address 01H**

- 2) Wait for the reset sequence to be completed. The status register (address 22H) can be read to verify that the INIT (bit 0) is set to "0" before proceeding.

| Bit      | 7   | 6 | 5 | 4 | 3   | 2     | 1    | 0    |
|----------|-----|---|---|---|-----|-------|------|------|
| Mnemonic | RSV |   |   |   | RSV | OPENL | NORM | INIT |
| Value    | 0   | 0 | 0 | 0 | 0   | 0     | 1    | 0    |

**Figure 32. STATUS register. Address 22H**

After power on reset or software reset, the DUTYR\_LO, DUTYR\_HI, DUTYG\_LO, DUTYG\_HI, DUTYB\_LO and DUTYB\_HI registers are '0'. The PWME bit of CONFIG1 register is set to '0'. This should turn off all the red, green and blue LEDs for an active high LED driver design.

However, for active low LED driver design, all the red, green and blue LEDs will turn on after a power or software reset.

- 3) Load the saved 51 bytes of data from non-volatile memory, starting with the CONFIG1 register. These 51 bytes of data have been saved in step 41 of the calibration procedure. For a system with dedicated EEPROM, download the 51 bytes of data from non-volatile memory by setting DWL\_CAL (bit 5) of the CTRL1 register high.

| Bit      | 7   | 6 | 5       | 4       | 3       | 2      | 1     | 0   |
|----------|-----|---|---------|---------|---------|--------|-------|-----|
| Mnemonic | RSV |   | DWL_CAL | UPL_ALL | DWL_ALL | UPL_CP | UD_CP | RSW |
| Value    | 0   | 0 | 1       | 0       | 0       | 0      | 0     | 0   |

**Figure 33. CTRL1 format. Address 01H**

- 4) Decide on the BRIGHT value. Write the BRIGHT\_HI register (address 1AH) and BRIGHT\_LO register (address 19H).
- 5) Write CIE\_X with CIE 1931 x-coordinate \* 1000. Write CIE\_Y with CIE 1931 y-coordinate \* 1000. Write DEVICE\_L with 1000. For example, write DEVICE\_L\_LO with E8H and DEVICE\_L\_HI with 03H.

Table 6 shows the data format.

**Table 6. Color set point format**

|             |  |
|-------------|--|
| DEVICE_L_HI | Write 3  |
| DEVICE_L_LO | Write 232                                      |
| CIE_X_HI    | Upper two bits of the integer value (x * 1000) |
| CIE_X_LO    | Lower 8 bits of the integer value (x * 1000)   |
| CIE_Y_HI    | Upper 2 bits of the integer value (y * 1000)   |
| CIE_Y_LO    | Lower 8 bits of the integer value (y * 1000)   |

Note:

1. All numbers in table 6 are decimal.
2. x - CIE 1931 chromaticity coordinate x
3. y - CIE 1931 chromaticity coordinate y

- 6) After entering the data in DEVICE\_L, CIE\_X and CIE\_Y, write the CTRL1 register with 02H to update the selected color point.

| Bit      | 7   | 6 | 5       | 4       | 3       | 2      | 1     | 0   |
|----------|-----|---|---------|---------|---------|--------|-------|-----|
| Mnemonic | RSV |   | DWL_CAL | UPL_ALL | DWL_ALL | UPL_CP | UD_CP | RSW |
| Value    | 0   | 0 | 0       | 0       | 0       | 0      | 1     | 0   |

**Figure 34. CTRL1 register. Address 01H**

When the UD\_CP bit goes '0', the color point data is updated.

- 7) Enable the PWM generator by setting the PWME (bit 0) of the CONFIG1 register high.

| Bit      | 7   | 6 | 5 | 4 | 3 | 2     | 1      | 0    |
|----------|-----|---|---|---|---|-------|--------|------|
| Mnemonic | RSV |   |   |   |   | AUTOL | PWML   | PWME |
| Value    | 0   | 0 | 0 | 0 | 0 | 0     | Note a | 1    |

**Figure 35. CONFIG1 format. Address 03H**

Note: a) Set PWML bit: '0' for PWM active high, '1' for PWM active low.

The ADJD-J823 system will display the specified color point.

- 8) Read the ERROR register (address 23H) to determine if there is any ERROR.

| Bit      | 7      | 6   | 5    | 4   | 3      | 2   | 1      | 0      |
|----------|--------|-----|------|-----|--------|-----|--------|--------|
| Mnemonic | NSSR   | RSV | NACK | DIM | BRIGHT | RSV | NLOCK  | RANGE  |
| Value    | Note a | X   | X    | X   | X      | X   | Note b | Note c |

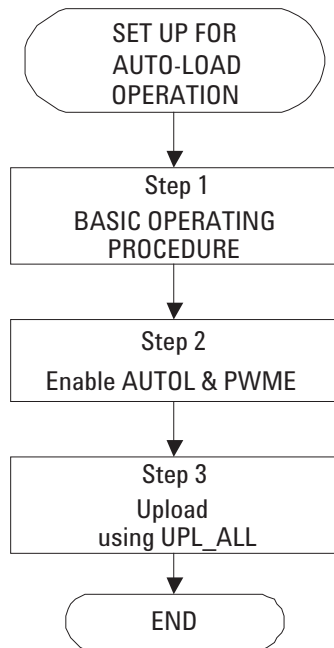
**Figure 36. ERROR register. Address 23H**

Notes:

- If NSSR (bit 7) of ERROR register is '1': NSSR error. Refer to step 7 of calibration procedure to enter the correct value for SENACT register. The calibration procedure must be done again to correct this error.
  - If NLOCK (bit 1) of ERROR register is '1': No Lock error. The required color set point could not be achieved. A value of '0': indicates the require color point is achieved.
  - If RANGE (bit 0) is '1': Out of Range error. Required color set point is outside the sensor measurement range. Previous set point is maintained.
- If the application is for multi-color points selection, steps 4, 5, 6 and 8 can be repeated to select a different color point.
  - If the application is for a single color point and there is no error in the previous step, the set up, color point and calibration data can be saved for stand-alone operation. Do the procedure outline in "Set up for stand-alone operation" section.

## Set up for Stand-alone Operation

Figure 37 shows the flowchart to setup the system for stand-alone operation.



**Figure 37. Flowchart to set up auto-load or stand-alone operation**

This section is applicable for a system with a dedicated EEPROM.

- 1) The basic operating procedure flow (Figure 30) from step 1 to step 8 must be done first.
- 2) Set AUTOL (bit 2) and PWME (bit 0) of CONFIG1 register to '1'.

| Bit      | 7   | 6 | 5 | 4 | 3 | 2     | 1      | 0    |
|----------|-----|---|---|---|---|-------|--------|------|
| Mnemonic | RSV |   |   |   |   | AUTOL | PWML   | PWME |
| Value    | 0   | 0 | 0 | 0 | 0 | 1     | Note a | 1    |

**Figure 38. CONFIG1 format. Address 03H**

Note: a) Set PWML bit: '0' for PWM active high, '1' for PWM active low.

- 3) Set UPL\_ALL (bit 4) of CTRL1 register to '1'.

| Bit      | 7   | 6 | 5       | 4       | 3       | 2      | 1     | 0   |
|----------|-----|---|---------|---------|---------|--------|-------|-----|
| Mnemonic | RSV |   | DWL_CAL | UPL_ALL | DWL_ALL | UPL_CP | UD_CP | RSW |
| Value    | 0   | 0 | 0       | 1       | 0       | 0      | 0     | 0   |

**Figure 39. CTRL1 register. Address 01H**

When UPL\_ALL bit goes '0', read the ERROR register. The 71 bytes of data consisting of the CONFIG1 register, offset, frequency, set up, calibration, brightness and color data are completely uploaded to the EEPROM if NACK (bit 5) of the ERROR register is '0'. These 71 bytes of data include the CONFIG1 register and data listed in Tables 14, 15, 16, 17, 18 and 19.

The next time the system is powered on, the system will automatically display the stored color point. Refer to the auto-load operating procedure for more information.

## Auto-load Operating Procedure

This section is applicable for a system with dedicated EEPROM. The flowchart is applicable to system after the set up for stand-alone operation has been done.

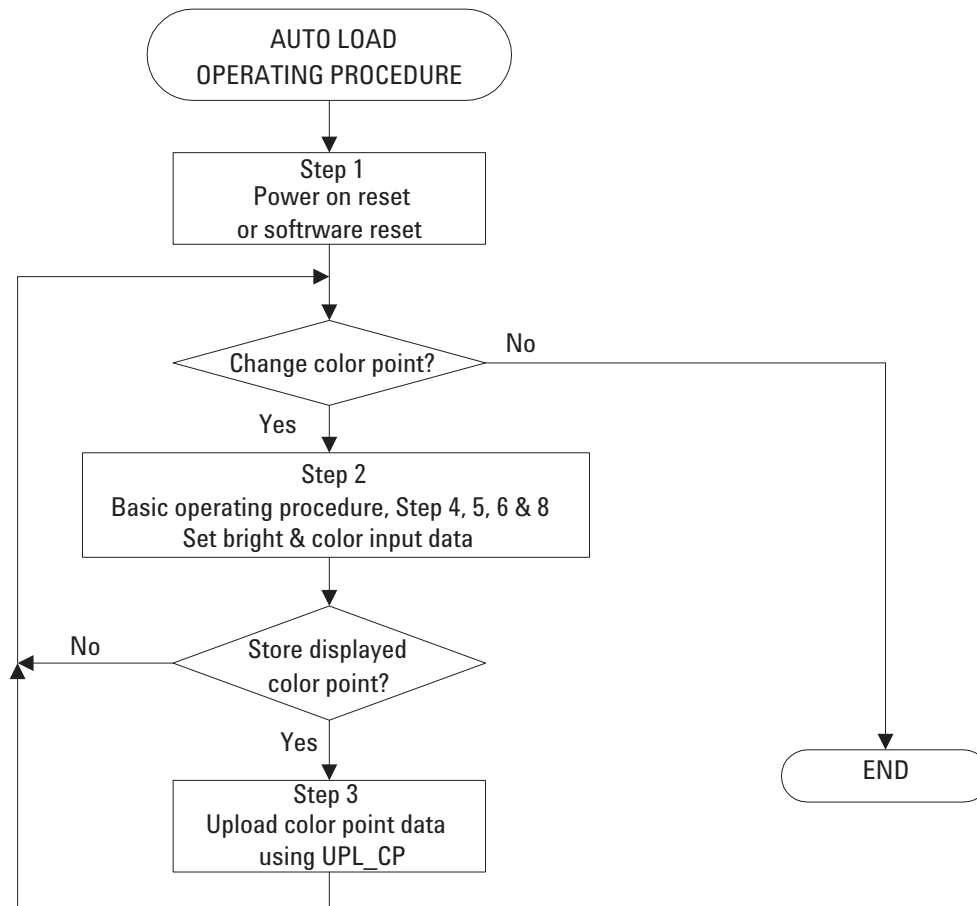


Figure 40. Auto-load operating procedure flowchart

- 1) Do an external power on reset or software reset. The setup, color set point and calibration data including CONFIG1 register setting will auto load. The stored color point will be displayed.
- 2) To change the color set point, i.e. to display a different color set point, perform steps 4, 5, 6 and 8 of the basic operating procedure.
- 3) If the stored color point is to be changed to the displayed color point, set UPL\_CP (bit 2) of CTRL1 register to '1'.

| Bit      | 7   | 6 | 5       | 4       | 3       | 2      | 1     | 0   |
|----------|-----|---|---------|---------|---------|--------|-------|-----|
| Mnemonic | RSV |   | DWL_CAL | UPL_ALL | DWL_ALL | UPL_CP | UD_CP | RSW |
| Value    | 0   | 0 | 0       | 0       | 0       | 1      | 0     | 0   |

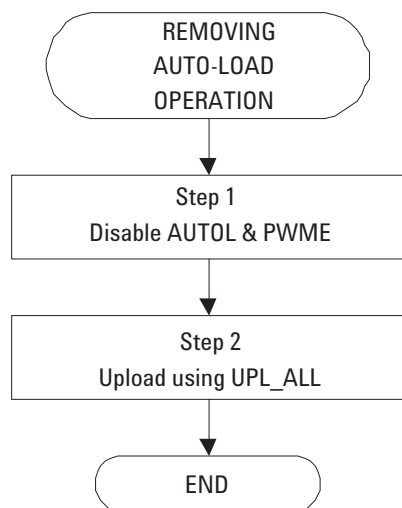
Figure 41. CTRL1 register. Address 01H

When UPL\_CP bit goes '0', read the ERROR register. The color set point data listed in Table 19 are completely uploaded to EEPROM if NACK (bit 5) of ERROR register is '0'.

The next time the system is turned on, the system will automatically display the new stored color point.

## Removing the Auto-load Operation

Figure 42 shows the flowchart to remove the auto-load operation.



**Figure 42. Flowchart to remove auto-load operation**

This section applies to a system with dedicated EEPROM.

- 1) After external power on reset or software reset, set AUTOL (bit 2) and PWME (bit 0) of CONFIG1 register to '0'.

| Bit      | 7   | 6 | 5 | 4 | 3 | 2     | 1      | 0    |
|----------|-----|---|---|---|---|-------|--------|------|
| Mnemonic | RSV |   |   |   |   | AUTOL | PWML   | PWME |
| Value    | 0   | 0 | 0 | 0 | 0 | 0     | Note a | 0    |

**Figure 43. CONFIG1 format. Address 03H**

Note: a) Set PWML bit: '0' for PWM active high, '1' for PWM active low.

- 2) Set UPL\_ALL (bit 4) of CTRL1 register to '1'.

| Bit      | 7   | 6 | 5       | 4       | 3       | 2      | 1     | 0   |
|----------|-----|---|---------|---------|---------|--------|-------|-----|
| Mnemonic | RSV |   | DWL_CAL | UPL_ALL | DWL_ALL | UPL_CP | UD_CP | RSW |
| Value    | 0   | 0 | 0       | 1       | 0       | 0      | 0     | 0   |

**Figure 44. CTRL1 register. Address 01H**

When the UPL\_ALL bit goes '0', read the ERROR register. The CONFIG1 register and the other 70 bytes of data are completely uploaded to EEPROM if NACK (bit 5) of ERROR register is '0'.

The next time the system is turned on, the system will not auto-load. The steps outlined in the basic operating procedure must be done to display the color set point.

## Appendix 1. Register Name, Width and Bit Format

**Table 7. Register name and width**

| Register name | Width | Table |
|---------------|-------|-------|
| CTRL1         | 8     | 9     |
| CTRL2         | 8     | 9     |
| CONFIG1       | 8     | 9     |
| CONFIG2       | 8     | 9     |
| STATUS        | 8     | 9     |
| ERROR         | 8     | 9     |
|               |       |       |
| DUTYB         | 12    | 10    |
| DUTYG         | 12    | 10    |
| DUTYR         | 12    | 10    |
|               |       |       |
| SENSOR_ADCZ   | 10    | 11    |
| SENSOR_ADCY   | 10    | 11    |
| SENSOR_ADCX   | 10    | 11    |
|               |       |       |
| CAL_CMZB      | 10    | 12    |
| CAL_CMYB      | 10    | 12    |
| CAL_CMXB      | 10    | 12    |
| CAL_CMZG      | 10    | 12    |
| CAL_CMYG      | 10    | 12    |
| CAL_CMXG      | 10    | 12    |
| CAL_CMZR      | 10    | 12    |
| CAL_CMYR      | 10    | 12    |
| CAL_CMXR      | 10    | 12    |
|               |       |       |
|               |       |       |
|               |       |       |

| Register name         | Width | Table   |
|-----------------------|-------|---------|
| CAL_SMZB              | 10    | 12      |
| CAL_SMYB              | 10    | 12      |
| CAL_SMXB              | 10    | 12      |
| CAL_SMZG              | 10    | 12      |
| CAL_SMYG              | 10    | 12      |
| CAL_SMXG              | 10    | 12      |
| CAL_SMZR              | 10    | 12      |
| CAL_SMYR              | 10    | 12      |
| CAL_SMXR              | 10    | 12      |
|                       |       |         |
| SENACT                | 8     | 13      |
|                       |       |         |
| OFFSET_Z              | 8     | 14      |
| OFFSET_Y              | 8     | 14      |
| OFFSET_X              | 8     | 14      |
|                       |       |         |
| PWMFREQ               | 8     | 15      |
| SAMPFREQ              | 16    | 15      |
|                       |       |         |
| SETUP 0 to SETUP24    | 8     | 16 & 18 |
|                       |       |         |
| CALDATA0 to CALDATA30 | 8     | 17      |
|                       |       |         |
| BRIGHT                | 12    | 19      |
| CIE_Y                 | 10    | 19      |
| CIE_X                 | 10    | 19      |
| DEVICE_L              | 10    | 19      |

Refer to the table listed in the 'Table' column for more information.

**Table 8. Register bit format**

| Width   | Register name |        | Format |       |       |       |       |       |       |       |
|---------|---------------|--------|--------|-------|-------|-------|-------|-------|-------|-------|
|         |               |        | Bit 7  | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 10 bits | REG[9:0]      | REG_LO | R7     | R6    | R5    | R4    | R3    | R2    | R1    | R0    |
|         |               | REG_HI |        |       |       |       |       |       | R9    | R8    |
|         |               |        |        |       |       |       |       |       |       |       |
| 12 bits | REG[11:0]     | REG_LO | R7     | R6    | R5    | R4    | R3    | R2    | R1    | R0    |
|         |               | REG_HI |        |       |       |       | R11   | R10   | R9    | R8    |
|         |               |        |        |       |       |       |       |       |       |       |
| 16 bits | REG[16:0]     | REG_LO | R7     | R6    | R5    | R4    | R3    | R2    | R1    | R0    |
|         |               | REG_HI | R15    | R14   | R13   | R12   | R11   | R10   | R9    | R8    |

Note

1. REG is any register with bit width greater than 8. Refer to table 7 for register name.
2. REG\_LO is the lower byte and REG\_HI is the upper byte.
3. R0 is least significant bit.

## Appendix 2. Register List By Group

**Table 9. General control, configuration, status and error register**

|    | Register | BIT 7   | BIT 6 | BIT 5   | BIT 4   | BIT 3   | BIT 2  | BIT 1 | BIT 0 | Reset Value Hex |
|----|----------|---------|-------|---------|---------|---------|--------|-------|-------|-----------------|
| 01 | CTRL1    | RSV     |       | DWL_CAL | UPL_ALL | DWL_ALL | UPL_CP | UD_CP | RSW   | 00              |
| 02 | CTRL2    | UD_DUTY | RSV   |         | UPL_CAL | SAGA    | GOFS   | GSSR  | RCAL  | 00              |
| 03 | CONFIG1  | RSV     |       |         |         |         | AUTOL  | PWML  | PWME  | 00              |
| 04 | CONFIG2  | RSV     |       |         |         |         |        |       | OPMD  | 00              |
| 22 | STATUS   | RSV     |       |         |         |         | OPENL  | NORM  | INIT  | 02              |
| 23 | ERROR    | NSSR    | RSV   | NACK    | DIM     | BRIGHT  | RSV    | NLOCK | RANGE | 00              |

**Table 10. Duty registers**

| Address Hex | Register | Description                   | Reset Value Hex |
|-------------|----------|-------------------------------|-----------------|
| 24          | DUTYB_LO | Blue LED duty. Lower 8 bits.  | 00              |
| 25          | DUTYB_HI | Blue LED duty. Upper 4 bits.  | 00              |
| 26          | DUTYG_LO | Green LED duty. Lower 8 bits. | 00              |
| 27          | DUTYG_HI | Green LED duty. Upper 4 bits. | 00              |
| 28          | DUTYR_LO | Red LED duty. Lower 8 bits.   | 00              |
| 29          | DUTYR_HI | Red LED duty. Upper 4 bits.   | 00              |

**Table 11. Sensor ADC output measurement registers**

| Address Hex | Register       | Description                               | Reset Value Hex |
|-------------|----------------|---|-----------------|
| 84          | SENSOR_ADCZ_LO | Sensor channel Z ADC value. Lower 8 bits. | 00              |
| 85          | SENSOR_ADCZ_HI | Sensor channel Z ADC value. Upper 2 bits. | 00              |
| 86          | SENSOR_ADCY_LO | Sensor channel Y ADC value. Lower 8 bits. | 00              |
| 87          | SENSOR_ADCY_HI | Sensor channel Y ADC value. Upper 2 bits. | 00              |
| 88          | SENSOR_ADCX_LO | Sensor channel X ADC value. Lower 8 bits. | 00              |
| 89          | SENSOR_ADCX_HI | Sensor channel X ADC value. Upper 2 bits. | 00              |

**Table 12. Input registers for calibration data processing**

| Address Hex | Register    | Description  | Reset Value Hex |
|-------------|-------------|--|-----------------|
| DC          | CAL_CMZB_LO | Scaled camera Z value when only blue LED on. Lower 8 bits  | 00              |
| DD          | CAL_CMZB_HI | Scaled camera Z value when only blue LED on. Upper 2 bits  | 00              |
| DE          | CAL_CMYB_LO | Scaled camera Y value when only blue LED on. Lower 8 bits  | 00              |
| DF          | CAL_CMYB_HI | Scaled camera Y value when only blue LED on. Upper 2 bits  | 00              |
| E0          | CAL_CMXB_LO | Scaled camera X value when only blue LED on. Lower 8 bits  | 00              |
| E1          | CAL_CMXB_HI | Scaled camera X value when only blue LED on. Upper 2 bits  | 00              |
| E2          | CAL_CMZG_LO | Scaled camera Z value when only green LED on. Lower 8 bits | 00              |
| E3          | CAL_CMZG_HI | Scaled camera Z value when only green LED on. Upper 2 bits | 00              |
| E4          | CAL_CMYG_LO | Scaled camera Y value when only green LED on. Lower 8 bits | 00              |
| E5          | CAL_CMYG_HI | Scaled camera Y value when only green LED on. Upper 2 bits | 00              |
| E6          | CAL_CMXG_LO | Scaled camera X value when only green LED on. Lower 8 bits | 00              |
| E7          | CAL_CMXG_HI | Scaled camera X value when only green LED on. Upper 2 bits | 00              |
| E8          | CAL_CMZR_LO | Scaled camera Z value when only red LED on. Lower 8 bits   | 00              |
| E9          | CAL_CMZR_HI | Scaled camera Z value when only red LED on. Upper 2 bits   | 00              |
| EA          | CAL_CMYR_LO | Scaled camera Y value when only red LED on. Lower 8 bits   | 00              |
| EB          | CAL_CMYR_HI | Scaled camera Y value when only red LED on. Upper 2 bits   | 00              |
| EC          | CAL_CMXR_LO | Scaled camera X value when only red LED on. Lower 8 bits   | 00              |
| ED          | CAL_CMXR_HI | Scaled camera X value when only red LED on. Upper 2 bits   | 00              |
| EE          | CAL_SMZB_LO | SENSOR_ADCZ_LO value when only blue LED on. Lower 8 bits   | 00              |
| EF          | CAL_SMZB_HI | SENSOR_ADCZ_HI value when only blue LED on. Upper 2 bits   | 00              |
| F0          | CAL_SMYB_LO | SENSOR_ADCY_LO value when only blue LED on. Lower 8 bits   | 00              |
| F1          | CAL_SMYB_HI | SENSOR_ADCY_HI value when only blue LED on. Upper 2 bits   | 00              |
| F2          | CAL_SMXB_LO | SENSOR_ADCX_LO value when only blue LED on. Lower 8 bits   | 00              |
| F3          | CAL_SMXB_HI | SENSOR_ADCX_HI value when only blue LED on. Upper 2 bits   | 00              |
| F4          | CAL_SMZG_LO | SENSOR_ADCZ_LO value when only green LED on. Lower 8 bits  | 00              |
| F5          | CAL_SMZG_HI | SENSOR_ADCZ_HI value when only green LED on. Upper 2 bits  | 00              |
| F6          | CAL_SMYG_LO | SENSOR_ADCY_LO value when only green LED on. Lower 8 bits  | 00              |
| F7          | CAL_SMYG_HI | SENSOR_ADCY_HI value when only green LED on. Upper 2 bits  | 00              |
| F8          | CAL_SMXG_LO | SENSOR_ADCX_LO value when only green LED on. Lower 8 bits  | 00              |
| F9          | CAL_SMXG_HI | SENSOR_ADCX_HI value when only green LED on. Upper 2 bits  | 00              |
| FA          | CAL_SMZR_LO | SENSOR_ADCZ_LO value when only red LED on. Lower 8 bits    | 00              |
| FB          | CAL_SMZR_HI | SENSOR_ADCZ_HI value when only red LED on. Upper 2 bits    | 00              |
| FC          | CAL_SMYR_LO | SENSOR_ADCY_LO value when only red LED on. Lower 8 bits    | 00              |
| FD          | CAL_SMYR_HI | SENSOR_ADCY_HI value when only red LED on. Upper 2 bits    | 00              |
| FE          | CAL_SMXR_LO | SENSOR_ADCX_LO value when only red LED on. Lower 8 bits    | 00              |
| FF          | CAL_SMXR_HI | SENSOR_ADCX_HI value when only red LED on. Upper 2 bits    | 00              |

**Table 13. Sensor acquisition constant**

| Address Hex | Register | Description                 | Reset Value Hex |
|-------------|----------|-----------------------------|-----------------|
| A9          | SENACT   | Sensor acquisition constant | 00              |

**Table 14. Offset registers**

| Address Hex | Register | Description | Reset Value Hex |
|-------------|----------|-------------|-----------------|
| 81          | OFFSET_Z | OFFSET Z    | 3C              |
| 82          | OFFSET_Y | OFFSET Y    | 3C              |
| 83          | OFFSET_X | OFFSET X    | 3C              |

**Table 15. Frequency registers**

| Address Hex | Register    | Description                         | Reset Value Hex |
|-------------|-------------|-------------------------------------|-----------------|
| 05          | PWMFREQ     | Pulse Width Modulation Frequency    | 00              |
| 06          | SAMPFREQ_LO | Sensor Sampling Frequency Low Byte  | 30              |
| 07          | SAMPFREQ_HI | Sensor Sampling Frequency High Byte | 75              |

**Table 16. Setup registers**

| Address Hex | Register | Description     | Reset Value Hex |
|-------------|----------|-----------------|-----------------|
| 08          | SETUP0   | Setup Registers | 2D              |
| 09          | SETUP1   |                 | 07              |
| 0A          | SETUP2   |                 | 07              |
| 0B          | SETUP3   |                 | 07              |
| 0C          | SETUP4   |                 | 1F              |
| 0D          | SETUP5   |                 | 1F              |
| 0E          | SETUP6   |                 | 1F              |
| 0F          | SETUP7   |                 | 07              |
| 10          | SETUP8   |                 | 07              |
| 11          | SETUP9   |                 | 07              |
| 1B          | SETUP10  |                 | 7F              |
| 1F          | SETUP11  |                 | 3C              |
| 20          | SETUP12  |                 | 0F              |

**Table 17. Calibration registers**

| <b>Address<br/>Hex</b> | <b>Register</b> | <b>Description</b>  | <b>Reset<br/>Value<br/>Hex</b> |
|------------------------|-----------------|---------------------|--------------------------------|
| 8A                     | CALDATA0        | Calibration data 0  | FF                             |
| 8B                     | CALDATA1        | Calibration data 1  | 0C                             |
| 8C                     | CALDATA2        | Calibration data 2  | 32                             |
| 8D                     | CALDATA3        | Calibration data 3  | 08                             |
| 8E                     | CALDATA4        | Calibration data 4  | DD                             |
| 8F                     | CALDATA5        | Calibration data 5  | 81                             |
| 90                     | CALDATA6        | Calibration data 6  | 79                             |
| 91                     | CALDATA7        | Calibration data 7  | 02                             |
| 92                     | CALDATA8        | Calibration data 8  | 7B                             |
| 93                     | CALDATA9        | Calibration data 9  | 1E                             |
| 94                     | CALDATA10       | Calibration data 10 | 0F                             |
| 95                     | CALDATA11       | Calibration data 11 | 8A                             |
| 96                     | CALDATA12       | Calibration data 12 | 24                             |
| 97                     | CALDATA13       | Calibration data 13 | 83                             |
| 98                     | CALDATA14       | Calibration data 14 | DB                             |
| 99                     | CALDATA15       | Calibration data 15 | 83                             |
| 9A                     | CALDATA16       | Calibration data 16 | 39                             |
| 9B                     | CALDATA17       | Calibration data 17 | 18                             |
| 9C                     | CALDATA18       | Calibration data 18 | 7F                             |
| 9D                     | CALDATA19       | Calibration data 19 | 8F                             |
| 9E                     | CALDATA20       | Calibration data 20 | 88                             |
| 9F                     | CALDATA21       | Calibration data 21 | A8                             |
| A0                     | CALDATA22       | Calibration data 22 | 6E                             |
| A1                     | CALDATA23       | Calibration data 23 | 8B                             |
| A2                     | CALDATA24       | Calibration data 24 | 85                             |
| A3                     | CALDATA25       | Calibration data 25 | 8E                             |
| A4                     | CALDATA26       | Calibration data 26 | 62                             |
| A5                     | CALDATA27       | Calibration data 27 | 1C                             |
| A6                     | CALDATA28       | Calibration data 28 | 03                             |
| A7                     | CALDATA29       | Calibration data 29 | FD                             |
| A8                     | CALDATA30       | Calibration data 30 | 0F                             |

**Table 18. Setup registers**

| Address<br>Hex | Register | Description     | Reset<br>Value<br>Hex |
|----------------|----------|-----------------|-----------------------|
| 00             | SETUP13  | Setup registers | 58                    |
| 12             | SETUP14  |                 | 1E                    |
| 13             | SETUP15  |                 | 04                    |
| 14             | SETUP16  |                 | 64                    |
| 15             | SETUP17  |                 | 00                    |
| 16             | SETUP18  |                 | 00                    |
| 17             | SETUP19  |                 | 50                    |
| 18             | SETUP20  |                 | 04                    |
| E2             | SETUP21  |                 | 30                    |
| E3             | SETUP22  |                 | 08                    |
| E4             | SETUP23  |                 | 04                    |
| E5             | SETUP24  |                 | 04                    |

**Table 19. Bright and color input registers**

| Address<br>Hex | Register    | Description                         | Reset<br>Value<br>Hex |
|----------------|-------------|-------------------------------------|-----------------------|
| 19             | BRIGHT_LO   | Brightness Control Low Byte         | 79                    |
| 1A             | BRIGHT_HI   | Brightness Control High Byte        | 0E                    |
| E8             | CIE_Y_LO    | CIE 1931 y-coordinate. Lower 8 bits | 00                    |
| E9             | CIE_Y_HI    | CIE 1931 y-coordinate. Upper 2 bits | 00                    |
| EA             | CIE_X_LO    | CIE 1931 x-coordinate. Lower 8 bits | 00                    |
| EB             | CIE_X_HI    | CIE 1931 x-coordinate. Upper 2 bits | 00                    |
| EC             | DEVICE_L_LO | Device luminance. Lower 8 bits      | 00                    |
| ED             | DEVICE_L_HI | Device luminance. Upper 2 bits      | 00                    |

### Appendix 3. Register Description

#### CTRL1: Control 1 Register (01H)

|             | 7   | 6 | 5       | 4       | 3       | 2      | 1     | 0   |
|-------------|-----|---|---------|---------|---------|--------|-------|-----|
| Mnemonic    | RSV |   | DWL_CAL | UPL_ALL | DWL_ALL | UPL_CP | UD_CP | RSW |
| Reset Value | 0   | 0 | 0       | 0       | 0       | 0      | 0     | 0   |

Figure A01: Control 1 Register Format

Table 20: Control 1 Register bit descriptions

| Mnemonic | Read or Write | Description  |
|----------|---------------|--|
| RSV      | N/A           | Reserved. Value is 0.  |
| DWL_CAL  | R/W           | Download calibration mode data. Set this bit high to download from EEPROM. The 50 bytes consisting of offsets, frequency, setup and calibration data (table 14, 15, 16 and 17) is loaded to the device. The PWML (bit 1) is also loaded to the CONFIG1 register. Other CONFIG1 bits are reset to 0. The device resets this bit low once all data downloads completely. This operation is available only in close loop mode.              |
| UPL_ALL  | R/W           | Upload all data. Set this bit high to upload to EEPROM. The data uploaded are CONFIG1 register and 70 bytes consisting of offset, frequency, setup, calibration, brightness and color data listed in Tables 14, 15, 16, 17, 18 & 19. The device resets this bit low once all registers are uploaded to EEPROM. This operation is available only in close loop mode.  |
| DWL_ALL  | R/W           | Download all data. Set this bit high to download from EEPROM. The CONFIG1 register and 70 bytes consisting of offset, frequency, setup, calibration, brightness and color input data (Tables 14 to 19) are downloaded. The device resets this bit low once all data downloads to the device. This operation is available only in close loop mode.  |
| UPL_CP   | R/W           | Upload color set point. Set this bit high to upload the current displayed color point data to EEPROM. These 8 bytes of data consist of brightness and color input data listed in Table 19. The device resets this bit low once data is completely uploaded to the EEPROM. This is useful when the device is already set to auto load. Refer to AUTO LOAD operating procedure. This operation is available only in normal operation mode. |
| UD_CP    | R/W           | Update color set point. Set this bit high to update the color set point in the device. This operation will transfer user color set point data to the device color set point and display the color. Color set point data includes color coordinates and brightness data listed in Table 19. The device resets this bit low once the color point data is updated.  |
| RSW      | R/W           | Reset Software. Set this bit high to perform a soft reset. The device clears this bit low during reset. The INIT (bit 0) of the STATUS register will be cleared to low once a reset is completed.  |

**CTRL2: Control 2 Register (02H)**

| Bit         | 7       | 6   | 5 | 4       | 3    | 2    | 1    | 0    |
|-------------|---------|-----|---|---------|------|------|------|------|
| Mnemonic    | UD_DUTY | RSV |   | UPL_CAL | SAGA | GOFS | GSSR | RCAL |
| Reset Value | 0       | 0   | 0 | 0       | 0    | 0    | 0    | 0    |

**Figure A02: Control 2 register format****Table 21: Control 2 register bit descriptions**

| Mnemonic | Read or Write | Description  |
|----------|---------------|--|
| UD_DUTY  | R/W           | Update duty. Set high to set the PWM, PWMG and PWMB pulse width to the corresponding specified duty values in RED LED duty, Green LED duty and Blue LED duty. PWME (bit 0) of the CONFIG1 register must be set to high for this update. The device will reset this bit low once the duty values are updated. This operation is only available in open loop mode.                               |
| RSV      | N/A           | Reserved. Value is 0.  |
| UPL_CAL  | R/W           | Upload calibration mode data. Set high to upload 50 bytes consisting of offset, frequency, setup and calibration data (Tables 14, 15, 16, and 17) to EEPROM. Only PWML (bit 1) of CONFIG1 register is uploaded. The device resets this bit low once data uploads completely. This operation is available only in open loop mode.   |
| SAGA     | R/W           | Sensor Auto Gain Adjustment. Set high to perform auto-gain adjustment to optimize the sensor acquisition. PWME (bit 0) of the CONFIG1 register must be set to high for this operation. Also, the SENACT register must be defined properly before running SAGA. The device resets this bit low once optimum sensor adjustment is completed. This operation is only available in open loop mode. |
| GOFS     | R/W           | Get Offsets. Set this bit high to acquire the offset values from each channel. The device reset this bit low once offset values are acquired. Offset values are stored in the OFFSET_X, OFFSET_Y and OFFSET_Z registers respectively. This operation is available only in open loop mode.  |
| GSSR     | R/W           | Get sensor readings. Set this bit high to acquire sensor readings. The device resets this bit low once sensor acquisition is completed for all channels. Sensor values are stored in the SENSOR_ADCX, SENSOR_ADCY and SENSOR_ADCZ registers respectively. This operation is available only in open loop mode.  |
| RCAL     | R/W           | Run Calibration. Set this bit high to compute calibration data. The device resets this bit low once computation is completed. This operation is available only in open loop mode.  |

**CONFIG1: Configuration 1 Register (03H)**

|             | 7   | 6 | 5 | 4 | 3 | 2     | 1    | 0    |
|-------------|-----|---|---|---|---|-------|------|------|
| Mnemonic    | RSV |   |   |   |   | AUTOL | PWML | PWME |
| Reset Value | 0   | 0 | 0 | 0 | 0 | 0     | 0    | 0    |

**Figure A03: Configuration 1 register format****Table 22: Configuration 1 register bit descriptions**

| Mnemonic | Read or Write | Description   |
|----------|---------------|---|
| RSV      | N/A           | Reserved. Value is 0.   |
| AUTOL    | R/W           | Self Download Enable. When “1”, the device will download all registers from EEPROM upon power up or software reset. Since the default value is “0”, this bit must be uploaded to EEPROM as high for self download operation. If PWME (bit 0) of the CONFIG1 register is stored as high in EEPROM, a system will try to download a color point from EEPROM. When “0”, a device will not download data from EEPROM. |
| PWML     | R/W           | Pulse Width Modulation Level select. When “1”, PWM output is active low. When “0”, PWM output is active high.   |
| PWME     | R/W           | Pulse Width Modulation Enable. When “1”, a PWM generator is enabled and LEDs can be turned ON. When “0”, a PWM generator is disabled and LEDs can be turned off.  |

**CONFIG2: Configuration 2 Register (04H)**

|             | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0    |
|-------------|-----|---|---|---|---|---|---|------|
| Mnemonic    | RSV |   |   |   |   |   |   | OPMD |
| Reset Value | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0    |

**Figure A04: Configuration 2 register format****Table 23: Configuration 2 register bit descriptions**

| Mnemonic | Read or Write | Description  |
|----------|---------------|--|
| RSV      | N/A           | Reserved. Value is 0.  |
| OPMD     | R/W           | Software Operation Mode. When “1”, the device is configured to operate in the open loop mode. When “0”, the device is configured to operate in the normal mode with sensor feedback. |

**STATUS: STATUS Register (22H)**

|             | 7   | 6 | 5 | 4 | 3 | 2     | 1    | 0    |
|-------------|-----|---|---|---|---|-------|------|------|
| Mnemonic    | RSV |   |   |   |   | OPENL | NORM | INIT |
| Reset Value | 0   | 0 | 0 | 0 | 0 | 0     | 1    | 0    |

**Figure A05. Configuration 2 register format****Table 24: Configuration 2 register bit descriptions**

| Mnemonic | Read or Write | Description   |
|----------|---------------|---|
| RSV      | N/A           | Reserved. Value is 0.   |
| OPENL    | R             | Open Loop Mode Flag. "1" indicates the device is in open loop mode and "0" indicates the device is not in open loop mode.       |
| NORM     | R             | Normal Loop Mode Flag. "1" indicates the device is in normal loop mode and "0" indicates the device is not in normal loop mode. |
| INIT     | R             | Initialization Mode Flag. "1" indicates the device is performing initialization. "0" indicates initialization is completed.     |

**ERROR: ERROR register (23H)**

|             | 7    | 6   | 5    | 4   | 3      | 2   | 1     | 0     |
|-------------|------|-----|------|-----|--------|-----|-------|-------|
| Mnemonic    | NSSR | RSV | NACK | DIM | BRIGHT | RSV | NLOCK | RANGE |
| Reset Value | 0    | 0   | 0    | 0   | 0      | 0   | 0     | 0     |

**Figure A06. ERROR register format**

**Table 25. ERROR register bit descriptions**

| Mnemonic | Read or Write | Description  |
|----------|---------------|--|
| NSSR     | R             | Invalid SENACT value. "1" indicates the device failed to complete sensor acquisition. Review the PWMFREQ, SAMPFREQ and SENACT register values and run the calibration procedure again. "0" indicates the device is able to complete sensor acquisition.  |
| NACK     | R             | No Acknowledge From EEPROM Flag. "1" indicates that no acknowledge signal was received from EEPROM or that the I2C communication with EEPROM was not successful. "0" indicates that acknowledge signal from the EEPROM was received and thus I2C communication with the EEPROM was successful. |
| DIM      | R             | Light Sources Dim Flag. "1" indicates that the light source is too dim. Review your sensor placement, filter or LED driver peak current design. "0" indicates the light source is not dim.   |
| BRIGHT   | R             | Light Sources Bright Flag. "1" indicates that light source is too bright. Review you sensor placement, filter and LED driver peak current design. "0" indicates the light source is not bright.  |
| RSV      | N/A           | Reserved. Ignore this bit.   |
| NLOCK    | R             | No Lock Flag. When '1', the required color set point cannot be achieved. When '0', the required color set point is achieved.   |
| RANGE    | R             | Out of Range Flag. '1' indicates the required color set point is lying outside the sensor measurement range and that the previous valid color set point is maintained. '0' indicates the required color set point is lying within sensor measurement range.                                    |

**PWMFREQ: Pulse Width Modulation Frequency Register (05H)**

|             | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Mnemonic    | PWMFREQ[7:0] |   |   |   |   |   |   |   |
| Reset Value | 0            | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure A07: Pulse Width Modulation frequency register format****Table 26: Pulse Width Modulation frequency register bit description**

| Mnemonic      | Read or Write | Description  |
|---------------|---------------|--|
| PWM-FREQ[7:0] | R/W           | <p>PWM Frequency setting</p> $\text{PWM Frequency} = \frac{\text{Clock Frequency}}{(\text{PWMFREQ} + 1) \times 4096}$ <p>Default nominal PWM frequency is 6.35 kHz with clock frequency of 26 MHz.</p> |

**SAMPFREQ: Sensor Sampling Frequency Register (06H~07H)****SAMPFREQ\_LO: Sensor Sampling Frequency Register (06H)**

|             | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---|---|---|---|---|---|---|
| Mnemonic    | SAMPFREQ[7:0] |   |   |   |   |   |   |   |
| Reset Value | 0             | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

**Figure A08: Sensor sampling frequency low byte register format****SAMPFREQ\_HI: Sensor Sampling Frequency Register (07H)**

|             | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|---|---|---|---|---|---|---|
| Mnemonic    | SAMPFREQ[15:8] |   |   |   |   |   |   |   |
| Reset Value | 0              | 1 | 1 | 1 | 0 | 1 | 0 | 1 |

**Figure A09: Sensor sampling frequency high byte register format****Table 27: Sensor sampling frequency register bit description**

| Mnemonic        | Read or Write | Description   |
|-----------------|---------------|---|
| SAMP-FREQ[15:0] | R/W           | <p>Sensor Sampling Frequency setting. The selected sampling frequency must ensure that the PWM frequency divided by the sampling frequency is at least four. For example, the PWM frequency must be at least four times the sampling frequency.</p> $\text{Sampling Frequency} = \frac{\text{Clock Frequency}}{\text{SAMPFREQ} \times 8}$ <p>Default nominal sampling frequency is 108 Hz with clock frequency of 26 MHz.</p> |

**SENACT: Sensor Acquisition Constant Register (A9H)**

|             | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Mnemonic    | SENACT[7:0] |   |   |   |   |   |   |   |
| Reset Value | 0           | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure A10: SENACT: Sensor acquisition constant register format**

**Table 28. SENACT register bit description**

| Mnemonic         | Read or Write | Description   |
|------------------|---------------|---|
| SEN-<br>ACT[7:0] | R/W           | <p>Sensor acquisition constant. Value is given by the equation:</p> $\text{SENACT} = 1/3 * \left\{ \frac{\text{SAMPFREQ}}{512(\text{PWMFREQ} + 1)} - 1 \right\} - 1$ <p>Rounded down to nearest integer.</p> <p>If SENACT is less than 0, the PWM frequency and the sampling frequency must be changed so that the PWM frequency is at least four times the sampling frequency.</p> <p>SENACT = 9, if the calculated value is greater than 9.</p> <p>If PWMFREQ = 0, SAMPFREQ = 7530H (or decimal 30000),<br/> SENACT = <math>1/3 * \{ 57.59375 \} - 1</math><br/> = 18.1979<br/> = 9</p> |

**BRIGHT: Brightness Control Register (19H ~ 1AH)**

BRIGHT\_LO: Brightness Control Low Byte Register (19H).

|             | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|---|---|---|---|---|---|---|
| Mnemonic    | BRIGHT_LO[7:0] |   |   |   |   |   |   |   |
| Reset Value | 0              | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

**Figure A11. BRIGHT\_LO register format**

BRIGHT\_HI: Brightness Control High Byte Register (1AH).

|             | 7   | 6 | 5 | 4 | 3               | 2 | 1 | 0 |
|-------------|-----|---|---|---|-----------------|---|---|---|
| Mnemonic    | RSV |   |   |   | BRIGHT_HI[11:8] |   |   |   |
| Reset Value | 0   | 0 | 0 | 0 | 1               | 1 | 1 | 0 |

**Figure A12. BRIGHT\_HI register format****Table 29. BRIGHT register bit description**

| Mnemonic         | Read or Write | Description   |
|------------------|---------------|---|
| RSV              | N/A           | Reserved. Value is '0'.   |
| BRIGHT<br>[11:0] | R/W           | <p>Brightness Control Register. The device will change the light source brightness by limiting the stabilized maximum PWM duty factor to be less than the value of BRIGHT. The default maximum BRIGHT value is 0E79H or decimal 3705. Do not exceed this maximum value. Brightness is scaled with respect to the ratio of BRIGHT/0E79H. For example, to scale the brightness by 50%, a value 073DH or decimal 1853 is written to the BRIGHT register.</p> |

**CIE\_Y: CIE 1931 y-coordinate Register (E8H~E9H)**

CIE\_Y\_LO: CIE 1931 y-coordinate Low Byte Register (E8H).

| Bit         | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------|---|---|---|---|---|---|---|
| Mnemonic    | CIE_Y[7:0] |   |   |   |   |   |   |   |
| Reset Value | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure A13. CIE 1931 y-coordinate low byte register format**

CIE\_Y\_HI: CIE 1931 y-coordinate High Byte Register (E9H).

| Bit         | 7   | 6 | 5 | 4 | 3 | 2 | 1          | 0 |
|-------------|-----|---|---|---|---|---|------------|---|
| Mnemonic    | RSV |   |   |   |   |   | CIE_Y[9:8] |   |
| Reset Value | 0   | 0 | 0 | 0 | 0 | 0 | 0          | 0 |

**Figure A14. CIE 1931 y-coordinate high byte register format****Table 30. CIE\_Y register bit description**

| Mnemonic       | Read or Write | Description   |
|----------------|---------------|---|
| RSV            | N/A           | Reserved. Value is '0'.   |
| CIE_Y<br>[9:0] | R/W           | CIE 1931 y-coordinate register.<br>Value<br>CIE 1931 chromaticity y-coordinate * 1000 |

**CIE\_X: CIE 1931 x-coordinate Register (EAH~EBH)**

CIE\_X\_LO: CIE 1931 x-coordinate Low Byte Register (EAH).

| Bit         | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------|---|---|---|---|---|---|---|
| Mnemonic    | CIE_X[7:0] |   |   |   |   |   |   |   |
| Reset Value | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure A15. CIE 1931 x-coordinate low byte register format**

CIE\_X\_HI: CIE 1931 x-coordinate High Byte Register (EBH).

| Bit         | 7   | 6 | 5 | 4 | 3 | 2 | 1          | 0 |
|-------------|-----|---|---|---|---|---|------------|---|
| Mnemonic    | RSV |   |   |   |   |   | CIE_X[9:8] |   |
| Reset Value | 0   | 0 | 0 | 0 | 0 | 0 | 0          | 0 |

**Figure A16. CIE 1931 x-coordinate high byte register format****Table 31. CIE\_X register bit description**

| Mnemonic   | Read or Write | Description   |
|------------|---------------|---|
| RSV        | N/A           | Reserved. Value is '0'.   |
| CIE_X[9:0] | R/W           | CIE 1931 x-coordinate register.<br>Value<br>CIE 1931 chromaticity x-coordinate * 1000 |

## DEVICE\_L: Device Luminance Register (ECH~EDH)

DEVICE\_L\_LO: Device Luminance Low Byte Register (ECH).

| Bit         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---|---|---|---|---|---|---|
| Mnemonic    | DEVICE_L[7:0] |   |   |   |   |   |   |   |
| Reset Value | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Figure A17. Device luminance low byte register format

DEVICE\_L\_HI: Device Luminance High Byte Register (EDH).

| Bit         | 7   | 6 | 5 | 4 | 3 | 2 | 1             | 0 |
|-------------|-----|---|---|---|---|---|---------------|---|
| Mnemonic    | RSV |   |   |   |   |   | DEVICE_L[9:8] |   |
| Reset Value | 0   | 0 | 0 | 0 | 0 | 0 | 0             | 0 |

Figure A18. Device luminance high byte register format

Table 32. DEVICE\_L register bit description

| Mnemonic      | Read or Write | Description   |
|---------------|---------------|---|
| RSV           | N/A           | Reserved. Value is '0'.   |
| DEVICE_L[9:0] | R/W           | Device luminance register.<br>Device luminance value is set to 03E8H. |

## Appendix 4. EEPROM Locations

**Table 33. EEPROM locations applicable to UPL\_ALL or DWL\_ALL**

| EPROM<br>LOCATION | REGISTER    |      |
|-------------------|-------------|------|
|                   | NAME        | ADDR |
| 01                | SETUP13     | 00   |
| 02                | CONFIG1     | 03   |
| 03                | PWMFREQ     | 05   |
| 04                | SAMPFREQ_LO | 06   |
| 05                | SAMPFREQ_HI | 07   |
| 06                | SETUP0      | 08   |
| 07                | SETUP1      | 09   |
| 08                | SETUP2      | 0A   |
| 09                | SETUP3      | 0B   |
| 0A                | SETUP4      | 0C   |
| 0B                | SETUP5      | 0D   |
| 0C                | SETUP6      | 0E   |
| 0D                | SETUP7      | 0F   |
| 0E                | SETUP8      | 10   |
| 0F                | SETUP9      | 11   |
| 10                | SETUP14     | 12   |
| 11                | SETUP15     | 13   |
| 12                | SETUP16     | 14   |
| 13                | SETUP17     | 15   |
| 14                | SETUP18     | 16   |
| 15                | SETUP19     | 17   |
| 16                | SETUP20     | 18   |
| 17                | BRIGHT_LO   | 19   |
| 18                | BRIGHT_HI   | 1A   |
| 19                | CIE_Y_LO    | E8   |
| 1A                | CIE_Y_HI    | E9   |
| 1B                | CIE_X_LO    | EA   |
| 1C                | CIE_X_HI    | EB   |
| 1D                | DEVICE_L_LO | EC   |
| 1E                | DEVICE_L_HI | ED   |
| 1F                | SETUP21     | E2   |
| 20                | SETUP22     | E3   |
| 21                | SETUP23     | E4   |
| 22                | SETUP24     | E5   |
| 23                | OFFSET_Z    | 81   |
| 24                | OFFSET_Y    | 82   |

| EPROM<br>LOCATION | REGISTER  |      |
|-------------------|-----------|------|
|                   | NAME      | ADDR |
| 25                | OFFSET_X  | 83   |
| 26                | CALDATA0  | 8A   |
| 27                | CALDATA1  | 8B   |
| 28                | CALDATA2  | 8C   |
| 29                | CALDATA3  | 8D   |
| 2A                | CALDATA4  | 8E   |
| 2B                | CALDATA5  | 8F   |
| 2C                | CALDATA6  | 90   |
| 2D                | CALDATA7  | 91   |
| 2E                | CALDATA8  | 92   |
| 2F                | CALDATA9  | 93   |
| 30                | CALDATA10 | 94   |
| 31                | CALDATA11 | 95   |
| 32                | CALDATA12 | 96   |
| 33                | CALDATA13 | 97   |
| 34                | CALDATA14 | 98   |
| 35                | CALDATA15 | 99   |
| 36                | CALDATA16 | 9A   |
| 37                | CALDATA17 | 9B   |
| 38                | CALDATA18 | 9C   |
| 39                | CALDATA19 | 9D   |
| 3A                | CALDATA20 | 9E   |
| 3B                | CALDATA21 | 9F   |
| 3C                | CALDATA22 | A0   |
| 3D                | CALDATA23 | A1   |
| 3E                | CALDATA24 | A2   |
| 3F                | CALDATA25 | A3   |
| 40                | CALDATA26 | A4   |
| 41                | CALDATA27 | A5   |
| 42                | CALDATA28 | A6   |
| 43                | CALDATA29 | A7   |
| 44                | CALDATA30 | A8   |
| 45                | SETUP10   | 1B   |
| 46                | SETUP11   | 1F   |
| 47                | SETUP12   | 20   |
| 48                | NOT USED  |      |

**Table 34. EEPROM locations used in DWL\_CAL or UPL\_CAL**

| EPROM<br>LOCATION | REGISTER    |      |
|-------------------|-------------|------|
|                   | NAME        | ADDR |
| 02                | CONFIG1     | 03   |
| 03                | PWMFREQ     | 05   |
| 04                | SAMPFREQ_LO | 06   |
| 05                | SAMPFREQ_HI | 07   |
| 06                | SETUP0      | 08   |
| 07                | SETUP1      | 09   |
| 08                | SETUP2      | 0A   |
| 09                | SETUP3      | 0B   |
| 0A                | SETUP4      | 0C   |
| 0B                | SETUP5      | 0D   |
| 0C                | SETUP6      | 0E   |
| 0D                | SETUP7      | 0F   |
| 0E                | SETUP8      | 10   |
| 0F                | SETUP9      | 11   |
| 23                | OFFSET_Z    | 81   |
| 24                | OFFSET_Y    | 82   |
| 25                | OFFSET_X    | 83   |
| 26                | CALDATA0    | 8A   |
| 27                | CALDATA1    | 8B   |
| 28                | CALDATA2    | 8C   |
| 29                | CALDATA3    | 8D   |
| 2A                | CALDATA4    | 8E   |
| 2B                | CALDATA5    | 8F   |
| 2C                | CALDATA6    | 90   |
| 2D                | CALDATA7    | 91   |
| 2E                | CALDATA8    | 92   |

| EPROM<br>LOCATION | REGISTER  |      |
|-------------------|-----------|------|
|                   | NAME      | ADDR |
| 2F                | CALDATA9  | 93   |
| 30                | CALDATA10 | 94   |
| 31                | CALDATA11 | 95   |
| 32                | CALDATA12 | 96   |
| 33                | CALDATA13 | 97   |
| 34                | CALDATA14 | 98   |
| 35                | CALDATA15 | 99   |
| 36                | CALDATA16 | 9A   |
| 37                | CALDATA17 | 9B   |
| 38                | CALDATA18 | 9C   |
| 39                | CALDATA19 | 9D   |
| 3A                | CALDATA20 | 9E   |
| 3B                | CALDATA21 | 9F   |
| 3C                | CALDATA22 | A0   |
| 3D                | CALDATA23 | A1   |
| 3E                | CALDATA24 | A2   |
| 3F                | CALDATA25 | A3   |
| 40                | CALDATA26 | A4   |
| 41                | CALDATA27 | A5   |
| 42                | CALDATA28 | A6   |
| 43                | CALDATA29 | A7   |
| 44                | CALDATA30 | A8   |
| 45                | SETUP10   | 1B   |
| 46                | SETUP11   | 1F   |
| 47                | SETUP12   | 20   |
|                   |           |      |

Note: For CONFIG1 register, only PWML bit is uploaded or downloaded. Other bits are reset to 0.

**Table 35. EEPROM locations used in UPL\_CP**

| EPROM<br>LOCATION | REGISTER    |      |
|-------------------|-------------|------|
|                   | NAME        | ADDR |
| 17                | BRIGHT_LO   | 19   |
| 18                | BRIGHT_HI   | 1A   |
| 19                | CIE_Y_LO    | E8   |
| 1A                | CIE_Y_HI    | E9   |
| 1B                | CIE_X_LO    | EA   |
| 1C                | CIE_X_HI    | EB   |
| 1D                | DEVICE_L_LO | EC   |
| 1E                | DEVICE_L_HI | ED   |

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