Desaturation Fault Detection

Optocoupler Gate Drive Products with Feature:
ACPL-333J, ACPL-330J, ACPL-332J, ACPL-331J and HCPL-316J

Application Note 5324

1. Introduction

A desaturation fault detection circuit provides protection for power semiconductor switches (IGBT or MOSFETs) against short-circuit current events which may lead to destruction of these power switches. This desaturation of the inverters can also occur due to an insufficient gate drive signal caused by inverter gate driver misperformance or by driver supply voltage issues. Other failure modes that can potentially cause excessive currents and excessive power dissipation in the inverters can be due to phase and/or rail supply short circuits due to incorrect user connections or bad wiring, control signal failures due to noise or computational errors, over load conditions induced by the load, and component failures in the gate drive circuitry. The drastically increased power dissipation very quickly overheats the power inverter and destroys it. To prevent catastrophic damage to the drive, desaturation fault detection and protection must be implemented to reduce or turn-off the overcurrents during the fault condition. This application note covers the design of the desaturation fault detection feature in Avago intelligent gate drivers.

How does the desaturation fault detection feature work in Avago drivers?

i. Fault Detection

The IGBT collector-emitter voltage, VCESAT, is monitored by the DESAT pin of the gate drive optocoupler (Pin 14 of Figure 1a and 1b). When there is short circuit in an application and a very high current flow through the IGBT, it will go into the desaturation mode; hence its VCESAT voltage will rise. A fault is detected by the optocoupler gate driver (while the IGBT is on) once this VCESAT voltage goes above the internal desaturation fault detection threshold voltage, which is typically 7.0 V. This fault detection triggers two events:

a. Vout of the optocoupler gate driver is slowly brought low in order to "softly" turn off the IGBT and prevent large di/dt induced voltage spikes.

b. An internal feedback channel is activated which brings the Fault output low for the purpose of notifying the microcontroller of the fault condition. At this point, the microcontroller must take the appropriate action to shutdown or reset the motor drive.

ii. Soft Turn-off

This feature exists in Avago gate optocouplers, (e.g. ACPL-333J, ACPL-330J, ACPL-332J, ACPL-331J and HCPL-316J). When a fault is detected by the DESAT feature, a weak pull-down device in the output drive stage will turn on to 'softly' turn off the IGBT and prevents large di/dt induced voltages. This device slowly discharges the IGBT gate to prevent fast changes in collector current that could cause damaging voltage spikes due to stray inductances. During the slow turn off, the large output pull-down device remains off until the output voltage falls below V_{EE} + 2 V, at which time the large pull-down device clamps the IGBT gate to V_{EE}.

iii. Off State and Reset

During the IGBT off state, the driver fault detection circuitry is disabled to prevent false 'fault' signals. The fault output, Pin 3 of Figure 1a, is pulled down and output Pin 11 goes low for the duration of the fault. In the ACPL-333J and ACPL-330J, the fault is self-reset after a fixed mute time of typically 26 μs. In the ACPL-332J and ACPL-331J, the fault is reset at the next positive input signal to the driver after a fixed mute time. The HCPL-316J has to be reset externally through the Reset pin (Pin 5 of Figure 1b). For both case, the reset will only be cleared when DESAT detection has gone to low (short-circuit is cleared).

iv. Undervoltage Lockout (UVLO) with Hysteresis

The output of the optocoupler gate driver and the FAULT status are controlled by a combination of V_{IN}, UVLO, and the detected IGBT DESAT condition. During power up, the UVLO feature prevents the application of insufficient gate voltage to the IGBT, by forcing the output of the optocoupler gate driver low. Once the power supply of the optocoupler gate driver is above the positive UVLO thresholds, the DESAT detection feature is the primary source of IGBT protection. The output of the optocoupler is safely brought low once the power supply of the optocoupler falls below the negative UVLO threshold level. Hysteresis in the positive UVLO and negative UVLO threshold levels provides an appropriate noise margin for the UVLO detection and output shutdown features.

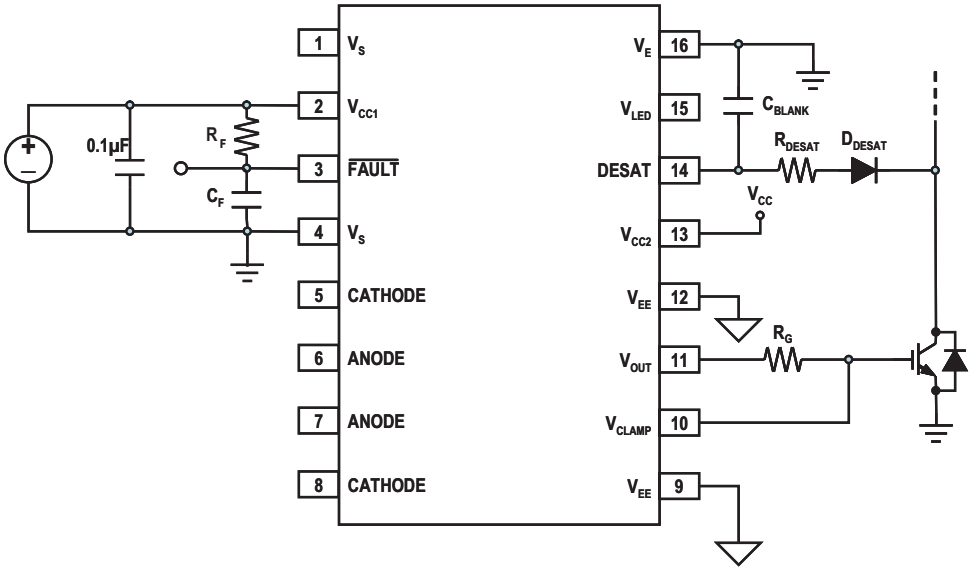

Figure 1a. Desaturation detection circuit for the ACPL-333J, ACPL-330J, ACPL-332J and ACPL-331J.

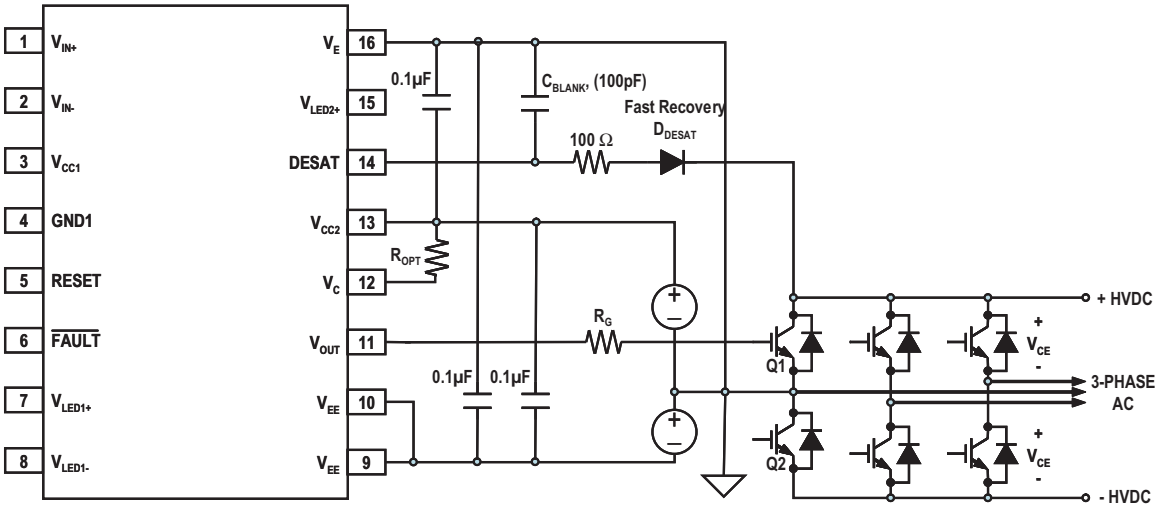

Figure 1b. Desaturation detection circuit for the HCPL-316J

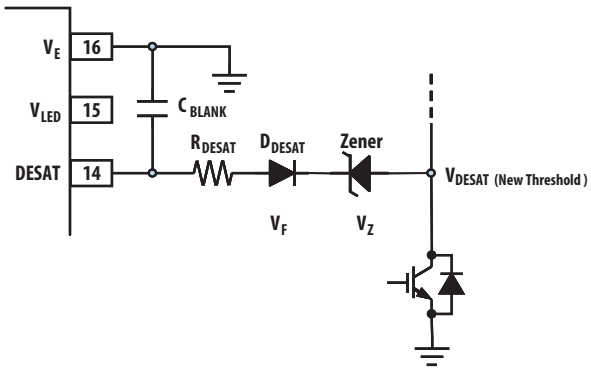

Figure 2. Zener diode and diode connection to adjust the DESAT threshold voltage

2. Basic DESAT detector circuit component selection

For typical applications, the three external components required to build the DESAT circuit are the DESAT diode, D_{DESAT}, DESAT resistor, R_{DESAT}, and blank capacitor, C_{BLANK}.

Blanking Time

The DESAT fault detection circuitry should remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the DESAT threshold. The time period, called the DESAT blanking time, ensures that there is no nuisance tripping during IGBT turn-on. This time also represents the time it takes for the driver to detect a fault condition. The blanking time is controlled by the internal DESAT charge current, I_{CHG}, of 250 μA (typ), the DESAT voltage threshold, V_{DESAT}, and the external blank capacitor, C_{BLANK}.

During operation, blank capacitor is discharged when the driver output is low (IGBT off). That is, the DESAT detection features becomes active only when the output of the gate driver optocoupler is in the high state, driving the IGBT into saturation. When the IGBT is turned on, the DESAT capacitor starts charging and protection becomes effective only if the DESAT threshold is exceeded after the blanking time.

Blanking Time Capacitor Sizing

$$t_{BLANK} = \frac{C_{BLANK} * V_{DESAT}}{I_{CHG}} \qquad (1)$$

Blanking time is determined using formula (1):

The recommended value is 100 pF which gives a blank time of 2.6 μs (Condition: I_{CHG} = 250 μA and V_{DESAT} = 6.5 V; Page 9 of the HCPL-316J datasheet AV01-0579EN).

HV Blocking Diode and DESAT Threshold

The DESAT diode function is to conduct forward current, allowing sensing of the IGBT's V_{CESAT}. In a high power application, the DESAT pin may be pulled low due to reverse recovery spikes of the freewheeling diode. This reverse recovery spike tend to forward bias the substrate diode of the HCPL-316J, which may respond by generating a "false" detection signal. In order to minimize this charging current and avoid false DESAT triggering, it is best to use very fast reverse recovery time diodes with very small reverse parasitic capacitance. Listed in the table below are fast-recovery diodes that are suitable for use as the DESAT diode, DDESAT.

The DESAT detection threshold voltage of 7 V (typical) can be reduced by placing a string of DESAT diodes in series or by placing a a low voltage zener diode in series with the DESAT diode.

For the string of DESAT diodes method,

$$V_{DESAT\ (New\ Threshold)} = 7.0 - n * V_F \qquad (2)$$

For the DESAT diode with Zener Diode method,

$$V_{DESAT\ (New\ Threshold)} = 7.0 - V_F - V_Z \qquad (3)$$

where n is the number of DESAT diodes, Vz is the zener voltage value and V_f is the forward voltage of DESAT diode. This allow the designer to choose the appropriate threshold voltage. Refer to Figure 2 for a diode and zener diode connection diagram.

DESAT Resistor

The anti-parallel diode of the IGBT can have a large instantaneous forward voltage transient which exceeds the nominal forward voltage of the diode. This may result in a large negative voltage spike on the DESAT pin which will draw a substantial amount of current out of the driver. To limit the current level drawn from the gate driver, a DESAT resistor can be added (100 Ω recommended) in series with the DESAT diode. The added resistor will not appreciably alter the DESAT threshold or the blanking time.

FAULT Output Pin

The FAULT pin (Pin 3 of the ACPL-332J/331J and Pin 6 of the HCPL-316J) is an open collector output and requires a pull-up resistor, RF (2.1 kΩ for ACPL-332J and 331J, 3.3 kΩ for HCPL-316J), to provide a high level signal. In order to prevent the FAULT pin from being "triggered" by high CMR noise, a filter capacitor, C_F, is included between the FAULT pin and ground (Figure 1a).

Part Number	Manufacturer	Trr (ns)	Max. Reverse Voltage Rating, VRRM (Volts)	Package Type
ERA34-10	Fuji Semiconductor	15	1000	Axial Leaded
MUR1100E	Motorola	75	1000	59-04 (axial leaded)
UF4007	General Semiconductor	75	1000	DO-204AL (axial leaded)
BYM26E	Philips	75	1000	SOD64 (axial leaded)
BYV26E	Philips	75	1000	SOD57 (axial leaded)
BYV99	Philips	75	600	SOD87 (surface mount)
MURS160T3	Motorola	75	600	Case 403A (surface mount)

3. Advanced desaturation detection topic

Internal Charging Current Source, ICHG, Wide Variation

The "blanking capacitor charge current" parameter in the data sheet (page 9 of the HCPL-316J datasheet), is listed as:

Blanking Capacitor Charging Current, I_{CHG}	Min	Typ	Max	Units
	130	250	330	μA

Based on a 7 V desaturation voltage threshold and the above charging current, we will get three different blanking time values; minimum, typical and maximum value.

$$I_{CHG} = C * \frac{\delta V}{\delta t} \qquad (3)$$

Using the above formula, the three I_{CHG} values, C_{BLANK} = 100 pF (Figure 1) and ΔV=7 V, we will have the following blanking times,

$$\Delta t\,(max) = \frac{100\ pF * 7V}{130\ \mu A} = 5.38\ \mu s$$

$$\Delta t\,(typ) = \frac{100\ pF * 7V}{250\ \mu A} = 2.8\ \mu s$$

$$\Delta t\,(min) = \frac{100\ pF * 7V}{330\ \mu A} = 2.12\ \mu s$$

For some application, this variation may not be a problem. However, to minimize the above variation, several external blanking circuits are suggested in this Application Note. These are shown in figures 3, 4 and 5.

4. Prevent false fault detection due to negative voltage spikes during power semiconductor switching operation

One of the situations that may cause the driver to generate a false fault signal is if the substrate diode of the driver becomes forward biased. This can happen if the reverse recovery spikes coming from the IGBT free wheeling diodes bring the DESAT pin below ground. Hence the DESAT pin voltage will be 'brought' above the threshold voltage. This negative going voltage spikes is typically generated by inductive loads or reverse recovery spikes of the IGBT/MOSFETs free-wheeling diodes.

In order to prevent a false fault signal, it is highly recommended to connect a zener diode and schottky diode across the DESAT pin and VE pin (e.g. for HCPL-316J, between pin 14 and 16). This circuit solution is shown in Figure 3. The schottky diode will prevent the substrate diode of the gate driver optocoupler from being forward biased while the zener diode (value around 7.5 to 8 V) is used to prevent any positive high transient voltage to affect the DESAT pin.

5. Other methods of tweaking DESAT detection blanking time

Besides the recommended circuits to adjust blanking time in Figures 1 and 2, two other methods are introduced in this application note. The first method, shown in Figures 3 and 4, uses additional capacitors, a resistor and a FET. The second simpler method, shown in Figure 5, requires only one additional resistor plus scaling of the blanking capacitor, CBLANK. The figures show how this can be connected using a HCPL-316J. This circuitry is applicable with other similar drivers like the ACPL-332J. Each of these circuitries must always come with a schottky diode connected to pin-14 (cathode) and pin-16 (anode) to prevent the device's substrate diode from being forward biased.

In Figures 3 and 4, the blanking time is controlled by Q1 with the time constant adjusted by a capacitor value of 680 pF and resistor of 1 kΩ. Designers may choose to adjust this value according to their desired blanking time. The 4*RC time constant with 680 pF and 1 kΩ gives a blanking time of 2.7 μs.

Figure 5 shows another concept for an external blanking circuit. This method uses one additional external resistor, R_B, connected from the output to the DESAT pin. This allows an additional blanking capacitor charging current component from the output of the gate driver optocoupler through R_B and adds to the internal current source of the gate drive optocoupler. This higher blanking capacitor charging current allows a designer greater flexibility in choosing both an appropriate value of the blanking capacitor and an appropriate current through a choice of the external resistor R_B. By adjusting the capacitance of the blanking capacitor and the additional current through R_B a designer can set a specific, precise blanking time, and an example calculation of the blanking time is shown below:

$$V_C(t) = V_i + V_f\,(1 - e^{-\frac{t}{RC}})$$

2 possible conditions can happen during the On period:

A) Desat pin voltage is fully discharged by the internal DMOS during previous Off period

During the Off period, the internal DMOS across Desat pin and V_E pin is turned on to discharge the external blanking capacitor's voltage to prepare for the On period.

Assuming that

V_{EE} = -9 V

V_E = 0 V

V_{CC2} = 17 V

R_B = 1000 Ω

C_{BLANK} = 4700 Ω

Therefore, at t = 0,

$V_i = V_E = 0\ V$

At t = ∞,

$V_c(\infty) = V_i + V_f = V_{CC2} = 17\ V$

$V_c(t) = V_i + V_f(1 - e^{-\frac{t}{RC}}) = V_{CC2}(1 - e^{-\frac{t}{RC}})$

$V_c(t) = 17(1 - e^{-\frac{t}{RC}})$, where $t = t_{BLANK}$ and $V_c(t) = V_c(t_{BLANK})$

$V_c(t_{BLANK}) = 7\ V = 17(1 - e^{-\frac{t_{BLANK}}{RC}})$

$e^{-\frac{t_{BLANK}}{RC}} = 1 - \frac{7}{17} = 0.588$

$-\frac{t_{BLANK}}{RC} = \ln(0.588)$

With $R_B = 1000$, $C_{BLANK} = 4700$ pF

$t_{BLANK} = 2.5\ \mu s$

B) Schottky Diode is forward biased by the freewheeling effect of the IGBT load

Due to the freewheeling effect of the IGBT load (motor inductance) before IGBT can turn-on, the schottky diode connected across Desat pin and V_E pin is being forward biased. (Note: without the schottky diode's protection, the device's substrate will be forward biased instead and this will cause Desat protection to be mistriggered).

Assuming that

$V_{EE} = -9\ V$

$V_E = 0\ V$

$V_{CC2} = 17\ V$

$R_B = 1000\ \Omega$

$C_{BLANK} = 4700\ \Omega$ and $V_{F(schottky)} = 0.4\ V$

Therefore, at t = 0,

$V_i = -0.4\ V$

At t = ∞,

$V_c(\infty) = V_i + V_f = V_{CC2} = 17\ V$

So, $V_f = V_{CC2} + 0.4\ V$

$V_c(t) = V_i + V_f(1 - e^{-\frac{t}{RC}}) = -0.4 + (V_{CC2} + 0.4)(1 - e^{-\frac{t}{RC}})$

Where $t = t_{BLANK}$ and $V_c(t) = V_c(t_{BLANK})$

$V_c(t_{BLANK}) = 7\ V = -0.4 + (17 + 0.4)(1 - e^{-\frac{t_{BLANK}}{RC}})$

$e^{-\frac{t_{BLANK}}{RC}} = 1 - \frac{7.4}{17.4} = 0.575$

$-\frac{t_{BLANK}}{RC} = \ln(0.575)$

With $R_B = 1000$, $C_{BLANK} = 4700$ pF

$t_{BLANK} = 2.6\ \mu s$

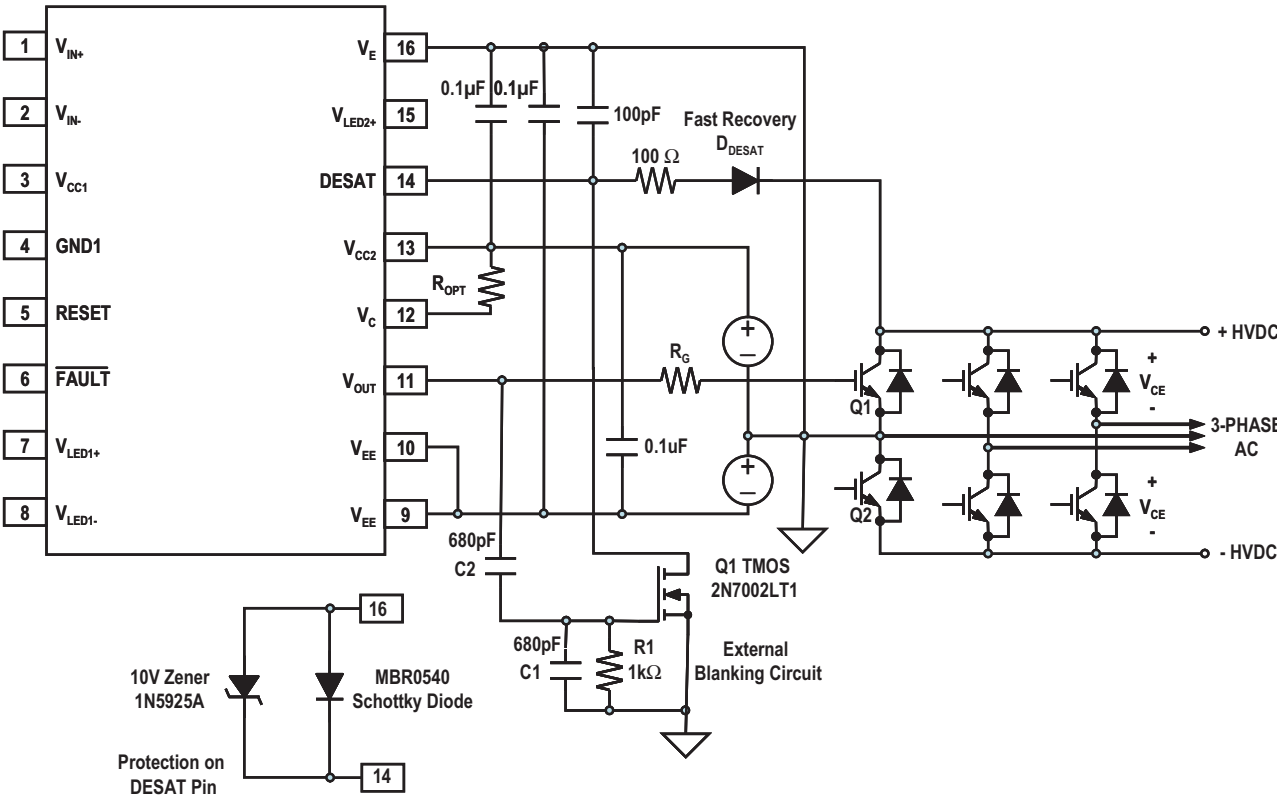

Figure 3. External blanking circuit with a 2.5 µs nominal blanking delay using the HCPL-316J

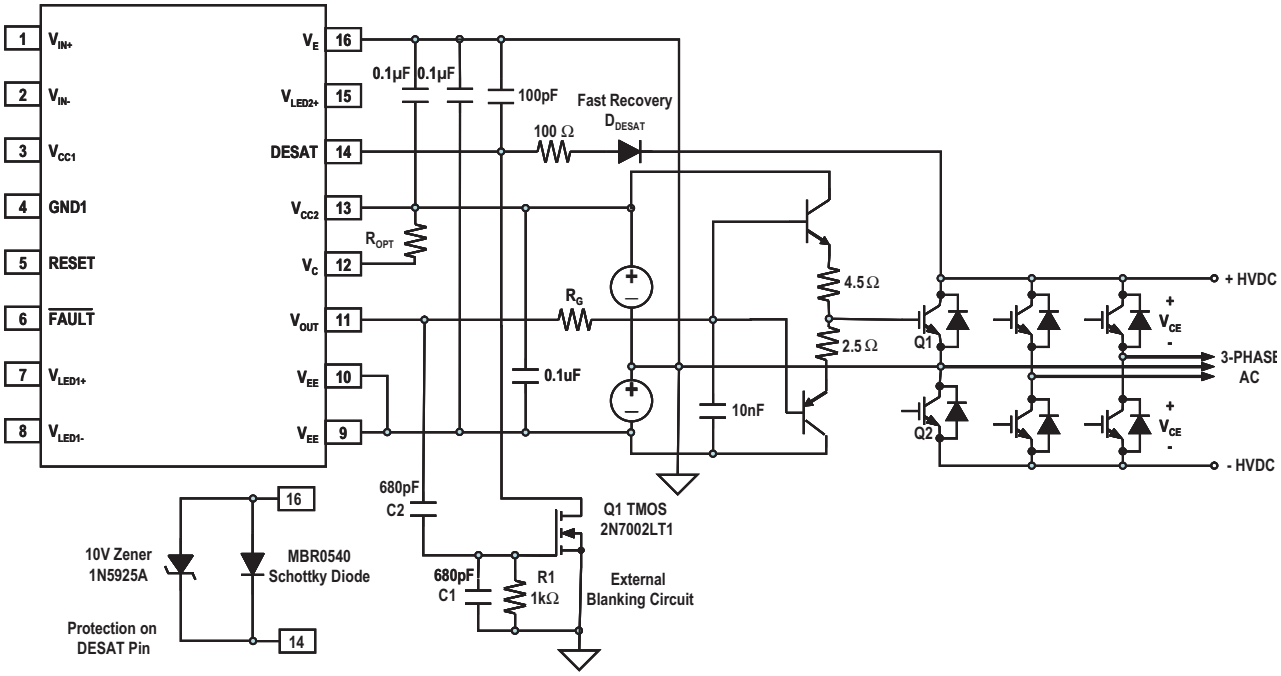

Figure 4. External blanking circuit with external buffer for high current drive using the HCPL-316J

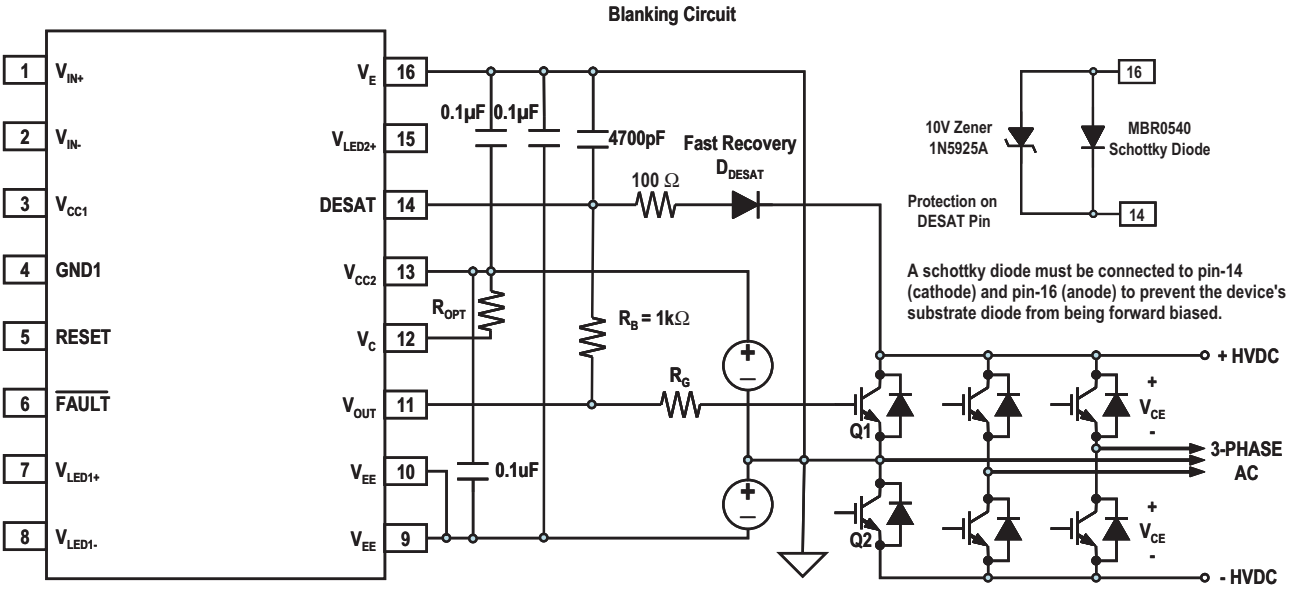

Figure 5. Second external blanking circuit method using the HCPL-316J

6. Experimental results

Figure 6 shows experimental waveforms for the desaturation and soft-shutdown conditions.

Operating Conditions (Refer to Figure 1a):

Switching Frequency = 10 kHz

V_{CC2} - V_{EE} = 15 V

C_L = 10 nF (simulate an IGBT load Q1)

R_G = 10 Ω (gate resistance)

C_{BLANK} = 100 pF

Figure 6. Channel 1 (Yellow) – Input LED, Channel 2 (Green) – Output Voltage, Channel 3 (Blue) – DESAT

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