RGB LED Color Mixing

Using Linear Dimming Techniques with Avago Technologies' Color Management Controllers

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White Paper

Abstract

This paper describes RGB LED color mixing control using linear dimming with Avago Technologies' color management controllers, ADJD-J823 and HDJD-J822. The evaluation circuit consists of the LED backlight driver board, the HDJD-JD04 kit, and a small LED backlight screen. The LED driver board has a field sequencing mode to sequence the RGB colors. The color mixing performance, i.e., du'v' measurements, is taken during linear dimming, with and without field sequencing. The control measurement is taken with PWM dimming and the du'v' is computed. From the results, linear dimming, with or without field sequencing, is a viable method to achieve precise RGB color control. The maximum du'v' result obtained is 0.006. One possible application in linear dimming is the DLP projector. This paper also explains why the pixel memory synchronization can be easily resolved with linear dimming.

Definitions

VLINR – linear dimming voltage for red LEDs

VLING – linear dimming voltage for green LEDs

VLINB – linear dimming voltage for blue LEDs

ENR – Enable Red LED

ENG – Enable Green LED

ENB – Enable Blue LED

PWM – Pulse width modulation

DLP – Digital light processor

PWMR – Pulse width modulation for red LEDs

PWMG – Pulse width modulation for green LEDs

PWMB – Pulse width modulation for blue LEDs

SYNC – Pulse to trigger the loading of image pixel data to DLP mirror

Introduction

PWM dimming is typically the preferred dimming method, as the wavelength (i.e., the color) does not shift during dimming. The RGB mixing application is easier to control with PWM.

Linear dimming is limited in RGB LED applications due to the wavelength shift caused by changes to the LED current during linear dimming. The shift in wavelength makes precise color control difficult to achieve. However, the use of Avago Technologies' color controller, ADJD-J823 or HDJD-J822, can provide precise color control. One possible application for linear dimming is in the DLP projector. The usage of LED lamps in the DLP projector allows for savings in the motor and color filter disc, with a potential reduction in lamp and maintenance costs.

Block diagram description

The ADJD-J823 from the HDJD-JD04 kit has three PWM outputs: PWMR, PWMG and PWMB, which enable Red, Green and Blue LEDs, respectively. The ADJD-J823 controls the proportion of Red, Green and Blue amounts by modifying the PWMR, PWMG, and PWMB duty cycles to produce the desired color on the backlight screen.

The LED backlight driver board has three similar channels. The Red channel is discussed and shown in Figure 1. The Green channel is the same, except the PWMG and ENG is used in place of PWMR and ENR, respectively. Similarly, the Blue channel uses PWMB and ENB signals instead of PWMR or ENR.

The key components involved with the linear dimming are the low pass filter and the AS1104 LED driver.

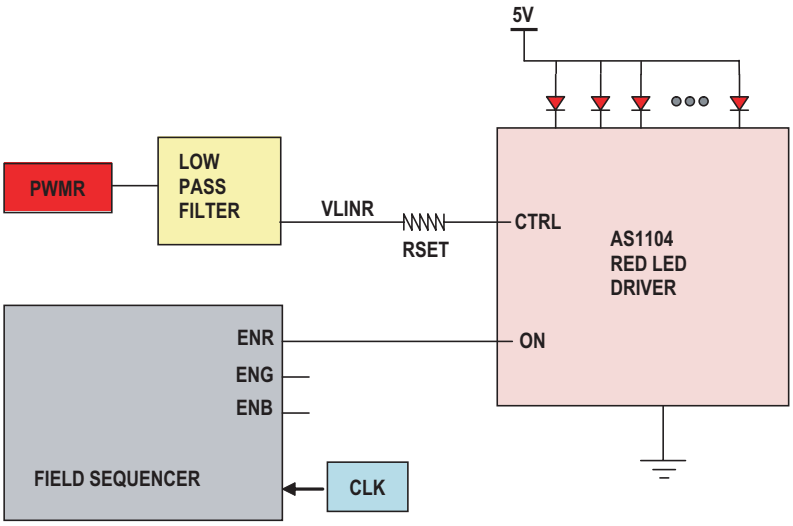

Figure 1. Linear dimming block diagram for the Red channel.

The low pass filter is a simple RC filter design. The main purpose is to generate an average analog voltage, VLINR, which is proportional to the PWMR duty cycle. This analog voltage, together with the RSET resistor, will set the LED current. The ON input of the AS1104 LED driver is connected to the ENR output of the field sequencer block.

Low pass filter design

The nominal PWM frequency from the ADJD-J823 is 6350Hz. A low pass filter averages the PWM signal, so that the gain is -40dB at the PWM frequency. Since the low pass filter roll off at -20dB per decade, two decades are required (i.e., the f3dB for the low pass RC filter = 6350/100 = 63.5Hz).

$$f_{3db} = \frac{1}{2\pi(RC)}, \quad \text{Taking C = 2.2uF, R = 1.1k.}$$

Field Sequencer

The field sequencer has three output control signals:

a) ENR
b) ENG
c) ENB

The universal shift register 74HC194 implements the field sequencer. There are two operating modes: Stop (normal), and Field Sequencing. If the field sequencer is stopped, all the color LEDs are set to turn ON at all times. If the field sequencer is on (Field Sequencing mode), the LEDS are on with one color at a time in equal intervals. The field sequencer frequency determines the LED "on" time which is 1/fCLK. The field sequencing clock is derived from the 555 timer IC. A bench top pulse generator can also be used.

Control Evaluation Board

The LED backlight driver board for control evaluation is shown in Figure 2.

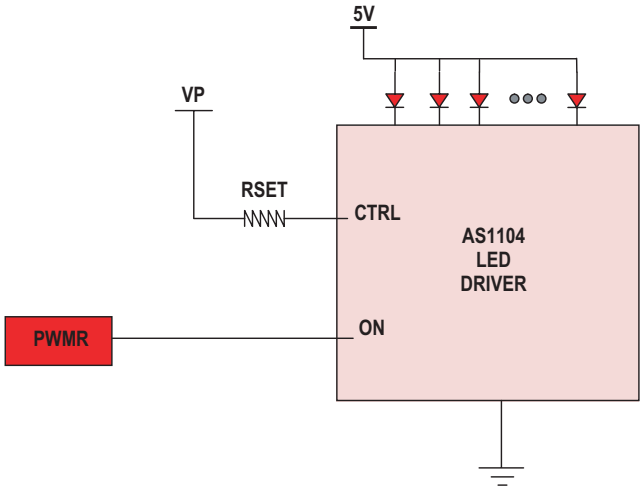

Figure 2. Block diagram to implement PWM dimming.

A fixed voltage VP and RSET program the peak LED current. The PWM signal is connected to the ON input of the AS1104 LED driver. The voltage VP is set to the maximum of the VLINR, VLING, and VLINB voltages. These output low pass filter voltages are obtained during linear dimming without field sequencing at 9000K white. This setting allows comparable luminance for the control PWM dimming.

Evaluation Results

The software provided with the HDJD-JD04 kit is used to perform an initial calibration and set the color points for measurement.

The Yxy measurements are obtained for the various color set points and converted to Yu'v'; du'v' is then calculated. The formulas used are:

$$u' = \frac{4x}{-2x+12y+3} \qquad v' = \frac{9y}{-2x+12y+3}$$

$$du'v' = \sqrt{(u'_m - u'_s)^2 + (v'_m - v'_s)^2}$$

where subscript 'm' represents the measured values, and subscript 's' represents the reference set point.

The du'v' are computed and listed in Table 1.

Table 1. The results of du'v' performance for various operating modes.

BRIGHT register %	Color	CIE Yxy Set point x	y	du'v' Linear no FS	Linear FS 183hz	PWM
88	white	0.287	0.296	0.002	0.003	0.001
88	cyan	0.191	0.353	0.001	0.004	0.001
88	yellow	0.460	0.506	0.001	0.004	0.001
88	pink	0.381	0.168	0.002	0.002	0.003
88	green	0.244	0.674	0.002	0.003	0.002
88	red	0.634	0.316	0.002	0.006	0.004
88	blue	0.175	0.094	0.002	0.005	0.004

Note: Refer to the Application Note 5241 ADJD-J823 programming manual.
1. BRIGHT register set to 88% (decimal 3432) or hexadecimal 0D68.
2. CIE_X register set to decimal (x-coordinate * 1000).
3. CIE_Y register set to decimal (y-coordinate *1000).
4. DEVICE_L register is set to decimal 1000 or hexadecimal 03E8.

Figure 3 shows the graphical result of the linear dimming with field sequencing. The centers of the Blue squares represent the set point, while the centers of the Red diamonds represent the color achieved by the LED backlight screen. The lowest performance (i.e., the maximum du'v') is 0.006 for Red.

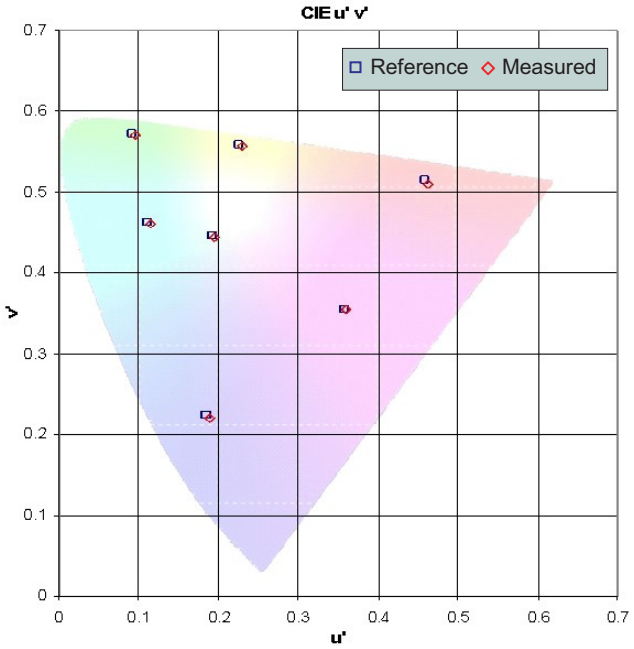

Figure 3. Linear dimming with field sequencing.

Table 2. Luminance measurement in candela per square meter.

BRIGHT register %	Set point X	Y	Luminance in cd/sq meter Linear no FS	Linear FS 183hz	PWM
88	0.287	0.296	844	299	789
88	0.191	0.353	654	231	618
88	0.460	0.506	889	318	839
88	0.381	0.168	644	242	627
88	0.244	0.674	628	220	599
88	0.634	0.316	599	224	610
88	0.175	0.094	266	91	267

Precise color control is achieved. Comparable performance is obtained for linear dimming without field sequencing and control PWM dimming. The slight performance difference is generally due to the luminance value. The higher the luminance value, the better the signal-to-noise ratio, and the lower (better) the du'v'.

Potential applications

One of the possible applications of linear dimming with field sequencing is the DLP projector with an LED RGB light source. For such an application, the HDJD-J822 must be used instead of the ADJD-J823. This is due to the additional low pass filter at the output of the color sensor which helps to filter the noise. The gain for the additional low pass filter at the color sensor output must be below -40dB at the RGB frame frequency.

The HDJD-J822 PWM nominal frequency is much lower at 610Hz. To achieve a similar f3db, i.e., 61Hz, the roll-off should be at - 40dB/decade. A second order Butterworth filter can be used.

Figure 4 shows the over-simplified system block diagram of a DLP projector application. This diagram illustrates the LED light source and its color management system. Refer to the LED TV paper listed in Reference 8, for the actual optical architecture.

The light from the Red, Green, and Blue LEDs is gathered and thoroughly mixed by the mixing block. A small window opening allows a color sensor to sense the mixed light. The converted analog voltages, VLINR, VLING, and VLINB, are derived from the HDJD-J822 PWM outputs: PWMR, PWMG, and PWMB, respectively. The HDJD-J822 will adjust these analog voltages so that a white reference light is obtained from the R, G, and B LEDs.

The ENABLE signals, ENR, ENG, and ENB from the DLP formatter memory activate one at a time. The LED light colors can be sequenced at equal times. The time span through one ENR, ENG, and ENB is set at the RGB frame period.

The sequenced R, G, B light is sensed by the HDJD-S722 color sensor. The output of the color sensor is passed through a low pass filter which provides optical feedback to the HDJD-J822.

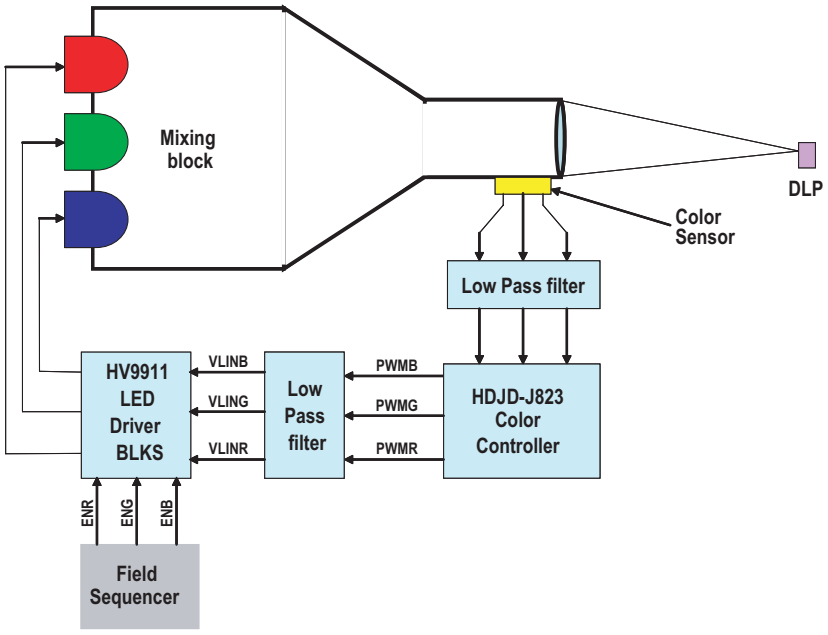

Figure 4. Block diagram of DLP application with the HDJD-J822 color controller.

The system designer has to set the RGB frame period sufficiently high to prevent a rainbow effect, and sufficiently slow for the DLP micromirrors to respond.

Figure 5 illustrates the field sequencing process and the pixel memory synchronization signal (SYNC). The SYNC signal is derived from the ENR, ENG, and ENB signals. To illustrate the derivation and pixel synchronization, refer to Figure 6 showing the ENR pulse.

Assume that the image pixel data is 8-bit wide, where the whole ENR high time corresponds to a pixel value of 256.

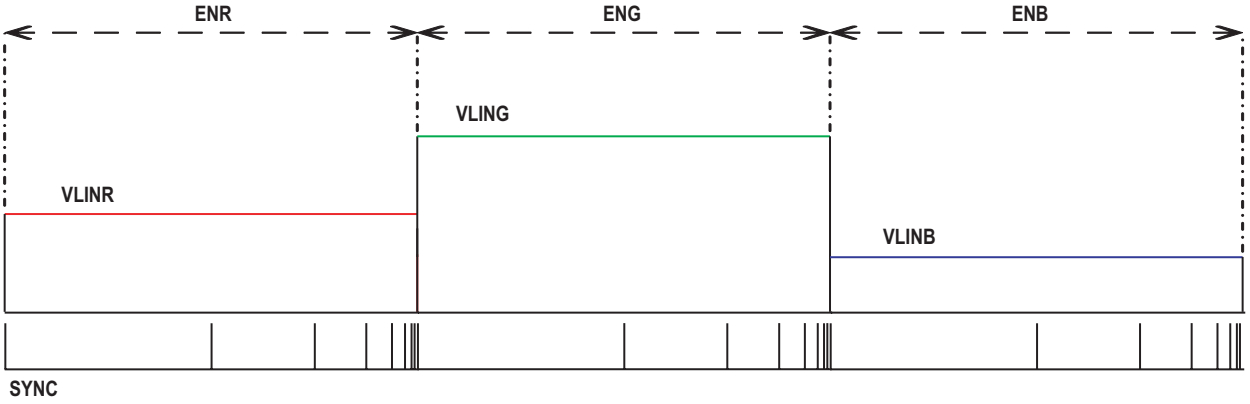

Figure 5. Pixel memory synchronization (SYNC) pulses.

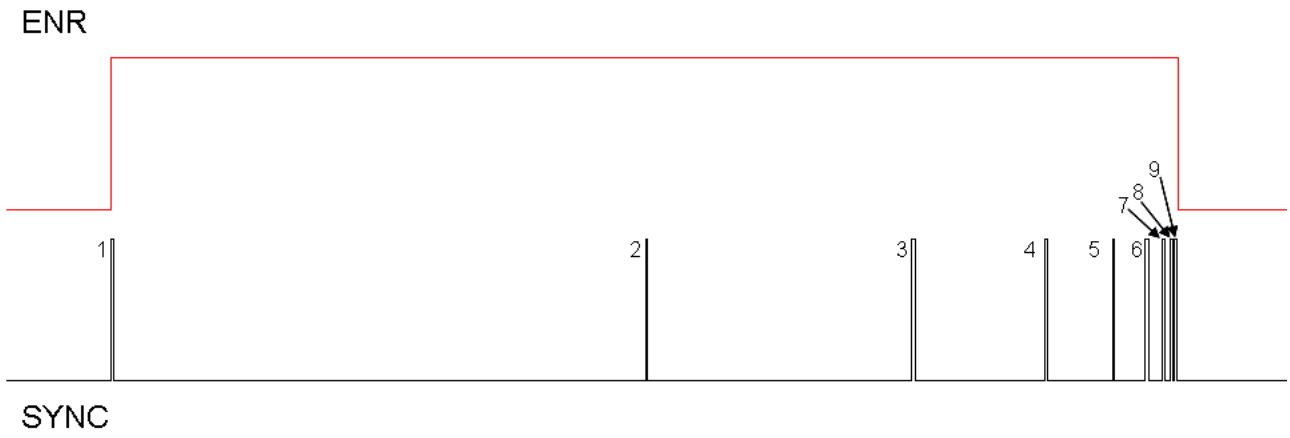

Figure 6. ENR (Red enable line) and pixel memory synchronization SYNC.

The first SYNC pulse is generated when the ENR transitions from 0 to 1. The second SYNC pulse is generated by dividing the remaining ENR high time by 2. The interval for SYNC pulse 1 to SYNC pulse 2 corresponds to a pixel weight of 128. Successive division of the remaining ENR high time by 2 gives SYNC pulse 3, 4, 5, 6, 7, 8, and 9. Table 3 shows the pixel weight associated with the interval between the SYNC pulses and the pixel memory bit that is loaded to the DMD mirror. A '0' turns off the DMD mirror, and a '1' turns on the DMD mirror.

The last interval from SYNC pulse 9 to the next color SYNC pulse 1 is set so the mirror is always off. (A '0' value is loaded to the DMD mirror.)

Table 3. SYNC pulses interval and pixel weight

From SYNC pulse	To SYNC pulse	Pixel value weight	Image pixel memory bit loaded
1	2	128	Bit 7 (MSB)
2	3	64	Bit 6
3	4	32	Bit 5
4	5	16	Bit 4
5	6	8	Bit 3
6	7	4	Bit 2
7	8	2	Bit 1
8	9	1	Bit 0 (LSB)
9	Next color SYNC 1	Mirror always off	'0'

As an example, to display a pixel with RGB = (129, 53, 243) decimal or RGB binaries (10000001,00110101,11110011), Table 4 shows the data that should be loaded when the trigger SYNC pulse goes from low to high.

Table 4. Example illustrating display pixel RGB value = (129, 53, 243)

Time	ENR	ENG	ENR	Trigger SYNC pulse	Pixel value weight	Pixel value loaded to DLP mirror	Decimal
0	1	0	0	1	128	1	129
$^{1}/_{2}$ P	1	0	0	2	64	0	
$^{3}/_{4}$ P	1	0	0	3	32	0	
$^{7}/_{8}$ P	1	0	0	4	16	0	
$^{15}/_{16}$ P	1	0	0	5	8	0	
$^{31}/_{32}$ P	1	0	0	6	4	0	
$^{63}/_{64}$ P	1	0	0	7	2	0	
$^{127}/_{128}$ P	1	0	0	8	1	1	
$^{255}/_{256}$ P	1	0	0	9	1	0	
P	0	1	0	1	128	0	53
P + $^{1}/_{2}$ P	0	1	0	2	64	0	
P + $^{3}/_{4}$ P	0	1	0	3	32	1	
P + $^{7}/_{8}$ P	0	1	0	4	16	1	
P + $^{15}/_{16}$ P	0	1	0	5	8	0	
P + $^{31}/_{32}$ P	0	1	0	6	4	1	
P + $^{63}/_{64}$ P	0	1	0	7	2	0	
P + $^{127}/_{128}$ P	0	1	0	8	1	1	
P + $^{255}/_{256}$ P	0	1	0	9	1	0	
2P	0	0	1	1	128	1	243
2P + $^{1}/_{2}$ P	0	0	1	2	64	1	
2P + $^{3}/_{4}$ P	0	0	1	3	32	1	
2P + $^{7}/_{8}$ P	0	0	1	4	16	1	
2P + $^{15}/_{16}$ P	0	0	1	5	8	0	
2P + $^{31}/_{32}$ P	0	0	1	6	4	0	
2P + $^{63}/_{64}$ P	0	0	1	7	2	1	
2P + $^{127}/_{128}$ P	0	0	1	8	1	1	
2P + $^{255}/_{256}$ P	0	0	1	9	1	0	

Note: P is the "on" time for each LED color or ENABLE high time.

(In this example, the "on" time for ENR, ENG, and ENB is the same.)

One way of increasing the luminance proportion of one color is to make the "on" time for that particular color longer. The HDJD-J822 will adjust the VLINR, VLING, and VLINB accordingly to obtain a white reference point.

Conclusion

Linear dimming, with or without field sequencing, can be implemented easily with Avago Technologies' color controller. Comparative performance in linear dimming and PWM dimming is obtained with Avago Technologies' color controller.

References

1. Datasheets: ADJD-J823, HDJD-J822, HDJD-S722, AS1104, 74HC194, LM555
2. HDJD-JD04 development kit:
   HDJD-JD04 Hardware user guide
   ICMv2 operating software manual
3. Application Note 5241: ADJD-J823 programming manual
4. Application Note 5070: Using the HDJD-J822 Color management system feedback controller ASIC
5. Application Note 5254: Method to expedite HDJD-J822 start up settling time
6. Application Note 5272: Method of Improving HDJD-J822 Brightness Change Response
7. "High Definition Display System Based on Digital Micromirror Device,"
   RJ Gove, V Markandey, SW Marshall, DB Doherty, G Sextro, M DuVal, Texas Instruments
8. "LED TV: Technology Overview and the DLP Advantage," DJ Segler, Texas Instruments

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