

AFBR-5978Z

Digital Diagnostic 650 nm Transceiver for Ethernet
(10/100 Mbps) with SC-RJ connector



Application Note 5289

Reference Design

Introduction

The AFBR-5978Z transceiver provides the system designer with the ability to implement Fast Ethernet (100 Mbps) or Ethernet (10 Mbps) over standard bandwidth 0.5 NA (numerical aperture) Plastic Optical Fiber (POF) and 0.37 NA Hard Clad Silica (HCS) fiber. The AFBR-5978Z transceiver features an advanced digital diagnostic interface, compliant to the "Digital Diagnostic Monitoring Interface for Optical Transceivers" SFF-8472 Multi-source Agreement. The connectivity available for the transceiver is SC-RJ. This product is lead free and compliant with RoHS.

Industrial Fast Ethernet

Industrial Fast Ethernet is defined as the use of the Ethernet protocol in an industrial environment, for automation and production machine control. Until recently, an industrial controller would communicate with a slave machine using one of several possible open or proprietary protocols such as ProfiBus, Foundation Fieldbus, and SERCOS. Increasingly, Ethernet is used as the link layer protocol (layer 2 in Open Systems Interconnection or OSI model) with proprietary protocols riding on top in the network to application layers (layer 3 and

up in OSI model). The advantages are increased speed, better interoperability, easy integration with TCP/IP based networks such as the internet and the ability to use standard routers, switches, hubs etc. Examples of protocols based on Industrial Fast Ethernet are ProfiNet, Fieldbus High Speed Ethernet and SERCOS III. While the Ethernet standard permits network nodes to be connected via central hubs with Carrier Sense Multiple Access with Collision Detection (CSMA/CD), the low cost of present day switching technology makes that Industrial Fast Ethernet is primarily used in a dedicated point to point topology. The use of this topology allows for time critical applications like motion control etc.

Industrial Fast Ethernet over POF/HCS has numerous advantages over copper solutions. While copper based communication links are susceptible to EM fields and emit EM noise which may interfere with other instrumentation, fiber optic links are immune to EM fields and do not generate them. Other advantages of fiber over copper are: low weight, complete galvanic separation between link partners, easy field termination and maintenance, easier installation due to short bending radius as well as reduced performance impact over temperature.

HCS® is a trademark of OFS Corporation

AFBR-5978Z is compatible with the SC-RJ Connecting System from Reichle & De-Massari AG, Switzerland

FO Network Components

The typical components used in an Industrial Fast Ethernet fiber optic link are depicted in figure 1:

- Network Interface Controller (NIC) comprising of a Media Access Controller (MAC), which handles link control and makes the data available to higher network layer functions and a Physical Layer Device (PHY) which serializes the data and performs clock and data recovery on the incoming data stream.
- Fiber Optic Transceiver which converts the serial data from the NIC to an optical signal and vice versa. Able to monitor the optical link quality and environment variables.
- Plastic Optical Fiber or Hard Clad Silica fiber to transport the optical information to the link partner. Maximum link distance at 100 Mbps is 50 m for POF and 100 m for HCS fiber, using the AFBR-5978Z transceiver.

Physical Layer Definitions

Industrial Fast Ethernet defines three signal types:

The optical signal is defined as the optical signal into, and out of, the fiber. See A in Figure 1. The optical signal is serial binary between two optical light levels. Since the DC balance of the optical signal needs to be kept within limits the serial binary stream is encoded. For Fast Ethernet (100 Mbps) the encoding is 4B/5B NRZI at 125 MBd and for Ethernet (10 Mbps) the encoding is

Manchester at 20 MBd. Auto-negotiation signals are encoded as Fiber Link Negotiation Pulses (FLNP) over a 1 MHz carrier.

The electrical signal is defined as the differential signal between the fiber optic transceiver and the NIC. See B in Figure 1. The electrical signal is differential serial binary between two PECL levels referenced to 3.3 V (also known as Low Voltage Pseudo Emitter Coupled Logic or LVPECL). Because the electrical signal is the quantized, amplitude limited conversion of the optical signal, the encoding is the same as the optical signal.

The electrical data is defined as the framed and clocked data between the PHY and the MAC, also known as Media Independent Interface (MII). See C in Figure 1. The clock is recovered from the incoming binary signal stream by the PHY and subsequently used to sample the data. On the transmitter side of the PHY (B in Figure 1), the data is encoded and transmitted based on the local clock.

AFBR-5978Z Recommended Termination

The AFBR-5978Z can easily be integrated into new and existing (industrial) Ethernet systems (see Figure 2). The recommended termination of the AFBR-5978Z, the LVPECL interface to the PHY and three different NIC configurations are illustrated in Figures 3 to 5. For details on the LVPECL interface between transceiver and the NIC see the AFBR-5978Z datasheet.

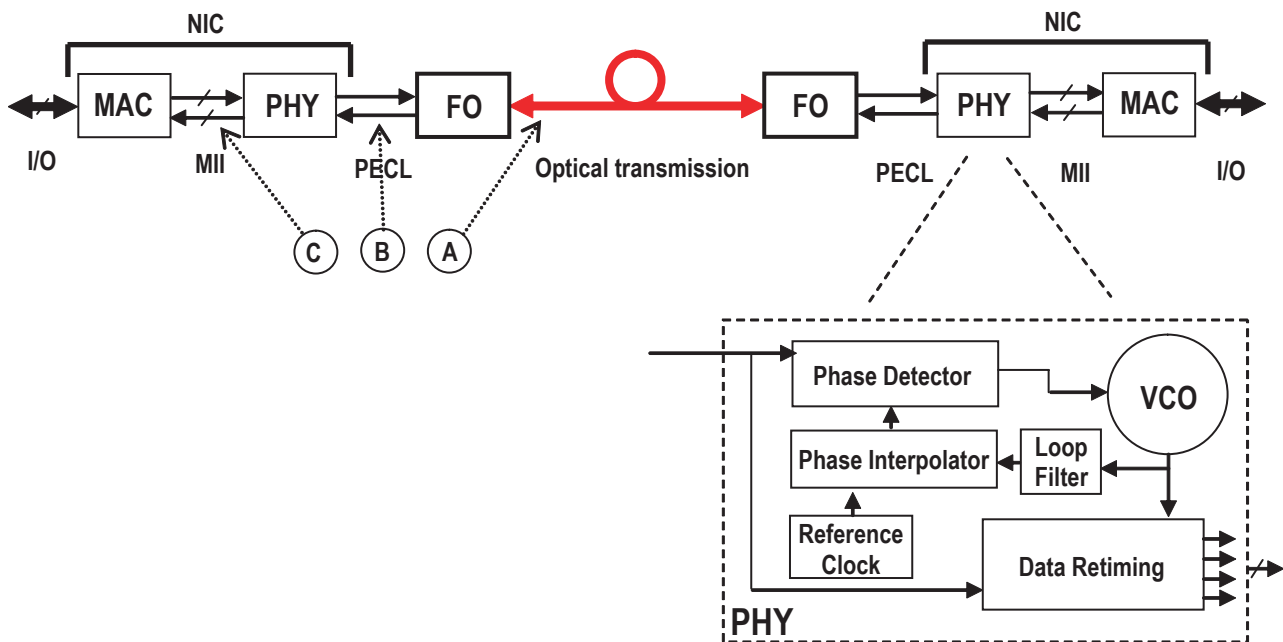


Figure 1. Block diagram of an industrial Ethernet link. Indicated are the optical (A), electrical (B) and data (C) signal types. The insert shows a block diagram of a typical clock/data recovery circuit of the receiver section of the PHY

Application: Media Converter

Ethernet uses different encoding for signals on copper and fiber links. A media converter is utilized to convert between these two signals. A media converter application using the AFBR-5978Z transceiver requires an interface IC with a LVPECL PHY connected to the AFBR-5978Z and a twisted pair PHY connected to the RJ-45 interface. See Figure 3. The LVPECL PHY needs to be compatible with one or more of the following Ethernet standards: 100BASE-FX, 100BASE-SX and 10BASE-FL. Examples of such interface ICs are the MicroLinear ML6652, DaviCom DM9301, etc.

The AFBR-0978Z evaluation board uses the MicroLinear ML6652 and is the basis of the AFBR-5978Z Reference Design.

Application: Industrial Network Device

An industrial network device based on the Ethernet protocol (like ProfiNet, Fieldbus HSE or SERCOS III) typically utilizes a protocol specific ASIC with MII interface, such

as the Siemens-NEC ERTEC series. An industrial network application using the AFBR-5978Z transceiver therefore requires a PHY that translates between the LVPECL signals of the AFBR-5978Z and MII signals of the protocol ASIC. See Figure 4. The LVPECL PHY must be compatible with one or more of the following Ethernet standards: 100BASE-FX, 100BASE-SX and 10BASE-FL. Examples of suitable PHY ICs are the MICREL KSZ8001, Intel LXT971A, etc.

Application: Communication Network Device

A communication network device for Ethernet and Fast Ethernet, like a PC motherboard, router or switch, requires a specialized IC with a LVPECL PHY connected to the AFBR-5978Z and a bus interface connected to the host system. See Figure 5. The LVPECL PHY needs to be compatible with one or more of the following Ethernet standards: 100BASE-FX, 100BASE-SX and 10BASE-FL. Example of such specialized ICs are the MICREL KS8695P and AMD Am79C973, both for the PCI bus.

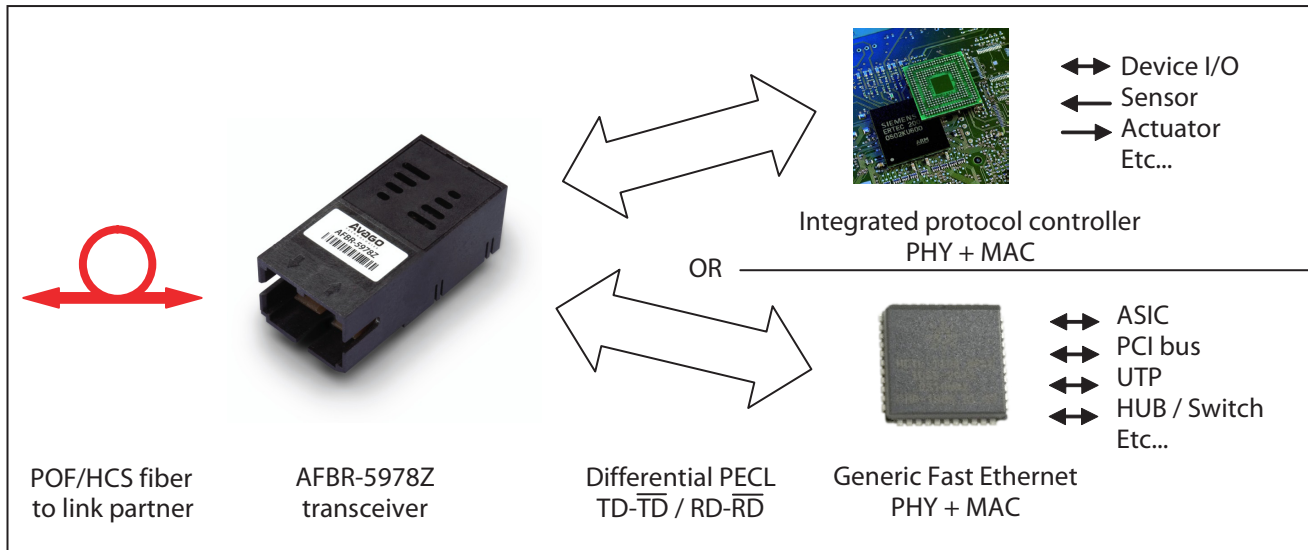


Figure 2. Diagram of an industrial Fast Ethernet link comprising of an optical transceiver and a PHY+MAC

Receiver

The LVPECL (RD and $\overline{\text{RD}}$) output consist of a differential pair of emitter followers. The output emitter followers should operate in the active region such that DC current is flowing at all times. In case of DC-coupling of the AFBR-5978Z to the NIC, the proper termination of the output is $50\ \Omega$ to $V_{cc} - 2\ \text{V}$. For a system operating at 3.3 V the LVPECL outputs should be pulled up to V_{cc} with a $130\ \Omega$ resistor and pulled down with an $82\ \Omega$ resistor.

In case AC-coupling is required for the PECL input structure of the NIC due to supply voltage for example, the transceiver PECL output needs to be biased by coupling it to ground with a resistor. Because the PECL output common-mode voltage is fixed at $V_{cc} - 1.3\ \text{V}$, the value of the resistor is calculated as $142\ \Omega$ assuming 14 mA DC current. However, it is recommended to increase this resistor slightly to $150\text{--}200\ \Omega$ to compensate for the AC component of the signal which is transmitted to the PECL receiver side and hence, lowers the termination resistance seen from the transceiver side. On the NIC side, PECL termination needs to be in place as recommended by the NIC manufacturer. See Avago application note AN-5325 for an example.

The choice of coupling capacitance needs to be balanced between high frequency performance (i.e. low jitter) and capability to carry prolonged periods of consecutive “1”s and “0”s or other slow signals like auto-negotiation (i.e. low cut-off frequency). For the AFBR-5978Z transceiver in an industrial Fast Ethernet application the recommended coupling capacitance is 10 nF.

Transmitter

The LVPECL (TD and $\overline{\text{TD}}$) input of the AFBR-5978Z is an AC coupled, $50\ \Omega$ terminated, self-biased current switching differential. The coupling capacitance is 10 nF. Due to the AC-coupled input of the transceiver proper biasing of the PECL output of the NIC needs to be in place, which is typically detailed in the NIC datasheet or application information. Placement of additional coupling capacitors between the NIC and AFBR-5978Z should be avoided.

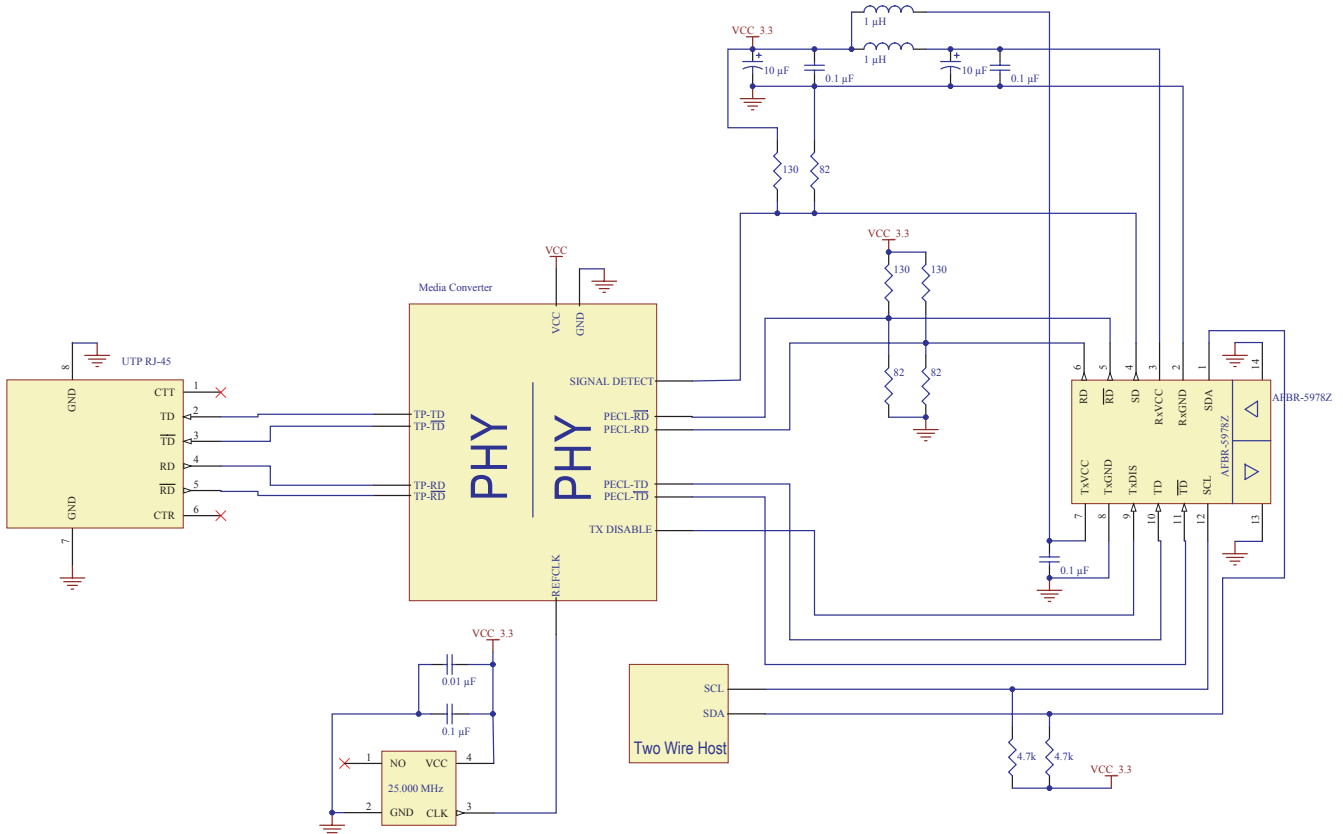


Figure 3. General AFBR-5978Z termination and interface schematic for a media converter application

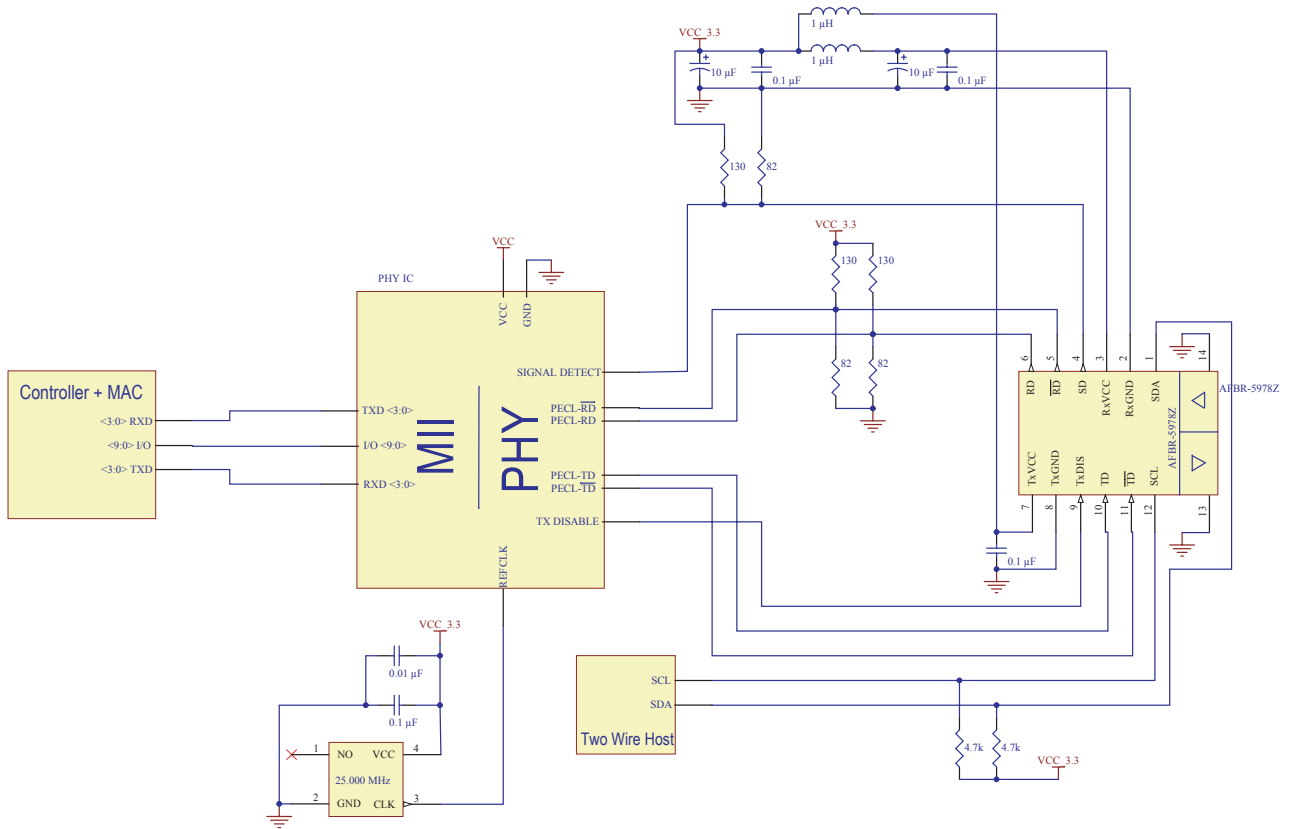


Figure 4. General AFBR-5978Z termination and interface schematic for an industrial network application

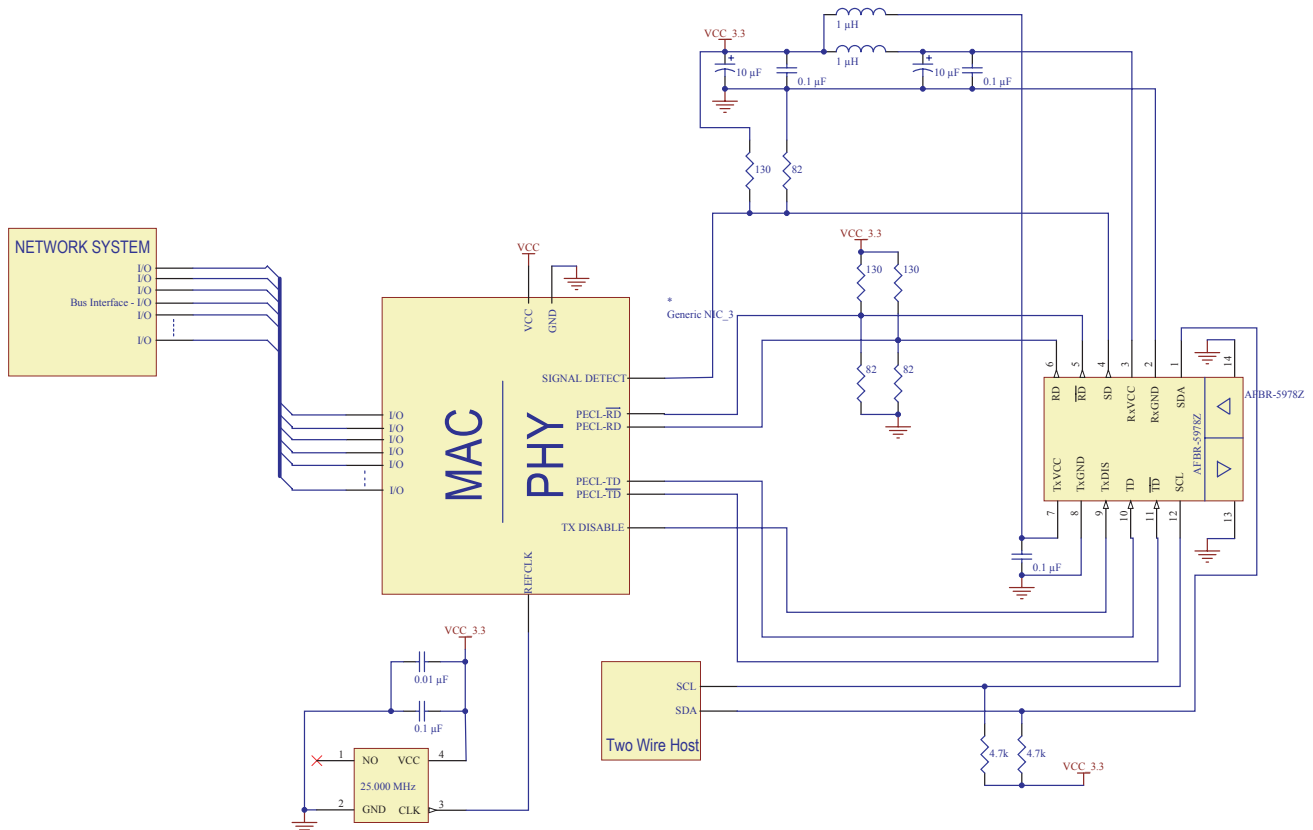


Figure 5. General AFBR-5978Z termination and interface schematic for a communication network device

General Design and Layout Rules

The following points need to be taken into account in a PCB design incorporating the AFBR-5978Z:

- The 10 μF and 0.1 μF decoupling capacitors and the ferrite inductors must be placed as close as possible to the transceiver. Tantalum or ceramic chip capacitors are recommended.
- When in the operating state, the transceiver induces relatively large current transients and therefore the power supply design needs to be of sufficient capacity and output stability. In the reference design the 3.3 V power plane is regulated by a LT1529 which is of sufficient current capacity but needs a large electrolytic capacitor on the output side for stabilization. See C9 + C29 in Figure 3.
- The ground pins of the transceiver need to be directly connected to a contiguous ground plane provided in the circuit board to provide a low inductance power supply ground.
- To ensure the best possible performance of the, typical bandwidth limited, industrial fiber optic link, it is good practice to optimize the electrical path between the transceiver and NIC. Therefore, the transmitter and receiver signal lines between the transceiver and NIC need to be differential pairs, equal in length, as short as possible, on one signal layer (no vias) and impedance matched to 50 Ω .
- The differential signal lines are best placed in a signal layer directly above a ground layer. The ground plane must not be interrupted or cut by a trace over the entire length of the differential signal lines. This ensures a low inductance signal return path and continuous impedance along the trace.
- The bias resistors in the receiver signal line need to be as close as possible to the NIC. This is recommended for both DC and AC coupling.
- If required by the NIC, any bias resistors in the transmitter signal line need to be as close as possible to the transceiver.
- It is recommended to provide a solid Vcc and ground plane under/around the transceiver such that it helps the transceiver dissipate thermal energy through the two Vcc and two Ground pins.
- When the signal detect pin (SD in Figure 3) of the transceiver is connected to LVPECL compatible logic, the proper termination needs to be in place. If signal detect is not used, the SD pin of the transceiver is best left floating.
- The transmitter disable pin (TxDIS in Figure 3) of the transceiver is internally pulled up to Vcc. Hence, if the transmitter disable functionality is not used in the application, this pin needs to be connected to ground for the transmitter to be operational. In this state, the software transmitter disable function is still operational.

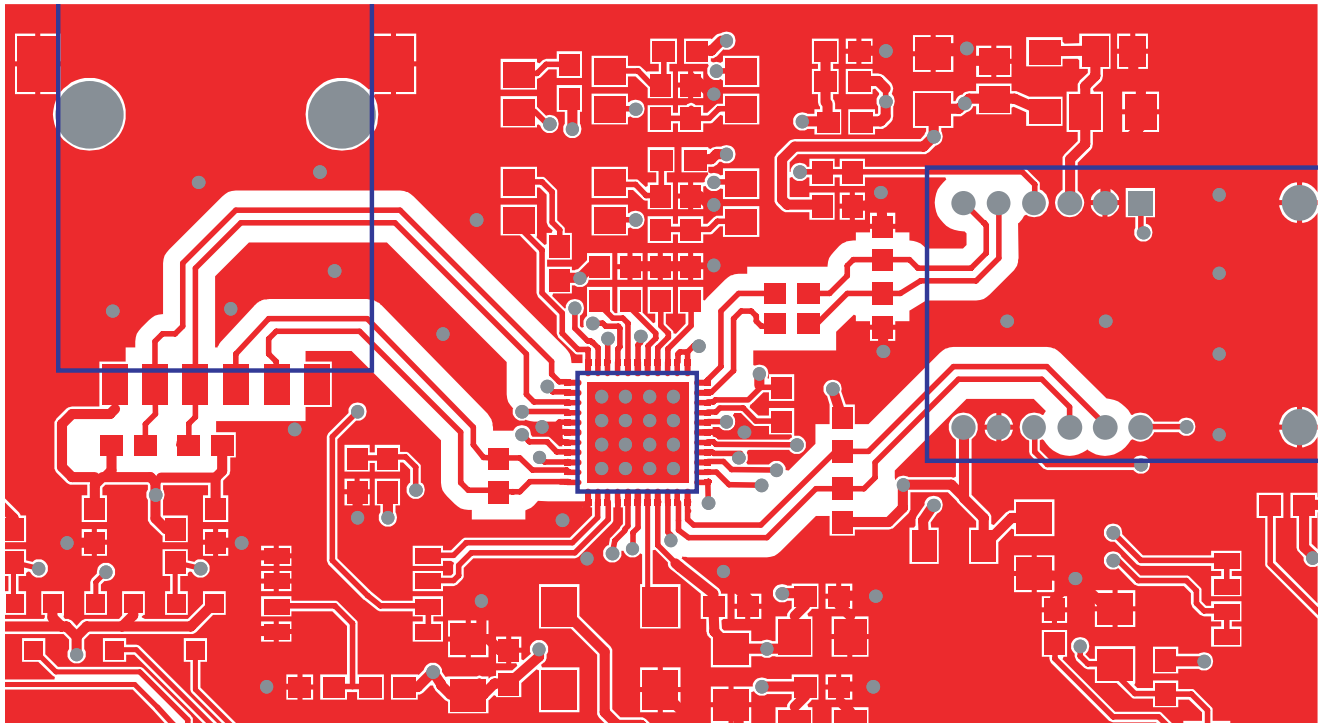


Figure 6. Top layer of the AFBR-0978Z with (indicated in blue left to right): RJ-45 jack, media converter IC and AFBR-5978Z transceiver. Clearly visible are the impedance matched differential signal lines to and from the IC

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries.
Data subject to change. Copyright © 2005-2010 Avago Technologies. All rights reserved.
AV02-0217EN - July 27, 2010

