BROADCOM®

Data Sheet

HCPL-3120/J312, HCNW3120

2.5A Output Current IGBT Gate Drive Optocoupler

Overview

The Broadcom® HCPL-3120 contains a GaAsP LED while the HCPL-J312 and the HCNW3120 contain an AlGaAs LED. The LED is optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by these optocouplers make them ideally suited for directly driving IGBTs with ratings up to 1200V/100A. For IGBTs with higher ratings, the HCPL-3120 series can be used to drive a discrete power stage, which drives the IGBT gate. The HCNW3120 has the highest insulation voltage of V_{IORM} = 1414 V_{PEAK} in the IEC/EN/DIN EN 60747-5-5. The HCPL-J312 has an insulation voltage of V_{IORM} = 1230 V_{PEAK}, and the V_{IORM} = 630 V_{PEAK} is also available with the HCPL-3120 (Option 060).

Features

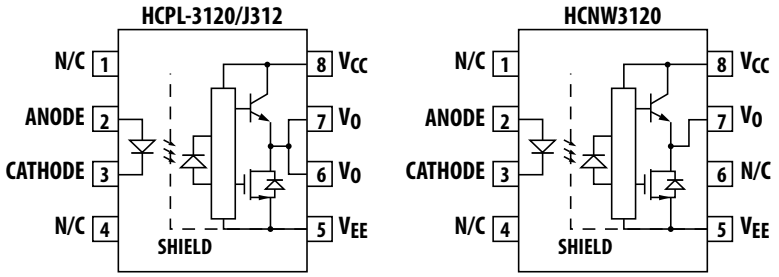
- 2.5A maximum peak output current
- 2.0A minimum peak output current
- 25 kV/µs minimum common mode rejection (CMR) at V_{CM} = 1500V
- 0.5V maximum low-level output voltage (V_{OL}) eliminates need for negative gate drive
- I_{CC} = 5 mA maximum supply current
- Under-voltage lockout protection (UVLO) with hysteresis
- Wide operating V_{CC} range: 15V to 30V
- 500-ns maximum switching speeds
- Industrial temperature range: –40°C to +100°C
- Regulatory approvals:
  - UL recognized:
    - 3750 V_{RMS} for 1 minute for HCPL-3120/J312
    - 5000 V_{RMS} for 1 minute for HCNW3120
  - CSA approval
  - IEC/EN/DIN EN 60747-5-5 approved:
    - V_{IORM} = 630 V_{PEAK} for HCPL-3120 (Option 060)
    - V_{IORM} = 1230 V_{PEAK} for HCPL-J312
    - V_{IORM} = 1414 V_{PEAK} for HCNW3120

Applications

- IGBT/MOSFET gate drive
- AC/Brushless DC motor drives
- Industrial inverters
- Switch mode power supplies

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage and degradation that might be induced by electrostatic discharge (ESD). The components featured in this data sheet are not recommended to be used in military or aerospace applications or environments.

Functional Diagram



Truth Table

LED	$V_{CC} - V_{EE}$ *Positive Going* (that is, Turn-On)	$V_{CC} - V_{EE}$ *Negative Going* (that is, Turn-Off)	V_O
OFF	0V to 30V	0V to 30V	LOW
ON	0V to 11V	0V to 9.5V	LOW
ON	11V to 13.5V	9.5V to 12V	TRANSITION
ON	13.5V to 30V	12V to 30V	HIGH

NOTE: A 0.1-µF bypass capacitor must be connected between pins 5 and 8.

Selection Guide

Part Number	HCPL-3120	HCPL-J312	HCNW3120	HCPL-3150[a]
Output Peak Current (I_O)	2.5A	2.5A	2.5A	0.6A
IEC/EN/DIN EN 60747-5-5 Approval	V_{IORM} = 630 V_{PEAK} (Option 060)	V_{IORM} = 1230 V_{PEAK}	V_{IORM} = 1414 V_{PEAK}	V_{IORM} = 630 V_{PEAK} (Option 060)

a. The HCPL-3150 data sheet is available. Contact a Broadcom sales representative or authorized distributor.

Ordering Information

HCPL-3120 and HCPL-J312 are UL recognized with 3750 V_{RMS} for 1 minute per UL1577. HCNW3120 is UL recognized with 5000 V_{RMS} for 1 minute per UL1577.

Part	Option		Package	Surface Mount	Gull Wing	Tape and Reel	IEC/EN/DIN Number	Quantity
	RoHS Compliant	Non-RoHS Compliant						
HCPL-3120	-000E	No option	300-mil, DIP-8					50 per tube
	-300E	#300		X	X			50 per tube
	-500E	#500		X	X	X		1000 per reel
	-060E	#060					X	50 per tube
	-360E	#360		X	X		X	50 per tube
	-560E/PE	#560		X	X	X	X	1000 per reel
HCPL-J312	-000E	No option	300-mil, DIP-8				X	50 per tube
	-300E	#300		X	X		X	50 per tube
	-500E	#500		X	X	X	X	1000 per reel
HCNW3120	-000E	No option	400-mil, DIP-8				X	42 per tube
	-300E	#300		X	X		X	42 per tube
	-500E	#500		X	X	X	X	750 per reel

NOTE: The notation #XXX is used for older products, while products launched since 15th July 2001 and RoHS compliant option will use -XXXE.

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-3120-560E to order product of 300-mil DIP gull wing surface-mount package in tape and reel packaging with IEC/EN/DIN EN 60747-5-5 safety approval in RoHS compliant.

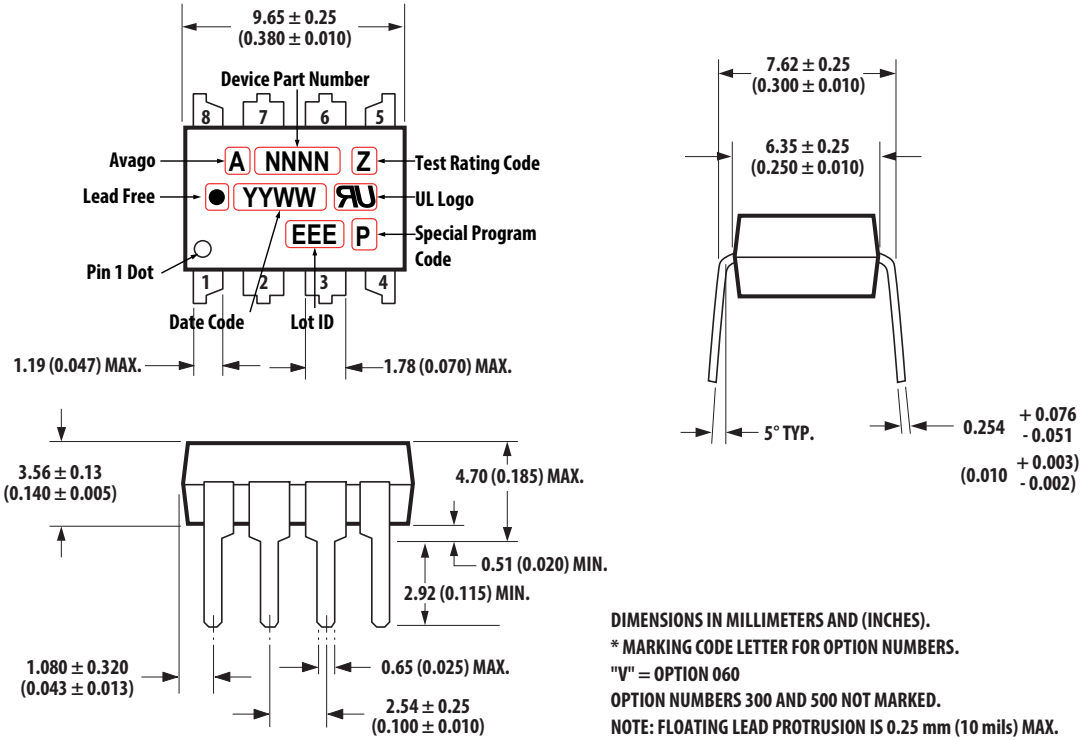
Example 2:

HCPL-3120 to order product of 300-mil DIP package in tube packaging and non-RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

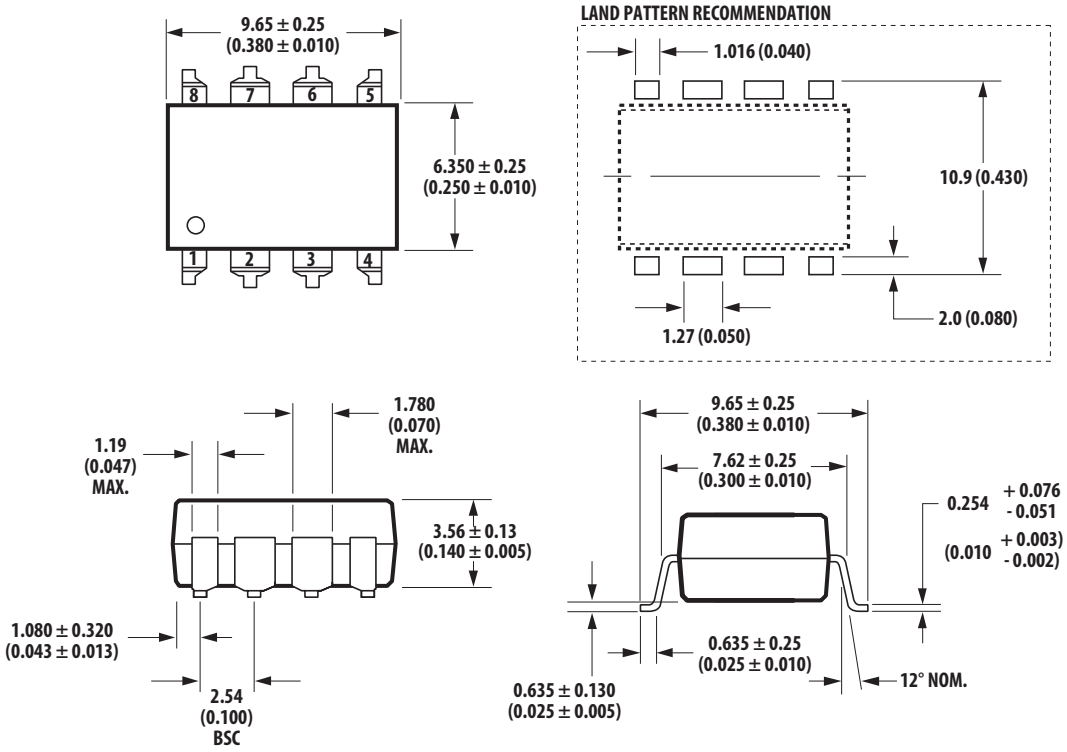
Package Outline Drawings

HCPL-3120 Outline Drawing (Standard DIP Package)



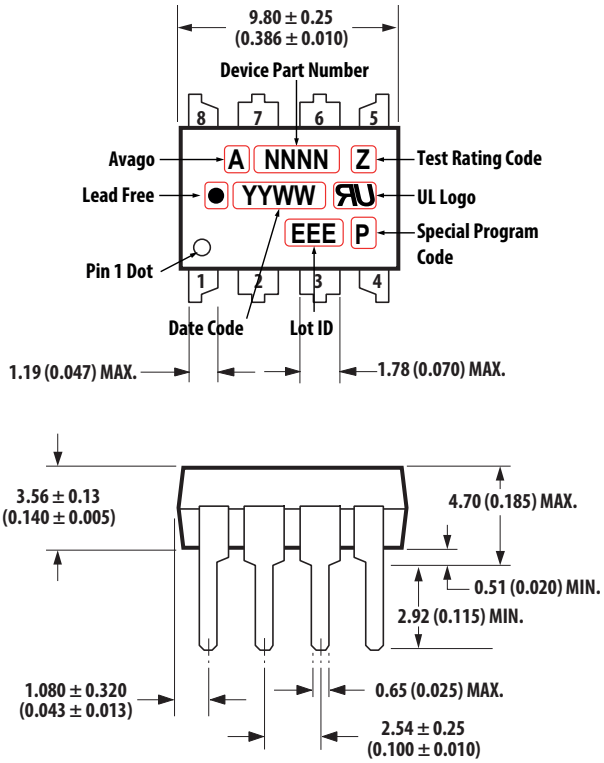
DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

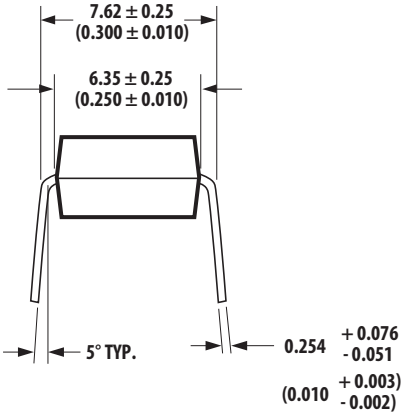
HCPL-3120 Gull Wing Surface-Mount Option 300 Outline Drawing



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

HCPL-J312 Outline Drawing (Standard DIP Package)



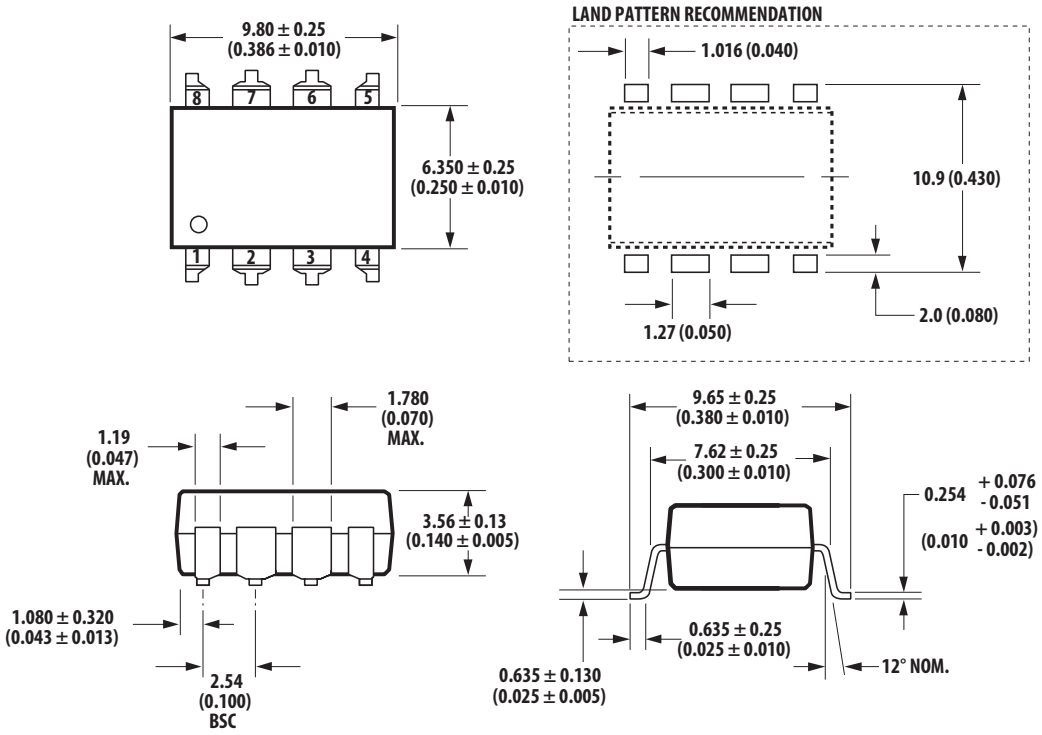


DIMENSIONS IN MILLIMETERS AND (INCHES).

OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

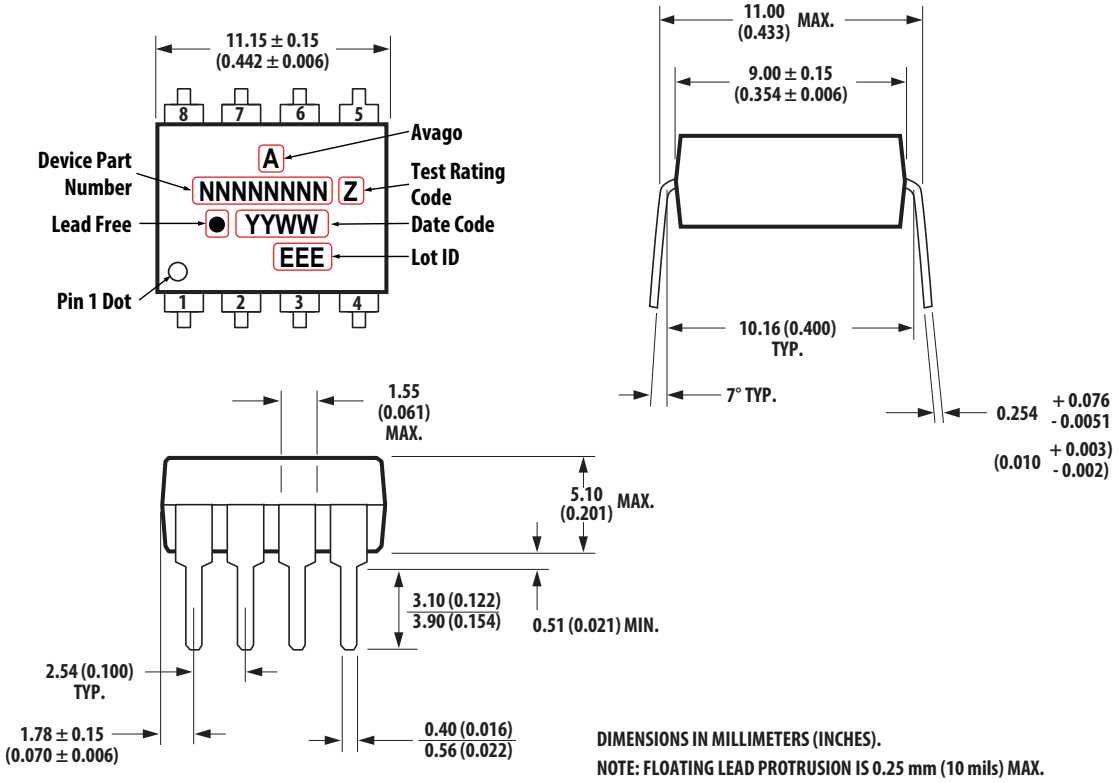
HCPL-J312 Gull Wing Surface-Mount Option 300 Outline Drawing



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

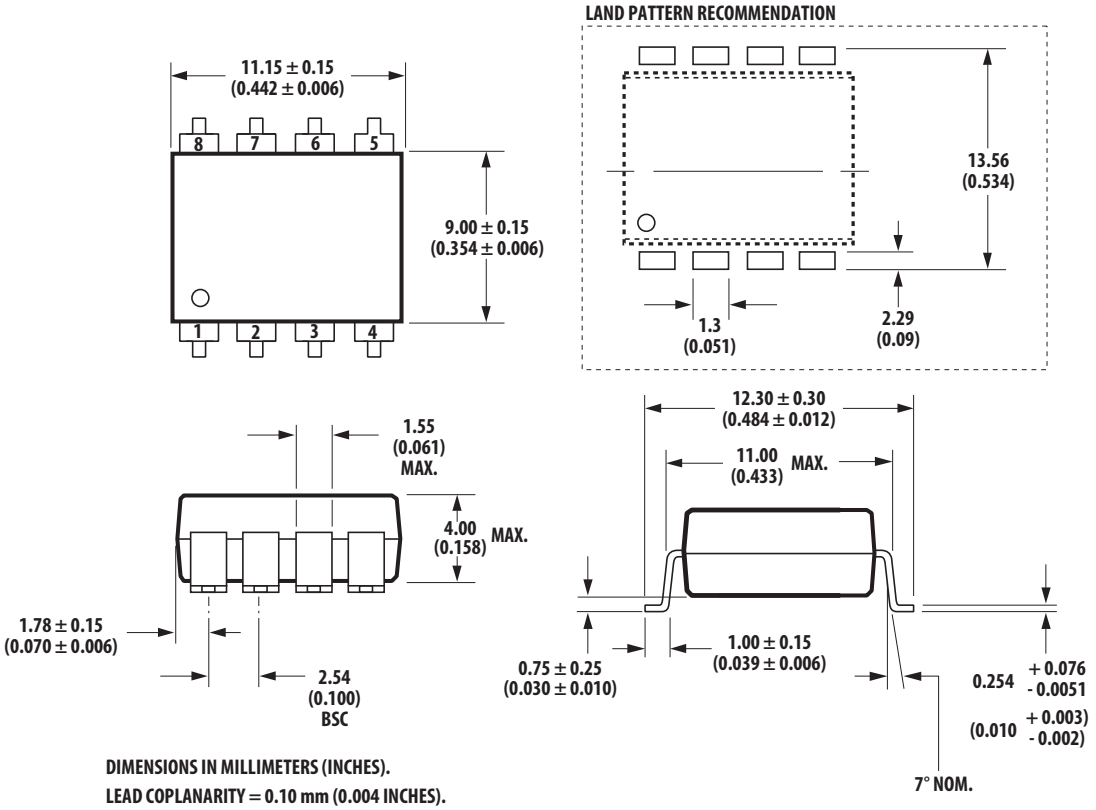
HCNW3120 Outline Drawing (8-Pin Wide Body Package)



DIMENSIONS IN MILLIMETERS (INCHES).

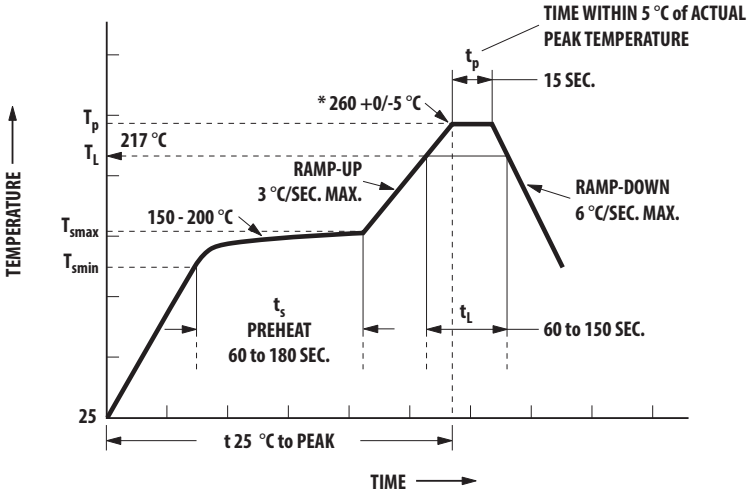
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

HCNW3120 Gull Wing Surface-Mount Option 300 Outline Drawing



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Solder Reflow Temperature Profile

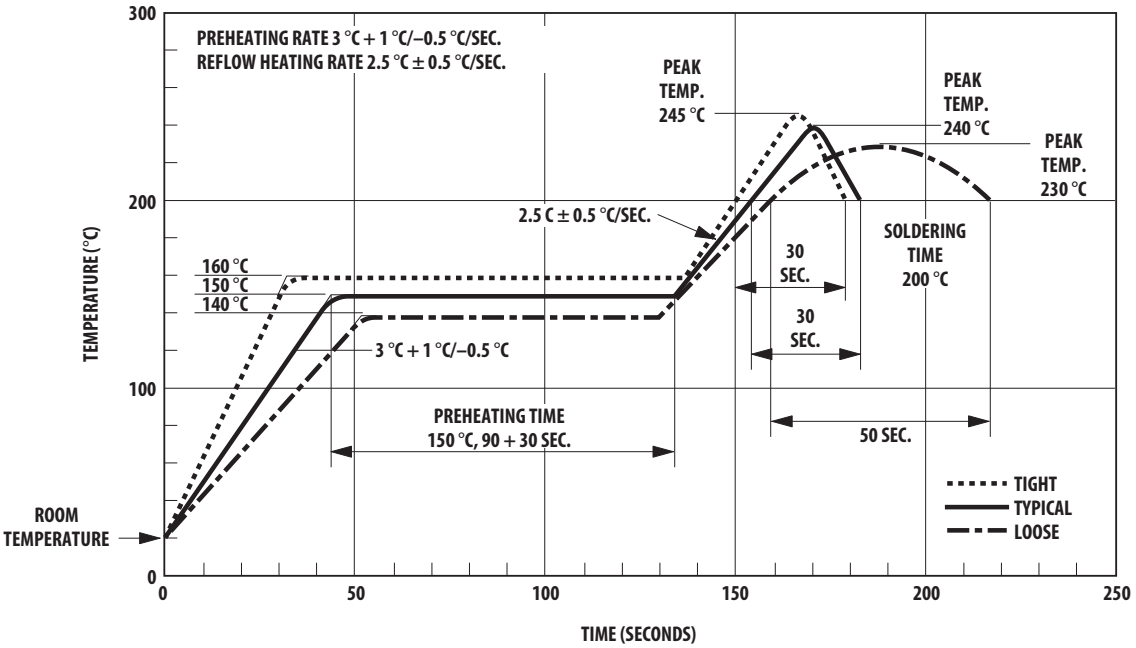


NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

NOTE: NON-HALIDE FLUX SHOULD BE USED.

* RECOMMENDED PEAK TEMPERATURE FOR WIDEBODY 400mils PACKAGE IS 245 °C

Recommended Pb-Free IR Profile



NOTE: NON-HALIDE FLUX SHOULD BE USED.

Regulatory Information

Agency/Standard	HCPL-3120	HCPL-J312	HCNW3120
Underwriters Laboratory (UL) Recognized under UL 1577, Component Recognition Program, Category, File E55361	Compliant	Compliant	Compliant
Canadian Standards Association (CSA) File CA88324, per Component Acceptance Notice #5	Compliant	Compliant	Compliant
IEC/EN/DIN EN 60747-5-5	Compliant Option 060	Compliant	Compliant

Insulation and Safety Related Specifications

Parameter	Symbol	Value			Unit	Conditions
		HCPL-3120	HCPL-J312	HCNW3120		
Minimum External Air Gap (Clearance)	L(101)	7.1	7.4	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	7.4	8.0	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.5	1.0	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	>200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

NOTE: Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs that may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics

NOTE: Isolation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in application. Surface-mount classification is class A in accordance with CECC 00802.

Description	Symbol	HCPL-3120 Option 060	HCPL-J312	HCNW3120	Unit
Installation Classification per DIN VDE 0110/1.89, Table 1					
For Rated Mains Voltage 150 V_{RMS}		I-IV	I-IV	I-IV	
For Rated Mains Voltage 300 V_{RMS}		I-IV	I-IV	I-IV	
For Rated Mains Voltage 450 V_{RMS}		I-III	I-III	I-IV	
For Rated Mains Voltage 600 V_{RMS}			I-III	I-IV	
For Rated Mains Voltage 1000 V_{RMS}				I-III	
Climatic Classification		55/100/21	55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	2	
Maximum Working Insulation Voltage	V_{IORM}	630	1230	1414	V_{PEAK}
Input to Output Test Voltage, Method b[a] V_{IORM} × 1.875 = V_{PR}, 100% Production Test, t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	1181	1670	2652	V_{PEAK}
Input to Output Test Voltage, Method a[a] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	1008	1968	2262	V_{PEAK}
Highest Allowable Overvoltage[a] (Transient Overvoltage, t_{ini} = 60 sec)	V_{IOTM}	6000	8000	8000	V_{PEAK}
Safety-Limiting Values – Maximum values allowed in the event of a failure, also see Figure 37.					
Case Temperature	T_S	175	175	150	°C
Input Current	$I_{S\ INPUT}$	230	400	400	mA
Output Power	$P_{S\ OUTPUT}$	600	600	700	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$\geq 10^9$	$\geq 10^9$	$\geq 10^9$	Ω

a. Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the *Broadcom Regulatory Guide to Isolation Circuits*, AV02-2041EN, for a detailed description of Method a and Method b partial discharge test profiles.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Note
Storage Temperature		T_S	–55	125	°C	
Operating Temperature		T_A	–40	100	°C	
Average Input Current		$I_{F(AVG)}$	—	25	mA	a
Peak Transient Input Current (<1 µs pulse width, 300 pps)		$I_{F(TRAN)}$	—	1.0	A	
Reverse Input Voltage	HCPL-3120	V_R	—	5	V	
	HCPL-J312		—	5		
	HCNW3120		—			
High Peak Output Current		$I_{OH(PEAK)}$	—	2.5	A	b
Low Peak Output Current		$I_{OL(PEAK)}$	—	2.5	A	b
Supply Voltage		$(V_{CC} – V_{EE})$	0	35	V	
Input Current (Rise/Fall Time)		$t_{r(IN)} / t_{f(IN)}$	—	500	ns	
Output Voltage		$V_{O(PEAK)}$	0	V_{CC}	V	
Output Power Dissipation		P_O	—	250	mW	c
Total Power Dissipation		P_T	—	295	mW	d
Lead Solder Temperature	HCPL-3120		260°C for 10 seconds, 1.6 mm below seating plane			
	HCPL-J312					
	HCNW3120		260°C for 10 seconds, up to seating plane			
Solder Reflow Temperature Profile			See Package Outline Drawings.			

a. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.

b. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with IO peak minimum = 2.0A. See Application Information for additional details on limiting I_{OH} peak.

c. Derate linearly above 70°C free-air temperature at a rate of 4.8 mW/°C.

d. Derate linearly above 70°C free-air temperature at a rate of 5.4 mW/°C. The maximum LED junction temperature should not exceed 125°C.

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Unit
Power Supply Voltage		$(V_{CC} – V_{EE})$	15	30	V
Input Current (ON)	HCPL-3120	$I_{F(ON)}$	7	16	mA
	HCPL-J312		7		
	HCNW3120		10		
Input Voltage (OFF)		$V_{F(OFF)}$	–3.6	0.8	V
Operating Temperature		T_A	–40	100	°C

Electrical Specifications (DC)

Over recommended operating conditions (T_A = –40°C to +100°C, for HCPL-3120, HCPL-J312 $I_{F(ON)}$ = 7 mA to 16 mA, for HCNW3120 $I_{F(ON)}$ = 10 mA to 16 mA, $V_{F(OFF)}$ = –3.6V to 0.8V, V_{CC} = 15V to 30V, V_{EE} = Ground) unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.[a]	Max.	Unit	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		0.5	1.5	—	A	$V_O = (V_{CC} – 4V)$	2, 3	b
			2.0	—	—	A	$V_O = (V_{CC} – 15V)$	17	c
Low Level Output Current	I_{OL}		0.5	2.0	—	A	$V_O = (V_{EE} + 2.5V)$	5, 6	b
			2.0	—	—	A	$V_O = (V_{EE} + 15V)$	18	c
High Level Output Voltage	V_{OH}		$(V_{CC} – 4)$	$(V_{CC} – 3)$	—	V	I_O = –100 mA	1, 3, 19	d, e
Low Level Output Voltage	V_{OL}		—	0.1	0.5	V	I_O = 100 mA	4, 6, 20	
High Level Supply Current	I_{CCH}		—	2.5	5.0	mA	Output Open, I_F = 7 mA to 16 mA	7, 8	
Low Level Supply Current	I_{CCL}		—	2.5	5.0	mA	Output Open, V_F = –3.0V to +0.8V		
Threshold Input Current Low to High	I_{FLH}	HCPL-3120	—	2.3	5.0	mA	I_O = 0 mA, V_O > 5V	9, 15	
		HCPL-J312		1.0				21	
		HCNW3120		2.3	8.0				
Threshold Input Voltage High to Low	V_{FHL}		0.8	—	—	V			
Input Forward Voltage	V_F	HCPL-3120	1.2	1.5	1.8	V	I_F = 10 mA	16	
		HCPL-J312 HCNW3120		1.6	1.95				
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$	HCPL-3120	—	–1.6	—	mV/°C	I_F = 10 mA		
		HCPL-J312 HCNW3120		–1.3					
Input Reverse Breakdown Voltage	BV_R	HCPL-3120	5	—	—	V	I_R = 10 µA		
		HCPL-J312 HCNW3120	3				I_R = 100 µA		
Input Capacitance	C_{IN}	HCPL-3120	—	60	—	pF	f = 1 MHz, V_F = 0V		
		HCPL-J312 HCNW3120		70					
UVLO Threshold	V_{UVLO+}		11.0	12.3	13.5	V	V_O > 5V, I_F = 10 mA	22, 34	
	$V_{UVLO–}$		9.5	10.7	12.0				
UVLO Hysteresis	$UVLO_{HYS}$		—	1.6	—				

a. All typical values at T_A = 25 °C and $V_{CC} – V_{EE}$ = 30V, unless otherwise notes.

b. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.

c. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 2.0 A. See Application Information for additional details on limiting I_{OH} peak.

d. In this test, V_{OH} is measured with a dc load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.

e. Maximum pulse width = 1 ms, maximum duty cycle = 20%.

Switching Specifications (AC)

Over recommended operating conditions (T_A = –40°C to +100°C, for HCPL-3120, HCPL-J312 $I_{F(ON)}$ = 7 mA to 16 mA, for HCNW3120 $I_{F(ON)}$ = 10 mA to 16 mA, $V_{F(OFF)}$ = –3.6V to 0.8V, V_{CC} = 15V to 30V, V_{EE} = Ground) unless otherwise specified.

Parameter	Symbol	Min.	Typ.[a]	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.10	0.30	0.50	µs	Rg = 10Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%	10, 11, 12, 13, 14, 23	b
Propagation Delay Time to Low Output Level	t_{PHL}	0.10	0.30	0.50	µs			
Pulse Width Distortion	PWD	—	—	0.3	µs			c
Propagation Delay Difference Between Any Two Parts	PDD ($t_{PHL} – t_{PLH}$)	–0.35	—	0.35	µs		35, 36	d
Rise Time	t_r	—	0.1	—	µs		23	
Fall Time	t_f	—	0.1	—	µs			
UVLO Turn On Delay	$t_{UVLO\ ON}$	—	0.8	—	µs	V_O > 5V, I_F = 10 mA	22	
UVLO Turn Off Delay	$t_{UVLO\ OFF}$	—	0.6	—	µs	V_O < 5V, I_F = 10 mA		
Output High-Level Common Mode Transient Immunity	$\|CM_H\|$	25	35	—	kV/µs	T_A = 25°C, I_F = 10 mA to 16 mA, V_{CM} = 1500V, V_{CC} = 30V	24	e, f
Output Low-Level Common Mode Transient Immunity	$\|CM_L\|$	25	35	—	kV/µs	T_A = 25°C, V_{CM} = 1500V, V_F = 0V, V_{CC} = 30V		e, g

a. All typical values at T_A = 25°C and $V_{CC} – V_{EE}$ = 30V, unless otherwise noted.

b. This load condition approximates the gate load of a 1200 V/75A IGBT.

c. Pulse width distortion (PWD) is defined as $|t_{PHL} – t_{PLH}|$ for any given device.

d. The difference between t_{PHL} and t_{PLH} between any two HCPL-3120 parts under the same test condition.

e. Pins 1 and 4 need to be connected to LED common.

f. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in the high state (that is, V_O > 15.0V).

g. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in a low state (that is, V_O < 1.0V).

Package Characteristics

Over recommended temperature (T_A = –40°C to +100°C) unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.[a]	Max.	Unit	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage[b]	V_{ISO}	HCPL-3120	3750	—	—	V_{RMS}	RH < 50%, t = 1 minute, T_A = 25°C		c, d
		HCPL-J312	3750	—	—				e, d
		HCNW3120	5000	—	—				f, d
Resistance (Input-Output)	R_{I-O}	HCPL-3120		10^{12}	—	Ω	V_{I-O} = 500 V_{DC}		d
		HCPL-J312			—				
		HCNW3120	10^{12}	10^{13}	—		T_A = 25°C		
			10^{11}		—		T_A = 100°C		
Capacitance (Input-Output)	C_{I-O}	HCPL-3120	—	0.6	—	pF	f = 1 MHz		
		HCPL-J312	—	0.8	—				
		HCNW3120	—	0.5	0.6				
LED-to-Case Thermal Resistance	θ_{LC}		—	467	—	°C/W	Thermocouple located at center underside of package	28	
LED-to-Detector Thermal Resistance	θ_{LD}		—	442	—	°C/W			
Detector-to-Case Thermal Resistance	θ_{DC}		—	126	—	°C/W			

a. All typicals at T_A = 25°C.

b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.

c. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 Vrms for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA).

d. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.

e. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA).

f. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA).

Figure 1: V_{OH} vs. Temperature

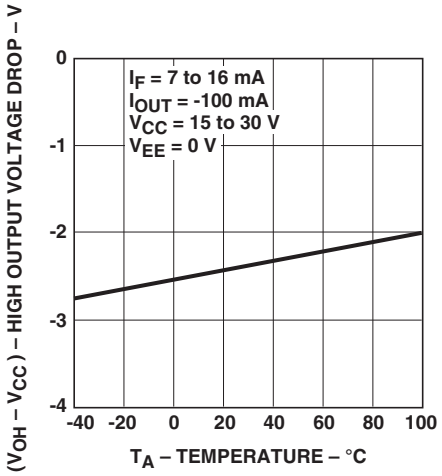


Figure 2: I_{OH} vs. Temperature

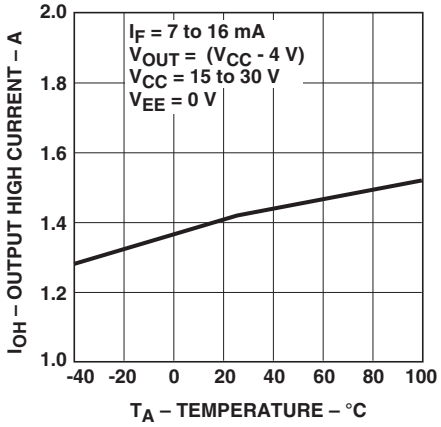


Figure 3: V_{OH} vs. I_{OH}

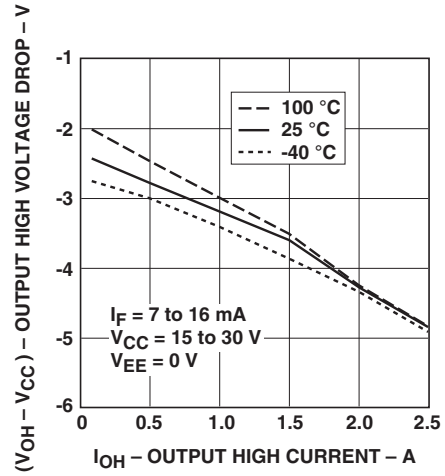


Figure 4: V_{OL} vs. Temperature

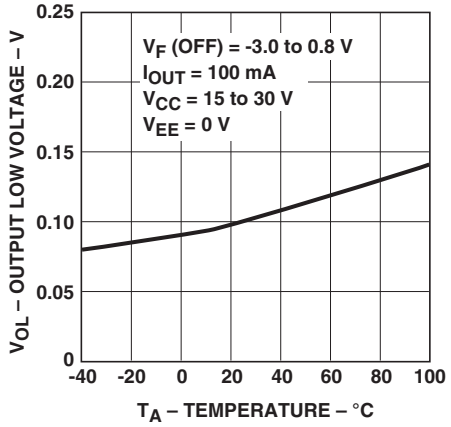


Figure 5: I_{OL} vs. Temperature

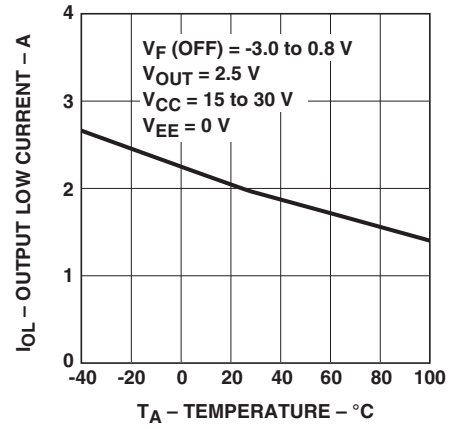


Figure 6: V_{OL} vs. I_{OL}

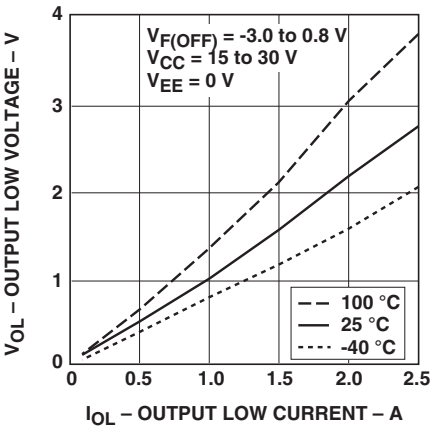


Figure 7: I_{CC} vs. Temperature

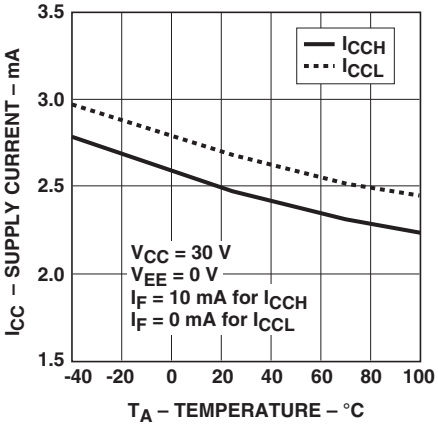


Figure 8: I_{CC} vs. V_{CC}

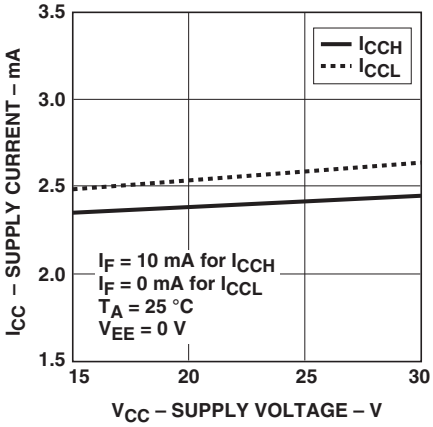
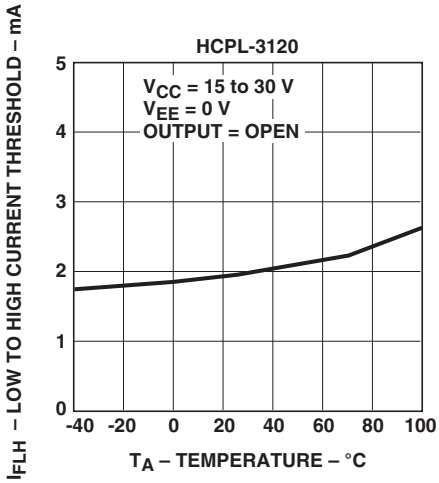
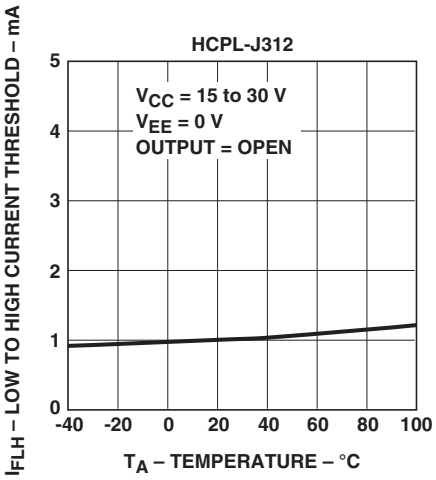


Figure 9: I_{FLH} vs. Temperature





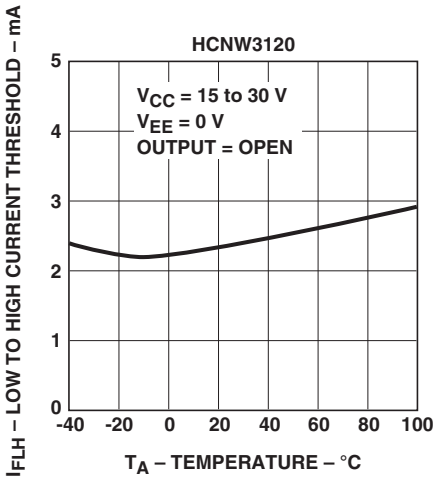


Figure 10: Propagation Delay vs. V_{CC}

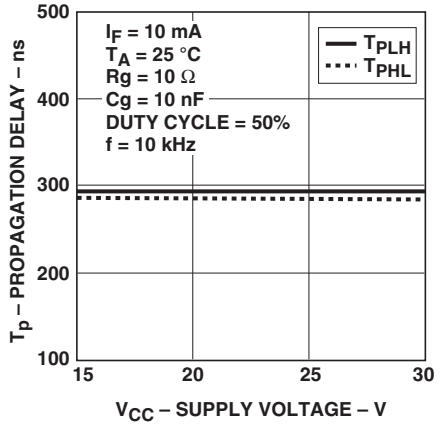


Figure 11: Propagation Delay vs. I_F

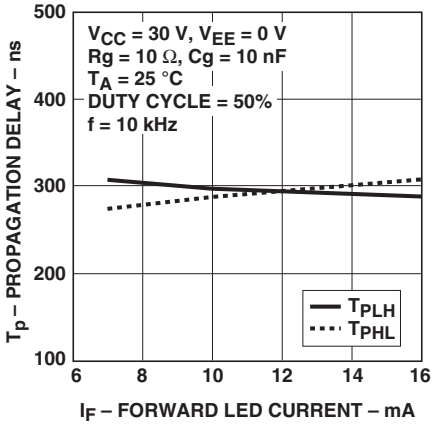


Figure 12: Propagation Delay vs. Temperature

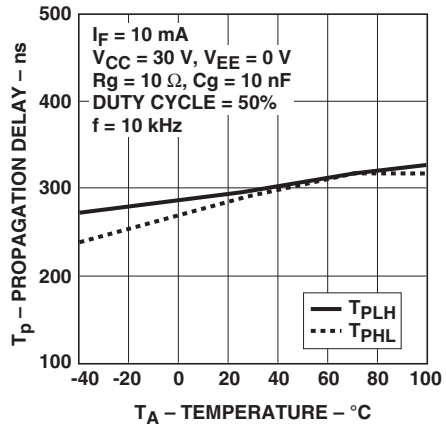


Figure 13: Propagation Delay vs. Rg

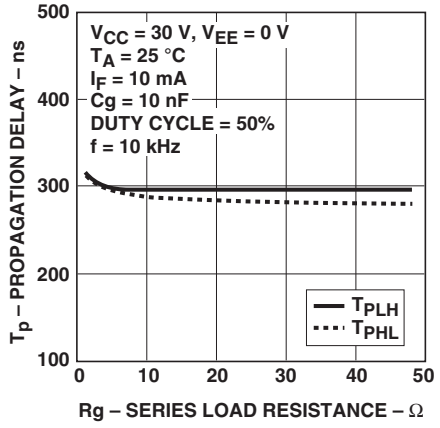


Figure 14: Propagation Delay vs. Cg

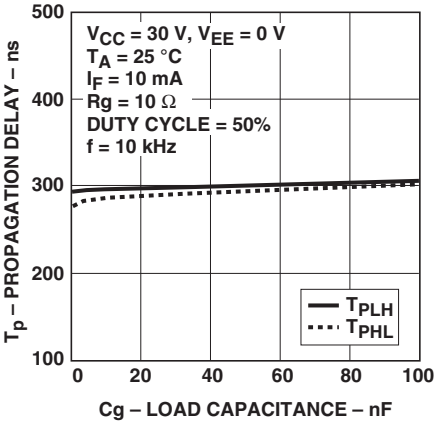


Figure 15: Transfer Characteristics

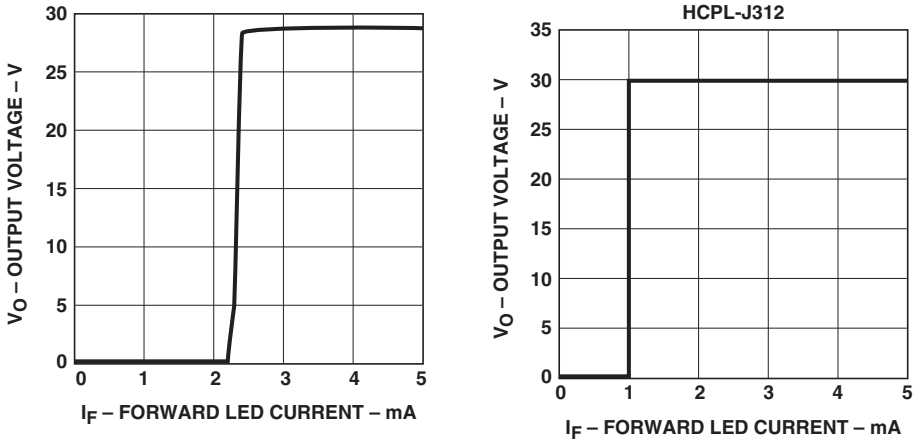


Figure 16: Input Current vs Forward Voltage

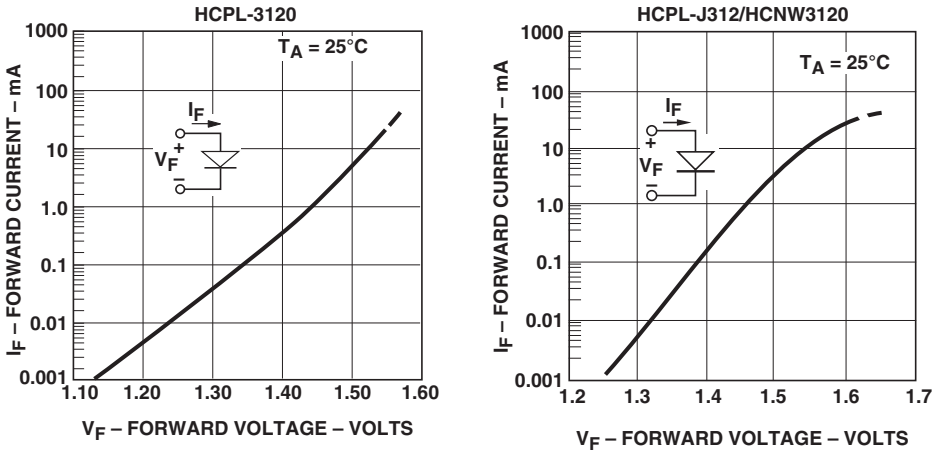


Figure 17: I_{OH} Test Circuit

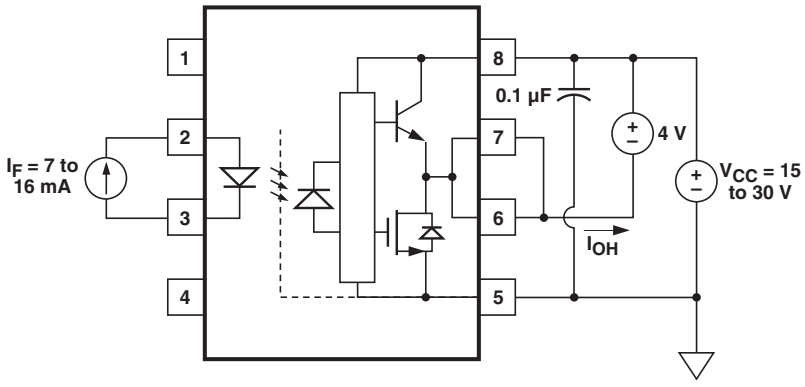


Figure 18: I_{OL} Test Circuit

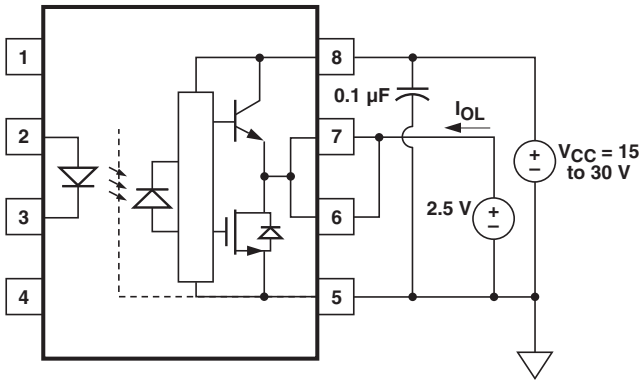


Figure 19: V_{OH} Test Circuit

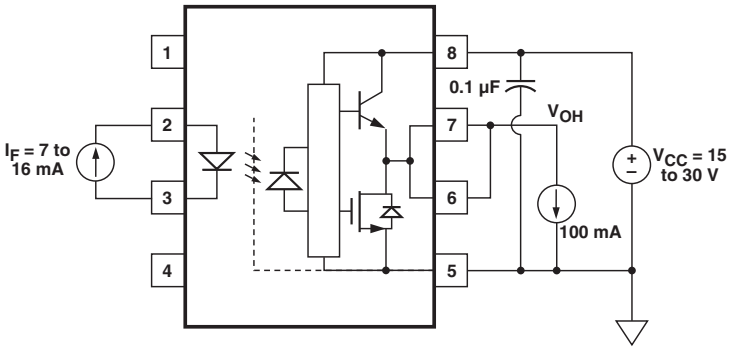


Figure 20: V_{OL} Test Circuit

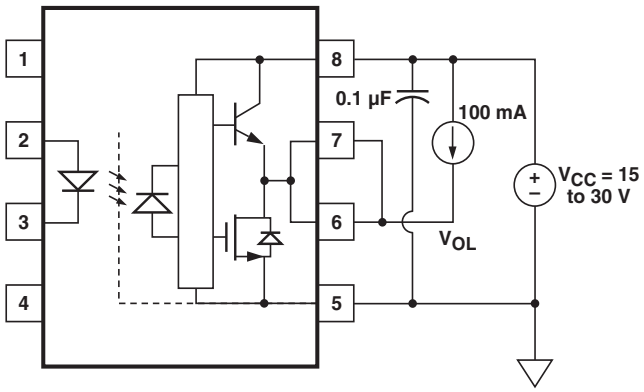


Figure 21: I_{FLH} Test Circuit

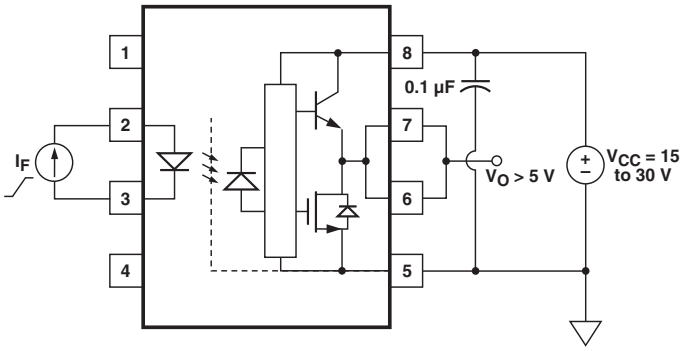


Figure 22: UVLO Test Circuit

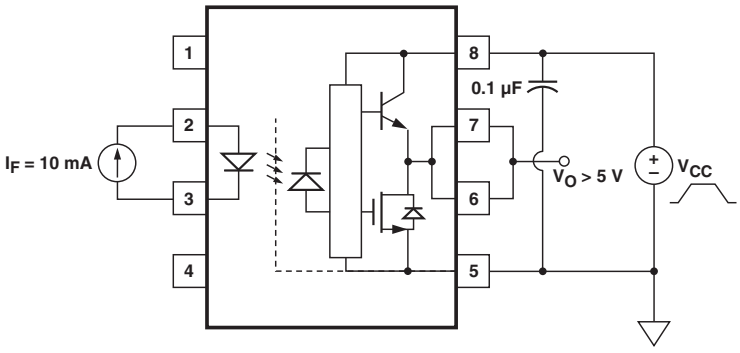


Figure 23: t_{PLH}, t_{PHL}, t_r, and t_f Test Circuit Waveforms

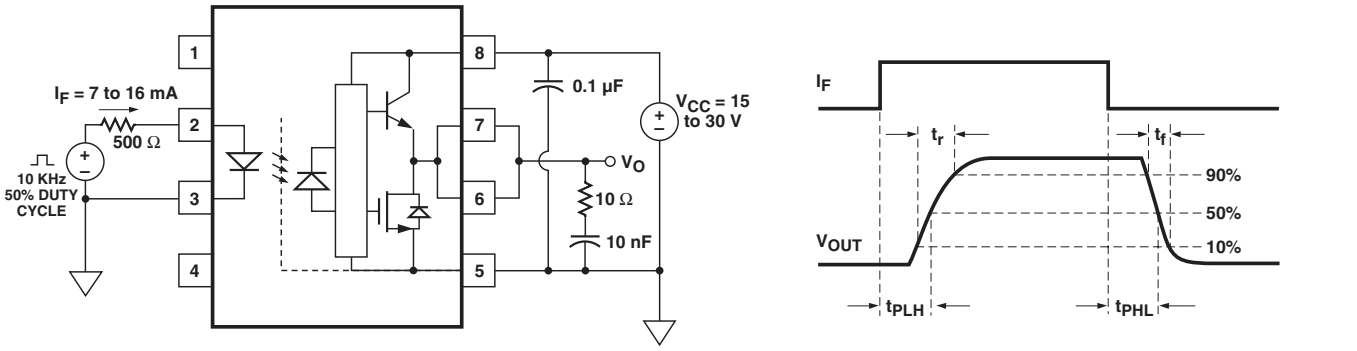
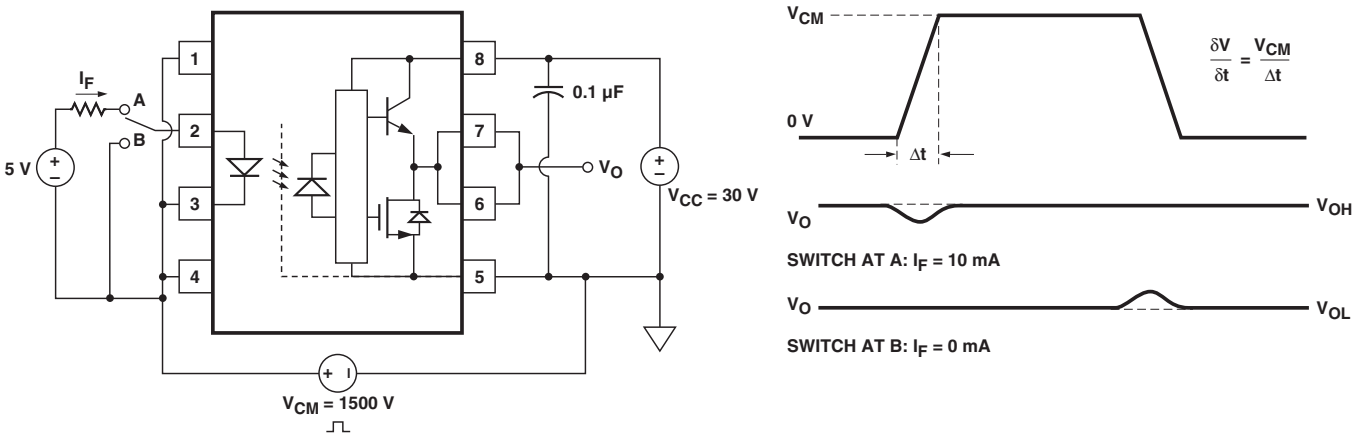


Figure 24: CMR Test Circuit and Waveforms



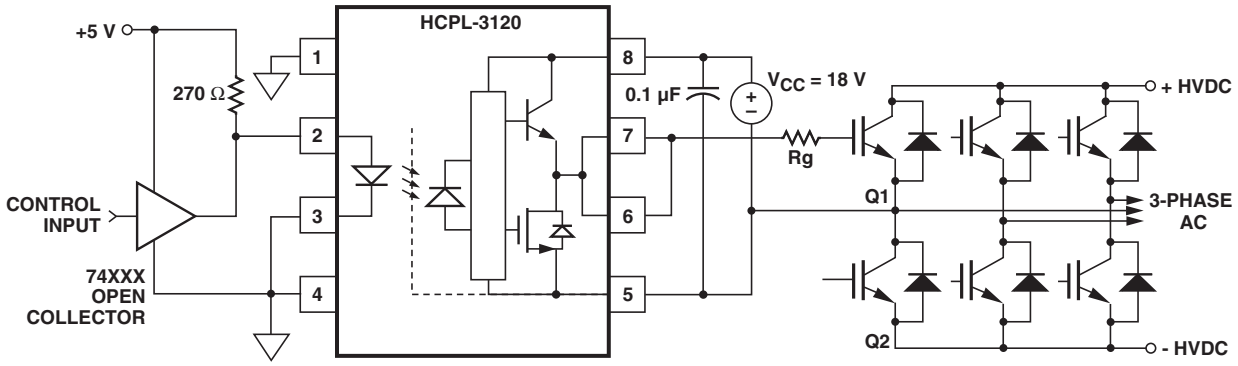
Application Information

Eliminating Negative IGBT Gate Drive

This section applies to HCPL-3120, HCPL-J312, and HCNW3120.

To keep the IGBT firmly off, the HCPL-3120 has a very low maximum V_{OL} specification of 0.5V. The HCPL-3120 achieves this very low V_{OL} by using a DMOS transistor with 1 (typical) on resistance in its pull-down circuit. When the HCPL-3120 is in the low state, the IGBT gate is shorted to the emitter by Rg + 1. Minimizing Rg and the lead inductance from the HCPL-3120 to the IGBT gate and emitter (possibly by mounting the HCPL-3120 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications, as shown in Figure 25. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-3120 input because this can result in unwanted coupling of transient signals into the HCPL-3120 and degrade performance. (If the IGBT drain must be routed near the HCPL-3120 input, then the LED should be reverse-biased when in the off state to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-3120.)

Figure 25: Recommended LED Drive and Application Circuit



Selecting the Gate Resistor (Rg) to Minimize IGBT Switching Losses

This section applies to HCPL-3120, HCPL-J312, and HCNW3120.

Step 1: Calculate Rg minimum from the I_{OL} peak specification. The IGBT and Rg in Figure 26 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-3120.

$$Rg \geq (V_{CC} - V_{EE} - V_{OL}) / I_{OLPEAK}$$

$$= (V_{CC} - V_{EE} - 2V) / I_{OLPEAK}$$

$$= (15V + 5V - 2V) / 2.5A$$

$$= 7.2\Omega \approx 8\Omega$$

The V_{OL} value of 2V in the previous equation is a conservative value of V_{OL} at the peak current of 2.5A (see Figure 6). At lower Rg values, the voltage supplied by the HCPL-3120 is not an ideal voltage step. This results in lower peak currents (more margin) than predicted by this analysis. When negative gate drive is not used, V_{EE} in the previous equation is equal to zero volts.

Step 2: Check the HCPL-3120 power dissipation and increase Rg if necessary. The HCPL-3120 total power dissipation (P_T) is equal to the sum of the emitter power (PE) and the output power (PO):

$$P_T = P_E + P_O$$

$$P_E = I_F \times V_F \times \text{Duty Cycle}$$

$$P_O = P_{O(BIAS)} + P_{O\ (SWITCHING)}$$

$$= I_{CC} \times (V_{CC} - V_{EE}) + E_{SW}(R_G, Q_G) \times f$$

For the circuit in Figure 26 with I_F (worst case) = 16 mA, Rg = 8Ω, Max Duty Cycle = 80%, Qg = 500 nC, f = 20 kHz and T_A max. = 85°C:

P_E = 16 mA × 1.8 V × 0.8 = 23 mW

P_O = 4.25 mA × 20 V + 5.2 µJ × 20 kHz

= 85 mW + 104 mW

= 189 mW > 178 mW ($P_{O(MAX)}$ at 85°C

= 250 mW/15°C × 4.8 mW/°C)

The value of 4.25 mA for I_{CC} in the previous equation was obtained by derating the I_{CC} max of 5 mA (which occurs at –40°C) to I_{CC} maximum at 85°C (see Figure 7).

Since PO for this case is greater than $P_{O(MAX)}$, Rg must be increased to reduce the HCPL-3120 power dissipation.

$P_{O(SWITCHING\ MAX)}$

= $P_{O(MAX)} - P_{O(BIAS)}$

= 178 mW – 85 mW

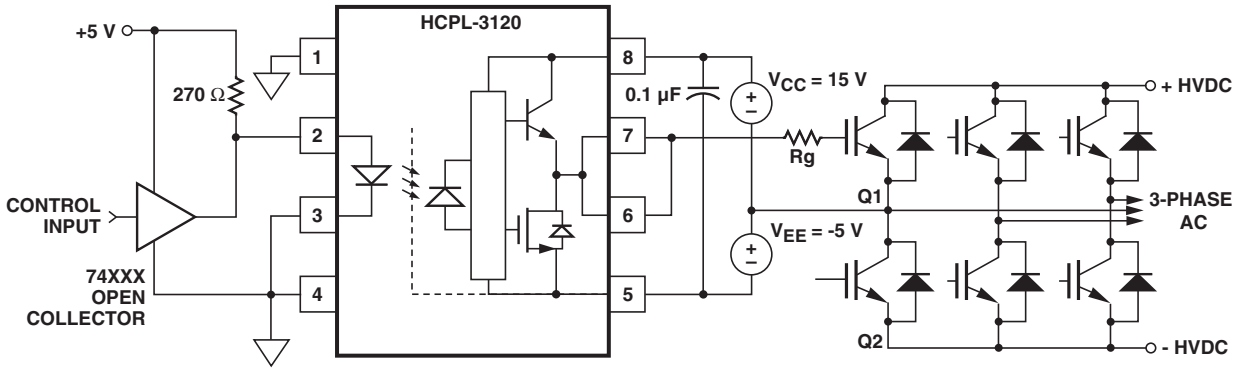
= 93 mW

$E_{SW(MAX)}$ = $(P_{O(SWITCHINGMAX)}) / f$

= 93 mW / 20 kHz = 4.65 µJ

For Qg = 500 nC, from Figure 27, a value of ESW = 4.65 µJ gives an Rg = 10.3Ω.

Figure 26: HCPL-3120 Typical Application Circuit with Negative IGBT Gate Drive



Thermal Model

This section applies to HCPL-3120, HCPL-J312, and HCNW3120.

The steady-state thermal model for the HCPL-3120 is shown in Figure 28. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. As shown by the model, all heat generated flows through θ_{CA}, which raises the case temperature T_C accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer. The value of θ_{CA} = 83°C/W was obtained from thermal measurements using a 2.5 × 2.5 inch PC board, with small traces (no ground plane), a single HCPL-3120 soldered into the center of the board and still air. The absolute maximum power dissipation derating specifications assume a θ_{CA}value of 83°C/W.

From the thermal mode in Figure 28, the LED and detector IC junction temperatures can be expressed as:

$$T_{JE} = P_E \approx (\theta_{LC}||(\theta_{LD} + \theta_{DC}) + \theta_{CA})$$

$$+ P_D \times (((\theta_{LC} \times \theta_{DC}) /(\theta_{LC} + \theta_{DC} + \theta_{LD})) + \theta_{CA}) + T_A$$

$$T_{JD} = P_E ((\theta_{LC} \times \theta_{DC}) /(\theta_{LC} + \theta_{DC} + \theta_{LD})) + \theta_{CA}$$

$$+ P_D \times (\theta_{DC}||(\theta_{LD} + \theta_{LC}) + \theta_{CA}) + T_A$$

Inserting the values for θ_{LC} and θ_{DC} shown in Figure 28 gives:

$$T_{JE} = P_E \times (256°C/W + \theta_{CA}) + P_D \bullet (57°C/W + \theta_{CA}) + T_A$$

$$T_{JD} = P_E \times (57°C/W + \theta_{CA}) + PD \times (111°C/W + \theta_{CA}) + T_A$$

For example, given P_E = 45 mW, P_O = 250 mW, T_A = 70 °C, and θ_{CA}= 83°C/W:

$$T_{JE} = P_E \times 339°C/W + P_D \times 140°C/W + T_A$$

$$= 45\ mW \times 339°C/W + 250\ mW \times 140°C/W + 70°C = 120°C$$

$$T_{JD} = P_E \times 140°C/W + P_D \times 194°C/W + T_A$$

$$= 45\ mW \times 140°C/W + 250\ mW \times 194°C/W + 70°C = 125°C$$

T_{JE} and T_{JD} should be limited to 125°C based on the board layout and part placement (θ_{CA}) specific to the application.

P_E Parameter	Description
I_F	LED Current
V_F	LED On Voltage
Duty Cycle	Maximum LED Duty Cycle

P_O Parameter	Description
I_{CC}	Supply Current
V_{CC}	Positive Supply Voltage
V_{EE}	Negative Supply Voltage
E_{SW}(Rg,Qg)	Energy Dissipated in the HCPL-3120 for each IGBT Switching Cycle (see Figure 27)
f	Switching Frequency

Figure 27: Energy Dissipated in the HCPL-3120 for Each IGBT Switching Cycle

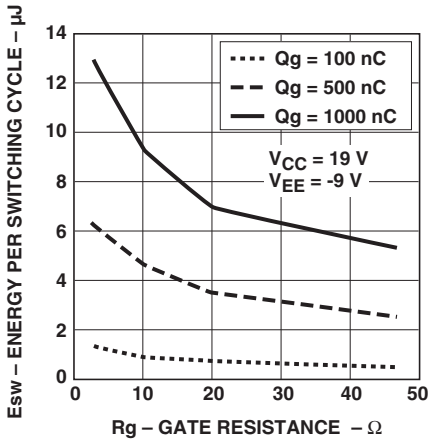
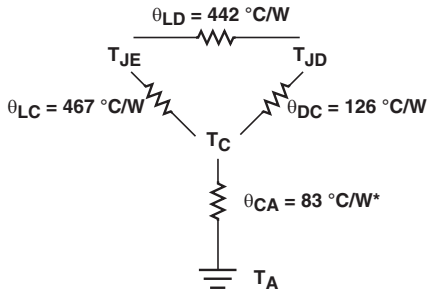


Figure 28: Thermal Model



T_{JE} = LED JUNCTION TEMPERATURE
T_{JD} = DETECTOR IC JUNCTION TEMPERATURE
T_C = CASE TEMPERATURE MEASURED AT THE CENTER OF THE PACKAGE BOTTOM
θ_{LC} = LED-TO-CASE THERMAL RESISTANCE
θ_{LD} = LED-TO-DETECTOR THERMAL RESISTANCE
θ_{DC} = DETECTOR-TO-CASE THERMAL RESISTANCE
θ_{CA} = CASE-TO-AMBIENT THERMAL RESISTANCE
*θ_{CA} WILL DEPEND ON THE BOARD DESIGN AND THE PLACEMENT OF THE PART.

LED Drive Circuit Considerations for Ultra-High CMR Performance

This section applies to HCPL-3120, HCPL-J312, and HCNW3120.

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 29. The HCPL-3120 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5–8 as shown in Figure 30. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 25), can achieve 25 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

Figure 29: Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers

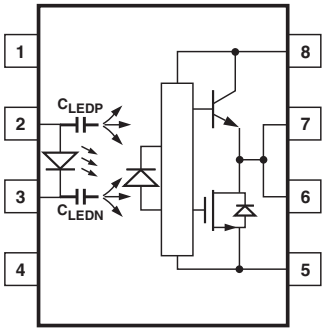
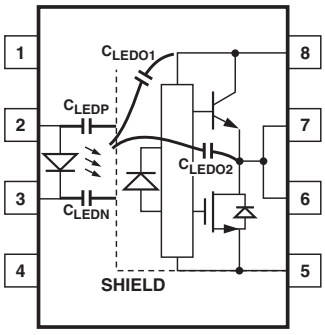


Figure 30: Optocoupler Input to Output Capacitance Model for Shielded Optocouplers



CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 10 mA provides adequate margin over the maximum I_{FLH} of 5 mA to achieve 25 kV/µs CMR.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{cm}/dt$ transient in Figure 31, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$, the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 31, cannot keep the LED off during a +dVcm/dt transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMRL performance. Figure 33 is an alternative drive circuit which, like the recommended application circuit (Figure 25), does achieve ultra high CMR performance by shunting the LED in the off state.

Figure 31: Equivalent Circuit for Figure 25 During Common Mode Transient

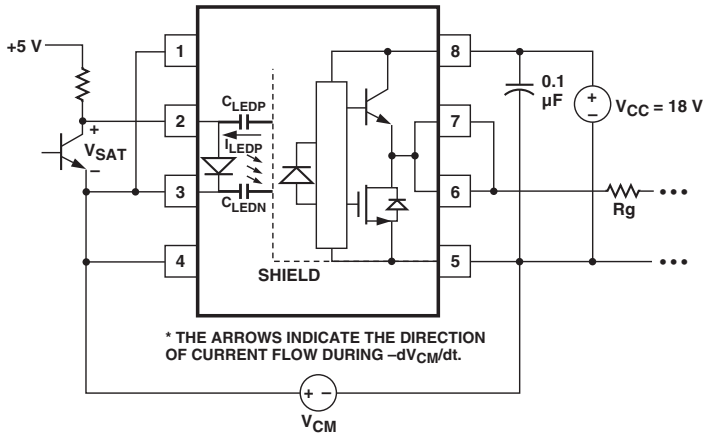


Figure 32: Not Recommended Open Collector Drive Circuit

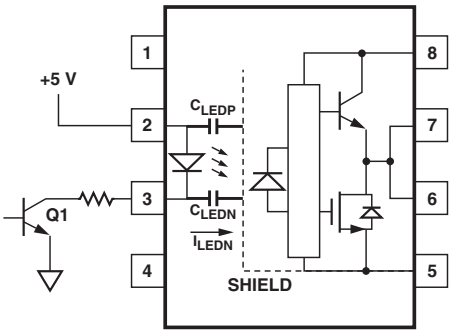


Figure 33: Recommended LED Drive Circuit for Ultra-High CMR

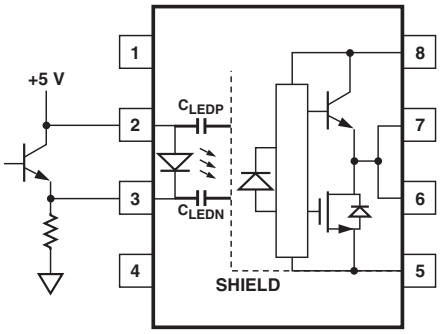
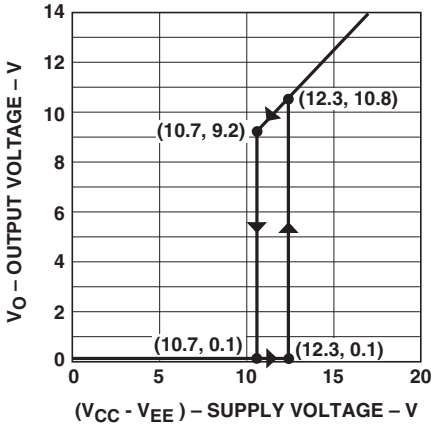


Figure 34: Under-voltage Lockout



Under-Voltage Lockout Feature

This section applies to HCPL-3120, HCPL-J312, and HCNW3120.

The HCPL-3120 contains an under-voltage lockout (UVLO) feature that is designed to protect the IGBT under fault conditions that cause the HCPL-3120 supply voltage (equivalent to the fully charged IGBT gate voltage) to drop below a level necessary to keep the IGBT in a low resistance state. When the HCPL-3120 output is in the high state and the supply voltage drops below the HCPL-3120 V_{UVLO-} threshold ($9.5 < V_{UVLO-} < 12.0$), the optocoupler output will go into the low state with a typical delay, UVLO Turn Off Delay, of 0.6 µs.

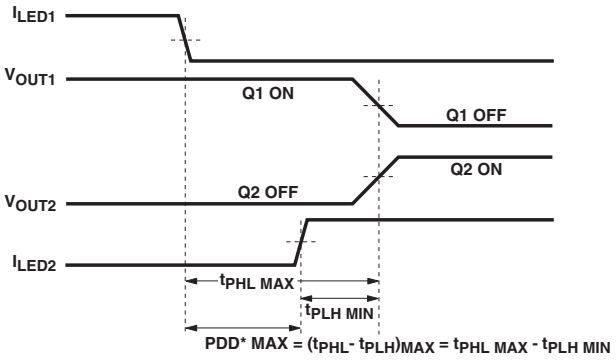
When the HCPL-3120 output is in the low state and the supply voltage rises above the HCPL-3120 V_{UVLO+} threshold ($11.0 < V_{UVLO+} < 13.5$), the optocoupler output will go into the high state (assumes LED is ON) with a typical delay, UVLO Turn On Delay, of 0.8 µs.

IPM Dead Time and Propagation Delay Specifications

This section applies to HCPL-3120, HCPL-J312, and HCNW3120.

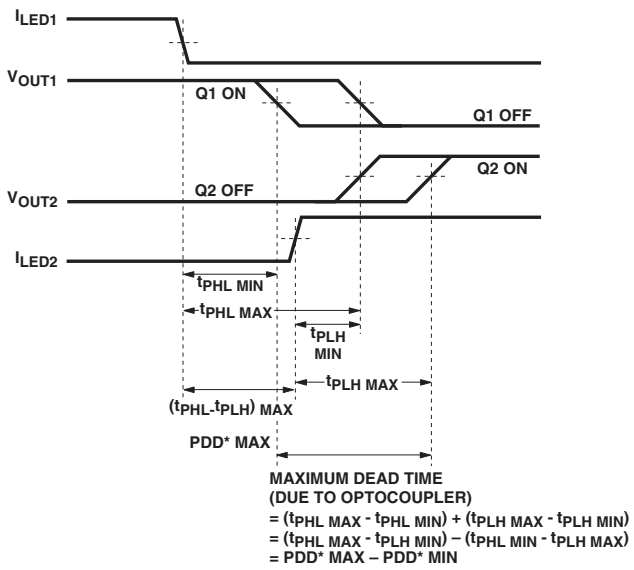
The HCPL-3120 includes a propagation delay difference (PDD) specification intended to help designers minimize *dead time* in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 25) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

Figure 35: Minimum LED Skew for Zero Dead Time



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 36: Waveforms for Dead Time



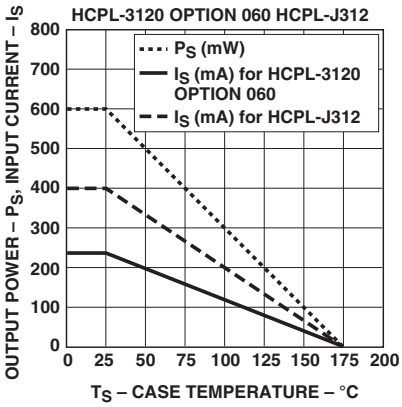
*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

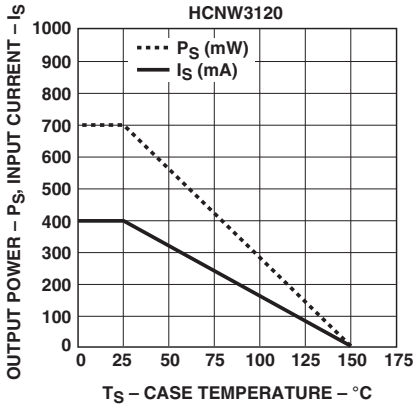
To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 35. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 350 ns over the operating temperature range of –40°C to +100°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 36. The maximum dead time for the HCPL-3120 is 700 ns (= 350 ns – (–350 ns)) over an operating temperature range of –40°C to +100°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

Figure 37: Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per IEC/EN/DIN EN 60747-5-5





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