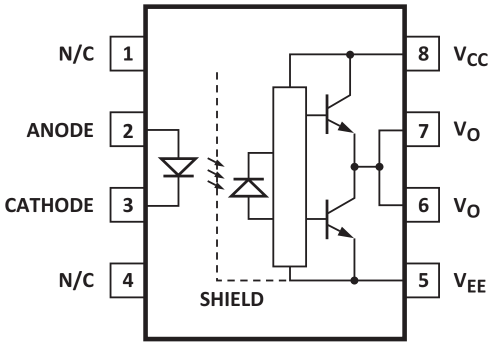
# HCPL-J314

## 0.6 Amp Output Current IGBT Gate Drive Optocoupler

## Description

The Broadcom® HCPL-J314 family of devices consists of an AlGaAs LED optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving small or medium power IGBTs. For IGBTs with higher ratings the HCPL-3150 (0.6A) or HCPL-3120 (2.5A) optocouplers can be used.

## Functional Diagram



HCPL-J314

**Table 1: Truth Table**

| LED | $V_O$ |
|---|---|
| OFF | LOW |
| ON | HIGH |

A 0.1-µF bypass capacitor must be connected between pins $V_{CC}$ and $V_{EE}$.

## Features

- 0.6A maximum peak output current
- 0.4A minimum peak output current
- High speed response:
  0.7 ìs max. propagation delay over temperature range
- Ultra-high CMR: min. 25 kV/µs at $V_{CM}$ = 1.5 kV
- Bootstrappable supply current: max. 3 mA
- Wide operating temperature range: –40°C to 100°C
- Wide $V_{CC}$ operating range: 10V to 30V over temperature range
- Available in DIP8 (single) and SO16 (dual) package
- Safety approvals:
  - UL Recognized, 3750$V_{rms}$ for 1 minute
  - CSA Approval
  - IEC/EN/DIN EN 60747-5-5 Approval.

**CAUTION!** Take normal static precautions in handling and assembling this component to prevent damage and/or degradation that might be induced by electrostatic discharge (ESD). The components featured in this data sheet are not to be used in military or aerospace applications or environments. The components are not AEC-Q100 qualified and are not recommended for automotive applications.

# Applications

- Isolated IGBT/Power MOSFET gate drive
- AC and brushless DC motor drives
- Inverters for appliances
- Industrial inverters
- Switch Mode Power Supplies (SMPS)
- Uninterruptable Power Supplies (UPS)

# Selection Guide

| Package Type | Part Number | Number of Channels |
|---|---|---|
| 8-pin DIP (300 mil) | HCPL-J314 | 1 |
| SO16 | HCPL-314J | 2 |

# Ordering Information

HCPL-J314 is UL Recognized with 3750$V_{rms}$ for 1 minute per UL1577.

| Part Number | Option |  | Package | Surface Mount | Gull Wing | Tape and Reel | IEC/EN/DIN EN 60747-5-5 | Quantity |
|---|---|---|---|---|---|---|---|---|
|  | RoHS Compliant | Non-RoHS Compliant |  |  |  |  |  |  |
| HCPL-J314 | -000E | No option | 300 mil DIP-8 | — | — | — | X | 50 per tube |
|  | -300E | #300 |  | X | X | — | X | 50 per tube |
|  | -500E | #500 |  | X | X | X | X | 1000 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1: HCPL-J314-500E to order product of 300 mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

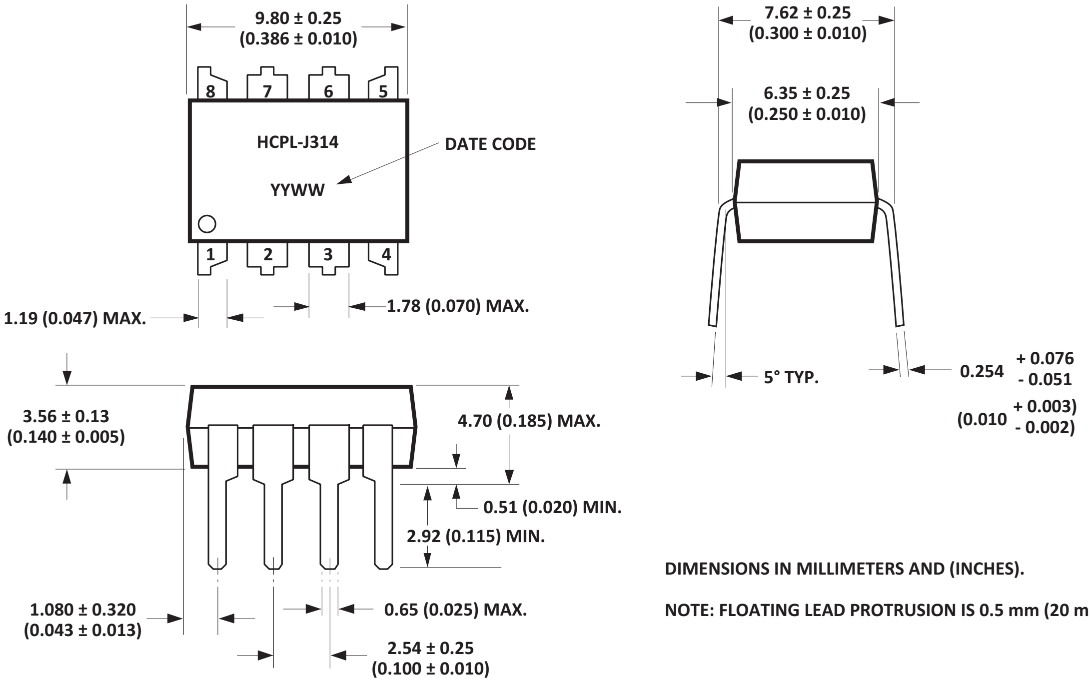
Example 2: HCPL-J314 to order product of 300 mil DIP package in tube packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and non-RoHS complaint

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option use '-XXXE'.

# HCPL-J314 Package Outline Drawings

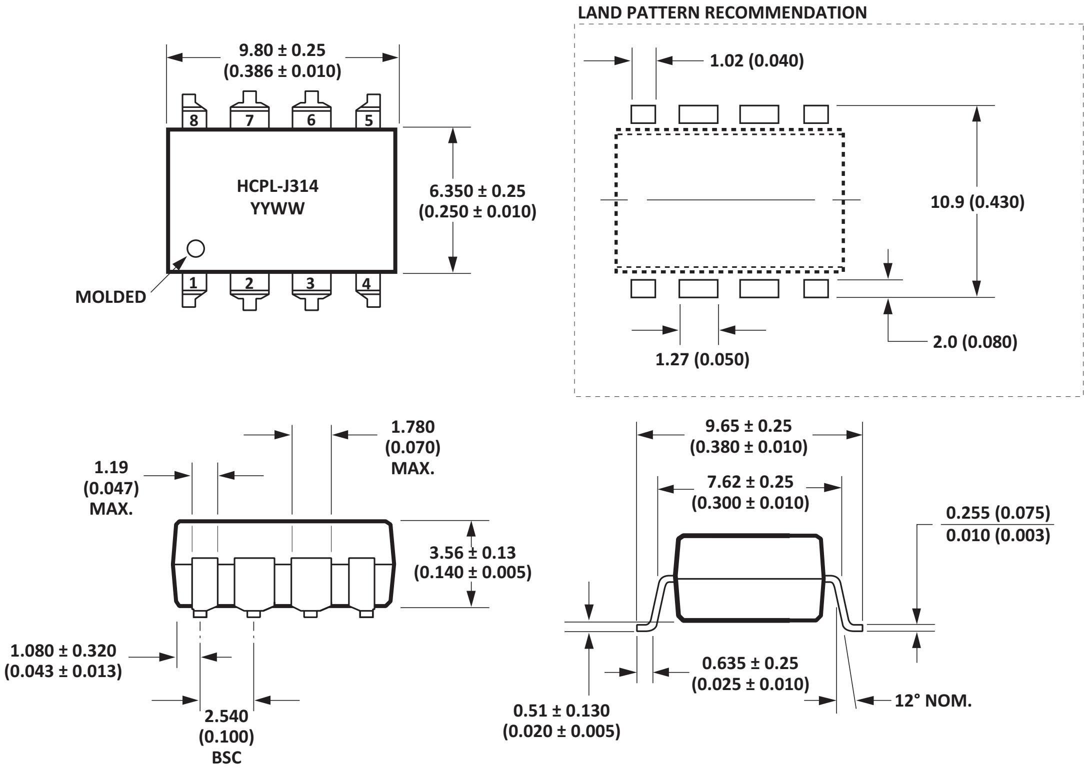
## Standard DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

## Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

# Recommended Pb-Free IR Profile

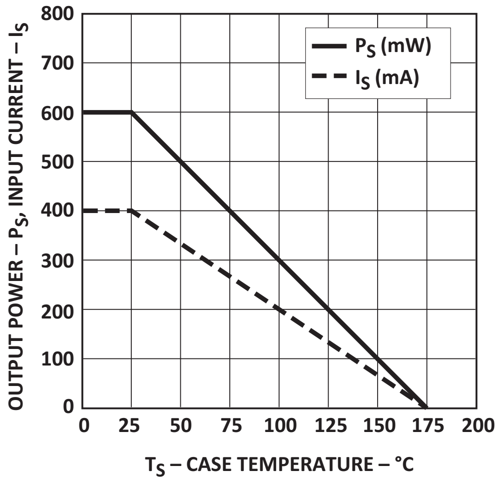
Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

# IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

| Description | Symbol | Characteristic | Unit |
|---|---|---|---|
| Installation classification per DIN VDE 0110/1.89, Table 1<br>For Rated Mains Voltage ≤ 150 $V_{rms}$<br>For Rated Mains Voltage ≤ 300 $V_{rms}$<br>For Rated Mains Voltage ≤ 600 $V_{rms}$ | | <br>I – IV<br>I – IV<br>I-III | |
| Climatic Classification | | 55/100/21 | |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 891 | $V_{PEAK}$ |
| Input to Output Test Voltage, Method b[a]<br>$V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m$ = 1 second, Partial discharge < 5 pC | $V_{PR}$ | 1670 | $V_{PEAK}$ |
| Input to Output Test Voltage, Method a[a]<br>$V_{IORM} \times 1.5 = V_{PR}$, Type and Sample Test, $t_m$ = 60 seconds, Partial discharge < 5 pC | $V_{PR}$ | 1336 | $V_{PEAK}$ |
| Highest Allowable Overvoltage<br>(Transient Overvoltage $t_{ini}$ = 10 seconds) | $V_{IOTM}$ | 6000 | $V_{PEAK}$ |
| Safety-limiting values – maximum values allowed in the event of a failure<br>Case Temperature<br>Input Current[b]<br>Output Power[b] | <br>$T_S$<br>$I_{S, INPUT}$<br>$P_{S, OUTPUT}$ | <br>175<br>400<br>1200 | <br>°C<br>mA<br>mW |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500V | $R_S$ | $>10^9$ | Ω |

[a] Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, IEC/EN/DIN EN 60747-5-5 for a detailed description of Method a and Method b partial discharge test profiles.

[b] Refer to the following figure for dependence of $P_S$ and $I_S$ on ambient temperature.



# Insulation and Safety-Related Specifications

| Parameter | Symbol | HCPL-J314 | Units | Conditions |
|---|---|---|---|---|
| Minimum External Air Gap (Clearance) | L(101) | 7.4 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (Creepage) | L(102) | 8.0 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | | 0.5 | mm | Through insulation, distance conductor to conductor, usually the straight-line distance thickness between the emitter and detector. |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | IIIa | — | Material Group (DIN VDE 0110, 1/89, Table 1) |

# Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units | Note |
|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | –55 | 125 | °C | |
| Operating Temperature | $T_A$ | –40 | 100 | °C | |
| Average Input Current | $I_{F(AVG)}$ | — | 25 | mA | 1 |
| Peak Transient Input Current (1 µs pulse width, 300 pps) | $I_{F(TRAN)}$ | — | 1.0 | A | |
| Reverse Input Voltage | $V_R$ | — | 5 | V | |
| High Peak Output Current | $I_{OH(PEAK)}$ | — | 0.6 | A | 2 |
| Low Peak Output Current | $I_{OL(PEAK)}$ | — | 0.6 | A | 2 |
| Supply Voltage | $V_{CC} - V_{EE}$ | –0.5 | 35 | V | |
| Output Voltage | $V_{O(PEAK)}$ | –0.5 | $V_{CC}$ | V | |
| Output Power Dissipation | $P_O$ | — | 260 | mW | 3 |
| Input Power Dissipation | $P_I$ | — | 105 | mW | 4 |
| Lead Solder Temperature | 260°C for 10 seconds, 1.6 mm below seating plane | | | | |
| Solder Reflow Temperature Profile | See HCPL-J314 Package Outline Drawings | | | | |

# Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Power Supply | $V_{CC} - V_{EE}$ | 10 | 30 | V | |
| Input Current (ON) | $I_{F(ON)}$ | 8 | 12 | mA | |
| Input Voltage (OFF) | $V_{F(OFF)}$ | –3.6 | 0.8 | V | |
| Operating Temperature | $T_A$ | –40 | 100 | °C | |

# Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Fig. | Notes |
|---|---|---|---|---|---|---|---|---|
| High Level Output Current | $I_{OH}$ | 0.2 | — | — | A | $V_O = V_{CC} – 4$ | 2 | 5 |
| | | 0.4 | 0.5 | — | A | $V_O = V_{CC} – 10$ | 3 | 2 |
| Low Level Output Current | $I_{OL}$ | 0.2 | 0.4 | — | A | $V_O = V_{EE} + 2.5$ | 5 | 5 |
| | | 0.4 | 0.5 | — | A | $V_O = V_{EE} + 10$ | 6 | 2 |
| High Level Output Voltage | $V_{OH}$ | $V_{CC} – 4$ | $V_{CC} – 1.8$ | — | V | $I_O = –100$ mA | 1 | 6, 7 |
| Low Level Output Voltage | $V_{OL}$ | — | 0.4 | 1 | V | $I_O = 100$ mA | 4 | |
| High Level Supply Current | $I_{CCH}$ | — | 0.7 | 3 | mA | $I_O = 0$ mA | 7, 8 | 14 |
| Low Level Supply Current | $I_{CCL}$ | — | 1.2 | 3 | mA | $I_O = 0$ mA | | |
| Threshold Input Current Low to High | $I_{FLH}$ | — | — | 6 | mA | $I_O = 0$ mA,<br>$V_O > 5V$ | 9, 15 | |
| Threshold Input Voltage Low to High | $V_{FHL}$ | 0.8 | — | — | V | | | |
| Input Forward Voltage | $V_F$ | 1.2 | 1.5 | 1.8 | V | $I_F = 10$ mA | 16 | |
| Temperature Coefficient of Input Forward Voltage | $\Delta V_F/\Delta T_A$ | — | –1.6 | — | mV/°C | $I_F = 10$ mA | | |
| Input Reverse Breakdown Voltage | $BV_R$ | 5 | — | — | V | $I_R = 10$ μA | | |
| Input Capacitance | $C_{IN}$ | — | 60 | — | pF | f = 1 MHz, $V_F = 0V$ | | |

# Switching Specifications (AC)

Over recommended operating conditions unless otherwise specified.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Fig. | Notes |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to High Output Level | $t_{PLH}$ | 0.1 | 0.2 | 0.7 | μs | Rg = 47Ω,<br>Cg = 3 nF,<br>f = 10 kHz,<br>Duty Cycle = 50%,<br>$I_F = 8$ mA,<br>$V_{CC} = 30V$ | 10, 11, 12, 13, 14, 17 | 14 |
| Propagation Delay Time to Low Output Level | $t_{PHL}$ | 0.1 | 0.3 | 0.7 | μs | | | |
| Propagation Delay Difference Between Any Two Parts or Channels | PDD | –0.5 | — | 0.5 | μs | | | 10 |
| Rise Time | $t_R$ | — | 50 | — | ns | | | |
| Fall Time | $t_F$ | — | 50 | — | ns | | | |
| Output High Level Common Mode Transient Immunity | $\|CM_H\|$ | 25 | 35 | — | kV/μs | $T_A = 25°C$,<br>$V_{CM} = 1.5$ kV | 18 | 11 |
| Output Low Level Common Mode Transient Immunity | $\|CM_L\|$ | 25 | 35 | — | kV/μs | | 18 | 12 |

# Package Characteristics

For each channel unless otherwise specified.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| Input-Output Momentary Withstand Voltage | $V_{ISO}$ | 3750 | — | — | $V_{rms}$ | $T_A = 25°C$<br>RH < 50% for 1 minute |  | 8, 9 |
| Output-Output Momentary Withstand Voltage | $V_{O-O}$ | 1500 | — | — | $V_{rms}$ |  |  | 15 |
| Input-Output Resistance | $R_{I-O}$ | — | $10^{12}$ | — | Ω | $V_{I-O} = 500$ V |  | 9 |
| Input-Output Capacitance | $C_{I-O}$ | — | 1.2 | — | pF | Freq. = 1 MHz |  |  |

**NOTE:**

1. Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with $I_O$ peak minimum = 0.4 A. See Applications Information for additional details on limiting $I_{OL}$ peak.
3. Derate linearly above 85°C, free air temperature at the rate of 4.0 mW/°C.
4. Input power dissipation does not require derating.
5. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.
6. In this test, $V_{OH}$ is measured with a DC load current. When driving capacitive load, $V_{OH}$ will approach $V_{CC}$ as $I_{OH}$ approaches zero amps.
7. Maximum pulse width = 1 ms, maximum duty cycle = 20%.
8. In accordance with UL 1577, each HCPL-J314 optocoupler is proof tested by applying an insulation test voltage ≥ 5000 $V_{rms}$ for 1 second (leakage detection current limit $I_{I-O} \leq 5$ µA). This test is performed before 100% production test for partial discharge (method B) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics table, if applicable.
9. Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.
10. PDD is the difference between $t_{PHL}$ and $t_{PLH}$ between any two parts or channels under the same test conditions.
11. Common mode transient immunity in the high state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse VCM to assure that the output will remain in the high state (for example, $V_O > 6.0V$).
12. Common mode transient immunity in a low state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, $V_{CM}$, to assure that the output will remain in a low state (for example, $V_O < 1.0V$).
13. This load condition approximates the gate load of a 1200V/25A IGBT.
14. For each channel. The power supply current increases when operating frequency and Qg of the driven IGBT increases.
15. The device is considered a two terminal device: Channel one output side pins shorted together, and channel two output side pins shorted together.

**Figure 1: $V_{OH}$ vs. Temperature**

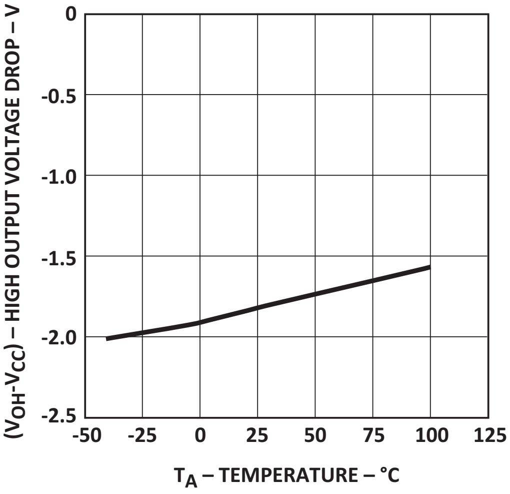


**Figure 2: $I_{OH}$ vs. Temperature**

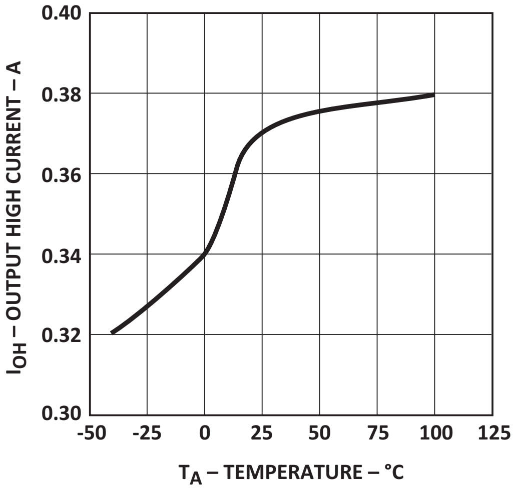


**Figure 3: $V_{OH}$ vs. $I_{OH}$**

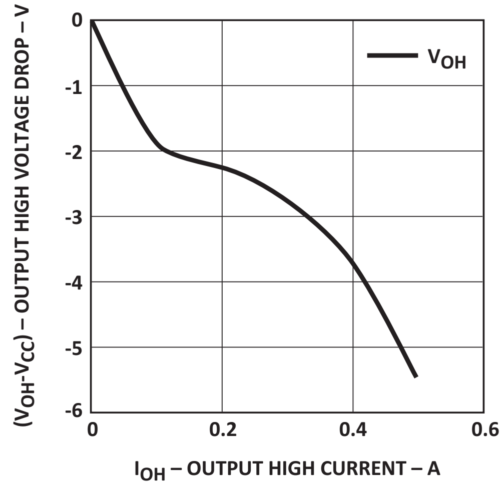


**Figure 4: $V_{OL}$ vs. Temperature**

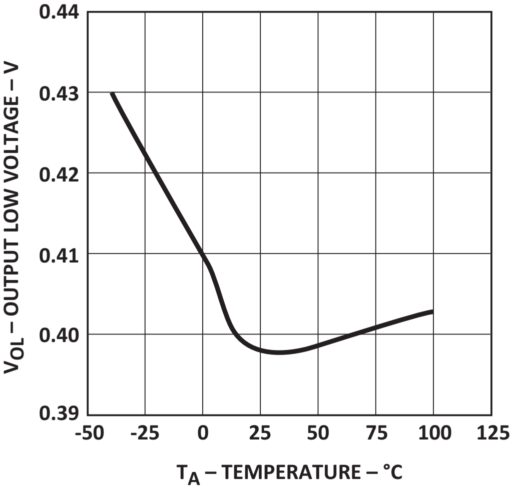


**Figure 5: $I_{OL}$ vs. Temperature**

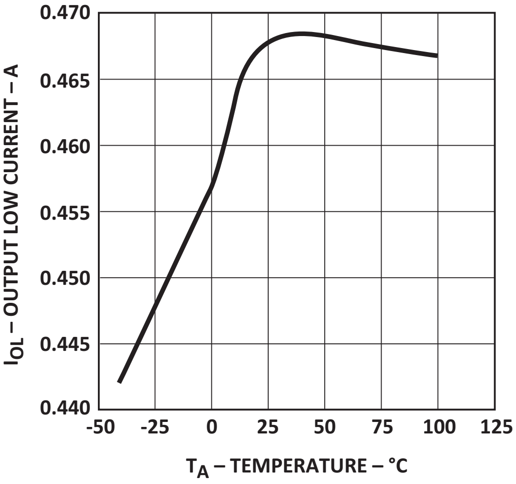


**Figure 6: $V_{OL}$ vs. $I_{OL}$**

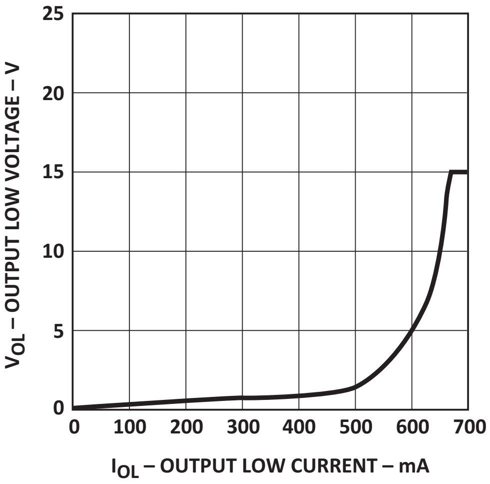


**Figure 7: $I_{CC}$ vs. Temperature**

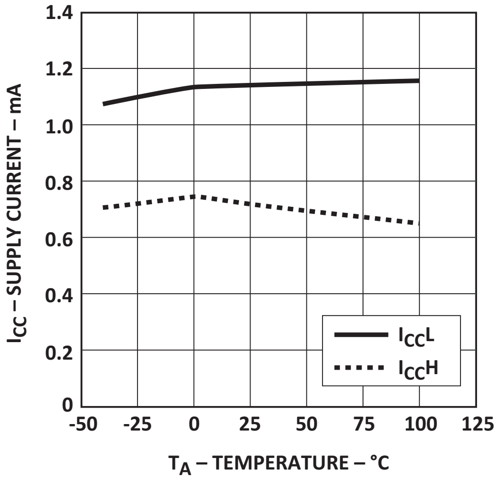


**Figure 8: $I_{CC}$ vs. $V_{CC}$**

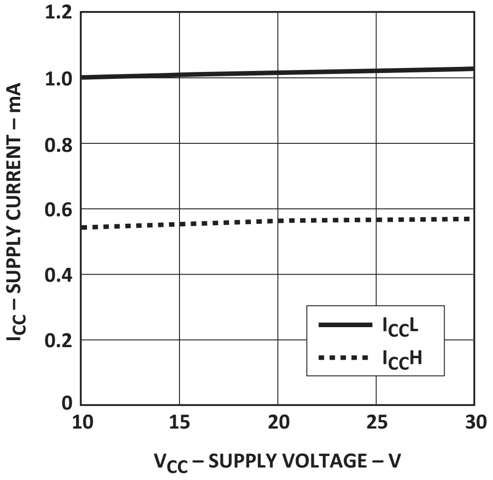


**Figure 9: $I_{FLH}$ vs. Temperature**

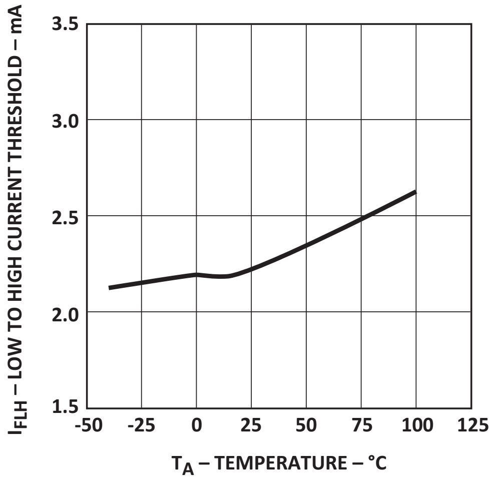


**Figure 10: Propagation Delay vs. $V_{CC}$**

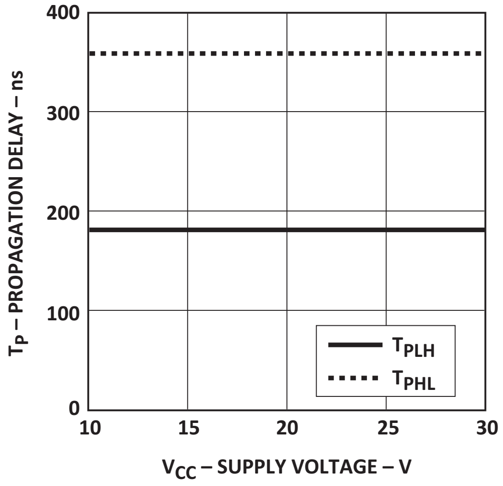


**Figure 11: Propagation Delay vs. $I_F$**

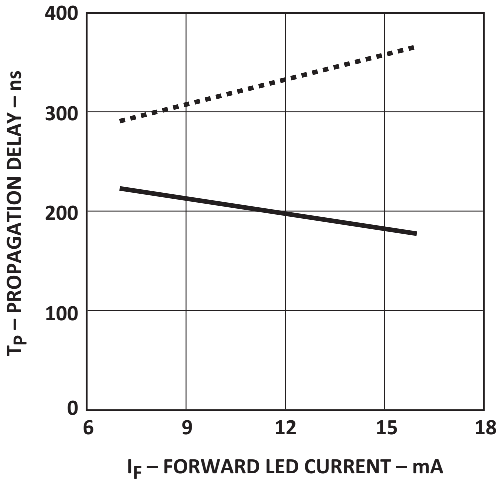
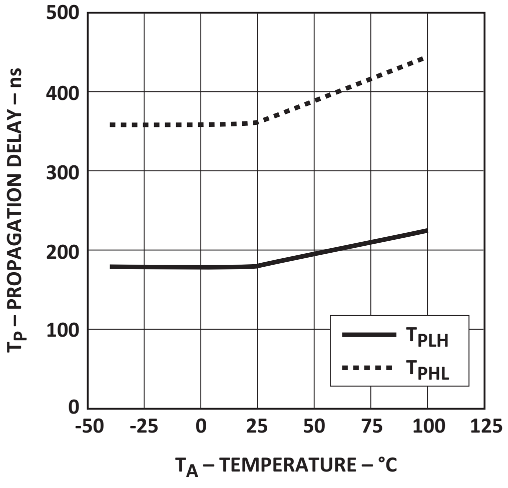
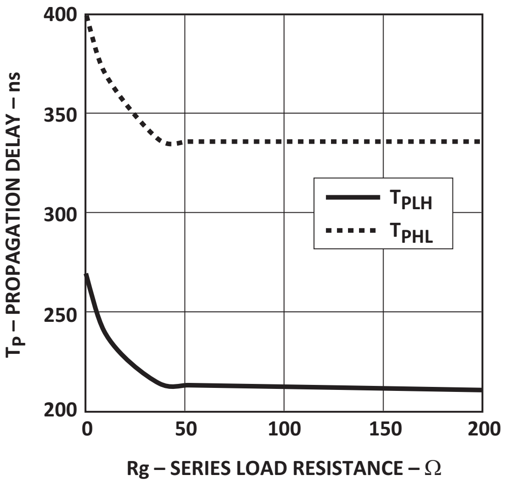


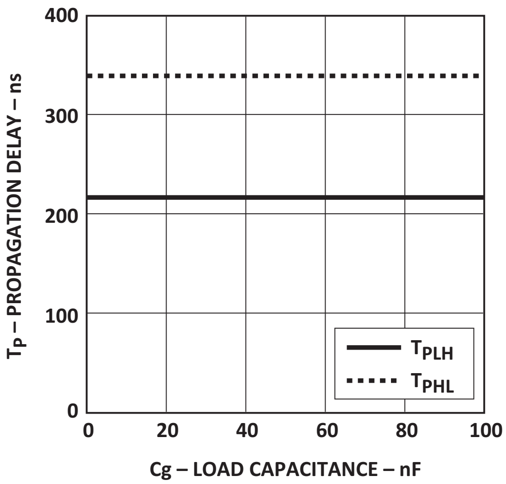
**Figure 12: Propagation Delay vs. Temperature**



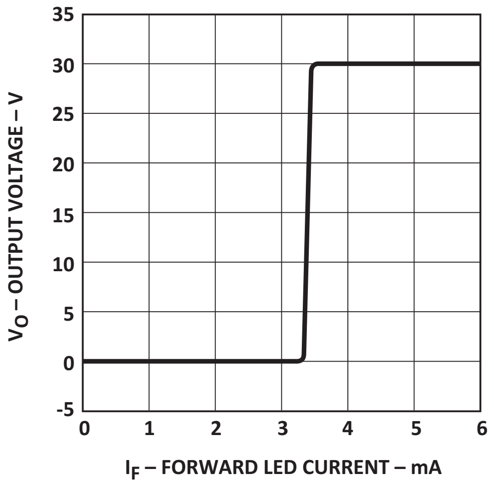
### Figure 13: Propagation Delay vs. Rg



### Figure 14: Propagation Delay vs. Cg



### Figure 15: Transfer Characteristics



### Figure 16: Input Current vs. Forward Voltage

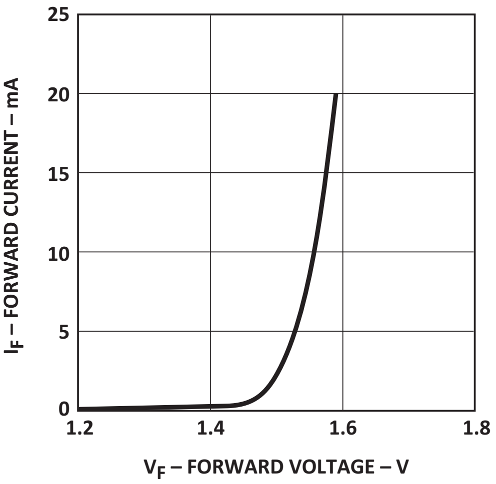


**Figure 17: Propagation Delay Test Circuit and Waveforms**

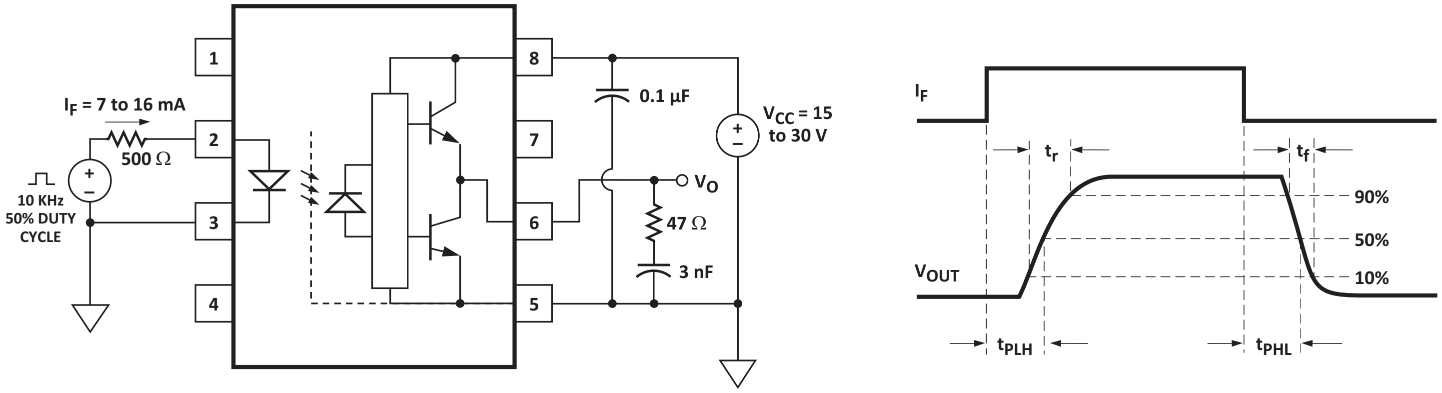
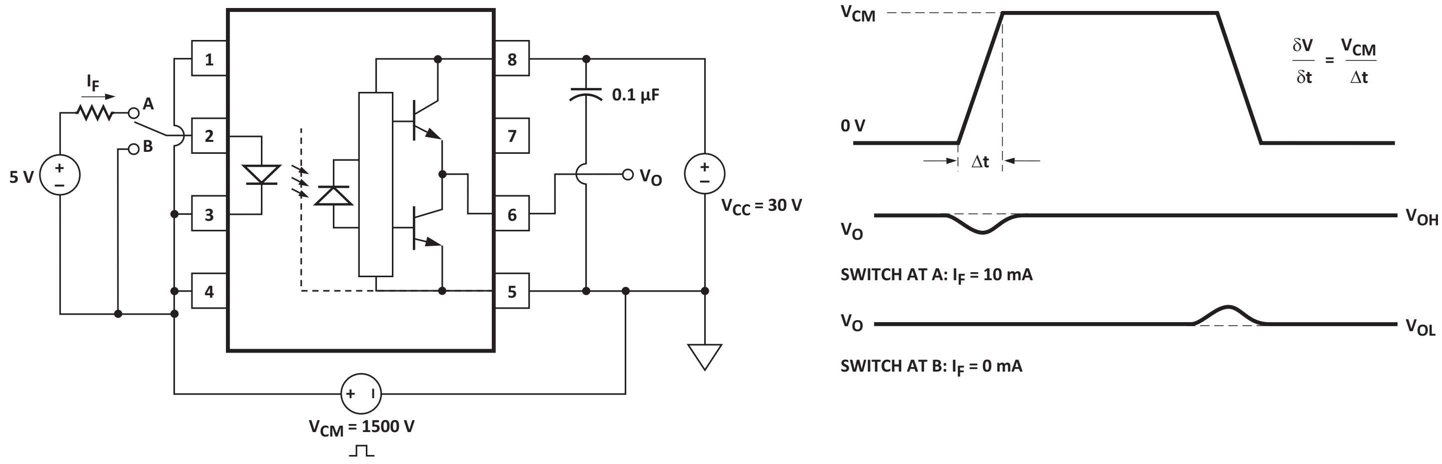


**Figure 18: CMR Test Circuit and Waveforms**

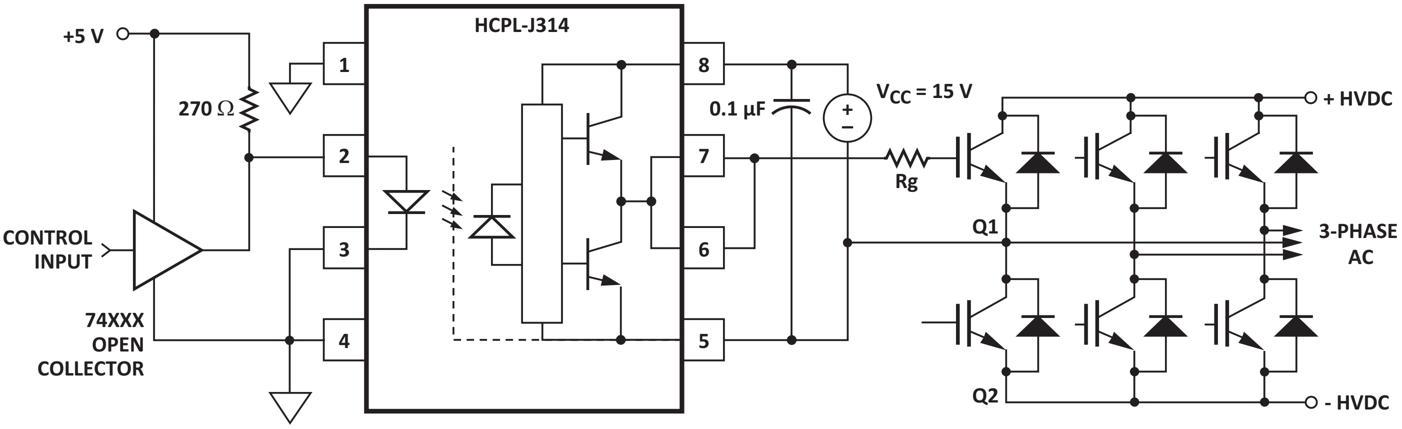


# Applications Information

## Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-J314 has a very low maximum $V_{OL}$ specification of 1.0V. Minimizing Rg and the lead inductance from the HCPL-J314 to the IGBT gate and emitter (possibly by mounting the HCPL-J314 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 19. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-J314 input as this can result in unwanted coupling of transient signals into the input of HCPL-J314 and degrade performance. (If the IGBT drain must be routed near the HCPL-J314 input, then the LED should be reverse biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-J314.)

**Figure 19: Recommended LED Drive and Application Circuit for HCPL-J314**



## Selecting the Gate Resistor (Rg)

1. Calculate Rg minimum from the IOL peak specification. The IGBT and Rg in Figure 19 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-J314.

$$Rg \geq \frac{V_{CC} - V_{OL}}{I_{OLPEAK}}$$

$$= \frac{24\ V - 5\ V}{0.6A}$$

$$= 32\ \Omega$$

The $V_{OL}$ value of 5V in the previous equation is the $V_{OL}$ at the peak current of 0.6A. See Figure 6.

2. Check the HCPL-J314 power dissipation and increase Rg if necessary. The HCPL-J314 total power dissipation ($P_T$) is equal to the sum of the emitter power ($P_E$) and the output power ($P_O$).

$P_T = P_E + P_O$

$P_E = I_F \times V_F \times \text{Duty Cycle}$

$P_O = P_{O(BIAS)} + P_{O(SWITCHING)}$

$= I_{CC} \times V_{CC} + E_{SW}(Rg,Qg) \times f$

$= (I_{CCBIAS} + K_{ICC} \times f) \times V_{CC} + E_{SW}(Rg, Qg) \times f$

where $K_{ICC} \times Qg \times f$ is the increase in $I_{CC}$ due to switching and $K_{ICC}$ is a constant of 0.001 mA/(nC*kHz). For the circuit in Figure 19 with $I_F$ (worst case) = 10 mA, Rg = 32 Ω, Max Duty Cycle = 80%, Qg = 100 nC, f = 20 kHz and $T_{AMAX}$ = 85°C:

$P_E = 10\ \text{mA} \times 1.8\text{V} \times 0.8 = 14\ \text{mW}$

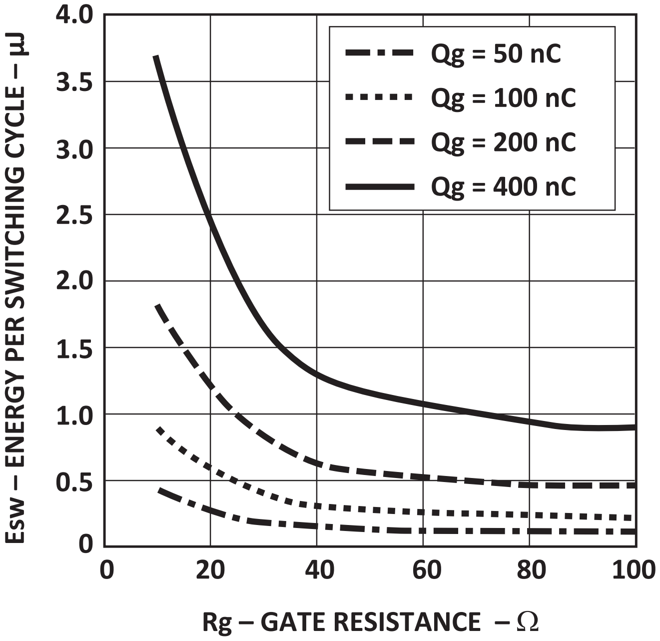
$P_O = (3\ \text{mA} + (0.001\ \text{mA/(nC} \times \text{kHz)}) \times 20\ \text{kHz} \times 100\ \text{nC}) \times 24\text{V} + 0.4\ \mu\text{J} \times 20\ \text{kHz} = 80\ \text{mW}$

$< 260\ \text{mW}\ (P_{O(MAX)}\ @\ 85°\text{C})$

The value of 3 mA for $I_{CC}$ in the previous equation is the max. $I_{CC}$ over the entire operating temperature range.

Since $P_O$ for this case is less than $P_{O(MAX)}$, Rg = 32 Ω is acceptable for the power dissipation.

**Figure 20: Energy Dissipated in the HCPL-J314 and for Each IGBT Switching Cycle**



## LED Drive Circuit Considerations for Ultra-High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 21. The HCPL-J314 improves CMR performance by using a detector IC with an optically-transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5 to 8 as shown in Figure 22. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 19) can achieve 10 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the following sections.

**Figure 21: Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers**

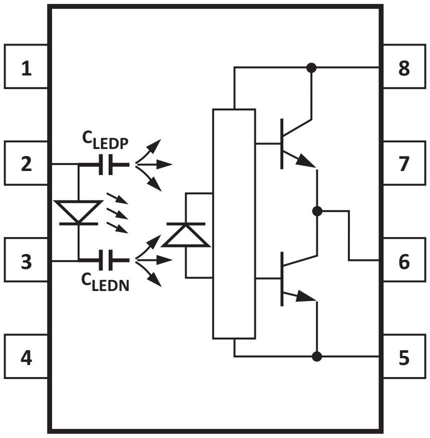


**Figure 22: Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers**

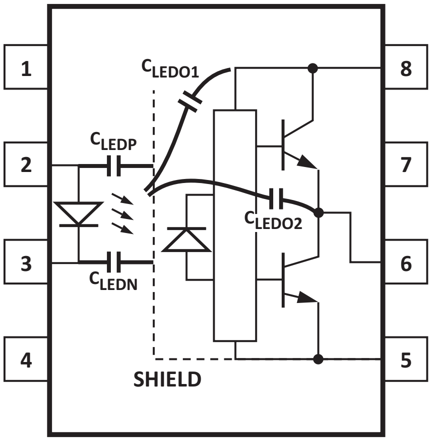
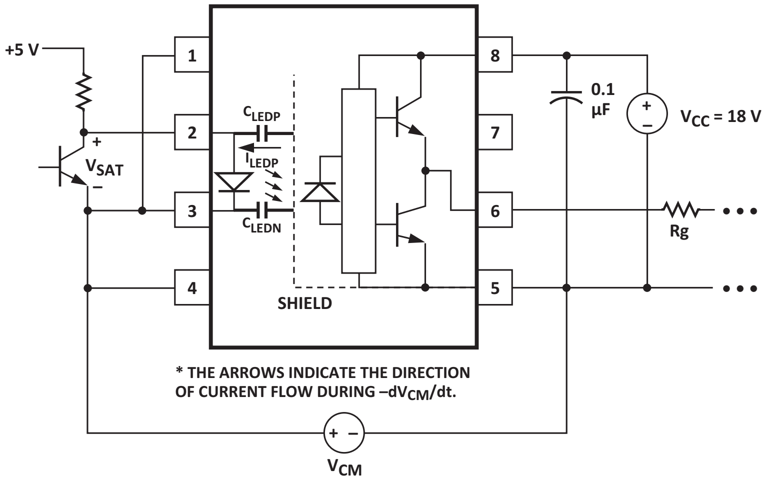


**Figure 23: Equivalent Circuit for Figure 17 During Common Mode Transient**



* THE ARROWS INDICATE THE DIRECTION OF CURRENT FLOW DURING $-dV_{CM}/dt$.

**Figure 24: Not Recommended Open Collector Drive Circuit**

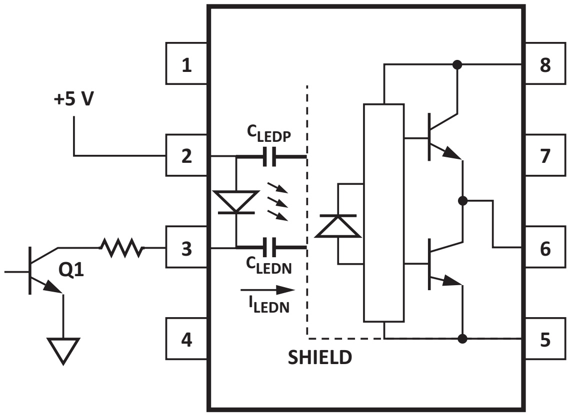
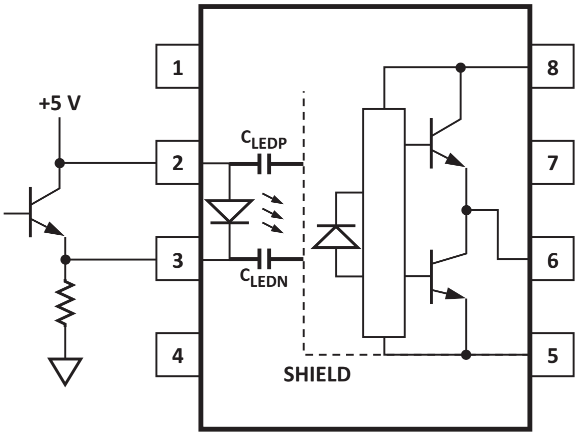


**Figure 25: Recommended LED Drive Circuit for Ultra-high CMR IPM Dead Time and Propagation Delay Specifications**



## CMR with the LED On ($CMR_H$)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 8 mA provides adequate margin over the maximum of 6 mA to achieve 25 kV/μs CMR. See Figure 26 and Figure 27.

## CMR with the LED Off ($CMR_L$)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{CM}/dt$ transient in Figure 23, the current flowing through $C_{LEDP}$ also flows through the RSAT and VSAT of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$, the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 24, can not keep the LED off during a $+dV_{CM}/dt$ transient, since all the current flowing through $C_{LEDN}$ must be supplied by the LED, and it is not recommended for applications requiring ultra-high CMR1 performance. The alternative drive circuit which, like the recommended application circuit (Figure 19), does achieve ultra-high CMR performance by shunting the LED in the off state.

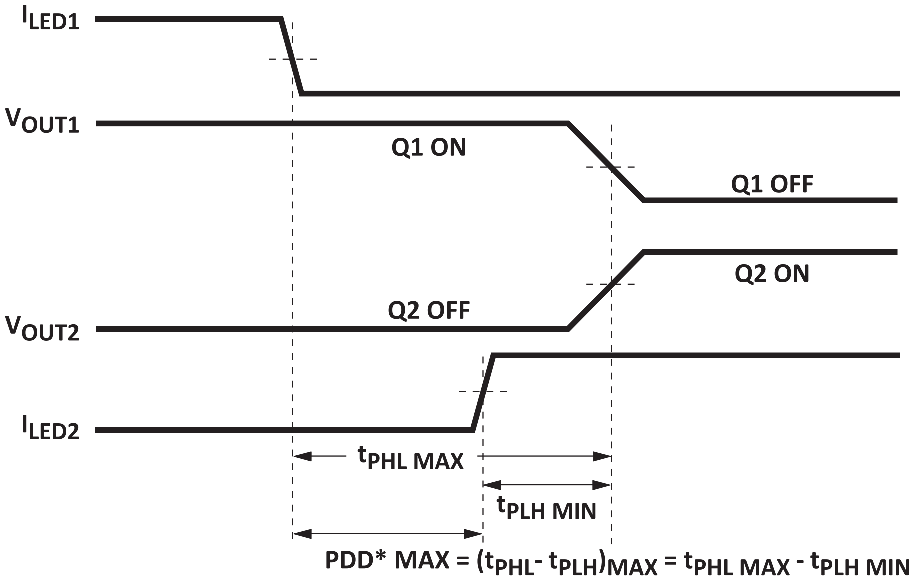
## IPM Dead Time and Propagation Delay Specifications

The HCPL-J314 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize *dead time* in their power inverter designs. Dead time is the time high-side and low-side power transistors are off. Any overlap in QI and Q2 conduction will result in large currents flowing through the power devices from the high-voltage to the low-voltage motor rails. To minimize dead time in a given design, the turn-on of LED2 should be delayed (relative to the turn-off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 26. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD max, which is specified to be 500 ns over the operating temperature range of –40° to 100°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specification as shown in Figure 27. The maximum dead time for the HCPL-J314 is 1 μs [= 0.5 μs – (–0.5 μs)] over the operating temperature range of –40°C to 100°C.

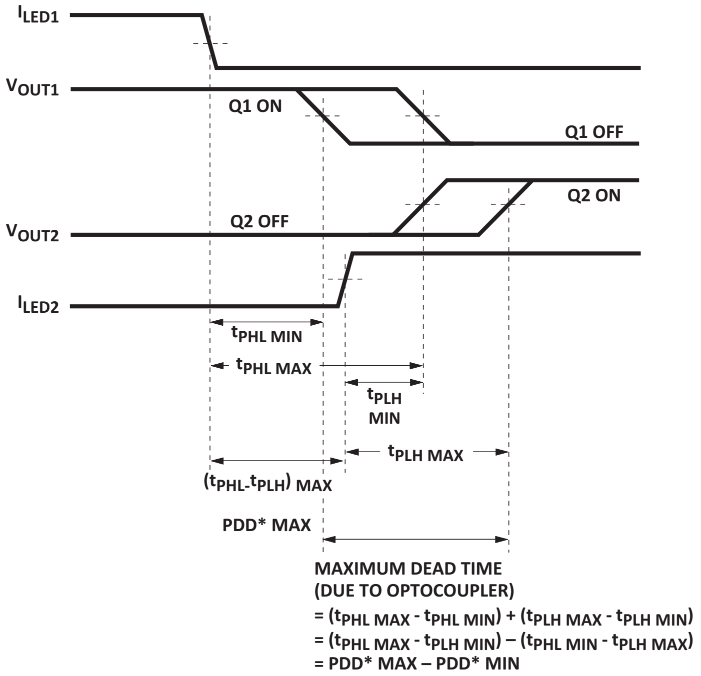
Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

**Figure 26: Minimum LED Skew for Zero Dead Time**



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS
ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

**Figure 27: Waveforms for Dead Time**



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION
DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

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