

Application Note 5314

Introduction

This application note covers the parasitic turn-on effect due to the Miller capacitor and how it is mitigated using an Active Miller Clamp.

One of the common problems faced when operating an IGBT is parasitic turn-on due to the Miller capacitor. This effect is noticeable in 0 to +15 V type gate drivers (single supply driver). Due to this gate-collector coupling, a high dV/dt transient created during IGBT turn-off can induce parasitic turn-on (Gate voltage spike), which is potentially dangerous (Figure 1).

Parasitic Turn-on via Miller Capacitor:

When turning on the upper IGBT, S1 in a half-bridge, a voltage change dV_{CE}/dt occurs across the lower IGBT, S2. A current flows through the parasitic Miller capacitor C_{CG} of S1, the gate resistor R_{GATE} and the internal gate resistor, R_{DRIVER} . Figure 1 shows the current flow through the capacitor. This current value can be approximated by the following formula:

$$I_{CG} = C_{CG} \frac{dV_{CE}}{dt} \quad (1)$$

This current creates a voltage drop across the gate resistor. If this voltage exceeds the IGBT gate threshold voltage, a parasitic turn-on occurs. It should be noted that rising IGBT chip temperature would lead to a slight reduction of gate threshold voltage.

This parasitic turn-on can also be seen on S1 when S2 is turned on.

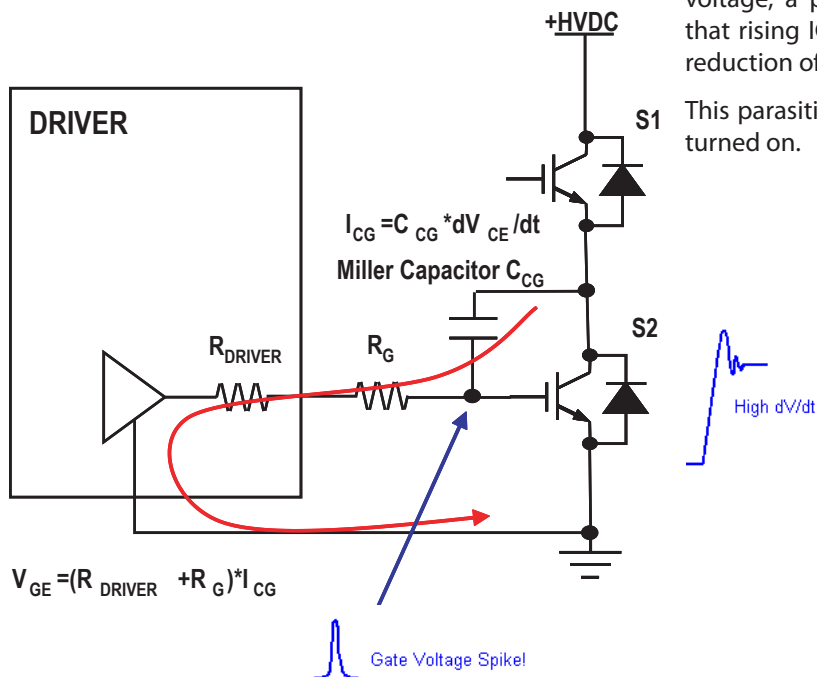


Figure 1. Bottom IGBT Parasitic Turn-On due to Miller Capacitor

There are two classical solution to the above problem; the first being to add a capacitor between gate and emitter (Figure 2), and the second solution is to use negative gate drive (Figure 3).

Additional gate emitter capacitor to shunt the Miller current: The additional capacitor C_G between gate and emitter will influence the switching behavior of the IGBT. C_G is to take up additional charge originating from the Miller capacitance. Due to the fact that the total input capacitance of the IGBT is $C_G || C_{CG}$, the gate charge necessary to reach the threshold voltage is increased (Figure 2).

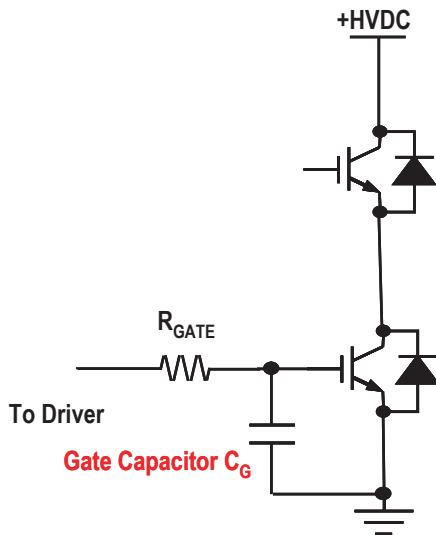


Figure 2. Additional Capacitor between Gate and Emitter

Also due to the additional capacitor, the required driver power is increased and the IGBT shows higher switching losses for the same R_{GATE} .

Negative Power Supply to Increase Threshold Voltage: The use of a negative gate voltage to safely turn-off and block the IGBT is typically used in an application with nominal current above 100 A. Due to cost, negative gate voltage is often not used in an IGBT application below 100 A. Figure 3 shows a typical circuit using a negative supply voltage.

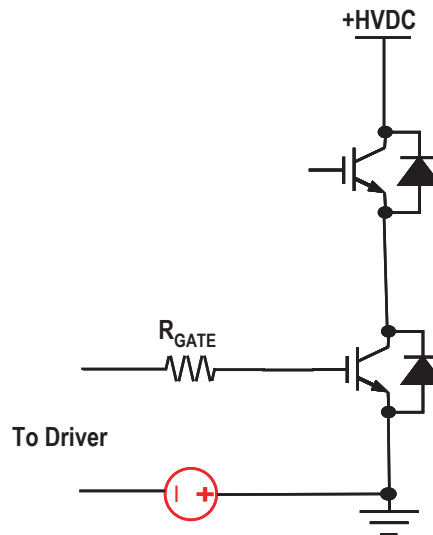


Figure 3. Negative Supply Voltage

Active Miller Clamp Solution

To avoid both efficiency loss due to C_G and additional cost for the negative supply voltage, another measure to prevent the unwanted IGBT turn-on is proposed by shorting the gate-to-emitter path. This can be achieved by an additional transistor between the gate and emitter. This 'switch' shorts the gate-emitter region after a threshold is reached. The occurring currents across the Miller capacitance are shunted by the transistor instead of flowing through the output driver pin, Vout (Pin 11). This technique is called Active Miller Clamp.

How it works: During turn-off, the gate voltage is monitored and the clamp is activated when the gate voltage goes below 2 V (relative to V_{EE}). The clamp voltage is typically $V_{OL} + 2.5$ V for a Miller current up to 1100 mA.

Figure 4 shows the ACPL-332J internal block diagram.

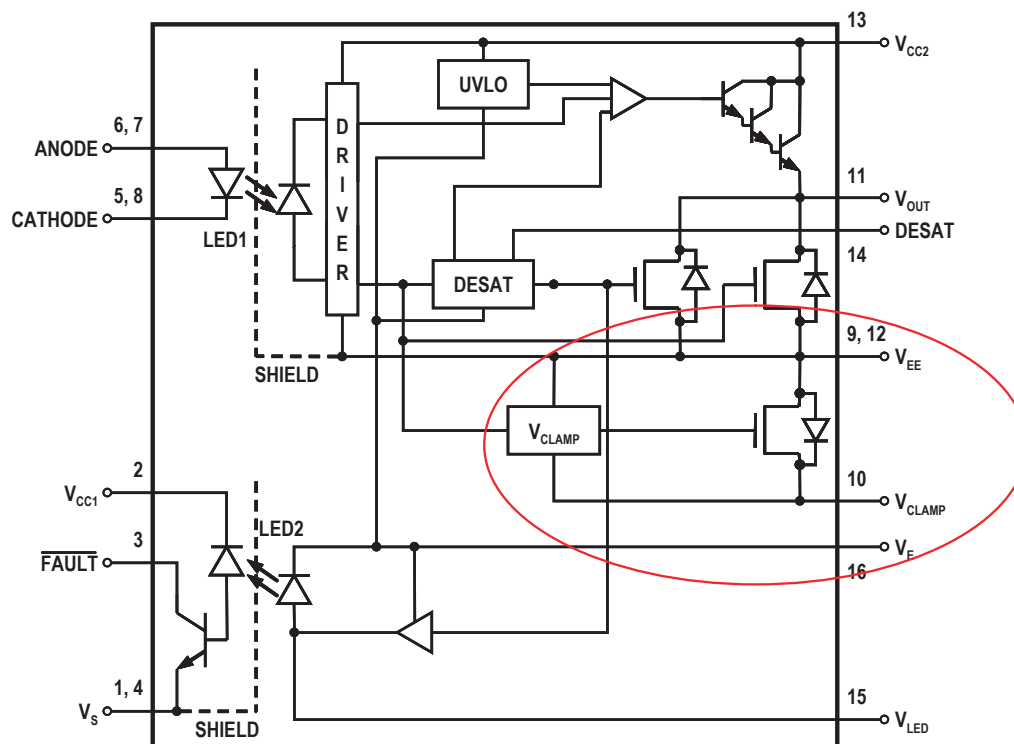


Figure 4. ACPL-332J Block Diagram; Active Miller Clamp Feature Circled in Red

Figures 5 to 7 show possible application circuits using Avago's Active Miller Clamp.

Application Note: If Active Clamp is not used, connect V_{CLAMP} to V_{EE}

Figure 5 is the recommended circuit for gate driver design with Miller Clamp (V_{CLAMP} pin).

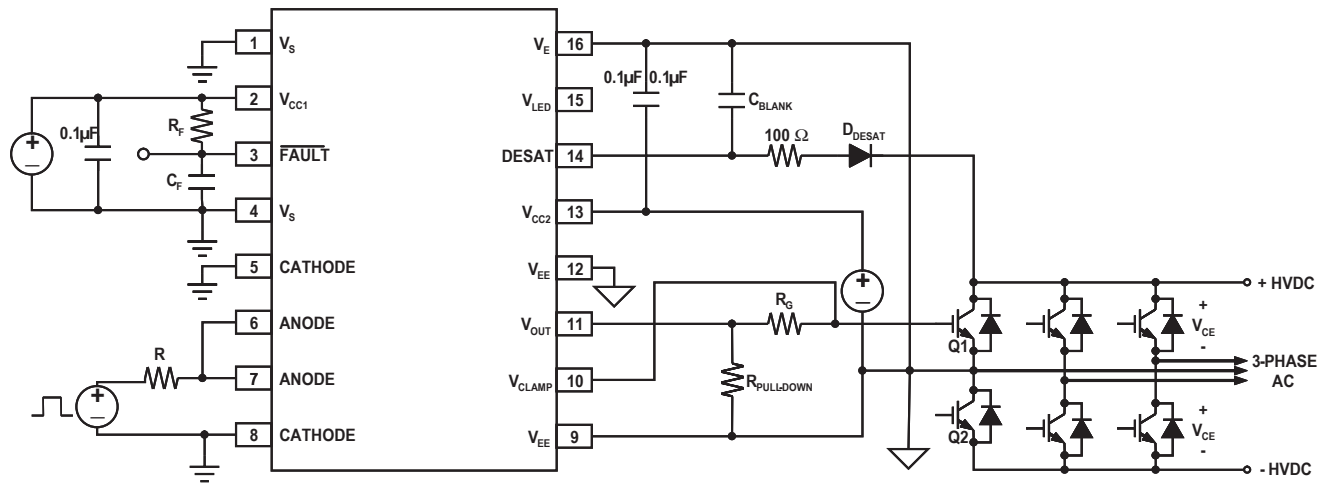


Figure 5. IGBT Driver with Single Power Supply, Desaturation Detection and Active Miller Clamp

Figure 6 shows the driver circuit using a negative gate driver for a high-power application. In such circumstances, the Miller clamp feature would not be required and hence Pin 10 is connected to pin 9, V_{EE} .

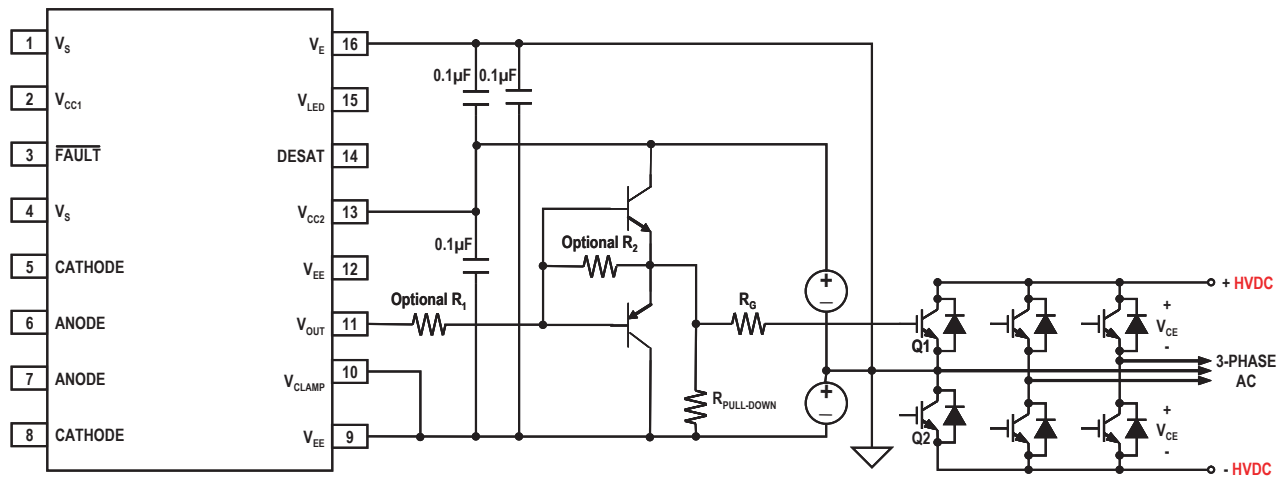


Figure 6. IGBT Driver with Negative Gate Drive for High-power Application

1. Use the clamp pin as a secondary gate discharge path (Figure 7a)
2. Use the clamp pin to control an additional PNP transistor to sink current. Connecting the Clamp DIRECTLY to the IGBT gate is not advisable for a high-power IGBT application as the internal clamp MOSFET is only rated up to 1.5 A. (Figure 7b)

For Figure 7, an optional resistor R1 may be added to reduce the current drawn from the driver. This will increase turn-on/off times of the IGBT. If not required, R1 should be shorted. Optional resistor R2 can be added to allow both the driver and buffer to provide current to the IGBT. R2 can be open circuited to prevent current being drawn from the driver to the IGBT.

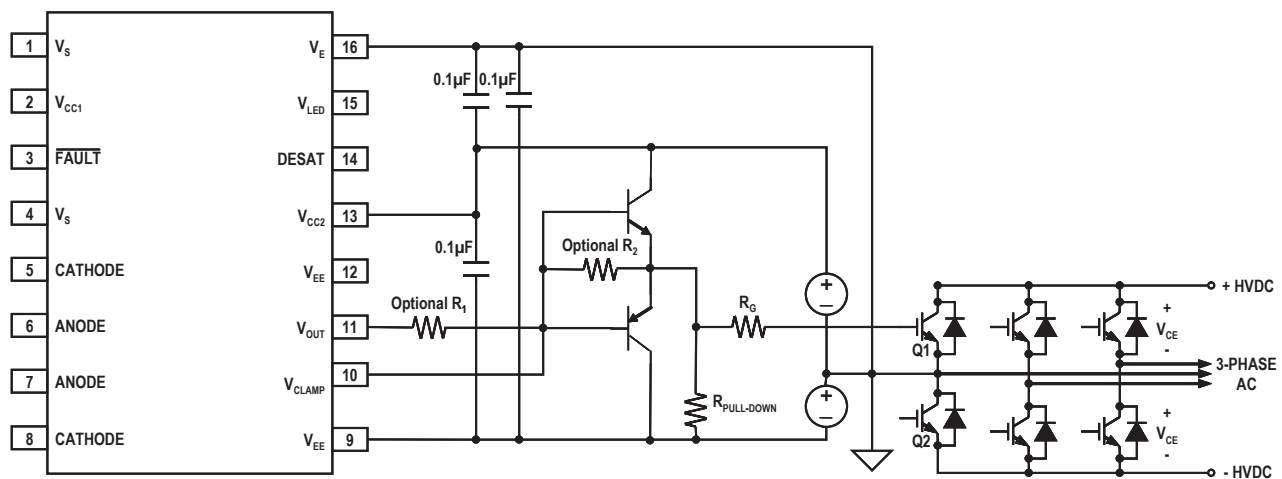


Figure 7a. Large IGBT Driver with Negative Gate Drive, External Buffer for High Current and Active Clamp as Secondary Gate Discharge

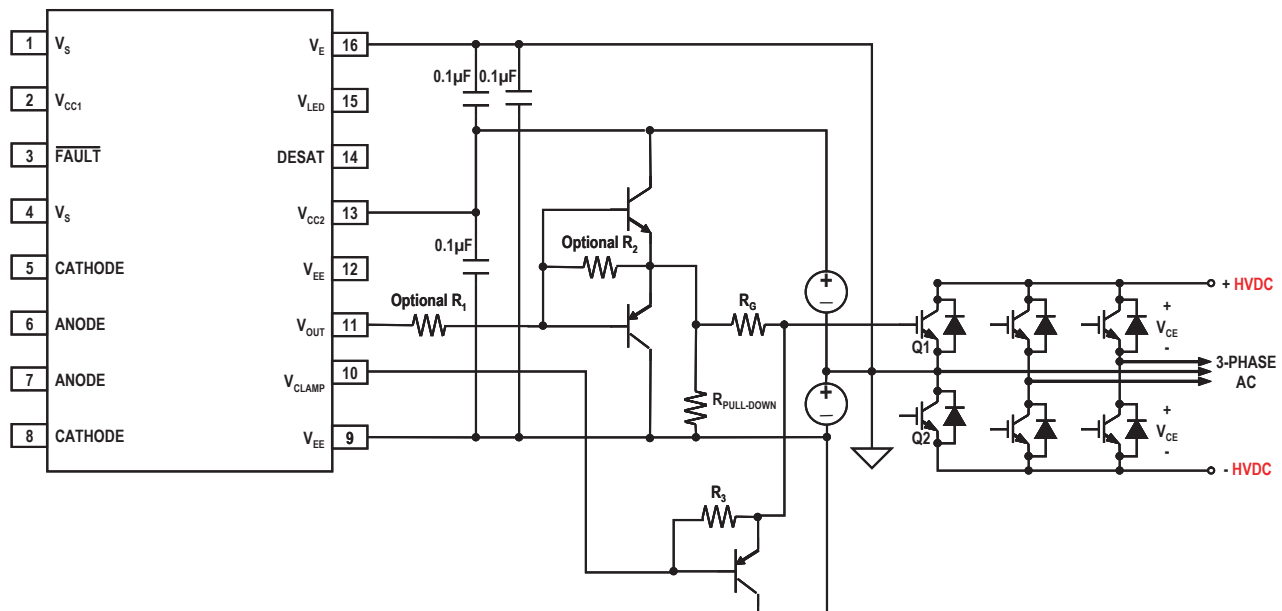


Figure 7b. Large IGBT Gate Drive with Negative Gate Drive, External Buffer for High Current and Active Clamp to Control Secondary Discharge Path For High Power Application

Conclusion

Avago Technologies gate optocouplers have a Miller Clamp function that controls the Miller current during a high dV/dt situation and keeps the IGBT totally off. It provides cost savings by eliminating the use of a negative supply voltage and additional capacitors that reduces driver efficiency.

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