

WS1413

4 x 4 Power Amplifier Module for CDMA PCS (1850–1910 MHz)



Data Sheet

Description

The WS1413, a Personal Communication Service (PCS) Power Amplifier (PA), is a fully matched 10-pin surface mount module developed for PCS and wireless local loop applications. This power amplifier module operates in the 1850-1910 MHz bandwidth. The WS1413 meets the stringent CDMA linearity requirements up to 28 dBm output power.

A low current (Vcont) pin is provided for high efficiency improvement of the low output power range. The WS1413 features CoolPAM circuit technology offering state-of-the-art reliability, temperature stability and ruggedness.

The WS1413 is self contained, incorporating 50ohm input and output matching networks.

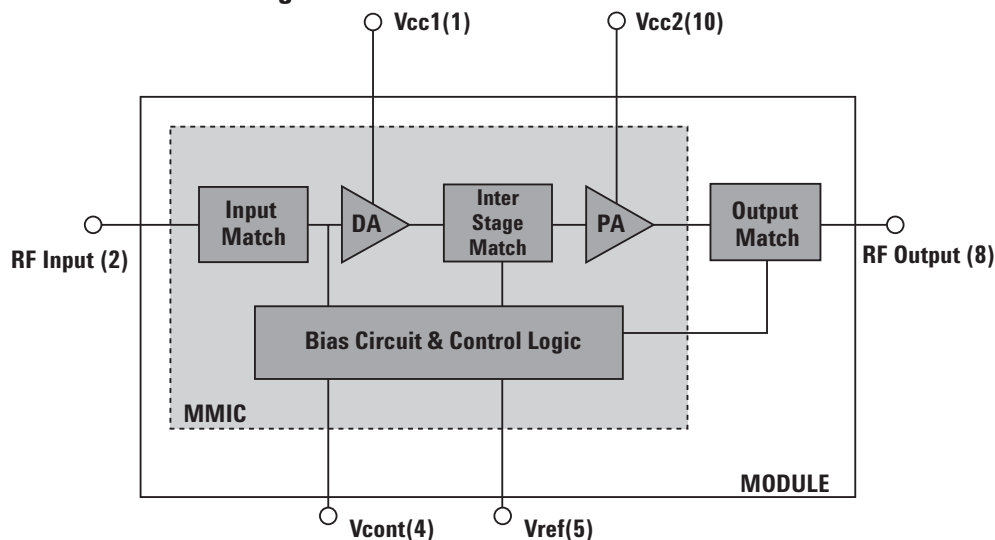
Features

- High efficiency
- 10-pin surface mounting package (4 mm x 4 mm x 1.4 mm)
- Low power-state control
- Low quiescent current
- Internal 50Ω matching networks for both RF input and output
- CDMA 95A/B, CDMA 2000-1X/EVDO

Applications

- Digital CDMA PCS
- Wireless Local Loop

Functional Block Diagram



Electrical Specifications

Table 1. Absolute Maximum Ratings⁽¹⁾

Parameter	Symbol	Min.	Nominal	Max.	Unit
RF Input Power	P_{in}	—	—	10.0	dBm
DC Supply Voltage	V_{cc}	—	3.4	5.0	V
DC Reference Voltage	V_{ref}	—	2.85	3.3	V
Storage Temperature	T_{stg}	-55	—	+125	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min.	Nominal	Max.	Unit
DC Supply Voltage	V_{cc}	3.2	3.4	4.2	V
DC Reference Voltage	V_{ref}	2.75	2.85	2.95	V
Mode Control Voltage					
– High Power Mode	V_{cont}	—	0	—	V
– Low Power Mode	V_{cont}	—	2.85	—	V
Operating Frequency	F_o	1850		1910	MHz
Ambient Temperature	T_a	-30	25	85	°C

Table 3. Power Range Truth Table

Power Mode	Symbol	Vref	Vcont ⁽²⁾	Range
High Power Mode ⁽³⁾	PR2	2.85	Low	~28 dBm
Low Power Mode ⁽³⁾	PR1	2.85	High	~18 dBm
Shut Down Mode ⁽⁴⁾	—	0.00	—	—

Notes:

1. No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.
2. High (1.5 V–3.0V), Low (0.0V – 0.5V).
3. To change between High Power Mode and Low Power Mode, switch Vcont accordingly.
4. In order to shut down the module, turn off Vref accordingly.

Electrical Specifications, continued

Table 4. Electrical Characteristics for CDMA Mode (Vcc = 3.4V, Vref = 2.85V, T = 25°C)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Gain	Gain_hi	Pout = 28.0 dBm	24	27		dB
	Gain_low	Pout = 18.0 dBm	17	21		dB
Power Added Efficiency	PAE_hi	Pout = 28.0 dBm	37	40		%
	PAE_low	Pout = 18.0 dBm	22	27		%
Total Supply Current	Icc_hi	Pout = 28.0 dBm		465	500	mA
	Icc_low	Pout = 18.0 dBm		65	80	mA
Quiescent Current	Iq_hi	High Power Mode	45	65	90	mA
	Iq_low	Low Power Mode	7	13	22	mA
Reference Current	Iref_hi	Pout = 28.0 dBm		3.5	7	mA
	Iref_low	Pout = 18.0 dBm		4	8	mA
Control Current ^[1]	Icont	Pout = 18.0 dBm		0.18	1	mA
Total Current in Power-down Mode	Ipd	Vref = 0.0V		0.2	5	μA
ACPR in High power mode	1.25 MHz offset ACPR1_hi	Pout = 28.0 dBm		-50	-45	dBc
	1.98 MHz offset ACPR2_hi	Pout = 28.0 dBm		-60	-56	dBc
ACPR in Low power mode	1.25 MHz offset ACPR1_low	Pout = 18.0 dBm		-52	-47	dBc
	1.98 MHz offset ACPR2_low	Pout = 18.0 dBm		-60	-56	dBc
Harmonic Suppression	Second 2fo	Pout = 28.0 dBm		-40	-30	dBc
	Third 3fo	Pout = 28.0 dBm		-55	-40	dBc
Input VSWR	VSWR			2:1	2.5:1	VSWR
Stability (Spurious Output)	S	VSWR 6:1, All phase			-60	dBc
Noise Power in RX Band	RxBN	Pout = 28 dBm		-136	-132	dBm/Hz
Ruggedness	Ru	Pout < 28 dBm, Pin < 10.0 dBm			10:1	VSWR

Note:

1. Control current when series 6.2kohm is used.

Characterization Data ($V_{cc}=3.4V$, $V_{ref}=2.85V$, $T=25^{\circ}C$, $F_o=1880\text{ MHz}$)

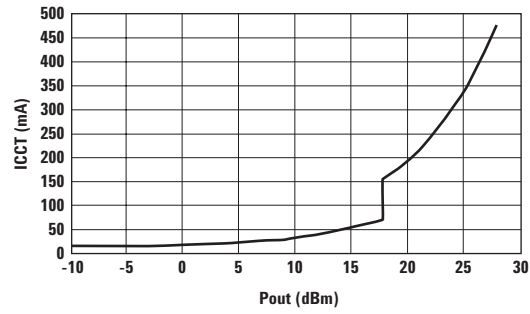


Figure 1. Total Current vs. Output Power.

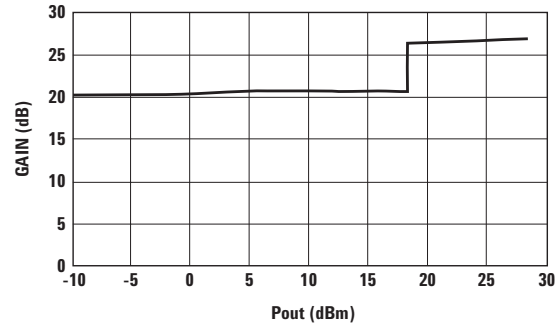


Figure 2. Gain vs. Output Power.

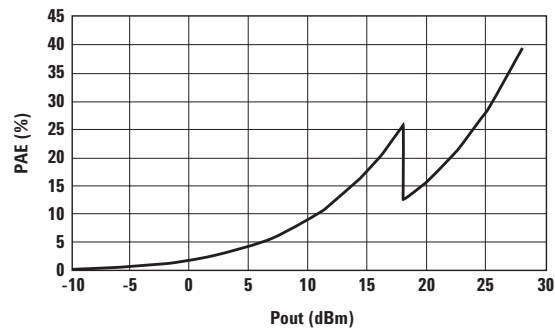


Figure 3. Power Added Efficiency vs. Output Power.

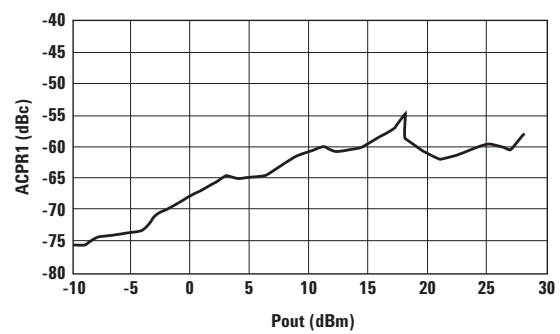


Figure 4. Adjacent Channel Power Ratio 1 vs. Output Power.

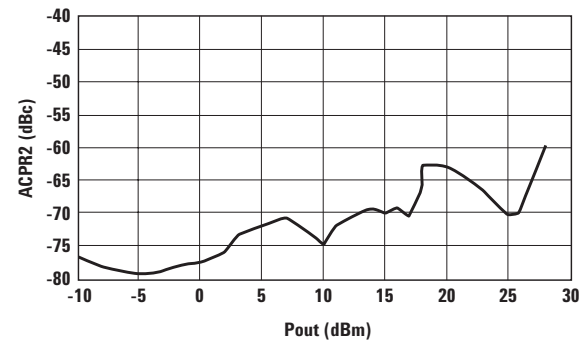


Figure 5. Adjacent Channel Power Ratio 2 vs. Output Power.

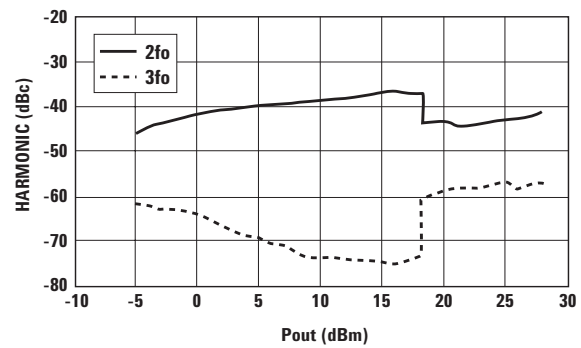


Figure 6. Harmonic Suppression vs. Output Power (Digital Mode).

Evaluation Board Description

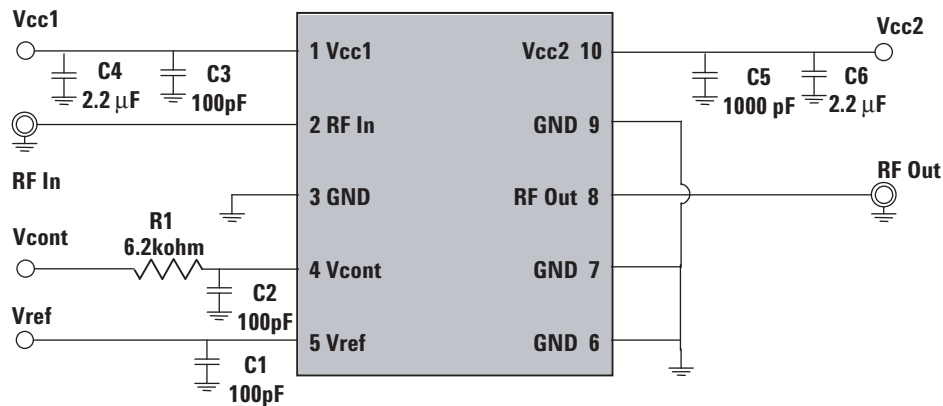


Figure 7. Evaluation Board Schematic.

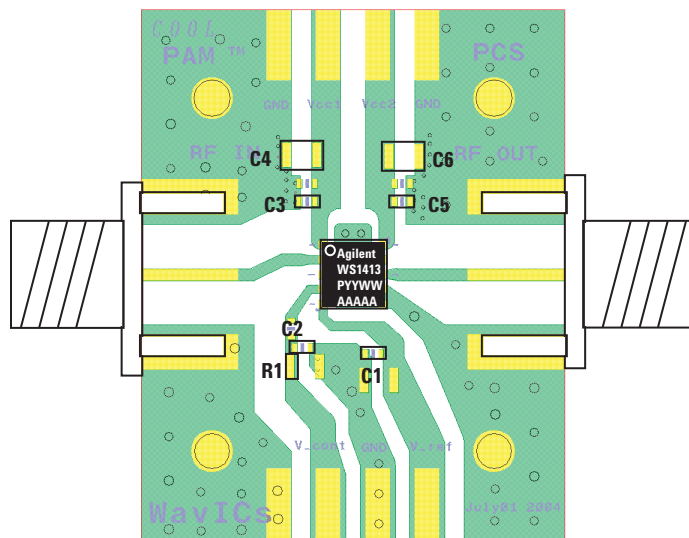


Figure 8. Evaluation Board Assembly Diagram.

Package Dimensions and Pin Descriptions

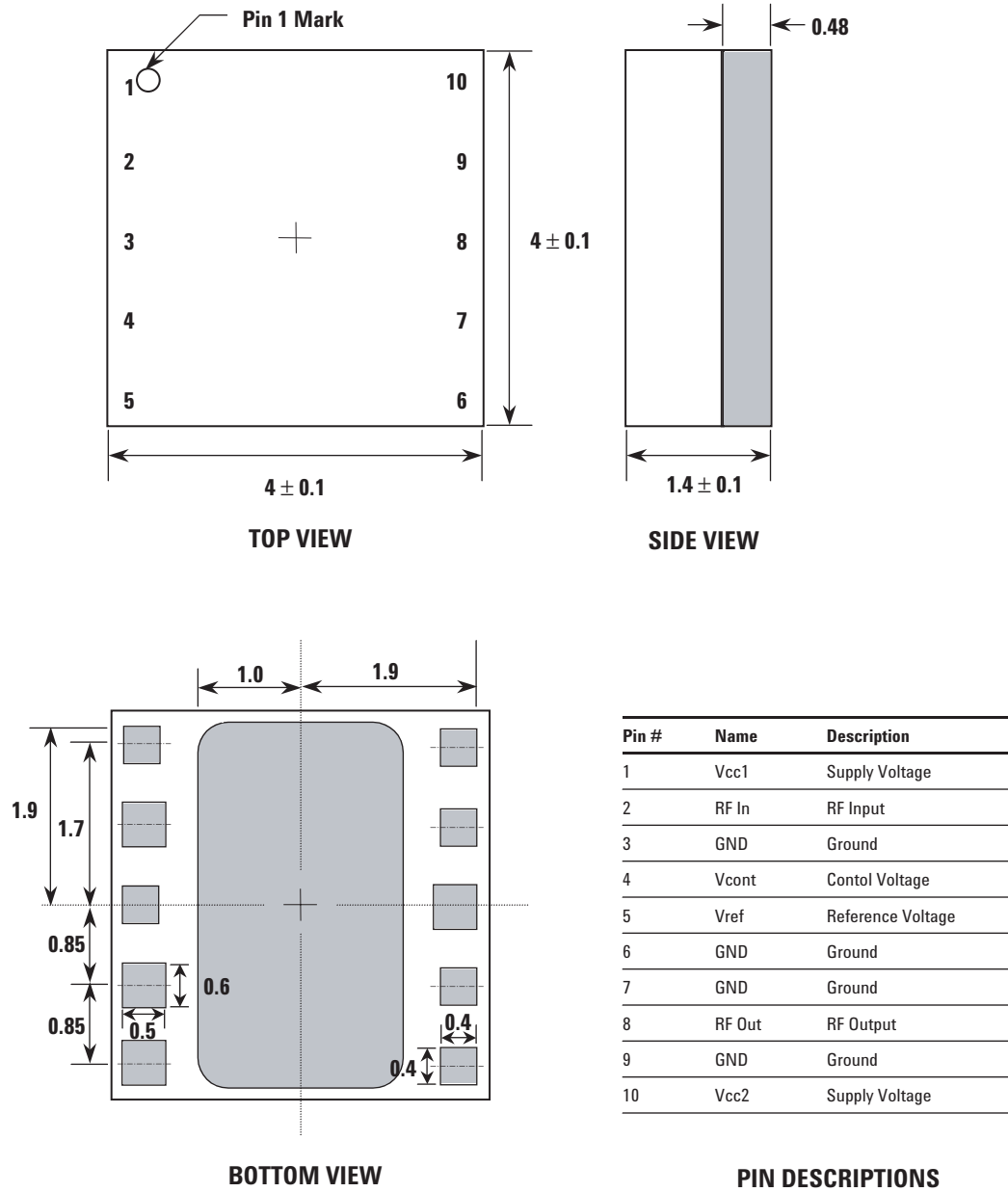


Figure 9. Package Dimensional Drawing and Pin Descriptions (all dimensions are in millimeters).

Package Dimensions and Pin Descriptions, continued

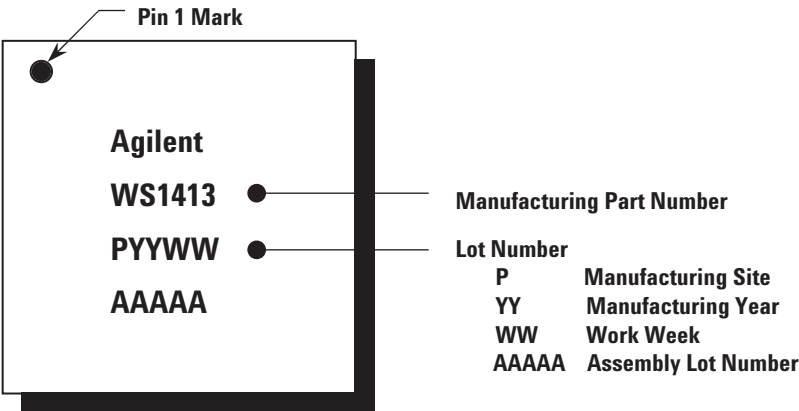


Figure 10. Marking Specifications.

Peripheral Circuit in Handset

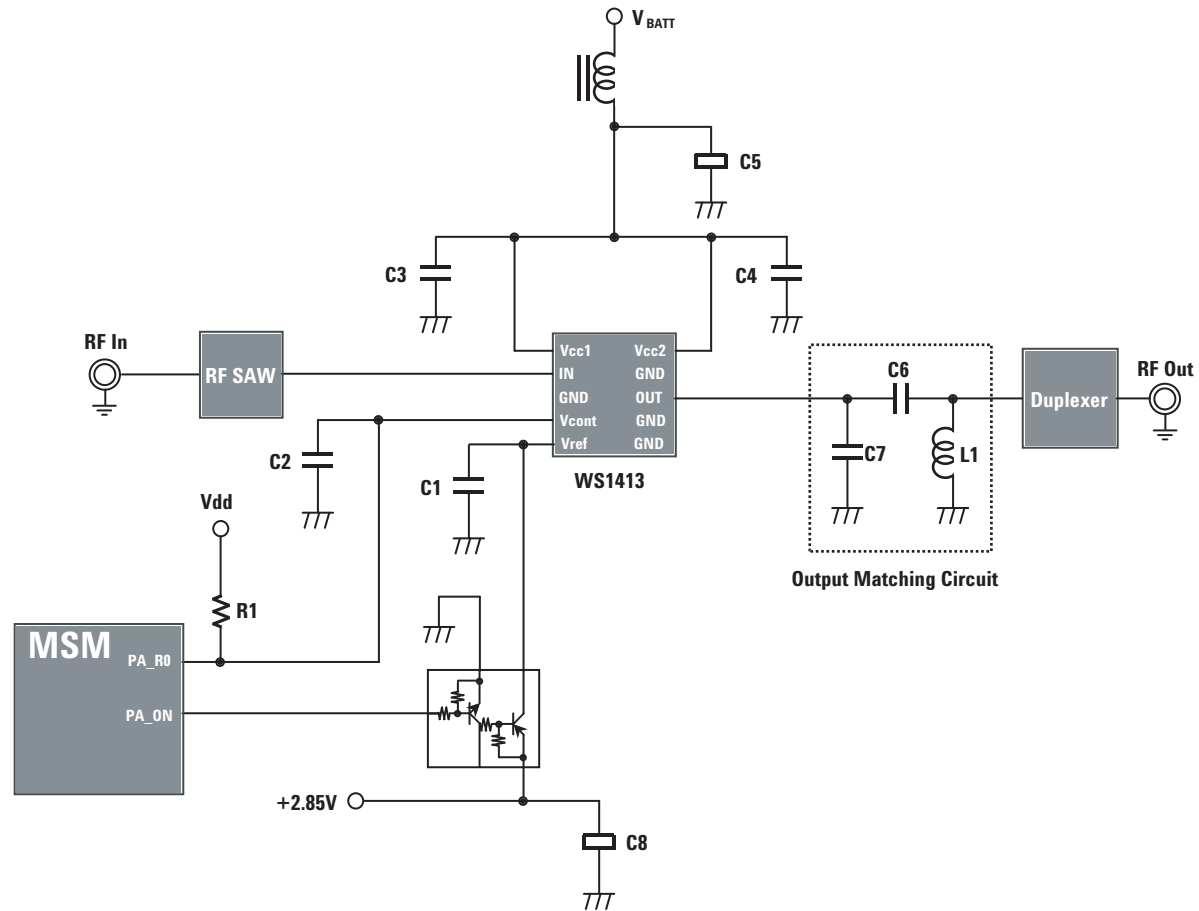


Figure 11. Peripheral circuit.

Notes:

1. Recommended voltage for Vref is 2.85V.
2. Place C1 near to Vref pin.
3. Place C3 and C4 close to pin 5 (Vcc1) and pin 6 (Vcc2). These capacitors can affect the RF performance.
4. Use 50 Ω transmission line between PAM and Duplexer and make it as short as possible to reduce conduction loss.
5. π -type circuit topology is good to use for matching circuit between PA and Duplexer.
6. Pull-up resistor (R1) should be used to limit current drain. 6.2 k Ω is recommended for WS1413.

Calibration

Calibration procedure is shown in Figure 12. Two calibration tables, high mode and low mode respectively, are required for Cool PAM, which is due to gain difference in each mode.

For continuous output power at the mode change points, the input power should be adjusted according to gain step during the mode change.

Offset Value

(difference between rising point and falling point)

Offset value, which is the difference between the rising point (output power where PA mode changes from low mode to high mode) and falling point (output

power where PA mode changes from high mode to low mode), should be adopted to prevent system oscillation. 3 to 5 dB is recommended for Hysteresis.

Average Current and Talk Time

Probability Distribution Function implies that what is important for longer talk time is the efficiency of low or medium power range rather than the efficiency at full power. WS1413 idle current is 13 mA and operating current at 18 dBm is 65 mA at nominal condition. Average current calculated with CDMA PDF is 31 mA in urban area and 54 mA in suburban area. This PA with low current consumption prolongs talk time by no less than 30 minutes compared to other PAs.

$$\text{Average current} = \int (\text{PDF} \times \text{Current}) dp$$

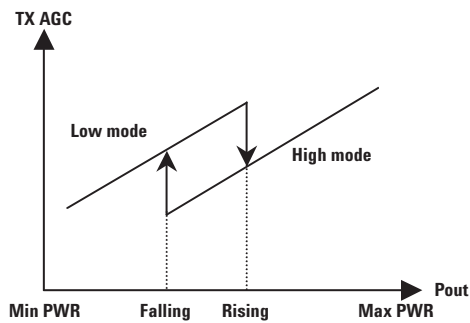


Figure 12. Calibration procedure.

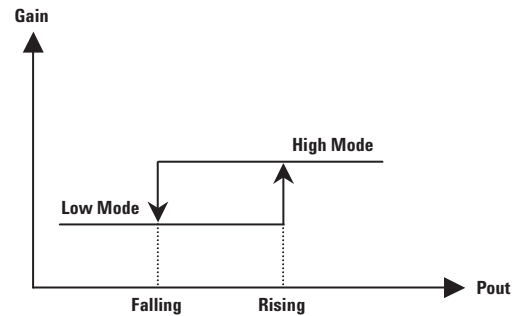


Figure 13. Setting of offset between rising and falling power.

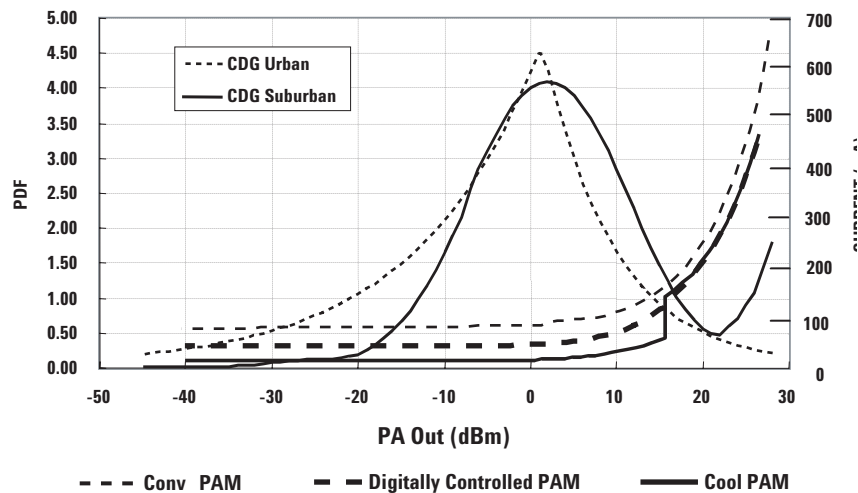


Figure 14. CDMA Power Distribution Function.

PCB Design Guidelines

The recommended WS1413 PCB

Land pattern is shown in Figures 15 and Figure 16. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads.

The recommended stencil layout is shown in Figure 17. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100 mm (4mils) or 0.127 mm (5mils) thick stainless steel which is capable of producing the required fine stencil outline.

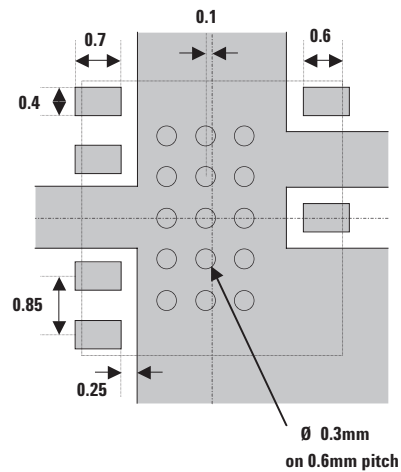


Figure 15. Metallization.

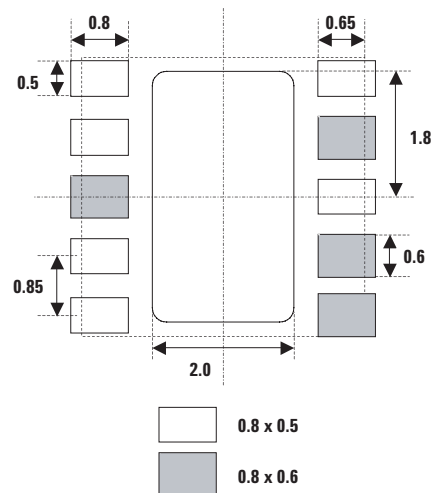


Figure 16. Solder Mask Opening.

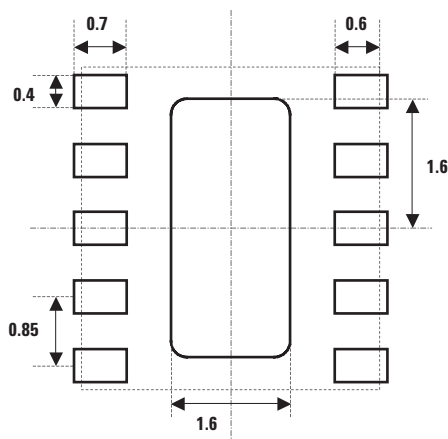
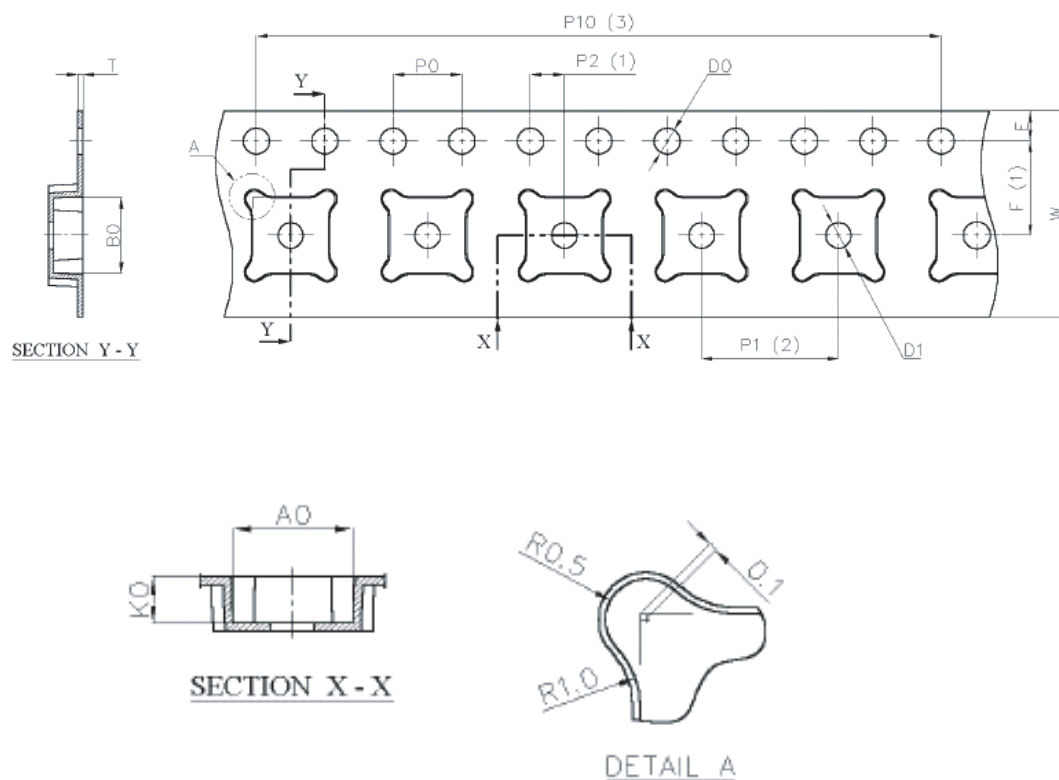


Figure 17. Solder Paste Stencil Aperture.

Ordering Information

Part Number	Number of Devices	Container
WS1413-BLK	100	Bulk
WS1413-TR1	2500	13" Tape and Reel

Tape and Reel Information



Dimension List

Annote	Millimeter	Annote	Millimeter
A0	4.40 ± 0.10	P2	2.00 ± 0.05
B0	4.40 ± 0.10	P10	40.00 ± 0.20
K0	1.70 ± 0.10	E	1.75 ± 0.10
D0	1.55 ± 0.05	F	5.50 ± 0.05
D1	1.60 ± 0.10	W	12.00 ± 0.30
P0	4.00 ± 0.10	T	0.30 ± 0.05
P1	8.00 ± 0.10		

Figure 18. Tape and Reel Format— 4 mm x 4 mm.

Figure 19. Plastic Reel Format–13"/14" (all dimensions are in millimeters).



Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature. Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is clas-

sified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test described below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

WS1413 is MSL3. Thus, according to the J-STD-033 p.11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked.

MSL classification reflow temperature for the WS1413 is targeted at 250°C +0/-5°C. Figure 20 and Table 7 show typical SMT profile for maximum temperature of 250°C +0/-5°C.

Table 5. ESD Classification

Pin#	Name	Description	HBM	CDM	Classification
1	Vcc1	Supply Voltage	± 2000V	± 200V	Class 2
2	RF In	RF Input	± 2000V	± 200V	Class 2
3	GND	Ground	± 2000V	± 200V	Class 2
4	Vcont	Control Voltage	± 2000V	± 200V	Class 2
5	Vref	Reference Voltage	± 2000V	± 200V	Class 2
6	GND	Ground	± 2000V	± 200V	Class 2
7	GND	Ground	± 2000V	± 200V	Class 2
8	RFOut	RF Output	± 2000V	± 200V	Class 2
9	GND	Ground	± 2000V	± 200V	Class 2
10	Vcc2	Supply Voltage	± 2000V	± 200V	Class 2

Note:

1. Module products should be considered extremely ESD sensitive.

Table 6. Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient ≤ 30°C/60% RH or as stated
1	Unlimited at ≤ 30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note:

1. The MSL Level is marked on the MSL Label on each shipping bag.

Handling and Storage, continued

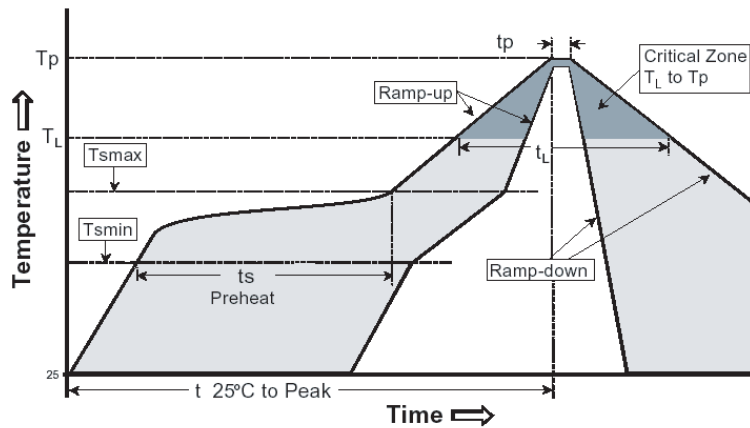


Figure 20. Typical SMT Reflow Profile for Maximum Temperature = 250+0/-5°C.

Table 7. Typical SMT Reflow Profile for Maximum Temperature = 250+0/-5°C

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (T _L to T _p)	3°C/sec max	3°C/sec max
Preheat		
- Temperature Min (T _{min})	100°C	100°C
- Temperature Max (T _{max})	150°C	150°C
- Time (min to max) (t _s)	60–120 sec	60–180 sec
T _{max} to T _L		
- Ramp-up Rate		3°C/sec max
Time maintained above:		
- Temperature (T _L)	183°C	217°C
- Time (T _L)	60–150 sec	60–150 sec
Peak Temperature (T _p)	225 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature (t _p)	10–30 sec	10–30 sec
Ramp-down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 min max.	8 min max.

Handling and Storage, continued

Storage Conditions

Packages described in this document must be stored in sealed moisture barrier, anti-static bags. Shelf life in a sealed moisture barrier bag is 12 months at <40°C and 90% relative humidity (RH) J-STD-033 p.7.

Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p.11 with factory conditions <30°C and 60% RH.

Baking

It is not necessary to re-bake the part if both conditions (storage conditions and out-of-bag conditions) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125°C for 12 hours J-STD-033 p.8.

CAUTION: Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework

Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures **shall** be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis

Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 and IPC-7721.

Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in Table 6. This approach, however, does not work if the factory humidity or temperature are greater than the testing conditions of 30°C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component packaging materials (ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device. Table 8 lists equivalent derated floor lives for humidities ranging from 20 – 90% RH for three temperatures, 20°C, 25°C, and 30°C. This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating Table 8:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = $0.121 \exp(-0.35\text{eV}/kT)$ mm²/s (this uses smallest known Diffusivity @ 30°C).
3. For >60% RH, use Diffusivity = $1.320 \exp(-0.35\text{eV}/kT)$ mm²/s (this uses largest known Diffusivity @ 30°C).

Handling and Storage, continued

Table 8. Recommended Equivalent Total Floor Life (days) @ 20°C, 25°C & 30°C For ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified)

Maximum Percent Relative Humidity												
Package Type and Body Thickness	Moisture Sensitivity Level	5%	10%	20%	30%	40%	50%	60%	70%	80%	90%	
Body Thickness ≥3.1 mm including PQFPs >84 pins, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞	∞	∞	60	41	33	28	10	7	6	30°C
		∞	∞	∞	78	53	42	36	14	10	8	25°C
		∞	∞	∞	103	69	57	47	19	13	10	20°C
	Level 3	∞	∞	10	9	8	7	7	5	4	4	30°C
		∞	∞	13	11	10	9	9	7	6	5	25°C
		∞	∞	17	14	13	12	12	10	8	7	20°C
	Level 4	∞	5	4	4	4	3	3	3	2	2	30°C
		∞	6	5	5	5	5	4	3	3	3	25°C
		∞	8	7	7	7	7	6	5	4	4	20°C
	Level 5	∞	4	3	3	2	2	2	2	1	1	30°C
		∞	5	5	4	4	3	3	2	2	2	25°C
		∞	7	7	6	5	5	4	3	3	3	20°C
Level 5a	∞	2	1	1	1	1	1	1	1	1	30°C	
	∞	3	2	2	2	2	2	1	1	1	25°C	
	∞	5	4	3	3	3	2	2	2	2	20°C	
Body 2.1 mm ≤ Thickness <3.1 mm including PLCCs (rectangular) 18-32 pins SOICs (wide body) SOICs ≥20 pins, PQFPs ≤80 pins	Level 2a	∞	∞	∞	∞	86	39	28	4	3	2	30°C
		∞	∞	∞	∞	148	51	37	6	4	3	25°C
		∞	∞	∞	∞	∞	69	49	8	5	4	20°C
	Level 3	∞	∞	19	12	9	8	7	3	2	2	30°C
		∞	∞	25	15	12	10	9	5	3	3	25°C
		∞	∞	32	19	15	13	12	7	5	4	20°C
	Level 4	∞	7	5	4	4	3	3	2	2	1	30°C
		∞	9	7	5	5	4	4	3	2	2	25°C
		∞	11	9	7	6	6	5	4	3	3	20°C
	Level 5	∞	4	3	3	2	2	2	1	1	1	30°C
		∞	5	4	3	3	3	3	2	1	1	25°C
		∞	6	5	5	4	4	4	3	3	2	20°C
Level 5a	∞	2	1	1	1	1	1	1	0.5	0.5	30°C	
	∞	2	2	2	2	2	2	1	1	1	25°C	
	∞	3	2	2	2	2	2	2	2	1	20°C	
Body Thickness <2.1 mm including SOICs <18 pins All TQFPs, TSOPs or all BGAs <1 mm body thickness	Level 2a	∞	∞	∞	∞	∞	∞	28	1	1	1	30°C
		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°C
		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°C
	Level 3	∞	∞	∞	∞	∞	11	7	1	1	1	30°C
		∞	∞	∞	∞	∞	14	10	2	1	1	25°C
		∞	∞	∞	∞	∞	20	13	2	2	1	20°C
	Level 4	∞	∞	∞	9	5	4	3	1	1	1	30°C
		∞	∞	∞	12	7	5	4	2	1	1	25°C
		∞	∞	∞	17	9	7	6	2	2	1	20°C
	Level 5	∞	∞	13	5	3	2	2	1	1	1	30°C
		∞	∞	18	6	4	3	3	2	1	1	25°C
		∞	∞	26	8	6	5	4	2	2	1	20°C
Level 5a	∞	10	3	2	1	1	1	1	1	0.5	30°C	
	∞	13	5	3	2	2	2	1	1	1	25°C	
	∞	18	6	4	3	2	2	2	2	1	20°C	

For product information and a complete list of distributors, please go to our web site:

www.avagotech.com

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies, Limited in the United States and other countries.

Data subject to change. Copyright © 2006 Avago Technologies, Limited. All rights reserved.

Obsoletes 5989-2539EN

AV01-0146EN May 3, 2006

