HCTL-2001-A00, HCTL-2017-A00 / PLC, HCTL-2021-A00 / PLC

Quadrature Decoder/Counter Interface ICs

Reliability Data Sheet

Description

The following cumulative test results have been obtained from testing performed at Agilent Technologies Malaysia in accordance with the latest revisions of MIL-STD-883 & JEDEC.

Agilent tests parts at the absolute maximum rated conditions recommended for the device. The actual performance you obtain from Agilent parts depends on the electrical and environmental characteristics of your application but will probably be better than the performance outlined in Table 1.

Failure Rate Prediction

The failure rate of semiconductor devices is determined by the junction temperature of the device.

The relationship between ambient temperature and actual junction temperature is given by the following:

$$T_J(°C) = T_A(°C) + \theta_{JA} P_{AVG}$$

where:

T_A = ambient temperature in °C

θ_{JA} = thermal resistance of junction-to-ambient in °C/Watt

P_{AVG} = average power dissipated in Watt

The estimated MTTF and failure rate at temperatures lower than the actual stress temperature can be determined by using an Arrhenius model for temperature acceleration.

Results of such calculations are shown in the table below using an activation energy of 0.43eV (reference MIL-HDBK-217) and ambient junction temperature rise of 10°C

Table 1. Life Tests

Demonstrated Performance [1]

Test Name	Stress Test Conditions	Total Device Hours	Units Tested	Total Failed [4]	Point Typical Performance	
					MTTF	Failure Rate (% /1 K Hours)
High Temperature Operating Life	V_{DD}=5.5V, T_A=85°C, Dynamic State, 1000hours	66,000	66	0	66,000	1.515
Temperature Humidity Operating Life	V_{DD}=5.5V, T_A=85°C, Rh = 85%, Biased Static State, 1000hours	22,000	22	0	22,000	4.545

Table 2. Failure Rate Prediction

Ambient Temperature (°C)	Junction Temperature (°C)	Point Typical Performance [2] in Time		Performance in Time[3] (90% Confidence)	
		MTTF [2]	Failure Rate (% / 1K Hours)	MTTF [3]	Failure Rate (% /1K Hours)
+85	+95	66,000	1.515	28,600	3.492
+75	+85	96,400	1.037	41,800	2.392
+65	+75	143,900	0.693	62,400	1.602
+55	+65	219,900	0.455	95,400	1.048
+45	+55	344,900	0.290	149,600	0.668
+35	+45	556,500	0.180	241,400	0.414
+25	+35	926300	0.108	401800	0.249

Notes:

1. These results are based on qualification of the basic CMOS process and PDIP and PLCC packaging processes in which they products are produced. The relevance of these data derives from the design-independent nature of many failure modes in a CMOS process and packaging system.
2. The point typical MTTF (which represents 60% confidence level) is the total device hours divided by the number of failures. In the case of zero failures, one failure is assumed for this calculation.
3. The 90% Confidence MTTF represents the minimum level of reliability performance, which is expected, from 90% of all samples. This confidence interval is based on the statistics of the distribution of failures. The assumed distribution of failures is exponential. This particular distribution is commonly used in describing useful life failures. Refer to MIL-STD-690B for details on this methodology.
4. A failure is any part which does not meet the datasheet specification.

Example of Failure Rate Calculation

Assume a device operating 8 hours/day, 5 days/week.

The utilization factor, given 168 hours/week is:

(8 hours/day) x (5 days/week) / (168 hours/week) = 0.24

The point failure rate per year (8760 hours) at 35°C ambient temperature is:

(0.180% / 1K hours) x 0.24 X (8760 hours/year) = 0.378% per year

Similarly, 90% confidence level failure rate per year at 35°C:

(0.414% / 1K hours) X 0.24 X (8760 hours/year) = 0.870% per year

Table 3. Environmental Tests

Test Name	Test Conditions	Units Tested	Units Failed
High Temperature Storage Test	+150°C, 1,000 hours	77	0
Low Temperature Storage Test	-55°C, 1000 hours	77	0
Temperature Cycle	-55°C to 150°C, 15 min dwell, 5 min transfer, 1,000 cycles	77	0
Pressure Pot	121°C/ 95-100 %RH, 2 Atmospheres, 240hrs	32	0
Solder Heat Resistance	Typical solder process with peak temperature of 260°C, 10 sec duration	32	0

Table 4. Electrical Tests

Test Name	Test Conditions	Units Tested	Units Failed
ESD (Human Body Model)	JESD22-A114-A Up to +/-2000 applied to all pins versus ground	3	0
ESD (Machine Model)	JESD22-A114-A Up to +/-100V applied to all pins versus ground	3	0
Latch-up	All pins tested for source/sink up to 200mA. V_{DD} = 5.0V	30	0

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