AS20-M42M-Pxx Series

Absolute Magnetic Encoder SPI 4-Wire Option

1 General Specification of SPI 4-Wire Serial Communication

Table 1: General Specification of Serial Communication

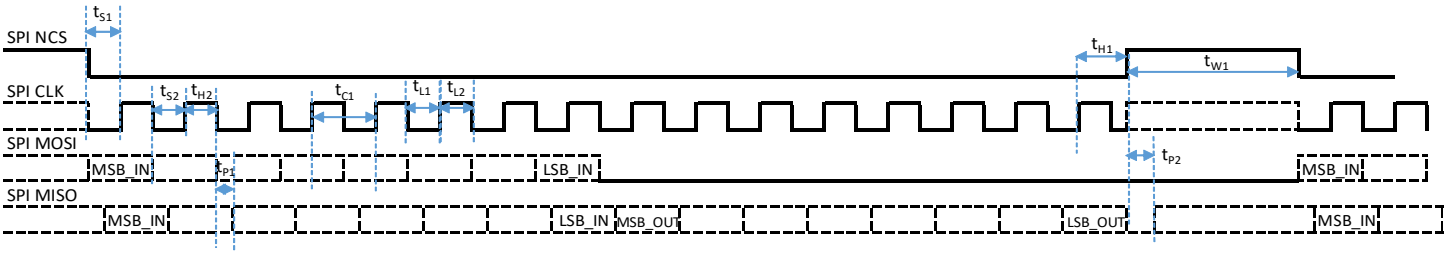
Item	Specification	Note
Transmission Type	Serial Peripheral Interface (SPI)	
Communication Type	Single-ended	
Synchronization Type	Synchronous	
Communication Baud Rate	Up to 10.0 Mb/s	
Transmission Error Checking	6/16 bit CRC	6-bit CRC equation: $G(X) = X^6 + X^1 + 1$ 16-bit CRC equation: $G(X) = X^{16} + X^{15} + X^{12} + X^7 + X^6 + X^4 + X^3 + 1$

2 General Format Definition of Transmission Frames between Host and Encoder

2.1 Overview of Communications

A one-to-one serial communication is established between the client encoder and the host (for example, a servo driver). The communications are in a single-ended transmission format that complies with the SPI electrical standard. The encoder will carry out specific operations based on the command requests made by the host.

Figure 1: General Transmission Frames Format for SPI 4-Wire Communications



NOTE:

- When NCS = 1, MISO = high-Z to support Multi-encoder Bus Mode.
- During the first eight clocks, MISO always echoes the Operation command received on MOSI, to support Multi-encoder Mode.
- SPI Mode 0 and SPI Mode 3.

Table 2: SPI 4-Wire Timing Specification

Symbol	Description	Min.	Max.	Unit
t_{C1}	Permissible clock cycle time	100	—	ns
t_{L1}	Clock signal low-level duration	50	—	ns
t_{L2}	Clock signal high-level duration	50	—	ns
t_{S1}	Setup time: NCS lo before SCLK, low to high	50	—	ns
t_{H1}	Hold time: NCS lo after SCLK, low to high	80	—	ns
t_{W1}	Wait time: Between NCS low to high, and NCS high to low	200	—	ns
t_{H2}	Hold time: MOSI stable after SCLK, low to high	15	—	ns
t_{S2}	Setup time: MOSI stable before SCLK, low to high	15	—	ns
t_{P1}	Propagation delay: MISO stable after SCLK, high to low	35	—	ns
t_{P2}	Propagation delay: MISO hi impedance after NCS, low to high	—	35	ns

2.2 Encoder Read-Out Frame Sets Format and Timing

Figure 2: Register Read Operation Diagram

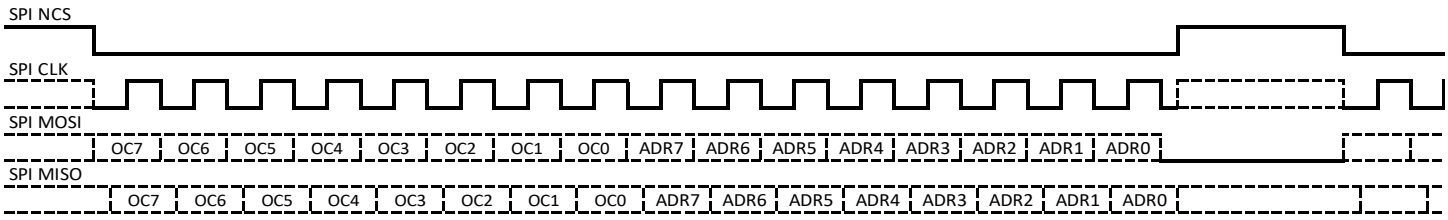


Table 3: SPI 4-Wire Operation Commands

Operation Command (OC)	Description	Ports	CLK Bits															
			Byte 1	Byte 2							Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
0xB0	Activate (1 encoder)	MOSI	B0	1	0	0	0	0	0	RA 0	PA 0								
		MISO	B0	0	0	1	0	0	0	0	0								
	Activate (2 encoder)	MOSI	B0	1	0	0	0	RA 0	PA 0	RA 1	PA 1								
		MISO	B0	0	0	0	0	1	0	0	0								
0xA6	Position Read	MOSI	A6																
		MISO	A6	Position Data + nError + nWarning + CRC/Position Data + nError + nWarning +nSequence + CRC														
0x81	Register Read (Continuous)	MOSI	81	ADDRESS(ADDR)							0x00							
		MISO	81	ADDRESS(ADDR)							0x00	DATA 1	DATA 2	…				
0xCF	Register Write (Continuous)	MOSI	CF	ADDRESS(ADDR)							DATA 1	DATA 2	…					
		MISO	CF	ADDRESS(ADDR)							DATA 1	DATA 2	…					
0x9C	Read Status	MOSI	9C															
		MISO	9C	0x00							ERR [7:0]	ERR [15:8]	ERR [23:16]	ERR [31:24]	WARN [7:0]	WARN [15:8]	WARN [23:16]	WARN [31:24]
0xD9	Write Command	MOSI	D9	COMMAND														
		MISO	D9	COMMAND														
0x97	Register Read (Single)	MOSI	97	ADDRESS(ADDR)														
		MISO	97	ADDRESS(ADDR)														
0xAD	Register Status/Data	MOSI	AD															
		MISO	AD	STATUS							DATA							
0xD2	Register Write (Single)	MOSI	D2	ADDRESS(ADDR)							DATA							
		MISO	D2	ADDRESS(ADDR)							DATA							

2.2.1 Memory Read Command

The Operation command (OC) 0x81h (continuous read on the current page of the memory register) is used to read data from any register address in the ASIC chip. See Table 3 for the data streams sent on MOSI with OC 0x81h followed by the address of the first register to be read and a delay of 0x00. These three bytes will reflect on the MISO line before sending out the register address (ADDR) data (DATA1). As long as the CLK continues to be sent, consecutive register address (ADDR+1) data (DATA2) is transmitted. This procedure continues until the clocks end or rising NCS.

The Operation command (OC) 0x97h followed by 0xADh is used to perform a single read data from any register address in the ASIC chip.

2.2.2 Memory Write Command

The Operation command (OC) 0xCFh (continuous write on the current page of internal memory register) is used to write data into any register address in the ASIC chip. See Table 3 for the data streams sent on MOSI with OC 0xCFh followed by the address of the first register to be written and the data. With each data byte, the address of the register to be written is incremented (ADDR+1). Data successfully received will be transmitted on the MISO line.

The Operation command (OC) 0xD2h followed by 0xADh is used to perform a single write data into any register address in the encoder memory and retrieve back the written data.

NOTE: Do not perform continuous write on external EEPROM.

2.2.3 Memory Read Status Command (Single – STATUS Description)

The Operation command (OC) 0xAD STATUS (STAT) description is shown below.

Table 4: Status Bits Description

Bit	Name	Description
7	Error/SC_EN	Invalid Operation command, specific command enable
6:3	—	Reserved
2	Fail	Data request failed
1	Busy	Encoder busy
0	Valid	Data valid

NOTE: If the last OC received is 0xD9, the STATUS bit-7 = 1 and the data value reflect the operation status.

2.2.4 SPI 4-Wire Specific Command

By sending an Operation command (OC) 0xD9 followed by the specific code listed in the table below, the AS20 encoder performs the associated special task. Once the command is received by the encoder, perform 0xAD to read back the status of the operation. “Data” value if 0xFF is error; if 0x00 is done; if “Code” is in progress. In case of an overwritten operation, for example a 0x97h register read, perform Operation command 0x00(NOP) to put the operation status back to buffer for 0xAD.

Table 5: Specific Command

Code	Name	Description
0x00	<NOP_OK>	<Return-code: last operation succeeded>
0x10	REBOOT	Reset, equivalent to power-cycle the encoder
0x18	MT_RESYNC	Re-synchronization of the MT device.
0x19	MT_RESET	Clear the FeRAM Value
0x20	SCLEAR	Clear the System Alarm and Warning registers
0x80	MTST_PRESET	Set current position as MT=0, ST=0
0x81	MT_PRESET	Set current position as MT=0
0xFF	<NOP_FAIL>	<Return-code: last operation failed>

2.2.5 Error or Warning Readout and Descriptions

Use the Operation command (OC) 0x9C to perform error or warning bits readout. To separate error bits and warning bits, see Table 12.

Table 6: Alarm or Error Bits Description

Bits	Alarms	Alarms Definition
31:30, 27, 25:22, 18:17, 14:13, 10, 8:6, 3:0	Reserved	■ 0: Default.
28	MT Sync Error	Detects wrong MT counting during MT synchronization upon the Startup operation or MT Sync Retry operation. ■ 1: Incorrect MT synchronization. ■ 0: MT synchronization is correct.
26	Multi-turn Err	Indicates bit jump occurs in the multi-turn value. Compare the MT delta for every 12.8 µs; the delta is > ±1 rev. ■ 1: Bit jump occurs. ■ 0: No bit jump occurs.
21	XC Error	Indicates an MT encoder miscount by comparing the MT encoder counter to the MT SW counter. ■ 1: EHMT; miscount or XCERR value overflow. ■ 1: BBMT/Gear; miscount. ■ 0: No MT miscount.
20	Speed MT Warning	Detects rotation speed greater than 30,000 rpm for MT synchronization. ■ 1: Rotation speed exceeds the limit detected. ■ 0: No over speed detected.
19	FeRAM CRC Error	Indicates a multi-turn block FeRAM communication CRC error. ■ 1: Multi-turn FeRAM CRC error. ■ 0: No CRC error.

Table 6: Alarm or Error Bits Description

Bits	Alarms	Alarms Definition
16	FeRAM Register Error	Detects an FeRAM error reading MT hardware. ■ 1: Error in FeRAM reading. ■ 0: No error in the MT position reading.
15	Chip Ready	Indicates the encoder status. ■ 1: Encoder is ready for normal operation (no fault status). ■ 0: Encoder has abnormality due to other alarm bit(s) triggered.
12	TempErr	Indicates the temperature is above the upper limit. ■ 1: Temperature above setting limit. ■ 0: Temperature below setting limit.
11	Memory Err	Indicates if loading internal and external EEPROM content upon encoder power up is successful. ■ 1: Failure loading internal EEPROM and external EEPROM memory data. ■ 0: Success loading external internal EEPROM and external EEPROM memory data.
9	STErr	Checks the integrity of ST position. Mcode = absolute code. ■ 1: Mcode jump, MLS-INC mismatch, or MLSErr flag. ■ 0: INC and Mcode function as normal.
5	Mag Hi	Detects an error in the magnetic field sensing. ■ 1: Magnetic field strength is too strong. ■ 0: Magnetic field strength is optimum for normal operation.
4	Mag Lo	Detects an error in the magnetic field sensing. ■ 1: Magnetic field strength is too weak. ■ 0: Magnetic field strength is optimum for normal operation.

2.2.6 Position Read

The Operation command (OC) 0xA6 is used to read absolute position data from the AS20 encoder.

- For nError (nE) and nWarning (nW) CRC selections, see the CRC setting in Table 13.
- Position latch is at the first rising clock.
- nError and nWarning trigger 0 if any of the error bits are triggered.
- The sequence counter (Seq Cnt) is the position read counter. Consecutively position-read the sequence counter (Seq Cnt +1) until 63 counts; rollover becomes 0 and restarts the counting.
- Single-turn bits (ST-bit) and multi-turn bits (MT-bit) are a continuous bit that non-patch zero.
- For bits selection, see Table 18.

Table 7: Multi-turn + Single-turn Position Read

Operation Command (OC)	Description	Ports	1 byte	<MT-bit>	<ST-bit>	2 bits		6 bits	2 bytes
0xA6	Position Read	MOSI	A6(8b)						
	Format = Basic	MISO	A6(8b)	MT Pos	ST Pos	nE	nW	CRC (6b)	
	Format = Extended	MISO	A6(8b)	MT Pos	ST Pos	nE	nW	Seq Cnt (6b)	CRC (16b)

2.2.7 Enable Encoders

The Operation command (OC) 0xB0 is used to activate encoders in a bus mode connection. Register Data Access (RAx) is used to access the memory register in the encoder. Position Data Access (PAx) is used to access position data in the encoder. 1 = enable; 0 = disable.

Table 8: Encoder Activation

OC	Description	Ports	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0xB0	Activate (1 encoder)	MOSI	B0								1	0	0	0	0	0	RA0	PA0
		MISO	B0								0	0	1	0	0	0	0	0
	Activate (2 encoders)	MOSI	B0								1	0	0	0	RA0	PA0	RA1	PA1
		MISO	B0								0	0	0	0	1	0	0	0

Figure 3: Bus-Type Connection for Multi Encoders

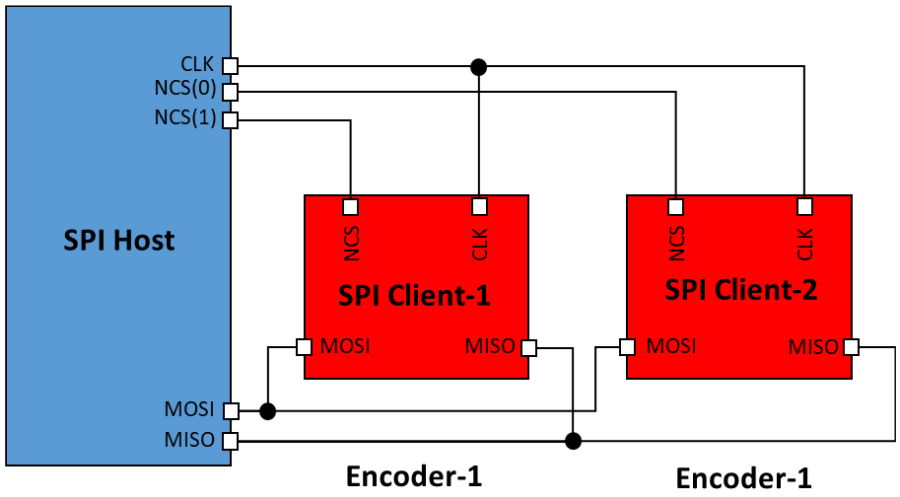


Table 9: Encoder Data Output Arrangement

OC	Encoder 1								Encoder 2				
	Description	Ports	1 byte	<Pos>	2 bits		6 bits	2 bytes	<Pos>	2 bits		6 bits	2 bytes
0xA6	Position Read	MOSI	A6 (8b)										
	format = Basic	MISO	A6 (8b)	MT+ST Pos	nE	nW	CRC (6b)		MT+ST Pos	nE	nW	CRC (6b)	
	format = Extended	MISO	A6 (8b)	MT+ST Pos	nE	nW	Seq Cnt (6b)	CRC (16b)	MT+ST Pos	nE	nW	Seq Cnt (6b)	CRC (16b)

3 Encoder Memory Area

3.1 User Area

The AS20 supports 8 Kb of register user area. The memory data is kept in non-volatile memory. The available register pages that are accessible by the user are listed in Table 10.

Table 10: User Memory Area with 8 Kb

Page [decimal]	Address [hex]	Remarks
0 to 4	0x00 to 0x7E	User area
11 to 13	0x00 to 0x7E	
Page Selection	0x7F	

NOTE:

1. Eight pages with 127 addresses each are allocated for user access.
2. The active page numbers are specified in address 0x7F; page change is done by writing to address 0x7F. Default page after powe-on is Page 0.
3. Once the page value is changed, allow a time delay of 18 ms.
4. The typical EEPROM read time is 200 µs, minimum.
5. The typical EEPROM write time is 6 ms, minimum.

3.2 Encoder System Area

Additional register pages are reserved for system areas that are protected against accidental writing during operation. The memory data is kept in non-volatile memory.

Table 11: Encoder System Memory Area

Page [decimal]	Address [hex]	Remarks
5 to 8	0x00 to 0x7E	System area
Page Selection	0x7F	

NOTE: Pages 9 and 10 are volatile memory addresses reserved for encoder system use.

4 Encoder Configuration

4.1 Error and Warning Setting

To enable the error or warning in Operation command (OC) 0x9C, set the respective bit to 1; to disable, set the bit to 0.

Table 12: Error and Warning Bit Configuration Addresses

Page	Address [hex]	Bit								Initialize Value
		7	6	5	4	3	2	1	0	
7	28	SPI4W Warning Mask [31:24]								8'h00
	29	SPI4W Warning Mask [23:16]								8'h10
	2A	SPI4W Warning Mask [15:8]								8'h10
	2B	SPI4W Warning Mask [7:0]								8'h30
	2C	SPI4W Error Mask [31:24]								8'h14
	2D	SPI4W Error Mask [23:16]								8'h29
	2E	SPI4W Error Mask [15:8]								8'h0A
	2F	SPI4W Error Mask [7:0]								8'h00
	30	SPI4W Alarm Enable [31:24]								8'h14
	31	SPI4W Alarm Enable [23:16]								8'h39
	32	SPI4W Alarm Enable [15:8]								8'h1A
	33	SPI4W Alarm Enable [7:0]								8'h30
	34	SPI4W Alarm Latch Enable [31:24]								8'h14
	35	SPI4W Alarm Latch Enable [23:16]								8'h29
	36	SPI4W Alarm Latch Enable [15:8]								8'h0A
	37	SPI4W Alarm Latch Enable [7:0]								8'h00

4.2 Cyclic Redundancy Check (CRC) Setting

Table 13: CRC Settings

Page	Address [hex]	Bit								Default Value	Description
		7	6	5	4	3	2	1	0		
7	22				SPI4W_Ext_EN					8'h00	6-bit CRC: 0 16-bit CRC: 1
	26	SPI4W CRC [15:8]								8'h00	CRC initial value
	27	SPI4W CRC [7:0]								8'h00	

4.3 Encoder Memory Map for Calibration and Special Functions

Table 14: General Volatile Memory Map (Page 9, 0x09)

No.	Item	Address	Bits							
			7	6	5	4	3	2	1	0
1	Unlock Memory	0x00	Unlock Memory by Writing 0xAB							
2	Program Memory	0x01	Program Memory by Writing 0xC0							
3	Clear Alarm/ Position	0x02					Alarm Clear		ST Zero Reset	MT Zero Reset
4	Calibration	0x04					OT_ Direction-2		OT_Without_ Accuracy	OT_ Direction-1
5	Reset	0x0B	Perform Hard Reset by Writing 0xA7							
6	Alarm/ Warning [31:24]	0x24	N/A	N/A	N/A	MT Sync Error	N/A	MT Error	N/A	N/A
7	Alarm/ Warning [23:16]	0x25	N/A	N/A	XCErr	Speed MT Warning	FeRAM CRC Err	N/A	N/A	Feram ECC A/B Reg Err
8	Alarm/ Warning [15:8]	0x26	Chip Ready	Reserved	N/A	Temp_ Err	Memory Err	N/A	ST_Err	N/A
9	Alarm/ Warning [7:0]	0x27	N/A	N/A	Mag Hi	Mag Lo	N/A	N/A	N/A	N/A
10	Calibration Status	0x28	Mem_ Busy	N/A	Internal_ Mem_Pass	Internal Mem_Fail	Zero_ Done	Zero_ Err	OT_Cal_ Done	OT_Cal_ Err

NOTE:

1. The Memory Program command is needed for the system area memory to be effective upon power cycle. This is applicable for changes to internal memory Page 5 to Page 8.
2. Perform the Memory Program command for changes to any of the affected bank before moving to other non-volatile memory banks.
3. Changes will be lost after a power cycle without a Memory Program command.

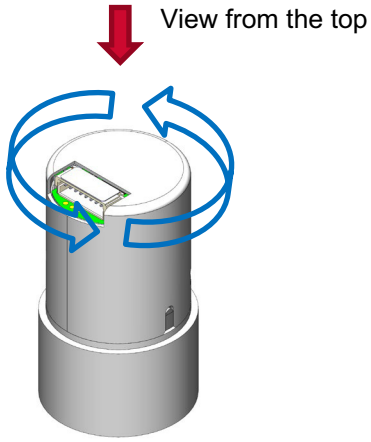
4.4 Counting Direction

Table 15: Register Bit for Counting Direction Selection

Page [Decimal]	Address [hex]	Bit								Default Value
		7	6	5	4	3	2	1	0	
7	20	NA	Counting Direction	N/A						8'h40

With the default setting, position data is counting up when rotating in the counterclockwise direction, as viewed from the top of the encoder.

Figure 4: Default Counting Direction



4.5 Zero Reset

The encoder zero-reset data can be accessed by reading the addresses in Table 16.

Table 16: User Zero-Reset Registers

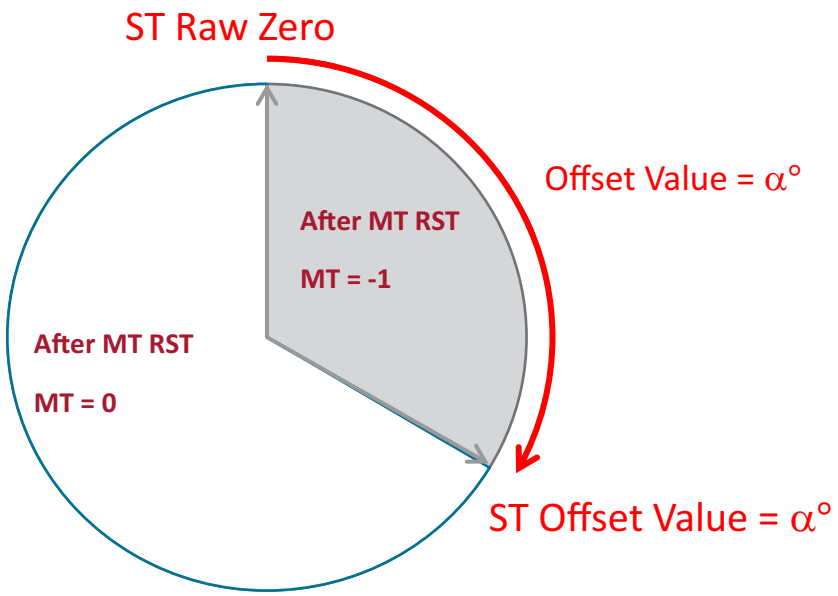
Page	Address [hex]	Bit							
		7	6	5	4	3	2	1	0
7	0E	0	MT_ZR[38:32]						
	0F	MT_ZR[31:24]							
	10	MT_ZR[23:16]							
	11	MT_ZR[15:8]							
	12	MT_ZR[7:0]							
	13	ST_ZR[17:10]							
	14	ST_ZR[9:2]							
	15	ST_ZR[1:0]		6’b000000					

For SPI protocol, the zero reset options are described in Table 5.

There is a dependency of the new MT position value if the ST zero registers are non-zero. Depending on the ST angle position, the MT reset may return -1 (0xFFFFFF if MT resolution is 24-bit, depending on the resolution), or zero. The exact position depends on the offset values (α) in the ST offset register.

An alternative for customers who must have MT values always set to zero is to implement the MT offset in the controller side. This is done by reading out MT position data and then offset at the controller display. In this case, the MT offset register needs to be set to zero.

Figure 5: Relationship of MT Position Values after Performing the MT Reset Command



4.6 Multi-turn and Single-Turn Absolute Resolution Setting

Select the configuration for the absolute position output by updating the Page 7 Address 0x16; see Table 17 and Table 18.

Table 17: Memory Map for Absolute Resolution Settings

Page	Address [Decimal]	Address [hex]	Bit								Default Value
			7	6	5	4	3	2	1	0	
7	22	16	N/A	MT_Select [2:0]			N/A	N/A	ST_Select [1:0]		8'h53

NOTE:

1. Unlock the memory.
2. Write in the new settings at Page 7; read back to ensure the setting is written successfully.
3. Program the memory.

Table 18: Multi-turn and Single-Turn Bits Settings

MT_Select	
Bits	**Resolution**
000	0
001	12
010	14
011	16
100	20
101	24
110	32
111	39

ST_Select	
Bits	**Resolution**
00	15
01	16
10	17
11	18

4.7 Temperature Setting

Read the temperature value via the register at Page 7 Address 0x05.

Table 19: Temperature Sensor Data

Temperature	TEMP[7:0]
–64°C	1100 0000
–40°C	1100 1110
–20°C	1110 1100
–1°C	1111 1111
0°C	0000 0000
1°C	0000 0001
10°C	0000 1010
25°C	0001 1001
50°C	0011 0010
85°C	0101 0101
127°C	0111 1111

NOTE:

1. The minimum support range for the temperature output is –64°C.
2. Negative values are from –1°C to –64°C only.
3. The maximum positive value is 191°C.

Table 20 lists the configuration for setting temperature values and alarms. The temperature upper limit defaults to 0x7D (125°C), referenced to the ambient temperature as measured by the AS20 encoder ASIC.

Table 20: Temperature Alarm Limit Setting and Temperature Output Address

Page	Address [hex]	Bit								Initialize Value
		7	6	5	4	3	2	1	0	
7	02	Temp Max Limit Offset [7:0]								8'h00
	03	Temp Offset [7:0]								8'h00
	04	Temperature Limit [7:0]								8'h7D
	05	Temperature Output [7:0]								N/A

Table 21 shows examples based on an initial Alarm (0x04) setting of 125°C. The temperature offset can be a positive or negative value.

Descriptions for the case examples in Table 21 are as follows:

- Case 1: No offset scenario.
- Case 2: If the temperature offset (0x03) is positive value, then the Temp. Upper Limit Offset (0x02) is also set to the same value.
- Case 3: If the temperature offset (0x03) is negative value, then the absolute value of this value needs to be added to the default Temp. Upper Limit (0x04).
- Case 4: Another negative offset value example.

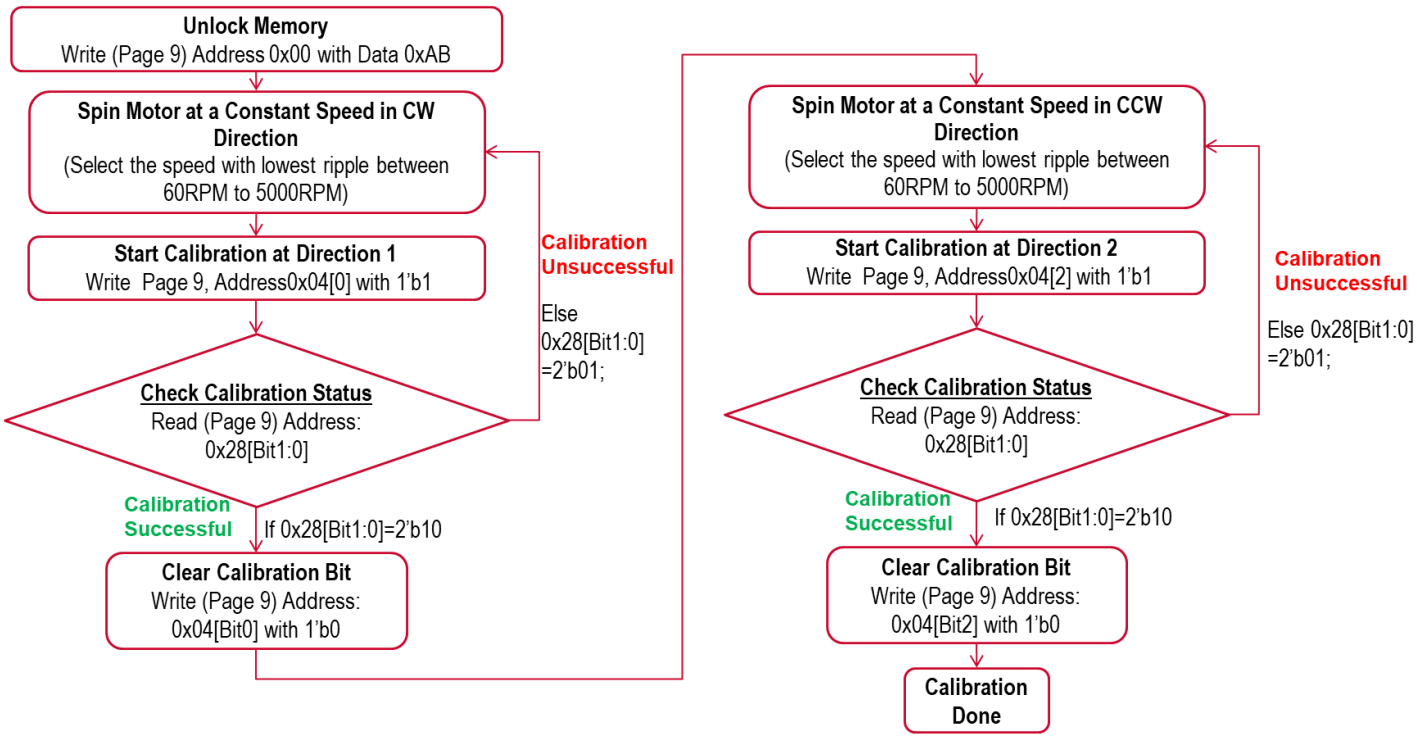
Table 21: Temperature Sensor Offset Setting Examples

Case	Temperature Sensor Offset Register	0x02	0x03	0x04	0x05	Raw Temperature without Offset (Dec)	Alarm Trigger
	Offset Value (Decimal)	Temperature Upper Limit Offset (hex)	Temperature Offset (hex)	Temperature Upper Limit (hex)	Temp Output Data (Dec)		
1	0	0	0	7D	124	124	N
					125	125	Y
					126	126	Y
2	10	0A	0A	7D	124	114	N
					125	115	Y
					126	116	Y
3	-1	0	FF	7D+01	124	125	N
					125	126	Y
					126	127	Y
4	-10	0	F6	7D+0A	124	134	N
					125	135	Y
					126	136	Y

5 Calibration of the AS20-M42M Encoder

5.1 Full Auto-Calibration with Accuracy Correction Enabled

Figure 6: Flow Chart for Full Auto-calibration Process



5.1.1 Calibrate in Clockwise (CW) Direction

1. Unlock the memory: write Page 9, Address 0x00 = 0xAB.
2. Spin the spindle motor in the clockwise direction at 60 rpm to 5000 rpm; select the least ripple speed, not to exceed 5000 rpm. Wait for the motor speed to be stable before continuing to the next step.
3. Write Page 9, Address 0x04[0] = 1b.
4. Loop read the Calibration Status, Address 0x28:
   a. If Address 0x28[1:0] = 00b, calibration is in progress.
   b. If Address 0x28[1:0] = 10b, calibration is done.
   c. If Address 0x28[1:0] = 01b, calibration is in error.
5. Clear the Calibration Register, Address 0x04 = 0h.
6. If calibration is unsuccessful, repeat Step 3 and Step 4. You may retry up to 10 times.

5.1.2 Calibrate in the Counterclockwise (CCW) Direction

1. Spin the spindle motor in the counterclockwise direction at 60 rpm to 5000 rpm; select the least ripple speed, not to exceed 5000 rpm. Wait for the motor speed to be stable before continuing to the next step.
2. Write Page 9, Address 0x04[2] = 1b.
3. Loop read the Calibration Status, Address 0x28:
   a. If Address 0x28[1:0] = 00b, calibration is in progress.
   b. If Address 0x28[1:0] = 10b, calibration is done.
   c. If Address 0x28[1:0] = 01b, calibration is in error.
4. Clear the Calibration Register, Address 0x04 = 0h.
5. If calibration is unsuccessful, repeat Step 2 and Step 3. You may retry up to 10 times.

5.2 Auto-Calibration without Accuracy Correction

1. Unlock the memory: write Page 9, Address 0x00 = 0xAB.
2. Spin the spindle motor in the clockwise direction at 60 rpm to 5000 rpm; select the least ripple speed, not to exceed 5000 rpm. Wait for the motor speed to be stable before continuing to the next step.
3. Write Page 9, Address 0x04[1] = 1b.
4. Loop read the Calibration Status, Address 0x28:
   a. If Address 0x28[1:0] = 00b, calibration is in progress.
   b. If Address 0x28[1:0] = 10b, calibration is done.
   c. If Address 0x28[1:0] = 01b, calibration is in error.
5. Clear the Calibration Register, Address 0x04 = 00h.
6. If calibration is unsuccessful, repeat Step 3 and Step 4. You may retry up to 10 times.

5.3 Auto Zero-Reset (Single-Turn)

1. Unlock the memory.
2. Write Page 9, Address 0x02[1] = 1b.
3. Loop read the Calibration Status, Address 0x28:
   a. If Address 0x28[3:2] = 00b, calibration is in progress.
   b. If Address 0x28[3:2] = 10b, calibration is done.
   c. If Address 0x28[3:2] = 01b, calibration is in error.

5.4 Auto Zero-Reset (Multi-Turn)

1. Unlock the memory.
2. Write Page 9, Address 0x02[0] = 1b.
3. Loop read the Calibration Status, Address 0x28:
   a. If Address 0x28[3:2] = 00b, calibration is in progress.
   b. If Address 0x28[3:2] = 10b, calibration is done.
   c. If Address 0x28[3:2] = 01b, calibration is in error.

5.5 Alarm Clear

1. Unlock the memory.
2. Write Page 9, Address 0x02[2] = 1b.

5.6 EH Pulse Voltage Monitoring

The AS20 has a built-in function to measure and monitor the EH pulse voltage level (VWC). Measurement must be conducted with the final encoder assembly, including the external cover.

1. Unlock the memory: write Page 9, Address 0x00 = 0xAB.
2. Enable the VWC Monitoring Self Check by writing Address 0x08 = 04h.
3. Spin the spindle motor in the clockwise direction for greater than 350 rotations at 3000 rpm.
4. Loop read the Calibration Status, Page 9, Address 0x45:
   a. If Address 0x45[3] = 1b, the measurement is done.
5. End the VWC Monitoring Self Check by writing Page 9, Address 0x08 = 00h.
6. Read Page 9, Address 0x46 to 0x47 for the measured data.
7. Stop the Motor.
8. Repeat Step 2 to Step 6 with rotation in the counterclockwise direction.

Figure 7: VWC Monitoring Self Test Flow Chart

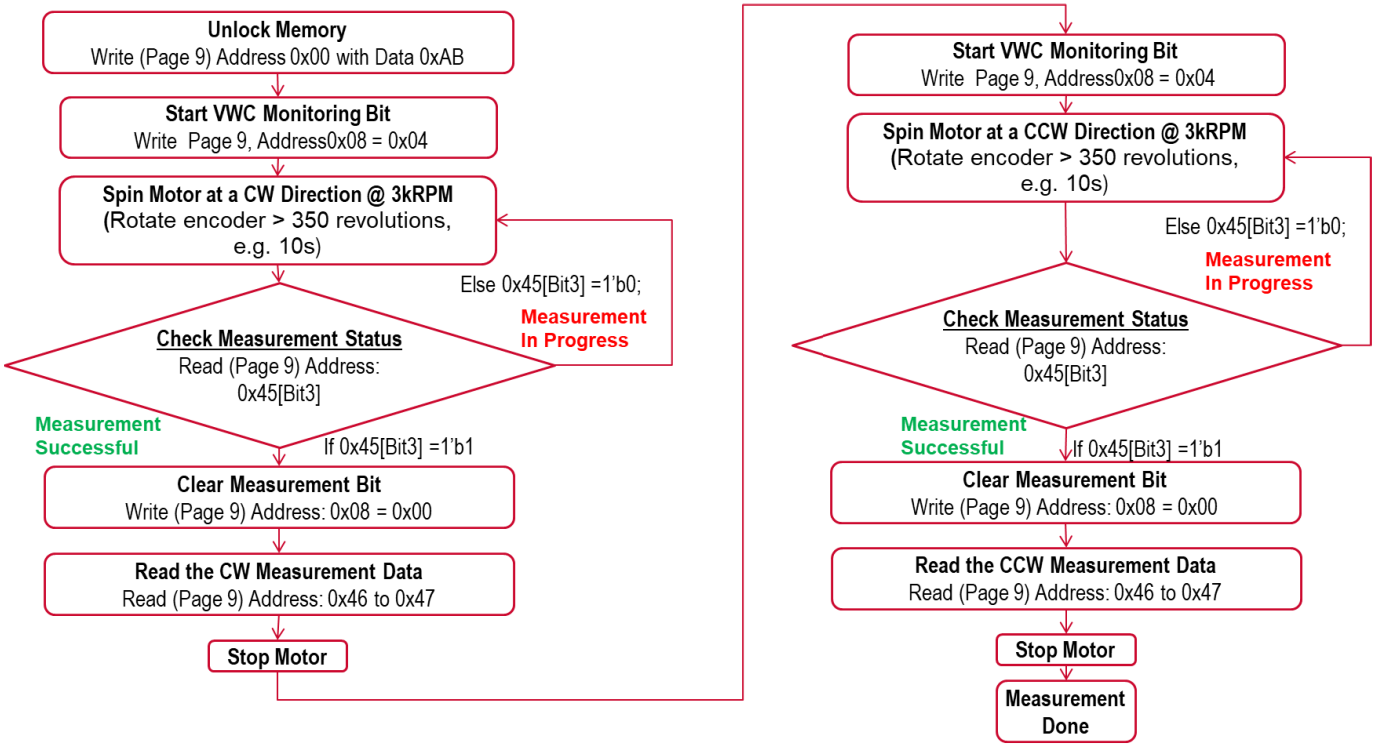


Table 22: EH Pulse Monitoring Measurement Registers

Page	Byte Address			Bit							
Page [dec]	[dec]	[hex]	Description	7	6	5	4	3	2	1	0
				7	6	5	4	3	2	1	0
9	8	08	Command						Vwc_Mon_Trig		
	69	45	Status					VWC Result Ready			
	70	46	MT Counter VWC	EH Pulse VWC data, Average – 4 Sigma (Target value: 48 to 80 decimal)							
	71	47		EH Pulse VWC data – Mean (Target: 48 to 80 decimal)							

5.7 Code Monotony Measurement

The AS20 has a built-in function to measure and monitor the code monotony of the ST position data. Measurement must be conducted with the final encoder assembly, including the external cover.

1. Unlock the memory: write Page 9, Address 0x00 = 0xAB.
2. Enable the Code Monotony measurement: write Page 9, Address 0x06 = 01h.
3. Spin the spindle motor in the clockwise direction for greater than three revolutions at low speed, for example 2 rpm to 10 rpm.
4. Read Page 9, Address 0x60 to 0x63 for the measured data.
5. End the Code Monotony measurement: write Page 9, Address 0x06 = 00h.
6. Stop the motor.
7. Repeat Step 2 to Step 5 with rotation in the counterclockwise direction.

Figure 8: Code Monotony Self Test Flow Chart

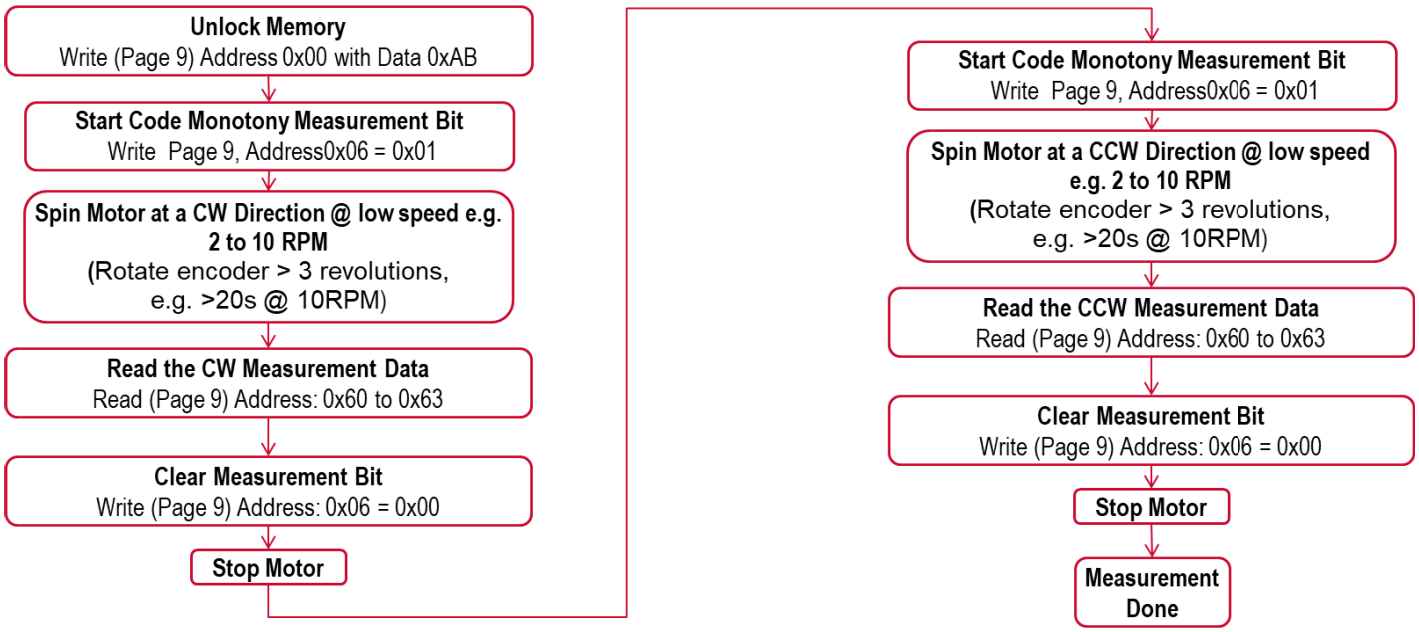


Table 23: Code Monotony Measurement Registers

SPI	Byte Address			Bit							
Page [dec]	**[dec]**	**[hex]**	**Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
9	6	06	CM Test								CM_Test_En
	96	60	CM_Max[15:0]	CM_Max[15:0]							
	97	61									
	98	62	CM_Min[15:0]	CM_Min[15:0]							
	99	63									

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