AS20-M42M-Kxx Series

Absolute Magnetic Encoder RS-485 Option

1 General Specification of RS-485 Serial Communication

Table 1: General Specification of Serial Communication

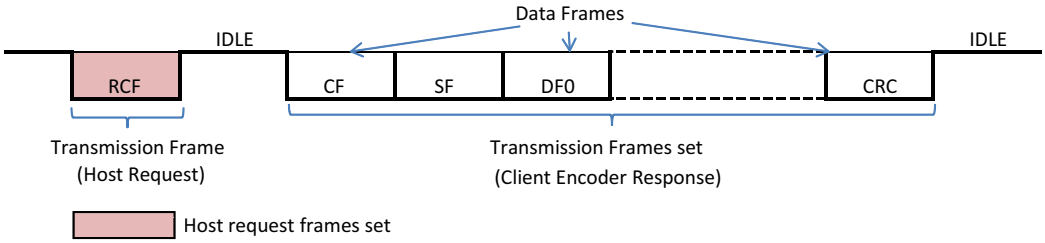
Item	Specification	Note
Transmission Type	Differential Transceiver	
Communication Type	Half duplex	Recommended transceiver: ISL8485E or equivalent
Transmission Code Type	Binary non-return-to-zero (NRZ) code	
Synchronization Type	Asynchronous	
Communication Baud Rate	2.5 MB/s, 5.0 MB/s, and 10.0 MB/s	
Frame Length	10 bits per frame	
Transmission Error Checking	8 bits CRC	CRC equation: $G(X) = X^8 + 1$, where X = CRC0 ~ CRC7

2 General Format Definition of Transmission Frames between Host and Client Encoder

2.1 Overview of Communications

One-to-one half-duplex serial communications are established between the client encoder and the host (for example, a servo driver). The communications are in a differential transmission format. The encoder will carry out specific operations based on the command requests made by the host. An acknowledgment of the command request is necessary before the encoder executes the requested operation, such as by checking the start bit, information data field and stop bit. If this check fails, the encoder will not acknowledge and execute the received command request.

Figure 1: General Transmission Frames Format on a Half-Duplex Line



NOTE:

- Start of transmission frames set: Upon detecting of the first logic of low state 0 on the transmission line after an idling state, and if the following three bits conform to the sync code, the encoder will acknowledge it as a valid request control field (RCF) and indicates the start of a transmission frame set. Otherwise, the encoder will continue to search for the next available logic of low state 0.
- End of transmission frames set: After the command frame is detected, if there is no start bit after the end bit of the last frame read, and no subsequent frame detected, the end of transmission frame set is concluded.
- Idle state: Idle state means a space between each transmission frames set and subsequent transmission frames. At idling state, the logic of output in transmission line is kept to high state 1.

2.2 Encoder Read-Out Frame Sets Format and Timing

Figure 2: Encoder Position Data Read-Out Frames Set

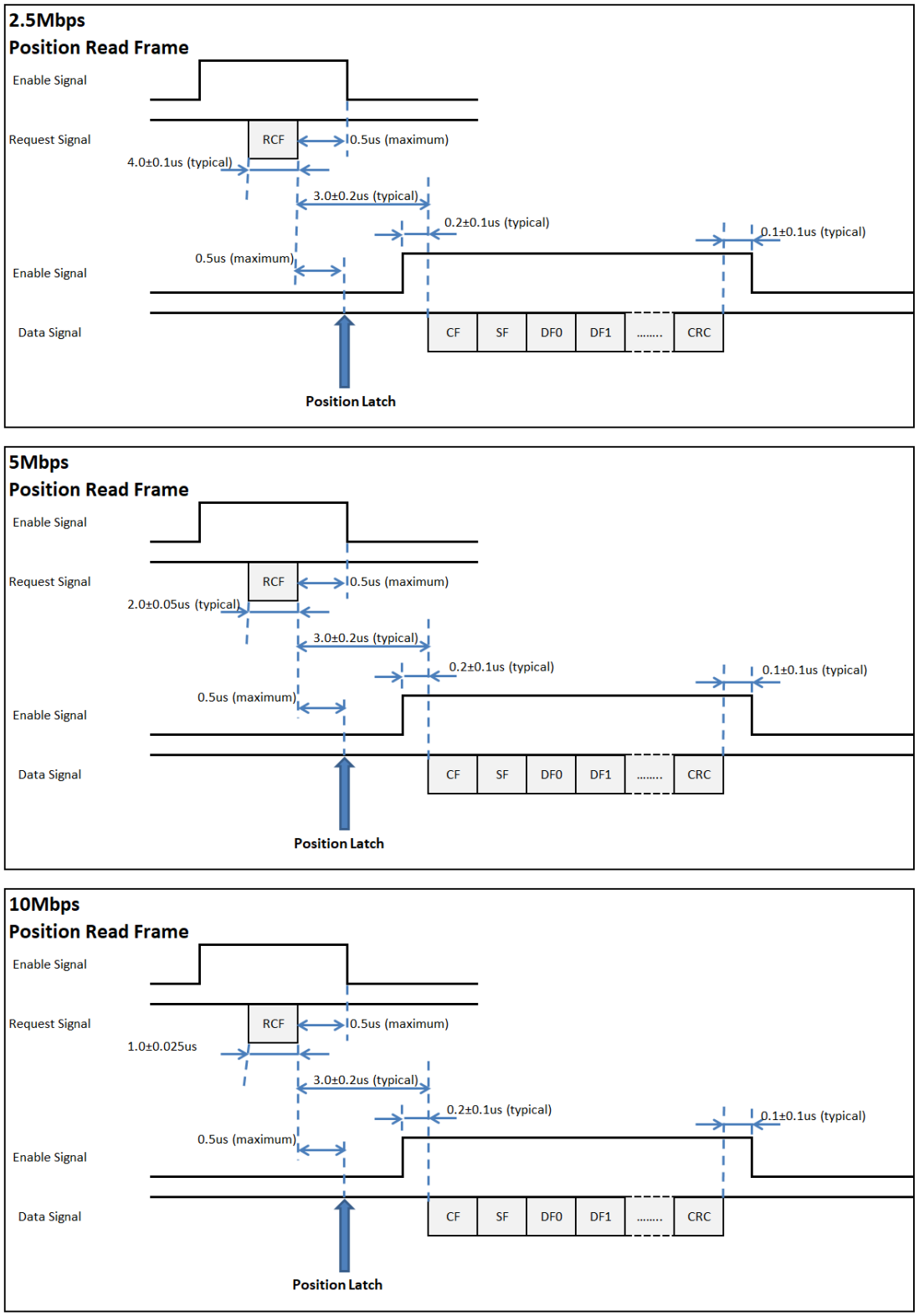
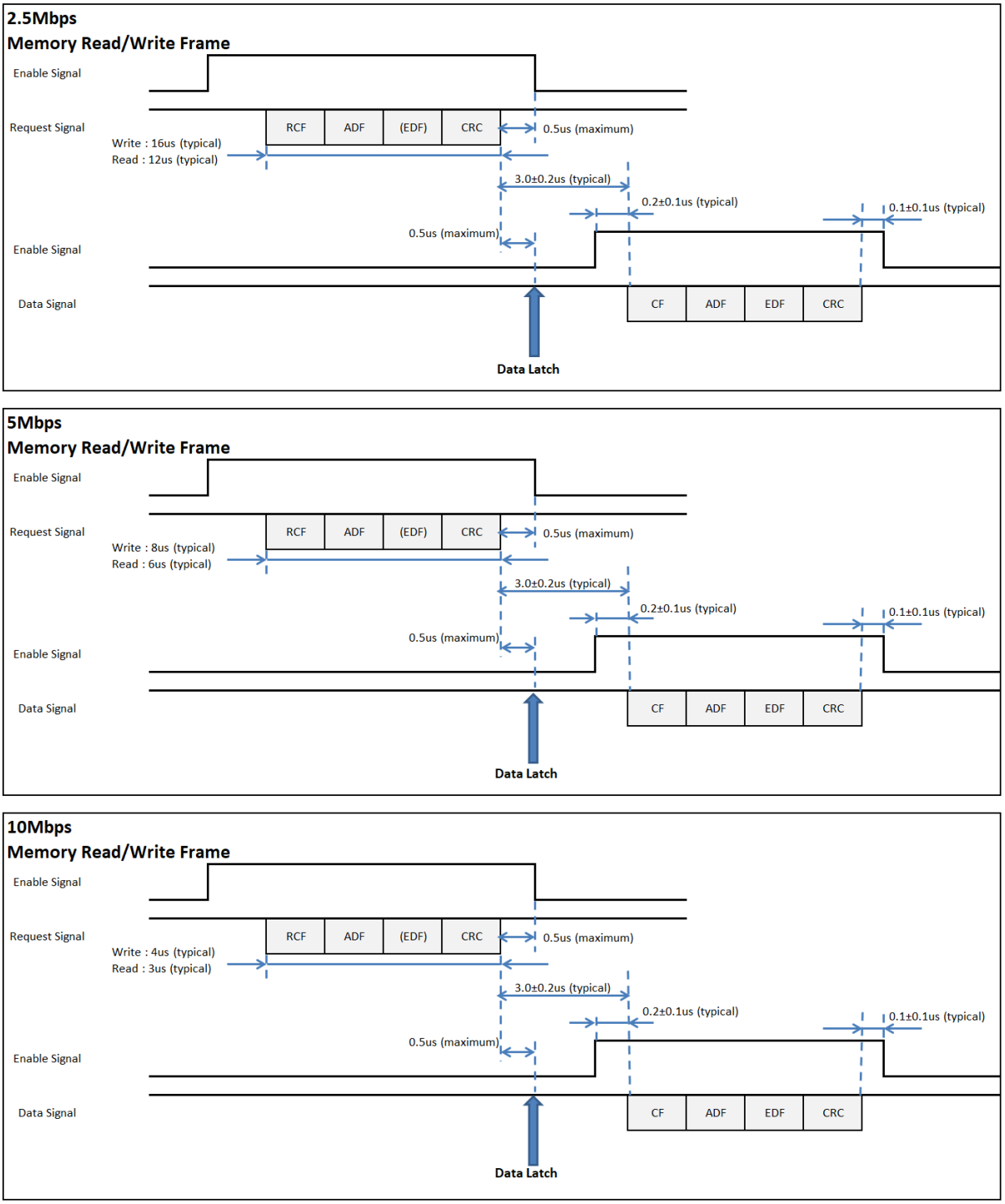


Figure 3: Encoder Memory Data Read and Write Frames Set



2.2.1 Encoder Position Data Read-Out Frame Sets

Upon the host issuing a RCF frame request, the encoder shall respond after 3.0 µs (typical) with an encoder data frames set with the following contents:

1. CF: Control field - corresponds to the command frame issued by the host
2. SF: Status field
3. DF0~DF7: Encoder data field
4. CRC: Cyclic redundancy check (CRC) frame
5. The encoder response data frame sets are dependent on the requested operation by the host, see Table 5.

2.2.2 Memory Data Read-Out Frames Set

The transmission frames contain the following information:

1. CF: Control field - this is the same for both the host command and the encoder response
2. ADF: Address data field - indicates the memory location to read
3. EDF: Memory data field - contains the data to be read from memory
4. CRC: Cyclic redundancy check (CRC) checking

2.2.3 Memory Data Write Frames Set

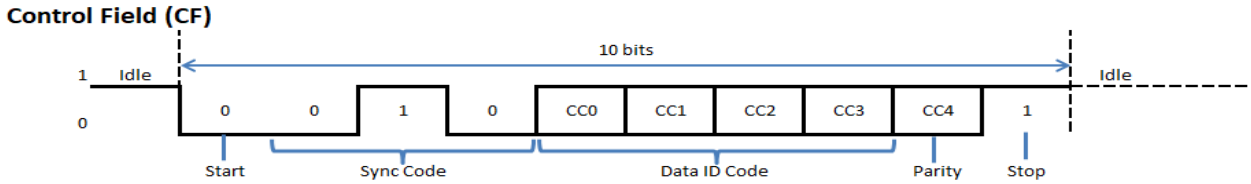
The transmission frames contain the following information:

1. CF: Control field - this the same for both the host command and the encoder response
2. ADF: Address data field - indicates the memory location to write
3. EDF: Memory data field - contains the data to be written to memory
4. CRC: Cyclic redundancy check (CRC) checking

3 Details Description of Data Frames

3.1 Control Field (CF)

Figure 4: Control Field Format



The contents of the CF frame are as follows:

1. Start Bit: Indicates the start of a frame, and is always 0.
2. Sync Code: Indicates a valid sync code has been issued, and is defined as 010.
3. Data ID: A combination of bits that define command instructions; see Table 2 and Table 3.
4. Parity Bit: The parity check bit for the data ID, see Table 2.
5. Stop Bit: Indicates the end of a frame, and is always 1.

3.1.1 Data ID and Client Encoder Operation Definition

Table 2: Encoder Operation Command Code Definition and Parity Bit

Encoder Operation	Data ID	Encoder Sync Code			Data ID Bits				Parity	HEX
		BIT 0	BIT 1	BIT 2	CC0	CC1	CC2	CC3	CC4	
Position or Encoder Information Read Command	0	0	1	0	0	0	0	0	0	02
	1	0	1	0	1	0	0	0	1	8A
	2	0	1	0	0	1	0	0	1	92
	3	0	1	0	1	1	0	0	0	1A
	4	0	1	0	0	0	1	0	1	A2
Memory Write Command	6	0	1	0	0	1	1	0	0	32
Alarm Clear Command	7	0	1	0	1	1	1	0	1	BA
Position Zero Reset Command	8	0	1	0	0	0	0	1	1	C2
Multi-turn and Alarm Clear Command	C	0	1	0	0	0	1	1	0	62
Memory Read Command	D	0	1	0	1	0	1	1	1	EA

3.1.2 Description of Encoder Operation

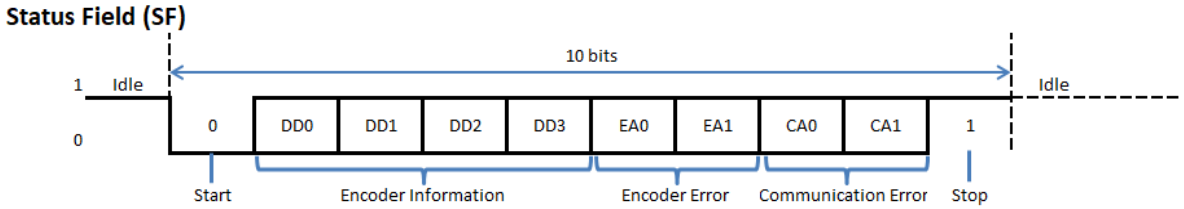
Table 3: Description of Encoder Operation

Operation	Data ID	Description of Operation
Position Read Command	0, 1, 2, 3, 4	Transmit Data ID code (see Table 2) to the Encoder according to the List of Data field.
Memory Write Command	6	Eight bits of data to be written into a designated memory address of the user-accessible area.
Alarm Clear Command a	7	Consecutive sending to perform the Alarm Clear command.
Position Zero Reset Command a	8	Consecutive sending to perform the Position Zero Reset command
Multi-turn and Alarm Clear Command a	C	Consecutive sending to perform the Multi-turn and Alarm Clear command
Memory Read Command	D	Eight bits of data to be read from a designated memory address of the user-accessible area.

NOTE: See Table 5 and Table 6 for the requirements of consecutive sending for the Clear and Reset commands.

3.2 Status Field (SF)

Figure 5: SF Frame Format



The contents of a SF frame are as follows:

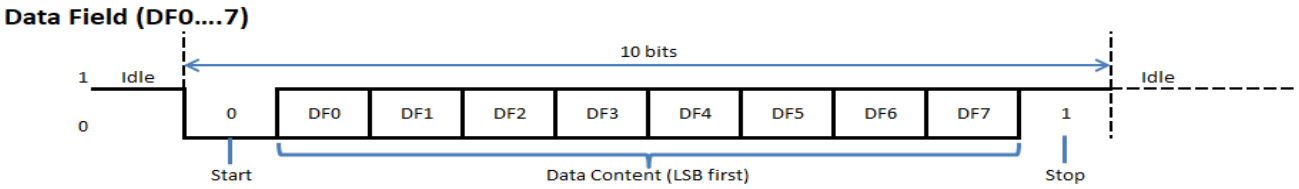
1. Start Bit: Indicates the start of a frame, and is always *0*.
2. Encoder Information: Defined as *0000*.
3. Encoder Error: Returns with state *1* if an encoder error is detected
4. Stop Bit: Indicates the end of a frame, and is always *1*.

Table 4: Status Field Description of Error Flags

Logic When Error Is Detected	Error Flag	Error Description
Encoder Error bit 1	EA0	Encoder counting error
	EA1	Multi-turn counting error
Communication Error bit 1	CA0	Parity error detected in Host Request frames set
	CA1	End bit error detected in Host Request frames set

3.3 Data Field (DF_n)

Figure 6: DF_n Frame Format



The contents of a DF_n frame are as follows:

1. Start Bit: Indicates the start of a frame, and is always *0*.
2. DF0~DF7: An 8-bit data set with the LSB first in the sequence.
3. End bit: Indicates the end of the frame, and is always *1*.

3.3.1 Description of Data Frames With Respective Data ID

The AS20 supports variants of output formats, depending on single-turn and multi-turn resolutions requirements. See Table 16 for the RS-485 format settings.

3.3.1.1 Data Frames Format for up to 24-bit MT Output

This is the default RS-485 format, which can transmit up to three bytes (24-bit) of MT data.

Table 5: Data Frames Content with Respective Data ID for up to 24-bit Multi-turn

Data ID	CF	SF	DF0	DF1	DF2	DF3	DF4	DF5	DF6	DF7	CRC	Remark	Frame Size
0	CF	SF	ABS0	ABS1	ABS2						Include CRC	Position read command	6
1	CF	SF	ABM0	ABM1	ABM2								6
2	CF	SF	ENID									Encoder identification	4
3	CF	SF	ABS0	ABS1	ABS2	ENID	ABM0	ABM1	ABM2	ALMC		Position read command	11
4	CF	SF	ABS0	ABS1	ABS2	ENID	ABM0	ABM1	ABM2	TEMP			11
6	CF	ADF	EDF									Memory or register write command	4
7	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to perform alarm clear command	6
8	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to perform ST zero reset command	6
C	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to perform MT and alarm clear command	6
D	CF	ADF	EDF									Memory or register read command	4

NOTE:

- ABSn: Single-turn counts. The LSB of the single-turn counts is located in ABS0, and the MSB of the counts data is located in ABS2. Combining ABS0 to ABS2 will provide a maximum total of 24 bits of single-turn data.
- ABMn: Multi-turn counts. The LSB of the multi-turn counts is in ABM0, and the MSB of the counts data is in ABM2. Combining ABM0 to ABM2 will provide a maximum total of 24 bits of multi-turn data.
- ENID: Encoder single-turn bits identification in 8-bit format. For example, 17-bit output is set to *11h*, and 18-bit output is set to *12h*.
- ALMC: Encoder alarm data in 8-bit format. See Table 8.
- TEMP: Encoder temperature readout data in 8-bit format. See Table 10.

3.3.1.2 Data Frames Format For up to 32-bit MT Output

Table 6: Data Frames Content with Respective Data ID up to 32-bit Multi-turn Resolution

Data ID	CF	SF	DF0	DF1	DF2	DF3	DF4	DF5	DF6	DF7	CRC	Remark	Frame Size
0	CF	SF	ABS0	ABS1	ABS2						Include CRC	Position read command	6
1	CF	SF	ABM0	ABM1	ABM2	ABM3							7
2	CF	SF	ENID									Encoder identification	4
3	CF	SF	ABS0	ABS1	ABS2	ABM0	ABM1	ABM2	ABM3	ALMC		Position read command	11
4	CF	SF	ABS0	ABS1	ABS2	ABM0	ABM1	ABM2	ABM3	TEMP			11
6	CF	ADF	EDF									Memory or register write command	4
7	CF	SF	ABS0	ABS1	ABS2							Consecutive 8x to perform alarm clear command	6
8	CF	SF	ABS0	ABS1	ABS2	ABM0	ABM1	ABM2	ABM3	ALMC		Consecutive 8x to perform ST zero reset command	11
C	CF	SF	ABM0	ABM1	ABM2	ABM3						Consecutive 8x to perform MT and alarm clear command	7
D	CF	ADF	EDF									Memory or register read command	4

NOTE:

- ABSn: Single-turn counts. The LSB of the single-turn counts is located in ABS0, and the MSB of the counts data is located in ABS2. Combining ABS0~ABS2 will provide a maximum total of 18 bits of single-turn data.
- ABMn: Multi-turn counts. The LSB of the multi-turn counts is in ABM0, and the MSB of the counts data is in ABM2. Combining ABM0~ABM3 will provide a maximum total of 32 bits of multi-turn data.
- ALMC: Encoder alarm bits. See Table 8.
- TEMP: Encoder temperature readout bit.

3.3.1.3 Data Frames Format For up to 39-bit MT Output

For the maximum MT data output of up to 39 bits, an additional byte of MT data (ABM4) is added to the 32-bit format as per Table 6. Command ID 1, 3, 4, and 8 will have an additional byte in the encoder data frames.

3.3.2 Single-Turn Encoder Identification Setting

To set the ENID value, use the configuration in Table 7.

Table 7: ENID Settings

RS-485			ENID								Default [hex]
Page	Address		Bit								
[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0	
7	1	0x01	ENID [7:0]								0x12

The default value is set to 12h, referenced to the 18-bit single-turn resolution of the AS20 encoder ASIC.

3.3.3 Encoder Alarm Definition

Table 8: ALMC Alarm Bits Definition

Bit Value	ALMC bit							
	DF7-0	DF7-1	DF7-2	DF7-3	DF7-4	DF7-5	DF7-6	DF7-7
0	N/A	Error	No Error	No Error	No Error	No Error	No Error	N/A
1		Chip Ready (No Error)	ST Error	XC Error / FeRAM CRC Error	Mag HI / Mag LO / Temp Error / MT Speed Warning	MT Error	Memory Error	
Encoder Error Status		N/A	EA0	EA1	N/A	EA1	N/A	

Table 9 shows the encoder alarms and their definitions.

Table 9: Alarms and Definitions

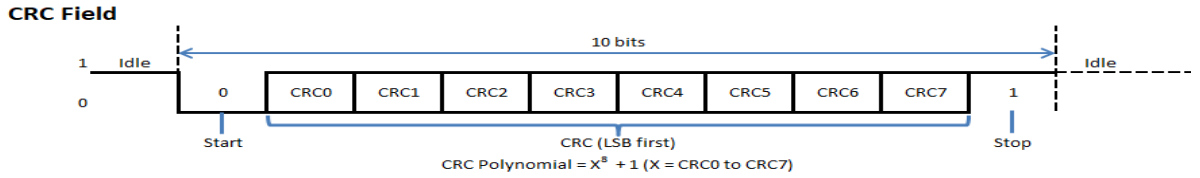
Alarms	Alarms Definition
ST Error Single-Turn Counting Error	Checks the integrity of the single-turn position. ■ 1: Error in the single-turn position. ■ 0: Normal operation, no error in the single-turn position.
MEM Error Memory Error	Indicates the EEPROM content loading status upon encoder power up, or the content read/write status during encoder calibration. ■ 1: Fail to load EEPROM memory data . ■ 0: Success to load EEPROM memory data.
XC Error / FeRAM CRC Error	Indicates a multi-turn block hardware counting error or FeRAM communication CRC error. ■ 1: Multi-turn hardware or FeRAM CRC error. ■ 0: No hardware or CRC error.
MT Error / FeRAM Register Error	Detects an error reading the MT hardware counter value or an I^2C communication error. ■ 1: Error in MT position reading. ■ 0: No error in MT position reading.
Speed MT Warning	Detects that the rotation speed is greater than 30,000 rpm for MT synchronization. ■ 1: Rotation speed exceeding the limit detected. ■ 0: No overspeed detected.

Table 9: Alarms and Definitions

Alarms	Alarms Definition
Temperature Error	Indicates the temperature exceeds the maximum preset limit. ■ 1: Temperature above preset limit. ■ 0: Temperature below preset limit.
Mag Hi / Mag Lo	Detects an error in the magnetic field sensing. ■ 1: Magnetic field strength is too strong or too weak. ■ 0: Magnetic field strength is optimum for normal operation.
Chip Ready	Indicates the encoder status. This status bit is disabled by default. ■ 1: Encoder is ready for normal operation (no fault status). ■ 0: Encoder has abnormality due to other alarm bits triggered.

3.4 Cyclic Redundancy Check Frame (CRC)

Figure 7: CRC Frame Format

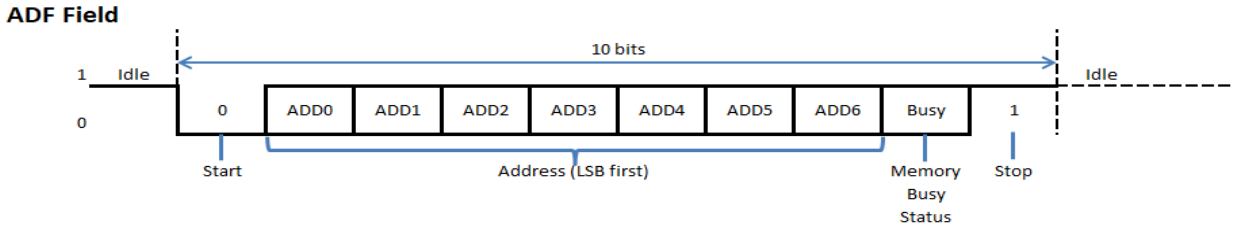


The contents of a CRC frame are as follows:

1. Start Bit: Indicates the start of a frame, and is always 0.
2. CRC0~CRC7: An 8-bit CRC data set with the LSB first in the sequence. The CRC codes are generated per the equation of G(X) = X8 + 1 (X = CRC0 ~ CRC7).
3. End Bit: Indicates the end of a frame, and is always 1.

3.5 Address Data Frame (ADF)

Figure 8: ADF Frame Format

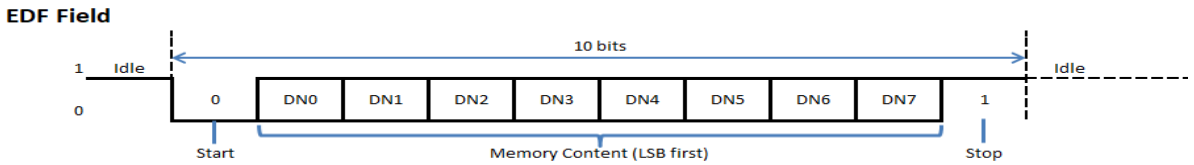


The contents of an ADF frame are as follows:

1. Start Bit: Indicates the start of a frame, and is always 0.
2. ADD0~ADD6: A 7-bit memory address data set with the LSB first in the sequence.
3. Busy: Memory Access Busy (MBSY) status flag.
4. End Bit: Indicates the end of a frame, and is always 1.

3.6 Memory Data Frame (EDF)

Figure 9: EDF Frame Format



The contents of an EDF frame are as follows:

1. Start Bit: Indicates the start of a frame, and is always 0.
2. DN0~DN7: An 8-bit memory data set with the LSB first in the sequence.
3. End Bit: Indicates the end of a frame, and is always 1.

3.7 Temperature Sensor

When reading using Command ID4 as per Table 5, the temperature data (TEMP) is available as the DF_7.

Encoder temperature readout bit, an example of the data as 2's complement is listed in Table 10.

Table 10: Temperature Sensor Data

Temperature °C	TEMP[7:0]
–64	1100 0000
–50	1100 1110
–20	1110 1100
–1	1111 1111
0	0000 0000
1	0000 0001
10	0000 1010
25	0001 1001
50	0011 0010
85	0101 0101
127	0111 1111
159	1001 1111
191	1011 1111

NOTE:

1. The minimum support range for the temperature output is –64°C.
2. Negative values are from –1°C to –64°C only.
3. The maximum positive value is 191°C.
4. Alternate temperature readout is available by accessing the memory register at Page 7, Address 0x05 (see Table 11).

Table 11 lists the configuration for setting temperature values and alarms. The temperature upper limit defaults to 0x7D (125°C), referenced to the ambient temperature as measured by the AS20 encoder ASIC.

Table 11: Temperature Sensor Settings

RS-485			Temperature Sensor								Default [hex]
Page	Address		Bit								
[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0	
7	2	0x02	Temperature Upper Limit Offset [7:0]								0x00
	3	0x03	Temperature Offset [7:0]								0x00
	4	0x04	Temperature Upper Limit [7:0]								0x7D
	5	0x05	Temperature Output Data (Read-only register)								

Table 12 is an example based on an initial alarm (Address 0x04) setting of 125°C. The temperature offset can be a positive or negative value.

Descriptions for the case examples detailed in Table 12 are as follows:

- Case 1: No offset.
- Case 2: If the temperature offset (Address 0x03) is positive value, then the temperature upper limit offset (Address 0x02) is also set to the same value.
- Case 3: If the temperature offset (Address 0x03) is negative value, then the absolute value of this value needs to be added to the default temperature upper limit (Address 0x04).
- Case 4: Negative offset value.

Table 12: Temperature Sensor Offset Setting Example

Case	Temperature Sensor Offset Register	0x02	0x03	0x04	0x05	Remarks	
	Offset Value (Decimal)	Temperature Upper Limit Offset (hex)	Temperature Offset (hex)	Temperature Upper Limit (hex)	Temperature Output (Dec)	Raw Temperature without Offset (Dec)	Alarm Trigger
1	0	0	0	7D	124	124	No
					125	125	Yes
					126	126	Yes
2	10	0A	0A	7D	124	114	No
					125	115	Yes
					126	116	Yes
3	–1	0	FF	7D+01	124	125	No
					125	126	Yes
					126	127	Yes
4	–10	0	F6	7D+0A	124	134	No
					125	135	Yes
					126	136	Yes

4 Encoder Memory Area

4.1 User Area

The AS20 supports 8 Kb of register user area. The memory data is kept in non-volatile memory. The available register pages that are accessible by the user are listed in Table 13.

Table 13: User Memory Area with 8 Kb

Page [decimal]	Address [hex]	Remarks
0 to 4	0x00 to 0x7E	User area
11 to 13	0x00 to 0x7E	
Page Selection	0x7F	

NOTE:

1. Eight pages with 127 addresses each are allocated for user access.
2. The active page numbers are specified in address 0x7F; page change is done by writing to address 0x7F. The default page after power-on is Page 0.
3. Once the page value is changed, allow a time delay of 18 ms.
4. The typical EEPROM read time is 200 µs, minimum.
5. The typical EEPROM write time is 6 ms, minimum.

4.2 Encoder System Area

Additional register pages are reserved for system areas that are protected against accidental writing during operation. The memory data is kept in non-volatile memory.

Table 14: Encoder System Memory Area

Page [decimal]	Address [hex]	Remarks
5 to 8	0x00 to 0x7E	System area
Page Selection	0x7F	

NOTE: Pages 9 and 10 are volatile memory addresses reserved for encoder system use.

5 Encoder Configuration

5.1 Encoder Memory Map for Calibration and Special Functions

Table 15: General Volatile Memory Map (Page 9, 0x09)

No.	Item	Address	Bits							
			7	6	5	4	3	2	1	0
1	Unlock Memory	0x00	Unlock Memory by Writing 0xAB							
2	Program Memory	0x01	Program Memory by Writing 0xC0							
3	Clear Alarm/ Position	0x02						Alarm Clear	ST Zero Reset	MT Zero Reset
4	Calibration	0x04						OT_ Direction-2	OT_Without_ Accuracy	OT_ Direction-1
5	Reset	0x0B	Perform Hard Reset by Writing 0xA7							
6	Alarm/ Warning[31:24]	0x24	N/A	N/A	N/A	MT Sync Error	N/A	MT Error	N/A	N/A
7	Alarm/Warning [23:16]	0x25	N/A	N/A	XCErr	Speed MT Warning	FeRAM CRC Err	N/A	N/A	Feram ECC A/B Reg Err
8	Alarm/Warning [15:8]	0x26	Chip Ready	Reserved	N/A	Temp_Err	Memory Err	N/A	ST_Err	N/A
9	Alarm/Warning [7:0]	0x27	N/A	N/A	Mag Hi	Mag Lo	N/A	N/A	N/A	N/A
10	Calibration Status	0x28	Mem_Busy	N/A	Internal_ Mem_Pass	Internal Mem_Fail	Zero_Done	Zero_Err	OT_Cal_ Done	OT_Cal_Err

NOTE:

1. The Memory Program command is needed for the system area memory to be effective upon power cycle. This is applicable for changes to internal memory Page 5 to Page 8.
2. Perform the Memory Program command for changes to any of the affected banks before moving to other non-volatile memory banks.
3. Changes will be lost after a power cycle without a Memory Program command.

5.2 RS-485 Encoder Configuration

User-configurable RS-485 protocol settings are listed in Table 16.

Table 16: RS-485 Encoder Settings

Page [decimal]	Address [hex]	Bits	Parameter	Function	Value [binary]	Setting	Default Value [binary]	Default Value [hex]
7	1D	7	Parity	Default Setting	0	0	0	8'h22
		6	Factory Setting	Default Setting	0	0	0	
		5	RS-485 Mode	Single RS-485 mode	1	Single Device	1	
		[4:3]	RS-485 Baud Rate	Default to 2.5 Mb/s	00 01	2.5 Mb/s	00	
					10	5.0 Mb/s		
					11	10 Mb/s		
		[2:0]	RS-485 Encoder Sync Code	Encoder Sync Code Address	010	010	010	
	1E	7:6	RS-485 Protocol Format Selection	Variance of RS-485 Format	00	24B MT	00	8'h24
					01	32B MT		
					10	39B MT		
					11	N/A		
		5:0	Default Factory Settings	Factory Preset	100100	Default	100100	

WARNING! Updating the RS-485 settings requires the host to also issue the subsequent commands with the same changes made. Otherwise, the communication between the host and the client encoder may fail.

NOTE:

1. The Memory Program command is needed for the system area memory to be effective upon power cycle. This is applicable for changes to internal memory Page 5 to Page 8.
2. Perform the Memory Program command for changes to any of the affected banks before moving to other non-volatile memory banks.
3. Changes will be lost after a power cycle without a Memory Program command.

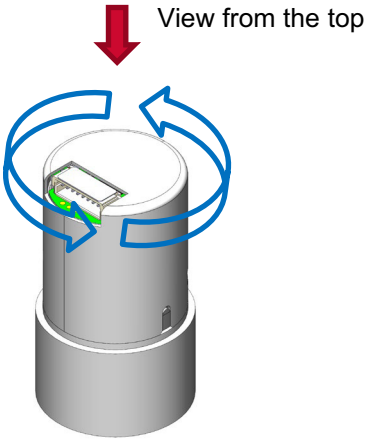
5.3 Counting Direction

Table 17: Register Bit for Counting Direction Selection

Page [Decimal]	Address [hex]	Bit								Default Value
		7	6	5	4	3	2	1	0	
7	20	N/A	Counting Direction	N/A						8'h40

With the default setting, position data is counting up when rotating in the counterclockwise direction, as viewed from the top of the encoder.

Figure 10: Default Counting Direction



5.4 Zero Reset

The encoder zero-reset data can be accessed by reading the addresses in Table 18. Perform a Memory Program step if the zero-reset data is updated manually.

Table 18: User Zero-Reset Registers

Page	Address [hex]	Bit							
		7	6	5	4	3	2	1	0
7	0E	0	MT_ZR[38:32]						
	0F	MT_ZR[31:24]							
	10	MT_ZR[23:16]							
	11	MT_ZR[15:8]							
	12	MT_ZR[7:0]							
	13	ST_ZR[17:10]							
	14	ST_ZR[9:2]							
	15	ST_ZR[1:0]	6'b000000						

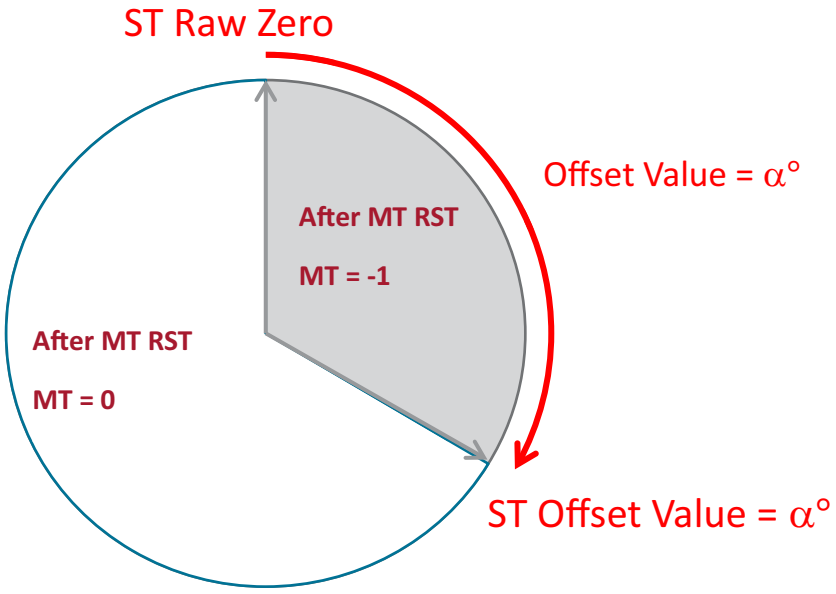
NOTE: Address 0x15[5:0] defaults to all zeros.

For the RS-485 protocol, the ST zero reset is carried out by sending of consecutive Command ID-8 to the encoder; see Table 5 and Table 6.

For the MT zero-reset command, through consecutive sending of Command ID-C, there is a dependency of the new MT position value if the ST zero registers are non-zero. Depending on the ST angle position, the MT reset may return -1 (0xFFFFFF if MT resolution is 24 bit, depending on the resolution) or zero. The exact position depends on the offset values (α) in the ST offset register.

An alternative for customers who must have MT values always set to zero is to implement the MT offset in the controller side. This is done by reading out MT position data and then offset at the controller display. In this case, the MT offset register needs to be set to zero.

Figure 11: Relationship of MT Position Values after Performing the MT Reset Command



5.5 Error and Warning Setting

To enable the Error or Warning bits in the ALMC field, set the respective bit to *1*. Set the bit to *0* to disable.

Table 19: Error and Warning Bits Configuration Addresses

Page	Address [hex]	Bit								Default Value
		7	6	5	4	3	2	1	0	
7	30	Alarm Enable [31:24]								8'h14
	31	Alarm Enable [23:16]								8'h39
	32	Alarm Enable [15:8]								8'h1A
	33	Alarm Enable [7:0]								8'h30
	34	Alarm Latch Enable [31:24]								8'h14
	35	Alarm Latch Enable [23:16]								8'h29
	36	Alarm Latch Enable [15:8]								8'h0A
	37	Alarm Latch Enable [7:0]								8'h00

5.6 Multi-turn and Single-Turn Absolute Resolution Setting

Select the configuration for the absolute position output by updating the Page 7 Address 0x16; see Table 20 and Table 21.

Table 20: Memory Map for Absolute Resolution Settings

Page	Address [Decimal]	Address [hex]	Bit								Default Value
			7	6	5	4	3	2	1	0	
7	22	16	N/A	MT_Select[2:0]			N/A	N/A	ST_Select[1:0]		8'h53

NOTE:

1. Unlock the memory.
2. Write in the new settings at Page 7; read back to ensure the setting is written successfully.
3. Program the memory.

Table 21: Multi-turn and Single-Turn Bits Settings

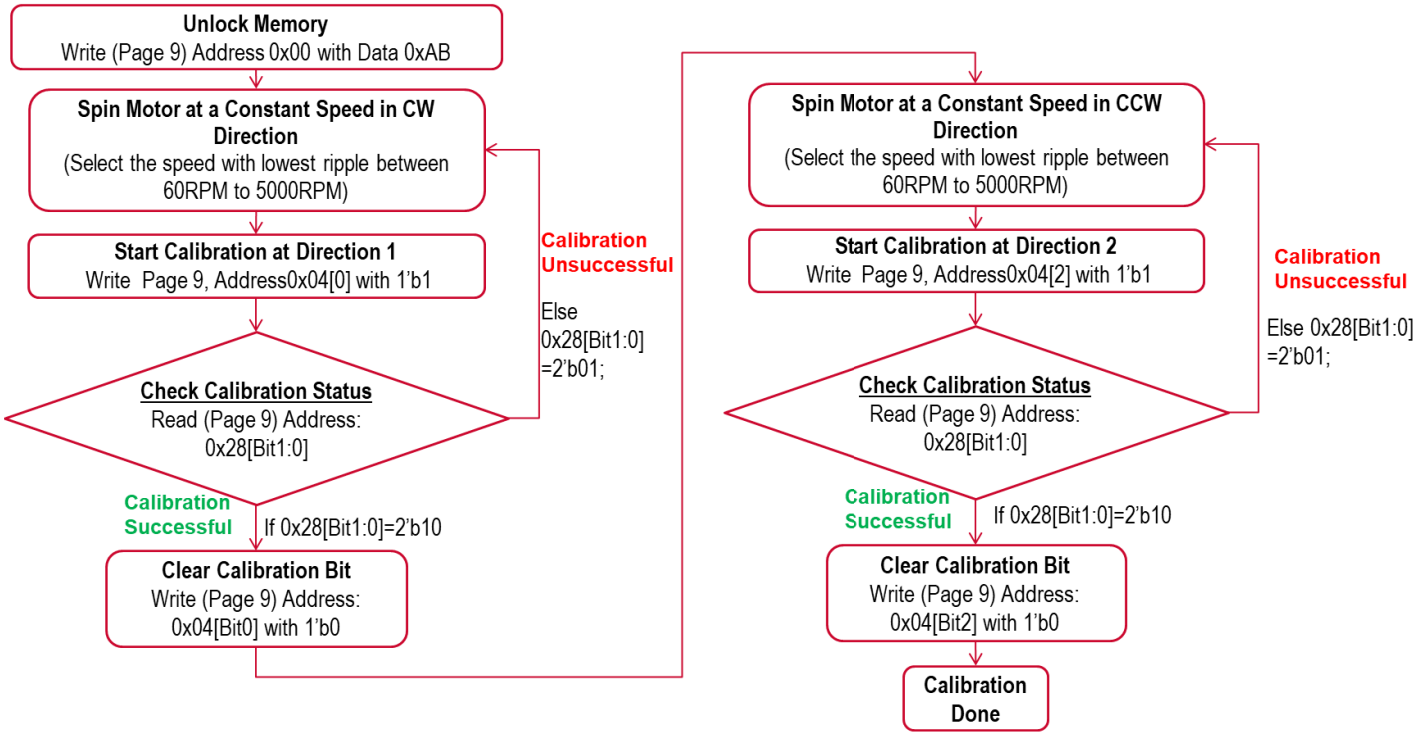
MT_Select	
Bits	**Resolution**
000	0
001	12
010	14
011	16
100	20
101	24
110	32
111	39

ST_Select	
Bits	**Resolution**
00	15
01	16
10	17
11	18

6 Calibration of the AS20-M42M Encoder

6.1 Full Auto-Calibration with Accuracy Correction Enabled

Figure 12: Flow Chart for Full Auto-calibration Process



6.1.1 Calibrate in the Clockwise (CW) Direction

1. Unlock the memory: write Page 9, Address 0x00 = 0xAB.
2. Spin the spindle motor in the clockwise direction at 60 rpm to 5000 rpm; select the least ripple speed, not to exceed 5000 rpm. Wait for the motor speed to be stable before continuing to the next step.
3. Write Page 9, Address 0x04[0] = 1b.
4. Loop read the Calibration Status, Address 0x28:
   a. If Address 0x28[1:0] = 00b, calibration is in progress.
   b. If Address 0x28[1:0] = 10b, calibration is done.
   c. If Address 0x28[1:0] = 01b, calibration is in error.
5. Clear the Calibration Register, Address 0x04 = 0h.
6. If calibration is unsuccessful, repeat Step 3 and Step 4. You may retry up to 10 times.

6.1.2 Calibrate in the Counterclockwise (CCW) Direction

1. Spin the spindle motor in the counterclockwise direction at 60 rpm to 5000 rpm; select the least ripple speed, not to exceed 5000 rpm. Wait for the motor speed to be stable before continuing to the next step.
2. Write Page 9, Address 0x04[2] = 1b.
3. Loop read the Calibration Status, Address 0x28:
   a. If Address 0x28[1:0] = 00b, calibration is in progress.
   b. If Address 0x28[1:0] = 10b, calibration is done.
   c. If Address 0x28[1:0] = 01b, calibration is in error.
4. Clear the Calibration Register, Address 0x04 = 0h.
5. If calibration is unsuccessful, repeat Step 2 and Step 3. You may retry up to 10 times.

6.2 Auto-Calibration without Accuracy Correction

With this option, the position accuracy correction table will not be updated. After assembly, other signal calibration will be performed.

1. Unlock the memory: write Page 9, Address 0x00 = 0xAB.
2. Spin the spindle motor in the clockwise direction at 60 rpm to 5000 rpm. Wait for the motor speed to be stable before continuing to the next step.
3. Write Page 9, Address 0x04[1] = 1b.
4. Loop read the Calibration Status, Address 0x28:
   a. If Address 0x28[1:0] = 00b, calibration is in progress.
   b. If Address 0x28[1:0] = 10b, calibration is done.
   c. If Address 0x28[1:0] = 01b, calibration is in error.
5. Clear the Calibration Register, Address 0x04 = 00h.
6. If calibration is unsuccessful, repeat Step 3 and Step 4. You may retry up to 10 times.

6.3 Auto Zero Reset (Single Turn)

6.3.1 Option 1 with Memory Bit Setting

1. Unlock the memory.
2. Write Page 9, Address 0x02[1] = 1b.

6.3.2 Option 2 with Command ID 8

Execute the Single-Turn Zero-Reset command by sending the Command ID C ten times consecutively for the default RS-485 format (eight times for other RS-485 formats) when the magnet/hub is stationary. The single-turn value will reset to the zero value.

6.4 Auto Zero Reset (Multi Turn)

6.4.1 Option 1 with Memory Bit Setting

1. Unlock the memory.
2. Write Page 9, Address 0x02[0] = 1b.

6.4.2 Option 2 with Command ID C

Execute the Multi-Turn Zero Reset and Alarm Clear command by sending the Command ID C 10 times consecutively for the default RS-485 format (eight times for other RS-485 formats).

6.5 Alarm Clear

6.5.1 Option 1 with Memory Bit Setting

1. Unlock the memory.
2. Write Page 9, Address 0x02[2] = 1b.

6.5.2 Option 2 with Command ID 7

Execute the Alarm Clear command by sending the Command ID 7 10 times consecutively for the default RS-485 format (eight times for other RS-485 formats).

6.5.3 Option 3 with Command ID C

Execute the Multi-Turn Zero Reset and Alarm Clear commands by sending the Command ID C 10 times consecutively for the default RS-485 format (eight times for other RS-485 formats). The multi-turn value will reset to the zero value.

6.6 EH Pulse Voltage Monitoring

The AS20 has a built-in function to measure and monitor the EH pulse voltage level (VWC). The measurement must be conducted with the final encoder assembly, including the external cover.

1. Unlock the memory: write Page 9, Address 0x00 = 0xAB.
2. Enable the VWC Monitoring Self Check by writing Address 0x08 = 04h.
3. Spin the spindle motor in the clockwise direction for greater than 350 rotations at 3000 rpm.
4. Loop read the Calibration Status, Page 9, Address 0x45
   a. If Address 0x45[3] = 1b, the measurement is done.
5. End the VWC Monitoring Self Check by writing Page 9, Address 0x08 = 00h.
6. Read Page 9, Address 0x46 to 0x47 for the measured data.
7. Stop the motor.
8. Repeat Step 2 to Step 6 with rotation in the counterclockwise direction.

Figure 13: VWC Monitoring Self Test Flow Chart

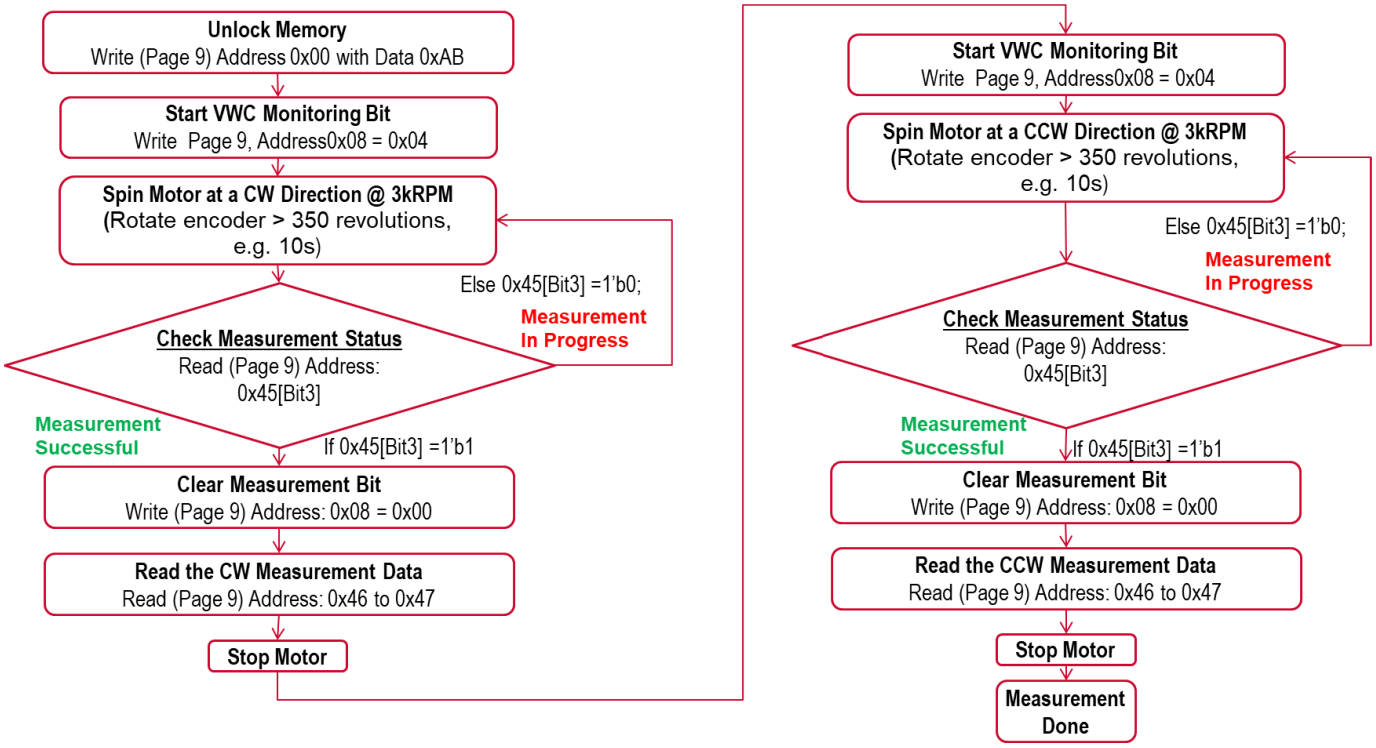


Table 22: EH Pulse Monitoring Measurement Registers

Page	Byte Address			Bit							
Page [dec]	[dec]	[hex]	Description	7	6	5	4	3	2	1	0
9	8	08	Command						Vwc_Mon_Trig		
	69	45	Status					VWC Result Ready			
	70	46	MT Counter VWC	EH Pulse VWC data, Average – 4 Sigma (Target value: 48 to 80 decimal)							
	71	47		EH Pulse VWC data – Mean (Target 48 to 80 decimal)							

6.7 Code Monotony Measurement

The AS20 has a built-in function that measures and monitors the code monotony of the ST position data. The measurement must be conducted with the final encoder assembly, including the external cover. The code monotony value is measured as an18-bit ST step at every 2-µs interval. The readout value is in 2's compliment; the upper positive limit is 7Fh and the lower negative limit is 80h.

1. Unlock the memory: write Page 9, Address 0x00 = 0xAB.
2. Enable the code monotony measurement: write Page 9, Address 0x06 = 01h.
3. Spin the spindle motor in the clockwise direction for more than three revolutions at low speed, for example, 2 rpm to 10 rpm.
4. Read Page 9, Address 0x60 to 0x63 for the measured data.

5. End the code monotony measurement: write Page 9, Address 0x06 = 00h.
6. Stop the motor.
7. Repeat Step 2 to Step 5 with rotation in the counterclockwise direction.

Figure 14: Code Monotony Self Test Flow Chart

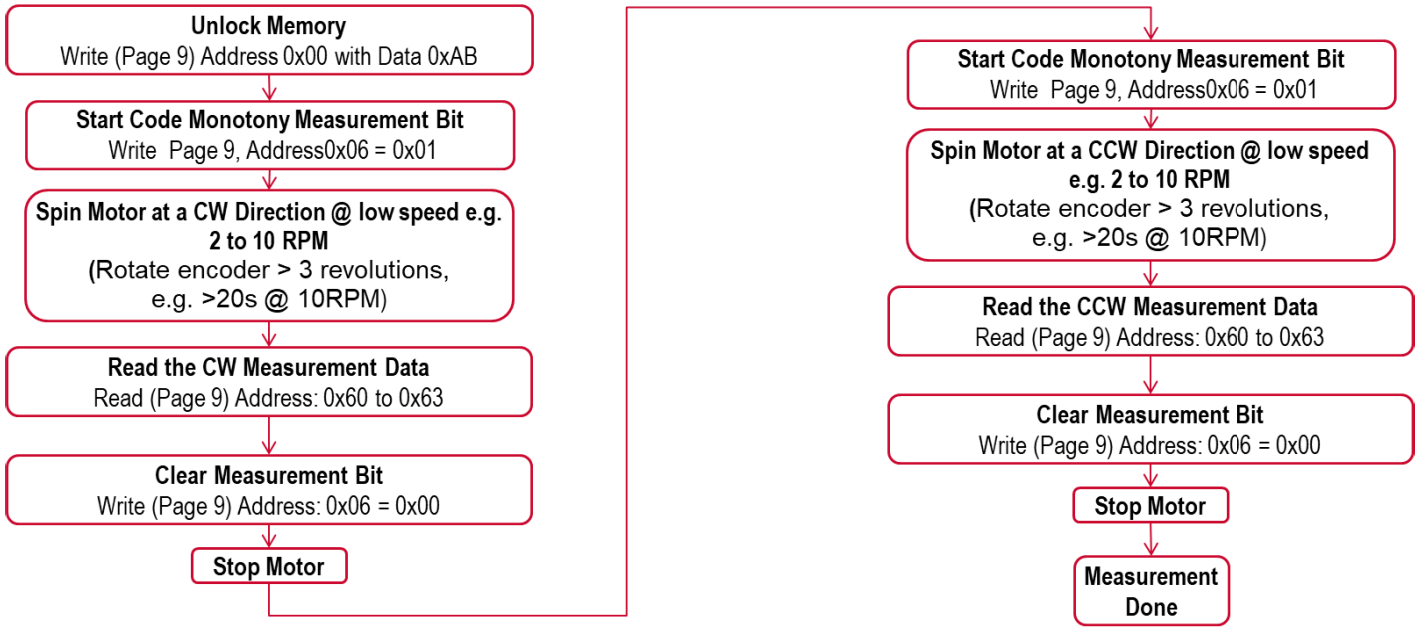
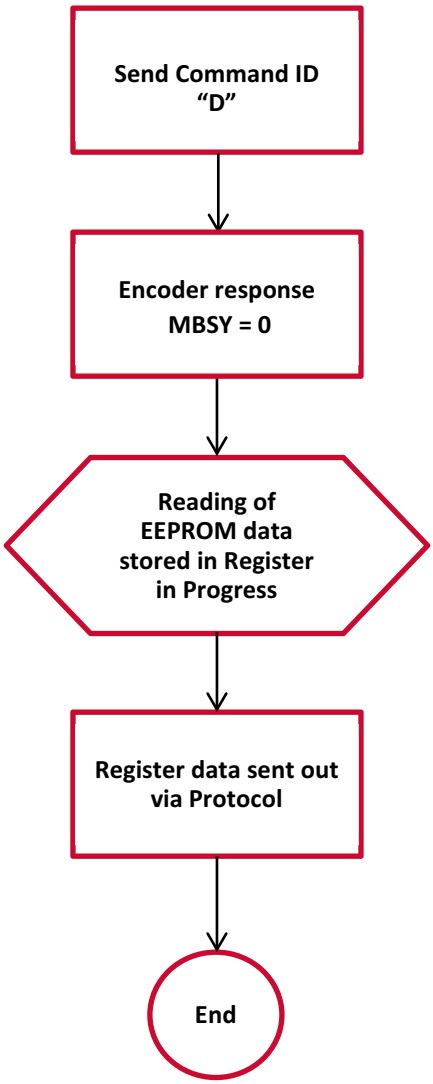


Table 23: Code Monotony Measurement Registers

RS485	Byte Address		Description	Bit							
Page [dec]	[dec]	[hex]		7	6	5	4	3	2	1	0
9	6	06	CM Test								CM_Test_En
	96	60	CM_Max[15:0]	CM_Max[15:0]							
	97	61									
	98	62	CM_Min[15:0]	CM_Min[15:0]							
	99	63									

7 Appendix A

Figure 15: Memory Read Flow Chart

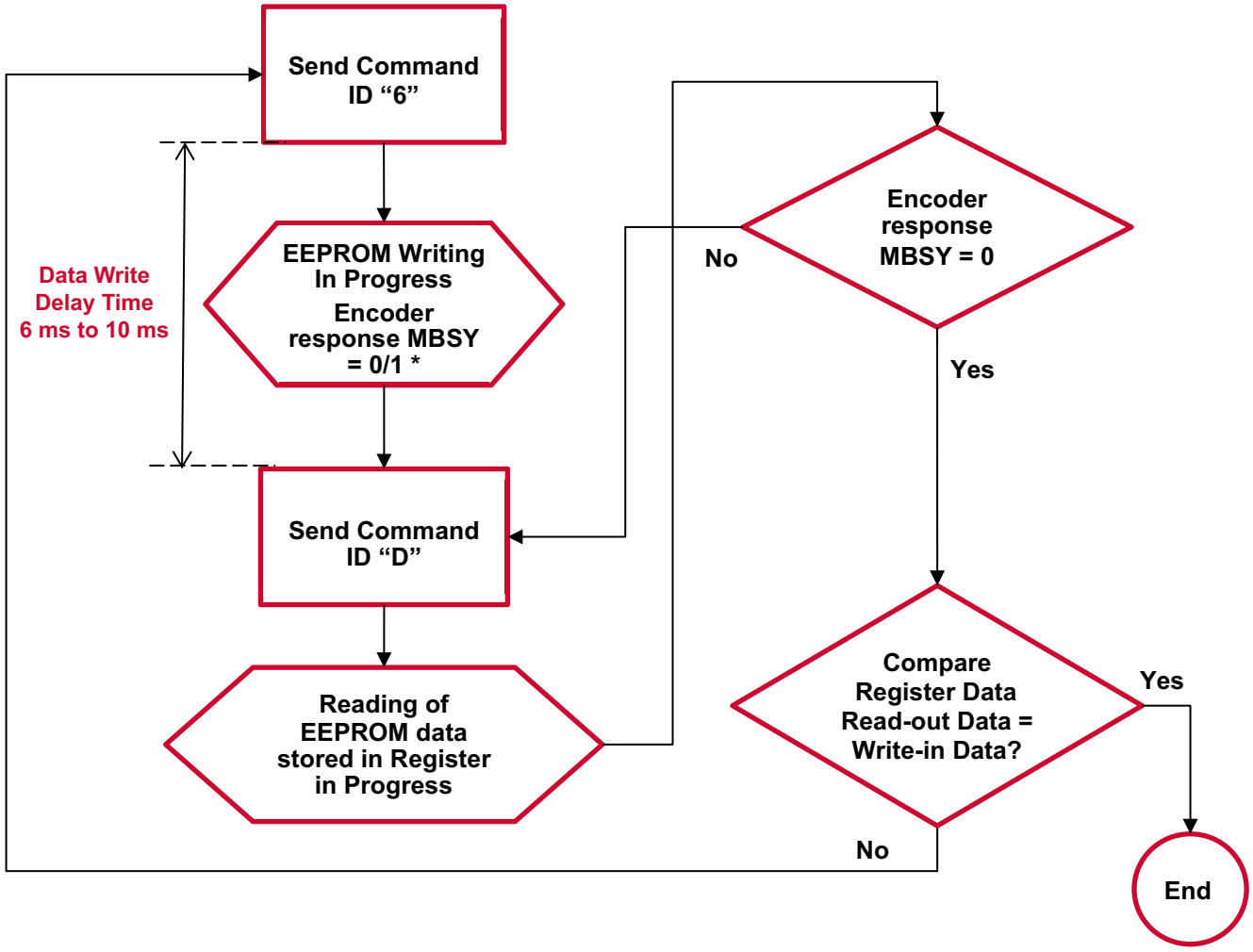


NOTE:

1. Each EEPROM reading requires sending a Command ID D from the host.
2. Each Command ID D from the host will initiate an EEPROM read process from the register; the MBSY flag will return a value of 0.

8 Appendix B

Figure 16: Memory Write Flow Chart



NOTE:

1. When issuing a Command ID 6 request to write to the external EEPROM, the EDF content writing may not be confirmed.
   a. The encoder will respond with an MBSY status of 1 if the EDF data is written to the external EEPROM (see Table 13) with a Command ID 6.
   b. The encoder will respond with an MBSY status of 0 if the EDF data is written to the internal registers (see Table 14) with a Command ID 6.
   c. The encoder will respond with an MBSY status of 1 if a page-change request (address 0x7F) is sent through a Command ID 6.
2. Issue a Command ID D request approximately 6 ms to 10 ms after issuing an EEPROM write request to read the designated EDF data and confirm that correct data had been written.
3. Reissue Command ID 6 if the written-in data does not equal the read-out data.

BROADCOM®