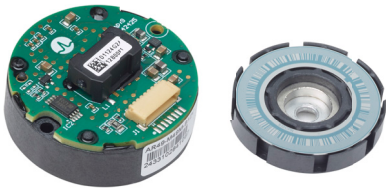
Application Note

AR49-M49M, AR49-M25S Series

25-Bit Optical Single-Turn with 24-Bit Energy-Harvesting Multi-Turn Absolute Encoder Modules



Overview

The Broadcom® AR49 series of optical absolute encoder modules offers up to 25-bit single-turn (ST) position information and 24-bit multi-turn (MT) counts, hence a combined 49-bit high resolution output. The ST block of the encoder consists of a patterned disk, a light source, and photosensitive elements to translate the mechanical motion into an electrical signal. It is designed with a selection of serial communication protocols, with a dedicated electronic circuit designed for a robust signal communication.

These encoders offer many intelligent features such as a built-in temperature sensor, user-programmable resolution, zero reset, system alarm, and more. They come with a recommended high-temperature range of –40°C to 115°C. One of the key advantages is the multi-turn tracking that employs a proprietary energy-harvesting (EH) technology by harvesting the magnetic energy while the patterned disk with magnet rotates. The counter ASIC harvests the energy generated by the EH sensor for processing rotational count and generating counting logics to the nonvolatile memory, which updates and stores the counting.

The entire operation of energy generation, counting, and storage processing is completed within limited energy and a short duration; hence, the kit encoder is suited for both low-speed and high-speed measurements.

Applications

- AC/DC servo motor feedback
- Medical and laboratory equipment
- Robotics
- Factory automation

CAUTION! This product is not specifically designed or manufactured for use in any specific devices. Customers are solely responsible for determining the suitability of the product for its intended application and solely liable for all loss, damage, expense, or liability in connection with such use. Contact Broadcom for further inquiry.

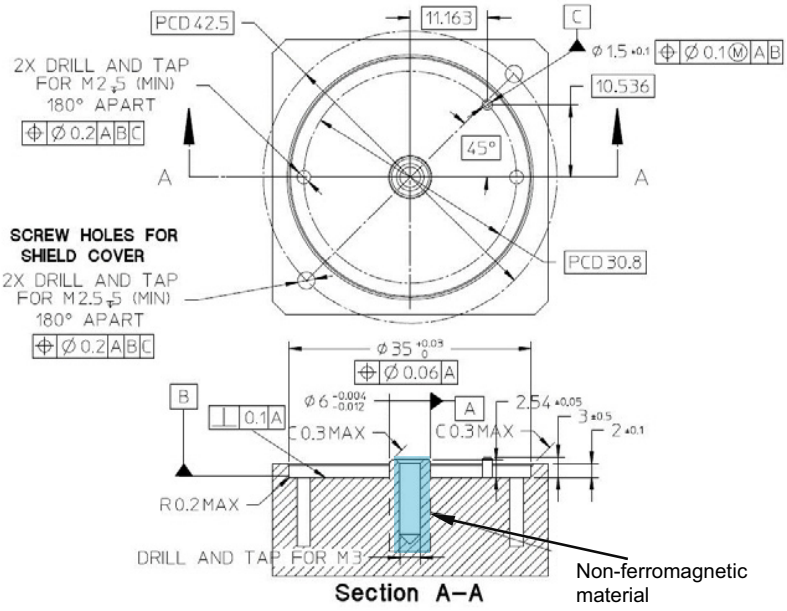
Mounting Requirement and Guideline

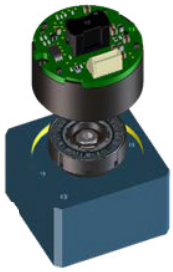
The AR49 encoder module is designed with two options of centering method.

For guiding with the outer diameter (OD) or the inner diameter (ID) of the encoder module, the recommended motor mounting dimensions are shown in Figure 1.

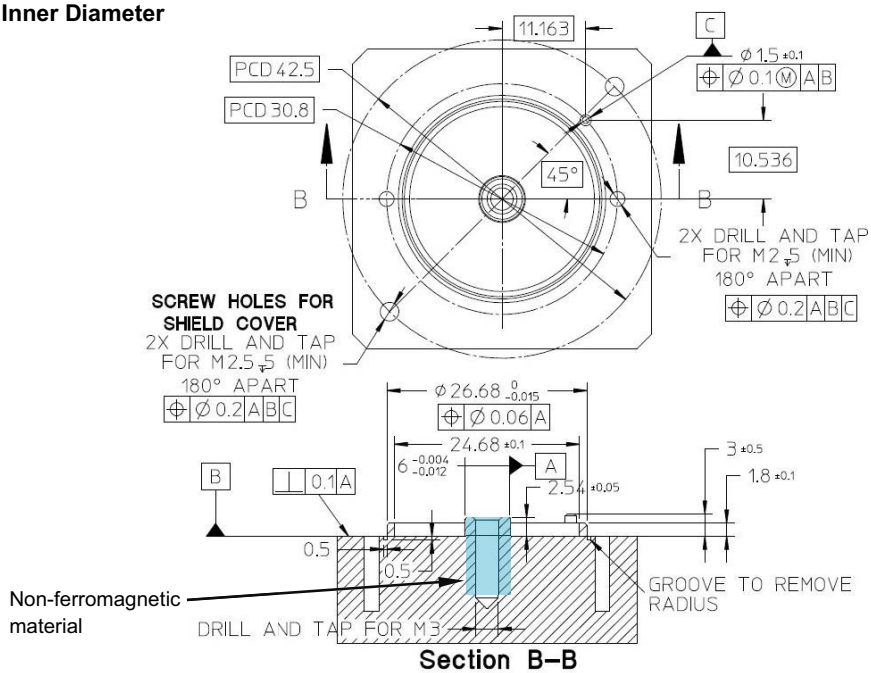
Figure 1: Motor Mounting Dimension with 6-mm Shaft Size

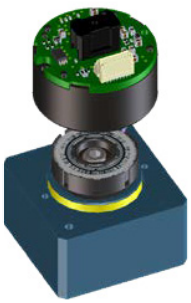
Guide Outer Diameter





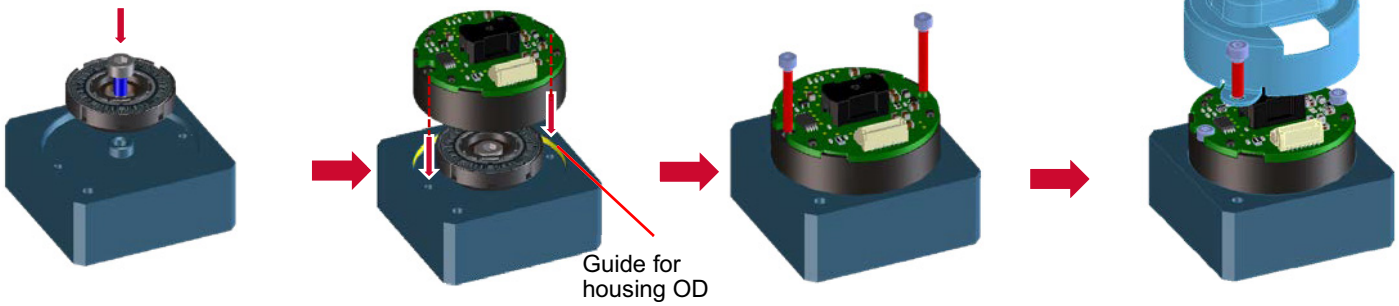
Guide Inner Diameter





Recommended motor shaft 6g6 (-0.004, -0.012) mm
Hub size: 6 mm + 0.000 + 0.012

Figure 2: Assembly Guidelines for Mounting Requirement with OD Guiding

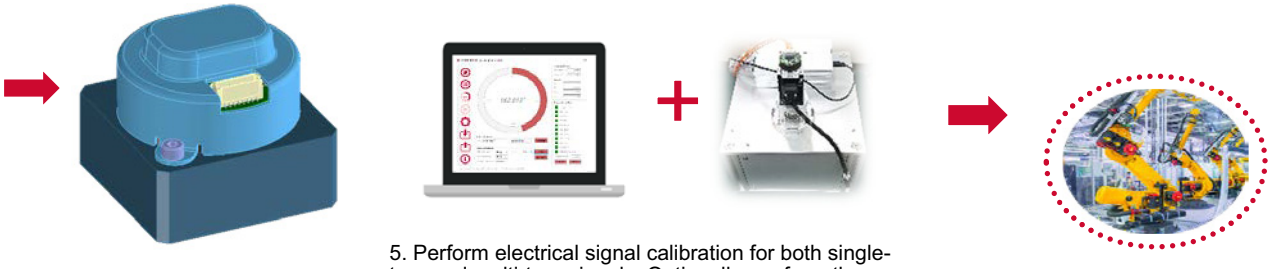


1. Tighten the codewheel hub assembly with M3 thread to the motor shaft.
Recommendations:
a. Apply thread lock.
b. Use M3 austenitic stainless steel class 80; tightening torque is 1.235 Nm to 1.3 Nm.

2. Align the housing OD to the guide on the motor base. Align the 2 screw holes on the housing to the holes on the motor base.

3. Secure the housing with 2x M2 screws.
Recommendations:
a. Apply thread lock.
b. Use M2 stainless steel class 80; the max. tightening torque is 0.285 Nm to 0.3 Nm.

4. Secure the mild steel shield cover with 2x M2.5 screws.
Recommendations:
a. Apply thread lock.
b. Use M2.5 class 12.9, socket head screw; tightening torque is 1.04 Nm to 1.09 Nm.

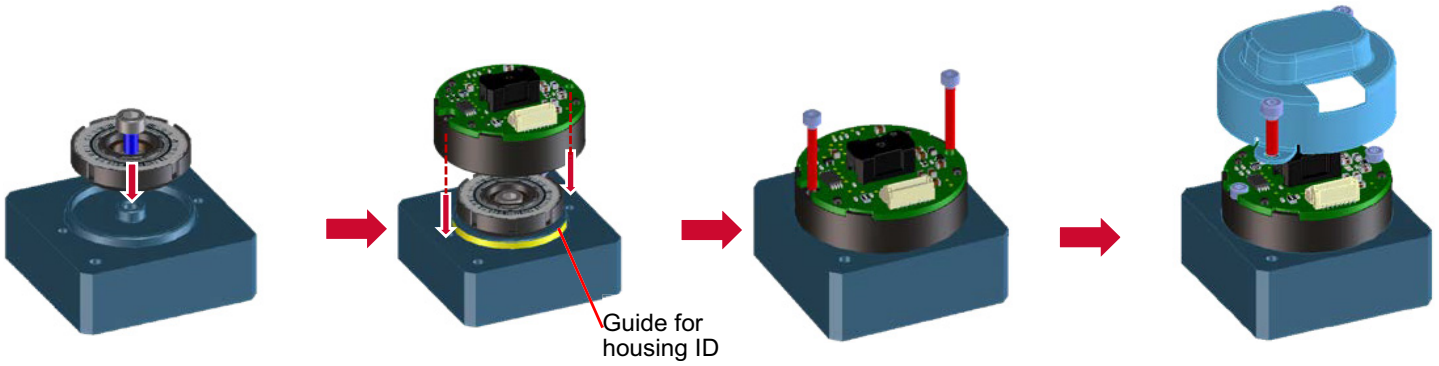


5. Perform electrical signal calibration for both single-turn and multi-turn signals. Optionally, perform the accuracy calibration.

Ready for end applications

NOTE: Applicable for both ST and MT options.

Figure 3: Assembly Guidelines for Mounting Requirement with ID Guiding

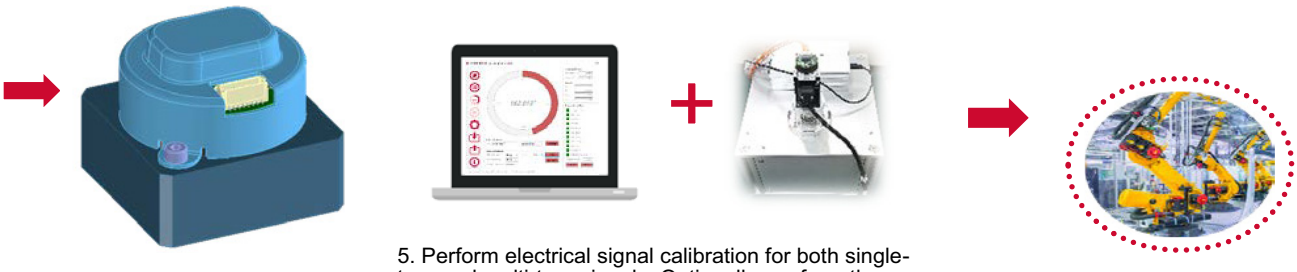


1. Tighten the codewheel hub assembly with M3 thread to the motor shaft.
Recommendations:
a. Apply thread lock.
b. Use M3 austenitic stainless steel class 80; tightening torque is 1.235 Nm to 1.3 Nm.

2. Align the housing ID to the guide on the motor base. Align the 2 screw holes on the housing to the holes on the motor base.

3. Secure the housing with 2x M2 screws.
Recommendations:
a. Apply thread lock.
b. Use M2 stainless steel class 80; the max. tightening torque is 0.285 Nm to 0.3 Nm.

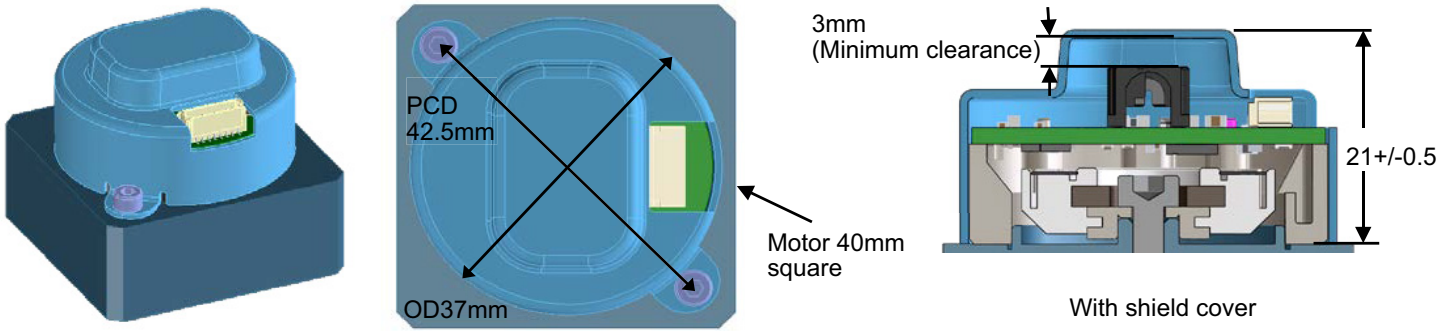
4. Secure the mild steel shield cover with 2x M2.5 screws.
Recommendations:
a. Apply thread lock.
b. Use M2.5 class 12.9, socket head screw; tightening torque is 1.04 Nm to 1.09 Nm.



5. Perform electrical signal calibration for both single-turn and multi-turn signals. Optionally, perform the accuracy calibration.

Ready for end applications

Figure 4: Recommended Shield Cover Dimensions



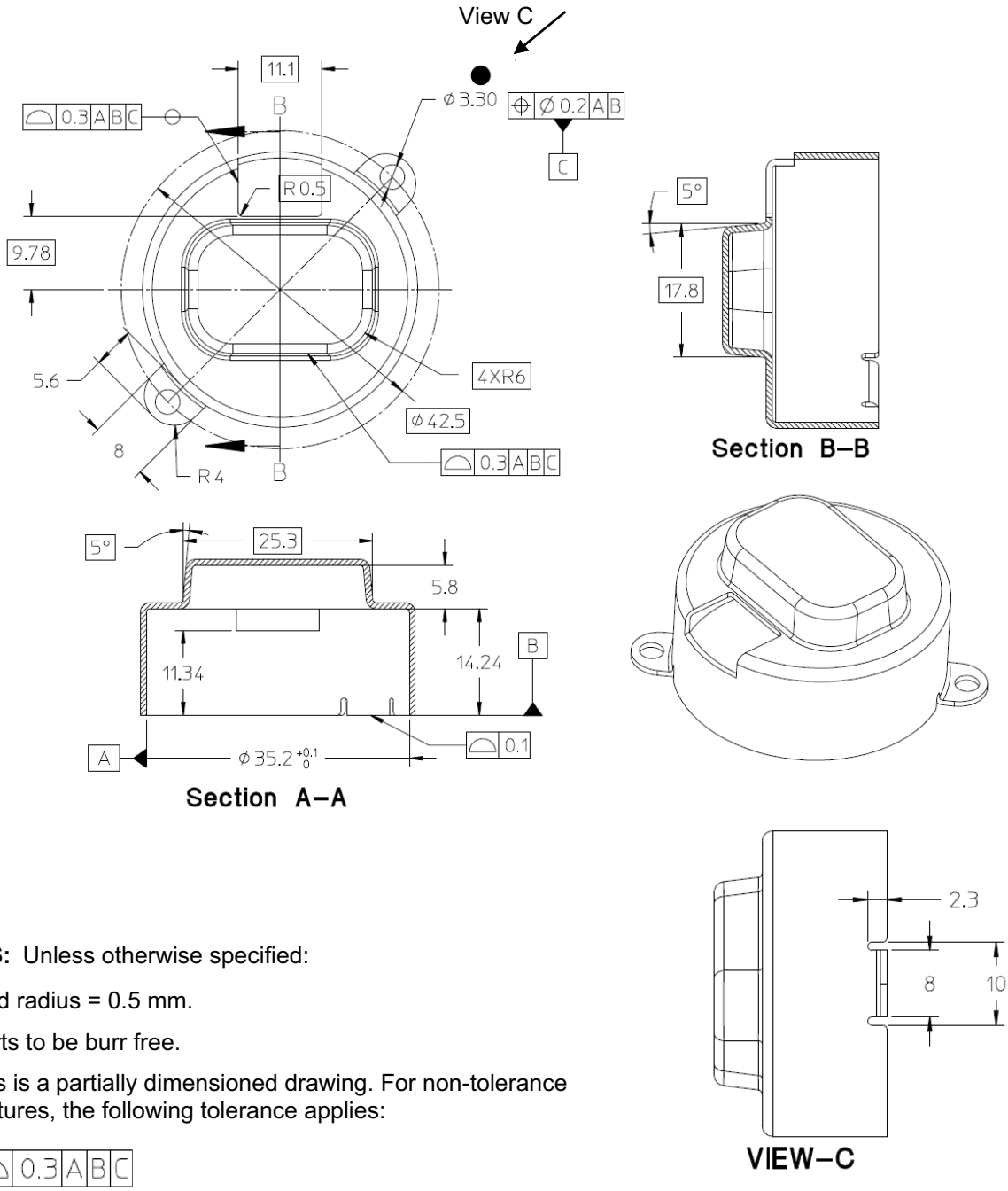
With shield cover

To eliminate or minimize the influence of the external magnetic field interference on encoder operation, use of shielding is mandatory for the AR49-M49M multi-turn options.

Recommended shield cover material: Mild steel SPCC-SD, thickness 0.8 mm (minimum).

Finishing: Ni plating 8 µm to 12 µm thick, with Cu under coating 2 µm to 4 µm.

Figure 5: Shield Cover Reference Design with Inner Diameter Guided Mounting



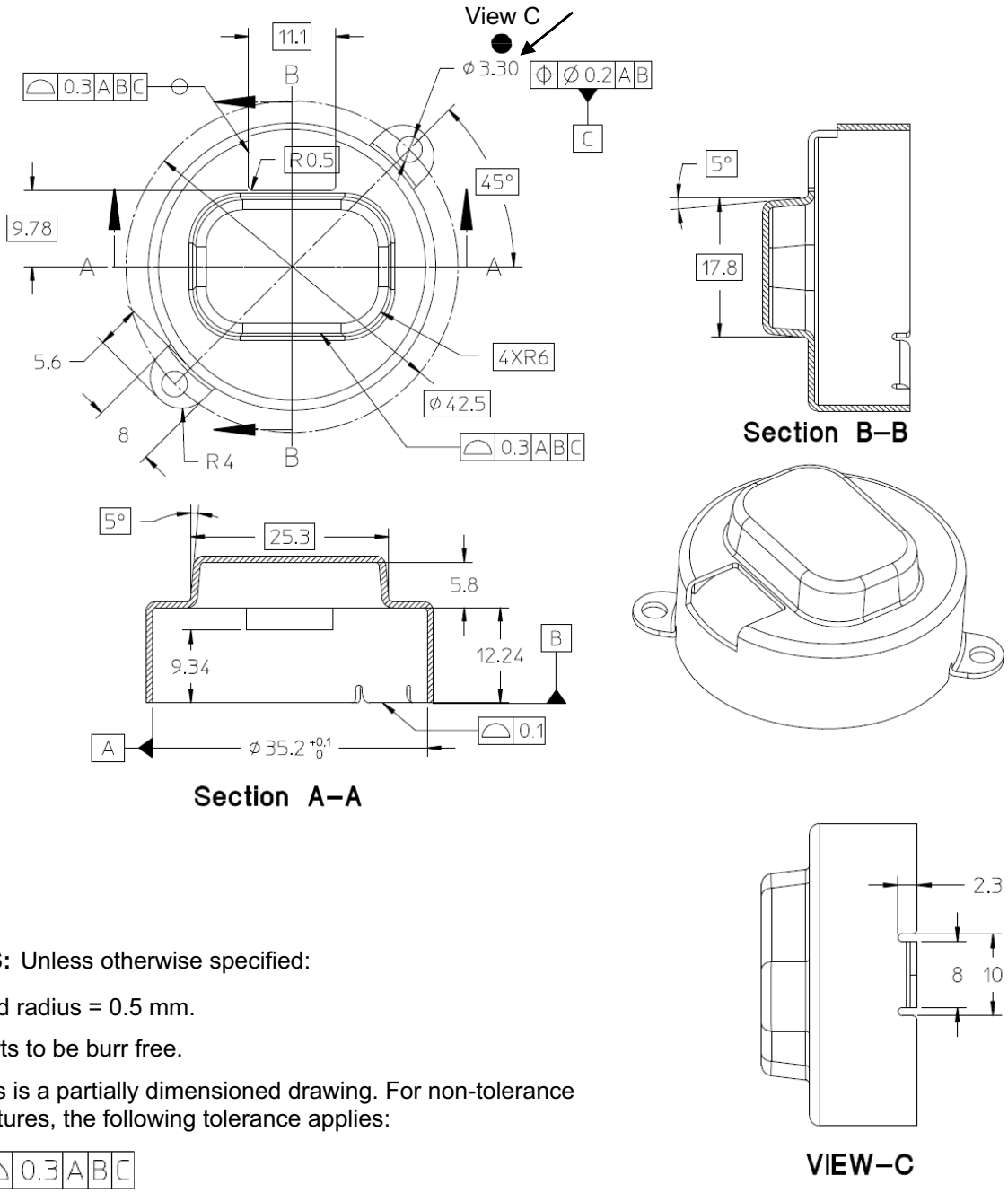
NOTES: Unless otherwise specified:

1. Fold radius = 0.5 mm.
2. Parts to be burr free.
3. This is a partially dimensioned drawing. For non-tolerance features, the following tolerance applies:

   0.3 A B C

4. ● Critical dimensions.

Figure 6: Shield Cover Reference Design with Outer Diameter Guided Mounting



NOTES: Unless otherwise specified:

1. Fold radius = 0.5 mm.
2. Parts to be burr free.
3. This is a partially dimensioned drawing. For non-tolerance features, the following tolerance applies:

   0.3 A B C

4. ● Critical dimensions.

Encoder Memory Area

The AR49 supports 8 kb of user register area. The memory data is kept in a nonvolatile memory. The available register pages and banks are accessible by the user and unlocked.

There are additional register pages reserved for system areas that are protected against accidental writing during operation. The memory data is kept in nonvolatile memories.

Table 1: AR49 Encoder Memory Overview

For SPI/RS485		For BiSS-C		Content
Page	**Address**	**Bank**	**Address**	
0 to 4	0x00	0 to 9	0x00	Nonvolatile Memory (External EEPROM) – User
	::		::	
	0x7E		0x3F	
5	0x00	10 to 11	0x00	Nonvolatile Memory (Internal – Accuracy, Sub-grating Correction, IEC LUT)
	::		::	
	0x7E		0x3F	
6	0x00	12 to 13	0x00	Nonvolatile Memory (Internal – Accuracy, Once-Around Correction, OAC LUT)
	::		::	
	0x7E		0x3F	
7	0x00	14 to 15	0x00	Nonvolatile Memory (Internal) – System-User Area
	::		::	
	0x7E		0x3F	
8	0x00	16 to 17	0x00	Nonvolatile Memory (Internal) – System-Factory Area
	::		::	
	0x7E		0x3F	
9 to 10	0x00	18 to 21	0x00	Fixed Volatile Memory (Registers)
	::		::	
	0x7E		0x3F	
11 to 13	0x00	22 to 27	0x00	Nonvolatile Memory (External EEPROM) – User
	::		::	
	0x7E		0x3F	

SPI/RS485 Memory

- A total of 8 pages with 127 addresses each are allocated for user access.
- The active page numbers are specified in address 0x7F. Page change is done by writing to address 0x7F. The default page after power-on is Page 0.
- Once the page value is changed, allow a time delay of 18 ms.
- Typical EEPROM read time is 200 µs minimum.
- Typical EEPROM write time is 6 ms minimum.
- Page 9 and 10 are volatile memory addresses reserved for encoder system use.

BiSS-C Memory

- A total of 16 banks with 64 addresses each are allocated for user access.
- The active page numbers are specified in address 0x40.
- Bank change is done by writing to address 0x40.
- Banks 18 to 21 are volatile memory addresses reserved for encoder system use.

System Memory for Encoder Configuration

Table 2: Encoder Memory Map for Calibration and Special Commands

BiSS-C			Standard SSI/SPI/RS485			AR49 Registers and Commands							
Bank	Address		Page	Address		Bit							
[dec]	[dec]	[hex]	[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0
	0	00		0	00	Unlock Register Write (ABh)							
	1	01		1	01	Memory Program (C0h)							
	2	02		2	02						Alarm Clear	ST Offset	MT Offset
	3	03		3	03	Factory Reserved (USER Prohibited Access)							
	4	04		4	04							AutoCal_ NoAcc_ En	AutoCal_ Full_En
	5	05		5	05		IEC_ Cal_En	Acc_Cal_ RST	Acc_ Cal2_En	Acc_ Cal1_En	MPhase_ En	MLS_ Vpp_Cal_ En	Inc_Cal_ En
	6	06		6	06				MT_Sync_ En	CMA_ CCW_En	CMA_ CW_En	FeRAM_ Clear	CM_Test_ En
	8	08		8	08						Vwc_ Mon_En	CMA_ Clear_ EN	XC_ Comp_ Clear_En
	9	09		9	09	EHMT Register Byte 0x7							
	10	0A		10	0A	EHMT_ Test_ Mode							
18	11	0B	9	11	0B	Hard Reset Register (A7h)							
	13	0D		13	0D	EHMT Parameter [15:8]							
	14	0E		14	0E	EHMT Parameter [7:0]							
	15	0F		15	0F	EHMT CMD[7:0]							
	34	0x22		34	0x22	Reserved			TempErr	Memory Err	Config Code Err	STErr	MLSErr
	35	0x23		35	0x23	Reserved				Reserved	Reserved	LisErr (IncErr)	LedErr
	40	28		40	28							AutoCal_ Error	Auto_ Cal_ Done
	41	29		41	29	Acc_Cal_ Err	Acc_Cal_ Done	MPhase_ Error	MPhase_ Done	MLS_ Vpp_ Error	MLS_ Vpp_ Done	Inc_Cal_ Error	INC_Cal_ Done
	42	2A		42	2A	EEPROM_ Err					CM_ Test_ Done		
	43	2B		43	2B		CMA_ Busy	CMA_ CCW_ Done	CMA_ CW_ Done	EHMT_ Error	EHMT_ XC_ Alarm	CMA_ Error	

NOTE:

- The memory program command is needed for the system area memory to be effective upon power cycle; applicable for changes to internal memory pages 5 to 8 (banks 10 to 17).
- Perform the memory program command for changes to any of the affected banks before moving to other nonvolatile memory banks.
- Changes will be lost after a power cycle without a memory program command.

Change Memory Page/Bank

1. Write the required page value in hex into Address 0x7F. For example, Data 09h (Go to Page 9) for RS485/SPI.
2. Write the required bank value in hex into Address 0x40. For example, Data 12h (Go to Bank 18) for BiSS-C.

Unlock Register Write

1. Go to Page 9, 0x09 (BiSS-C Bank 18, 0x12).
2. Write address 0x00: Data ABh (unlock Level 1).

Memory Programming

1. Go to Page 9, 0x09 (BiSS-C Bank 18, 0x12).
2. Write address 0x01: Data C0h (page programming).
3. Wait at least 320 ms.
4. Power cycle the encoder.

EHMT Counter Soft Reset

1. Unlock Register Write.
2. Go to Page 9, 0x09 (BiSS-C Bank 18, 0x12).
3. Write address 0x0F: Data 0Fh.

Table 3: Encoder Memory Map for MT Related Data

Standard			BiSS-C			Energy-Harvesting Multi-Turn (EHMT)							
Page	Address		Bank	Address		Bit							
[dec]	[dec]	[hex]	[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0
9	57	39	18	57	39	EHMT Returned Data							
	62	3E		62	3E	EHMT CMA Offset Value [15:8]							
	63	3F		63	3F	EHMT CMA Offset Value [7:0]							
	64	40	19	0	00	EHMT_XC_ERR_Compensation [15:8]							
	65	41		1	01	EHMT_XC_ERR_Compensation [7:0]							
	66	42		2	02	EHMT_ALARM 2 Bytes							
	67	43		3	03								
	68	44		4	04	EHMT Status 2 Bytes							
	69	45		5	05								
	70	46		6	06	EHMT_VWC_DATA 2 Bytes							
	71	47		7	07								

Table 4: EHMT Status and Alarm Registers

BiSS-C			Standard			Energy-Harvesting Multi-Turn (EHMT)							
Bank	Address		Page	Address		Bit							
[dec]	[dec]	[hex]	[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0
19	02	0x02	9	66	0X42							MemErr	MagLO
	03	0x03		67	0x43	VWC Quality	XC_ Error	CMA_ Timeout	VWC_ Timeout	Speed_ VWC	Speed_ CMA	Speed_ MT	MT Error
	04	0x04		68	0x44	Alarm Trigger			DUT Ready				
	05	0x05		69	0x45			Reserved	Reserved	VWC Result Ready	CMA CCW Ready	CMA CW Ready	MT Ready

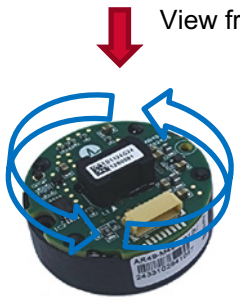
Register Bit for Counting Direction Selection

Table 5: Encoder Counting Direction

Page [Decimal]	Address [hex]	Bit								Default Value
		7	6	5	4	3	2	1	0	
7	20	N/A	Counting Direction	N/A						8'h40h

With the default setting (bit 6 = 0), position data is counting up when rotating in a counter-clockwise direction, as viewed from the top of the encoder.

Figure 7: Default Counting Direction



Position Zero Reset

The encoder zero reset data can be accessed by reading the addresses in Table 6.

Table 6: User Zero-Reset Registers

Page	SPI/RS485 Address		Bank	BiSS-C Address		Bit								Default
[dec]	[dec]	[dec]	[dec]	[hex]	[hex]	7	6	5	4	3	2	1	0	
7	16	10	14	16	10	MT_ZR[23:16]								00h
	17	11		17	11	MT_ZR[15:8]								00h
	18	12		18	12	MT_ZR[7:0]								00h
	19	13		19	13	ST_ZR[24:17]								00h
	20	14		20	14	ST_ZR[16:9]								00h
	21	15		21	15	ST_ZR[8:1]								00h

Auto Zero-Reset (Single-Turn Position)

When the codewheel/hub is stationary, execute the ST Reset command so that the single-turn position output value will be reset to the zero value.

1. Option 1 with memory bit setting:
   a. Unlock Register Write.
   b. Write Page 9/Bank 18, Address 0x02[1] = 1b.
2. Option 2 with the dedicated zero reset commands for the RS485, SPI or BiSS-C protocols.

Auto Zero-Reset (Multi-Turn Counter Output)

1. Option 1 with memory bit setting:
   a. Unlock Register Write.
   b. Write to Page 9/Bank 18, Address 0x02[0] = 1b.
2. Option 2 with the dedicated multi-turn zero reset commands for the RS485, SPI or BiSS-C protocols.

The multi-turn value will be reset to the zero value when this command is completed.

Multi-Turn and Single-Turn Absolute Resolution Setting

Select the configuration for the absolute position output by updating the Page 7/Bank 14 Address 0x16, see Table 7 and Table 8.

1. Unlock Register Write.
2. Write in the new settings at Page 7/Bank 14, read back to ensure the setting is written successfully.
3. Program memory.

Table 7: Multi-Turn and Single-Turn Bits Setting Description for SPI/SSI/BiSS-C Protocols

Page (SPI/SSI)	Bank (BiSS-C)	Address	Bits	Name	Settings	SPI/SSI 25-Bit Output
0x07	0x0E	0x16	7	Reserved	x	N/A
			6:4	MT_Select [2:0]	000	0
					001	12
					010	14
					011	16
					100	18
					101	20
					110	22
					111	24
			3:0	ST_Select [3:0]	0000	15
					0001	16
					0010	17
					0011	18
					0100	19
					0101	20
					0110	21
					0111	22
					1000	23
					1001	24
					101x	25
					11xx	25

NOTE: For ST only option, the MT selection is defaulted to binary 000.

Table 8: Multi-Turn and Single-Turn Bits Setting Description for RS485 Protocols

Page	Address	Bits	Name	Settings	RS485 24 Bits ST Output	RS485 25 Bits ST Output
0x07	0x16	7	Reserved	x	N/A	N/A
		6:4	MT_Select [2:0]	000	0	0
				001	12	12
				010	14	14
				011	16	16
				100	18	N/A
				101	20	
				110	22	
				111	24	
		3:0	ST_Select [3:0]	0000	17	15
				0001	18	16
				0010	19	17
				0011	20	18
				0100	21	19
				0101	22	20
				0110	23	21
				0111	24	22
				1000	N/A	23
				1001		24
				1010		25

Encoder Error and Warning Setting

To enable the Error or Warning bits in the ALMC field, set the respective bit to 1, disable 0.

Table 9: Error and Warning Bits Configuration Addresses

Page	Address [hex]	Bit								Default Value
		7	6	5	4	3	2	1	0	
7	30	Alarm Enable [31:24]								1Fh
	31	Alarm Enable [23:16]								FFh
	32	Alarm Enable [15:8]								1Bh
	33	Alarm Enable [7:0]								0Fh
	34	Alarm Latch Enable [31:24]								1Fh
	35	Alarm Latch Enable [23:16]								FFh
	36	Alarm Latch Enable [15:8]								0Bh
	37	Alarm Latch Enable [7:0]								0Eh

Table 10: AR49 Alarm Bits Assignment

Alarm Bits							
31	30	29	28	27	26	25	24
Reserved			MT Sync Error	Reserved	MT Protocol Err	Reserved	
23	22	21	20	19	18	17	16
Reserved		XCErr	Reserved	EHMT Counter Err[9:3]	EHMT Counter Err[2]	EHMT Counter Err[1]	EHMT Counter Err[0]
15	14	13	12	11	10	9	8
Reserved			TempErr	Memory Err	Reserved	STErr	MLSErr (McodeErr)
7	6	5	4	3	2	1	0
Reserved						LisErr (IncErr)	LEDErr

SPI4 Error or Warning Readout and Descriptions

For SPI4 protocol option, send the operation command (OC) 0x9Ch to perform error or warning bits readout. To perform segregation between Error or Warning bits, see the AR49 alarm bits settings in Table 10. Enable the Error or Warning bits in the operation command (OC) 0x9Ch by setting the respective bit to 1. Conversely, setting a bit to 0 will disable the particular bit.

Table 11: SPI4 Protocol Error and Warning Bits Masking Assignment

Page	Address [hex]	Bit								Default Value
		7	6	5	4	3	2	1	0	
7	28	SPI4 Warning Mask [31:24]								00h
	29	SPI4 Warning Mask [23:16]								10h
	2A	SPI4 Warning Mask [15:8]								10h
	2B	SPI4 Warning Mask [7:0]								03h
	2C	SPI4 Error Mask [31:24]								1Fh
	2D	SPI4 Error Mask [23:16]								EFh
	2E	SPI4 Error Mask [15:8]								0Bh
	2F	SPI4 Error Mask [7:0]								0Ch

Encoder Alarm Definition

The following table shows the encoder alarm bits and their definition across all protocol options.

Table 12: AR49-M49M and AR49-M25S General Encoder Alarms and Definition Table

Alarms	Alarms Definition	Check Frequency
TempErr	Temperature Error. To indicate the temperature exceeds the maximum preset limit. ■ 1: Temperature above preset limit. ■ 0: Temperature below preset limit.	Every 90 ms
Memory Err	MEM Error (Memory Error). To indicate if loading of internal and external EEPROM contents upon encoder power up is successful. ■ 1: Failure to access EEPROM memory data/or there is a checksum error in the memory. ■ 0: Normal operation, no EEPROM memory access error	Upon power-up and memory read
STErr	Single-turn Counting Error. To check the integrity of ST position. ■ 1: Error in Absolute (MLS) code or MLSErr flag has triggered. ■ 0: Normal operation, no error in single-turn position.	Per ADC sample
MLSErr (McodeErr)	To detect error in MLS code generation. ■ 1: MLS code error. ■ 0: MLS code good.	Per ADC sample
LisErr (IncErr)	Lissajous (Incremental) Error. A measure of integrity of ADC Sin & Cos signals by means of Lissajous specifications. ■ 1: Lissajous out of specification. ■ 0: Lissajous within specification.	Per ADC sample
LEDErr	LED Error. To indicate if LED current is out of operating range. ■ 1: LED out of operating range. ■ 0: LED within operating range.	Continuous detect

Table 13: AR49-M49M Encoder Multi-Turn Alarms and Definition Table

Alarms	Alarms Definition	Check Frequency
MT Sync Error	EHMT Sync Error. To detect wrong MT counting during MT counter synchronization. ■ 1: Error in multi-turn synchronization. ■ 0: No error in multi-turn synchronization.	Upon MT synchronization
MT Protocol Error	To detect an MT encoder protocol error – energy harvesting (Wiegand). ■ 1: MT encoder protocol error. ■ 0: No MT encoder protocol error.	Per MT encoder polling
XCErr	To indicate an MT encoder miscount by comparing the EHMT counter vs. the MT software counter. ■ 1: EHMT: Miscount or XCERR value overflow. ■ 0: No MT miscount.	Each time ST rolls over

Table 13: AR49-M49M Encoder Multi-Turn Alarms and Definition Table (Continued)

Alarms	Alarms Definition	Check Frequency
EHMT Counter Err[9:3]	MT Counter Error. To detect error receive from EHMT counter. ■ 1: EHMT Counter Error Bits [9:3] triggers. ■ 0: No EHMT counter errors.	Per MT encoder polling
EHMT Counter Err[2]	MT Counter Error. To detect Error receive from EHMT counter. ■ 1: EHMT Counter Error Bit[2] triggers. ■ 0: No EHMT Counter Errors	Per MT encoder polling
EHMT Counter Err[1]	MT Counter Error. To detect error receive from EHMT counter. ■ 1: EHMT Counter Error Bit[1] triggers. ■ 0: No EHMT counter errors.	Per MT encoder polling
EHMT Counter Err[0]	MT Error. To detect error on reading MT Hardware counter value or I^2C communication error. ■ 1: Error in MT position reading, the EHMT Counter Error Bit[0] triggers. ■ 0: No error in MT position reading.	Per MT encoder polling
MT Counter Error	MT Counter Error. To detect Error bit received from the EHMT Counter Error register. ■ 1: Any of the EHMT Counter Err[9:1] bit triggers. ■ 0: No EHMT counter error.	Per MT encoder polling
MT Error	MT Error for BiSS-C and RS485 Protocols. To detect error on reading MT hardware counter value or I^2C communication error. Same as the EHMT Counter Error Bit[0] triggers.	Per MT encoder polling

Table 14: AR49-M49M EHMT Counter Error Register Definition

EHMT Counter Error Bit	Name	EHMT Counter Error[9:0] Description
0	MT Error	Error occurs on reading hardware multi-turn value or I^2C stuck.
1	Speed_MT	Motor exceeds 15000RPM for MT synchronization.
2	Speed_CMA	Motor exceeds 200RPM for CMA calibration.
3	Speed_VWC	Motor exceeds speed limit for VWC monitoring.
4	VWC_Timeout	Less than 700 VWC pulses detected within 90 seconds.
5	CMA_Timeout	VWC pulses not detected within 10 seconds.
6	Counter XC_Error	Continuous miscount for 5 revolutions.
7	VWC Quality	VWC voltage less than 4.0V.
8	MT_MagLO	MT Counter ASIC detects no or low magnetic field.
9	MT_MemErr	FeRAM related error.

Alarm Clear:

1. Option 1 with memory bit setting
   a. Unlock Register Write.
   b. Write to Page 9/Bank 18, Address 0x02[2] = 1b.
2. Option 2 with Alarm Clear Command of the respective RS485, SPI, or BiSS-C protocols.

Temperature Sensor

For the setting of temperature values and alarms, the configuration is as listed in Table 15. The temperature upper limit is defaulted to 0x7D, which is 125°C, referenced to the ambient temperature as measured by the AR49 encoder ASIC. The encoder temperature readout bit, which is an example of the data as 2's complement, is listed in Table 17.

Table 15: SSI/SPI/RS485 Temperature Sensor Setting

SSI/SPI/RS485			Temperature Sensor								Default [hex]
Page	Address		Bit								
[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0	
7	2	02	Temperature Upper Limit Offset [7:0]								00h
	3	03	Temperature Offset [7:0]								00h
	4	04	Temperature Upper Limit [7:0]								7Dh
	5	05	Temperature Output Data (Read only register)								—

Table 16: BiSS-C Temperature Sensor Setting

BiSS-C			Temperature Sensor								Default [hex]
Bank	Address		Bit								
[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0	
14	2	02	Temperature Upper Limit Offset [7:0]								00h
	3	03	Temperature Offset [7:0]								00h
	4	04	Temperature Upper Limit [7:0]								7Dh
	5	05	Temperature Output Data (Read only register)								—
—	117	75	Temperature Output Data (Read only register)								—
	73	49						Temp. Alarm			0

Table 17 is an example based on an initial alarm (Page 7/Bank 14, Address 0x04) setting of 125°C. The temperature offset can be a positive or negative value.

Table 17: Temperature Sensor Offset Setting Example

Case	Temperature Sensor Offset Register	0x02	0x03	0x04	0x05	Remarks	
	Offset Value (Decimal)	Temperature Upper Limit Offset (hex)	Temperature Offset (hex)	Temperature Upper Limit (hex)	Temperature Output (Dec)	Raw Temperature without Offset (Dec)	Alarm Trigger
1	0	0	0	7D	124	124	No
					125	125	Yes
					126	126	Yes
2	10	0A	0A	7D	124	114	No
					125	115	Yes
					126	116	Yes

Table 17: Temperature Sensor Offset Setting Example (Continued)

Case	Temperature Sensor Offset Register	0x02	0x03	0x04	0x05	Remarks	
	Offset Value (Decimal)	Temperature Upper Limit Offset (hex)	Temperature Offset (hex)	Temperature Upper Limit (hex)	Temperature Output (Dec)	Raw Temperature without Offset (Dec)	Alarm Trigger
3	–1	0	FF	7D+01	124	125	No
					125	126	Yes
					126	127	Yes
4	–10	0	F6	7D+0A	124	134	No
					125	135	Yes
					126	136	Yes

NOTE:

- Case 1: No offset scenario.
- Case 2: If the temperature offset (Address 0x03) is a positive value, the temperature upper limit offset (Address 0x02) is also set to the same value.
- Case 3: If the temperature offset (Address 0x03) is a negative value, the absolute value of this value must be added to the default temperature upper limit (Address 0x04).
- Case 4: Another negative offset value example.
- The register addresses are at SPI/RS485 Page 7 or BiSS-C Bank14.

Table 18: Temperature Sensor Data

Temperature	TEMP[7:0]
–64	1100 0000
–50	1100 1110
–20	1110 1100
–1	1111 1111
0	0000 0000
1	0000 0001
10	0000 1010
25	0001 1001
50	0011 0010
85	0101 0101
127	0111 1111
159	1001 1111
191	1011 1111

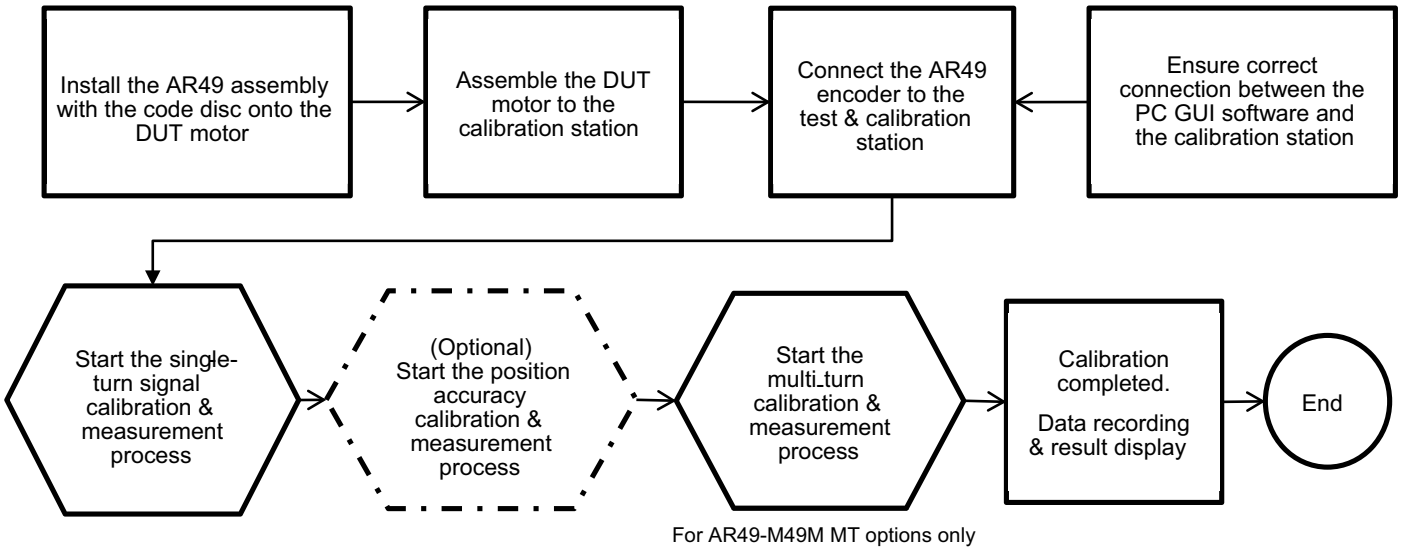
NOTE:

- The minimum support range for temperature output is –64°C.
- The negative values are from –1°C to –64°C only.
- The maximum positive value is 191°C.
- The temperature readout is found by accessing memory register at Page 7 Address 0x05 (see Table 15).
- For BiSS-C, the temperature readout is found by accessing the memory register at Address 0x75 (see Table 16).
- When reading using RS485-24-Bit format Command ID4 as per Table 39, the temperature data (TEMP) is available as the DF_7.

Encoder Calibration

The Broadcom encoder employs an intelligent calibration method by performing an auto signal optimization once the encoder is mounted within assembly tolerances. This eliminates the hassle of mechanically adjusting the encoder position to a very tight gap and mechanical center.

Figure 8: Encoder Signal Optimization and Accuracy Calibration Flow



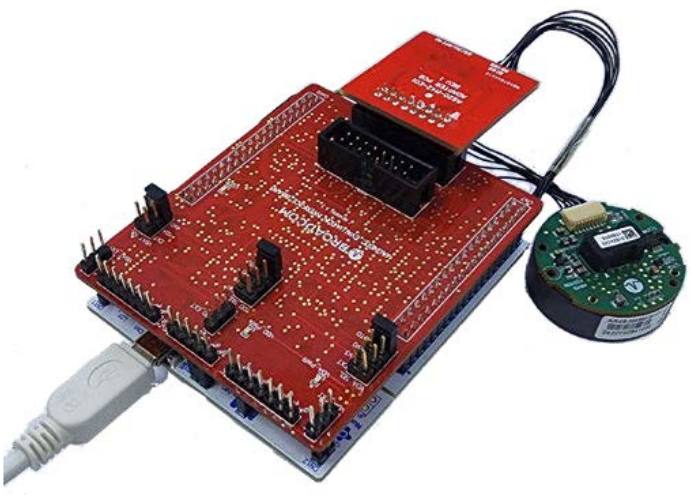
Upon completion of the encoder assembly to the motor, perform the calibration process as follows:

1. Connect the AR49-M49-E01 programming and calibration kit to a computer via USB connection.
2. Connect encoder cable-end to encoder.
3. Follow the required steps to complete the ST and MT calibrations.
4. Update any user-specific configurations after calibration is completed.
5. The encoder is ready to use.

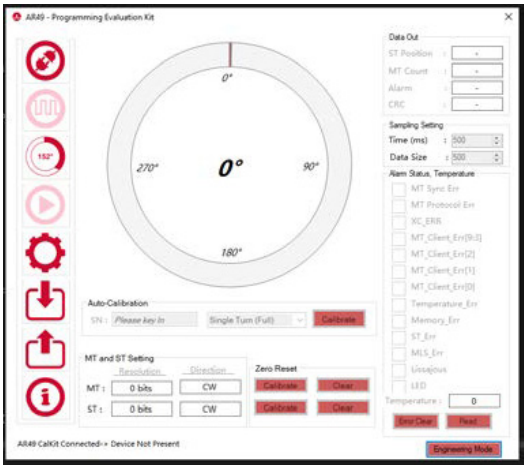
NOTE:

- If the calibration continues to fail after consecutive trials, confirm the encoder codewheel and module installation again by referring to the codewheel and encoder mounting requirements and guidelines.
- Clear the ST and MT offset registers to all zeros before starting the ST and MT calibration process.

Figure 9: Example of the AR49-M49-E01 Calibration Kit and Its User Interface Software



The Programming/Calibration Kit with a USB PC Interface Cable and an Encoder Connecting Cable



The Programming/Calibration GUI Software

ST Angular Position Accuracy Correction

Figure 10: Accuracy Correction with Reference Encoder Using the AR25-AC25 Calibration Station

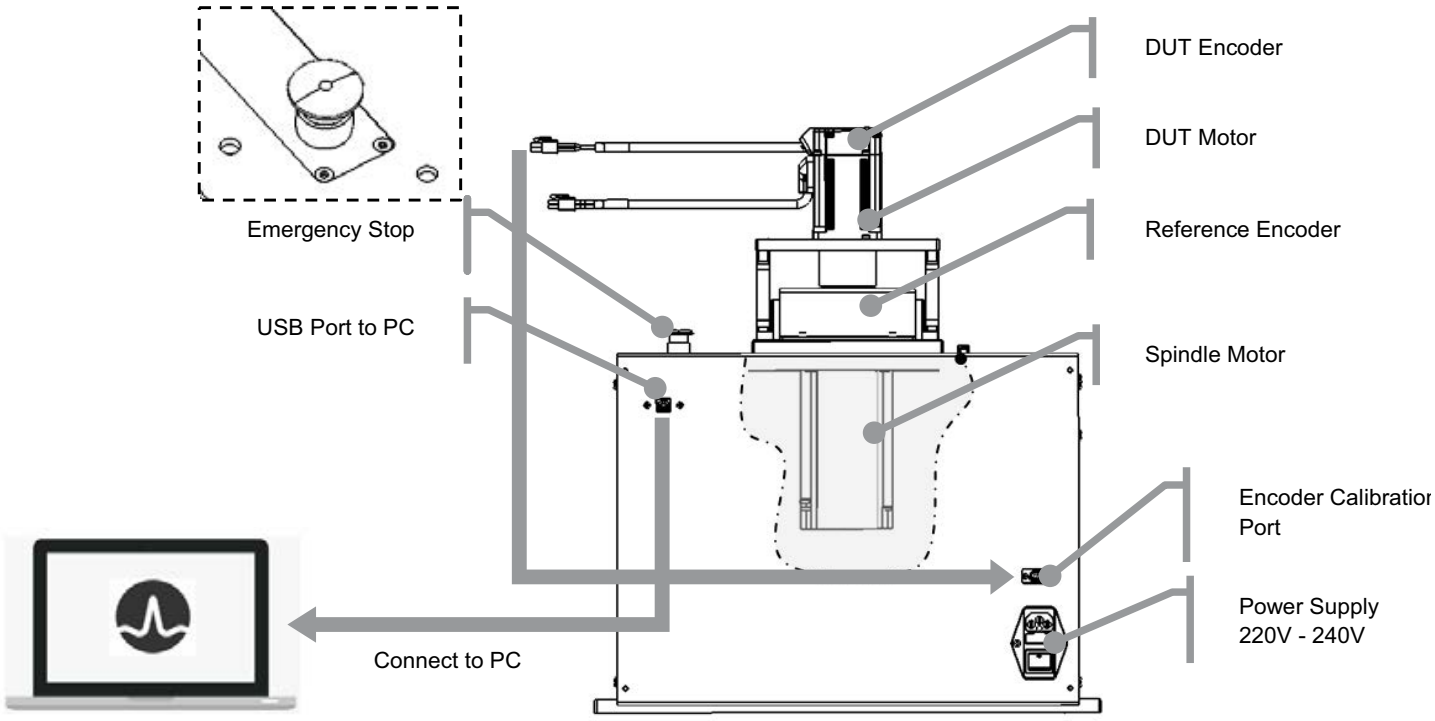
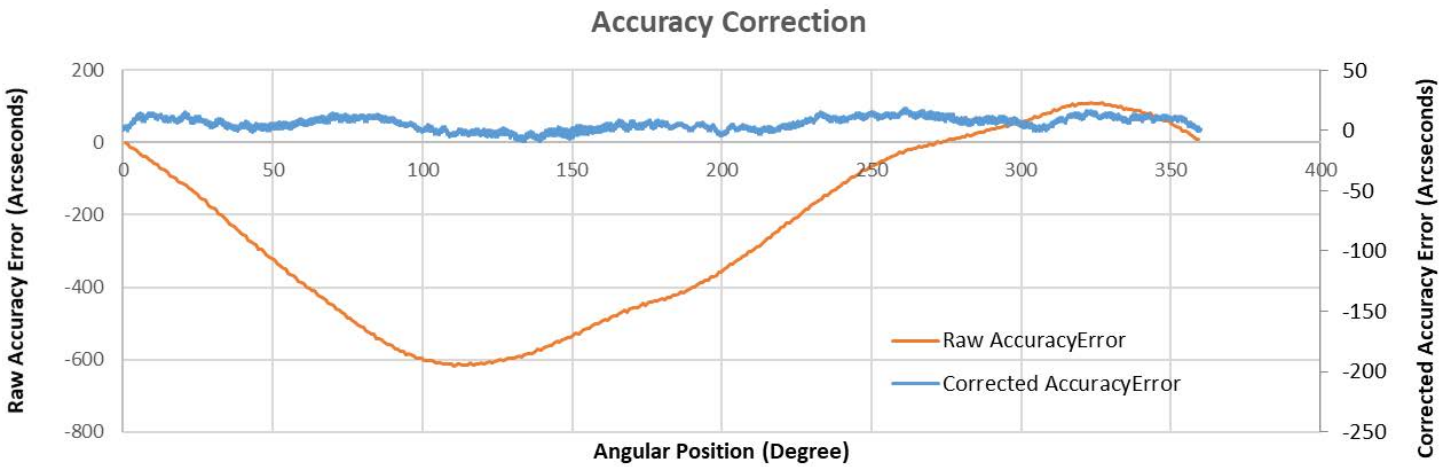


Figure 11: Example of the Position Accuracy Error Before and After Correction



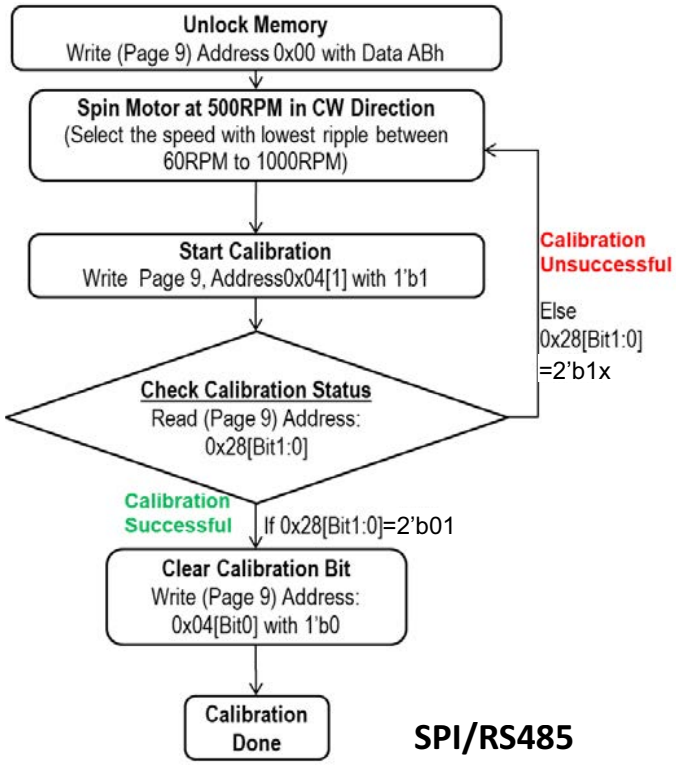
ST Calibration of the AR49-M49M/M25S Encoders

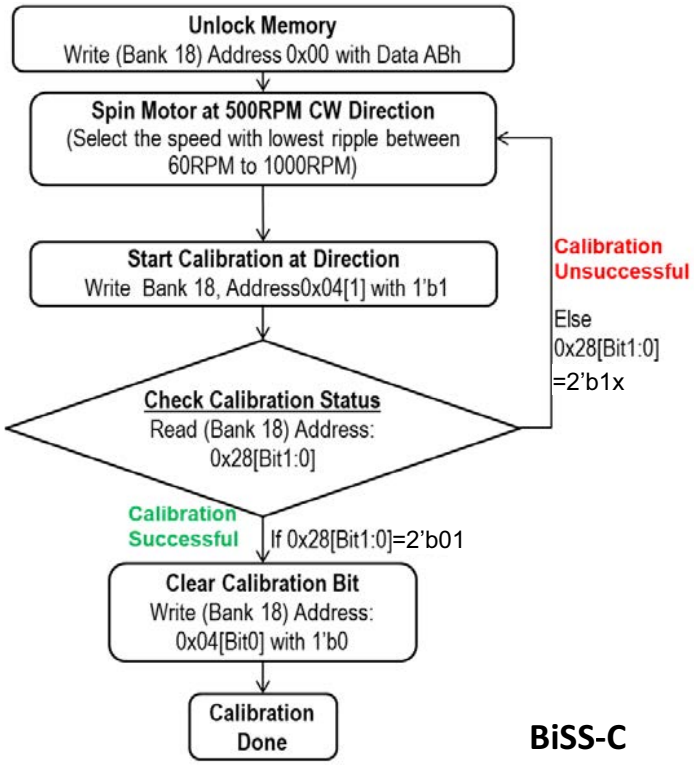
ST Auto-Calibration without Accuracy Correction

The position accuracy correction table will not be updated. The other signals' calibration after assembly will be performed. It is recommended to perform this calibration option unless the spindle motor (to drive the AR49 + motor assembly) can fulfill the low-speed ripple requirements for accuracy correction.

1. Unlock memory (Write Page 9/Bank 18, Address 0x00 = ABh).
2. Spin the spindle motor in a clockwise (CW) direction at a fixed constant speed. It is recommended to be within 60 rpm to 1000 rpm. Wait for the motor speed to be stable before starting the next step.
3. Write Page 9/Bank 18, Address 0x04[1] = 1b1.
4. Loop reading calibration status at Address 0x28.
5. If Address 0x28[1:0] = 00b, the calibration is in progress. Otherwise, if the value is 01b, the calibration is done; or if the value is 1xb, there is a calibration error and the calibration is not successful.
6. Clear the calibration register, Address 0x04 = 00h. If unsuccessful, repeat Steps 3 to 5 (repeat up to 10 times).
7. Check the assembly of the codewheel and encoder for any abnormality if calibration is not successful.

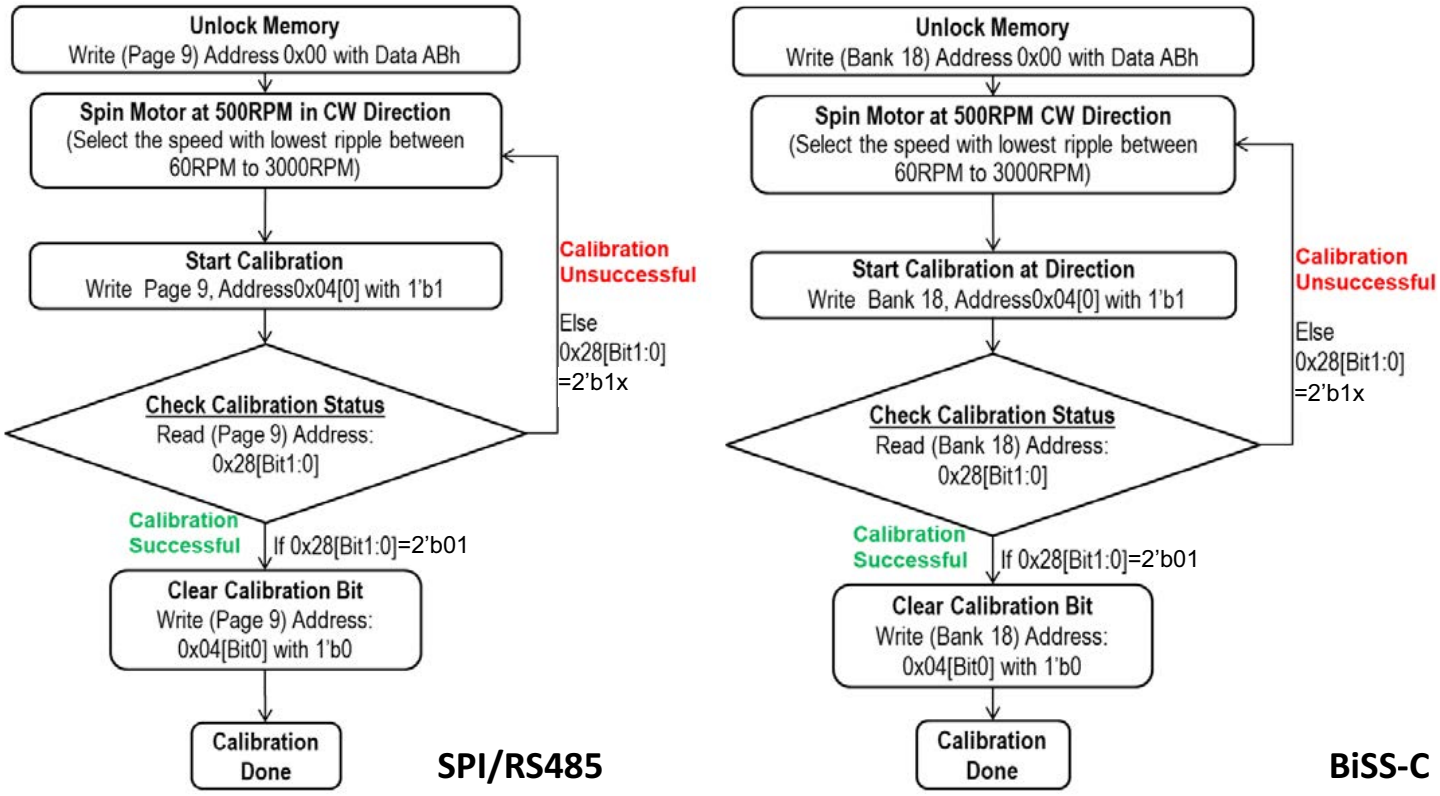
Figure 12: Flowchart for Full Auto-Calibration Process without Accuracy Correction





Full ST Auto-Calibration with Accuracy Correction Enabled

Figure 13: Flowchart for Full Auto-Calibration Process



Calibrate in Clockwise (CW) Direction

1. Unlock memory (Write Page 9/Bank 18, Address 0x00 = ABh).
2. Spin the spindle motor in a CW direction at a fixed constant speed within 60 rpm to 3000 rpm (it is recommend to select the least ripple speed, not to exceed 5000 rpm). Wait for the motor speed to be stable before starting the next step.
3. Write Page 9/Bank 18, Address 0x04[0] = 1b.
4. Loop reading calibration status at Address 0x28.
5. If Address 0x28[1:0] = 00b, the calibration is in progress. Otherwise, if the value is 01b, the calibration is done; or if the value is 1xb, there is a calibration error and it is not successful.
6. Clear the calibration register, Address 0x04 = 00h. If unsuccessful, repeat Steps 3 to 5 (repeat up to 10 times).
7. Check the assembly of the codewheel and encoder for any abnormality if calibration is not successful.

CAUTION! Only calibrate the encoder with the full auto-calibration mode with accuracy correction when the assembled AR49 encoder is being driven by a highly stable servo motor; for example, controlled to the speed of 1000 rpm ± 0.2%, or better.

CAUTION! The ST offset register has to be cleared to all zeros before this calibration process that involves generating the accuracy correction look-up table (LUT).

ST Position Code Monotony Measurement

The AR49 encoder has a built-in function to measure and monitor the code monotony of the ST position data. This step is not mandatory but provides a way to verify that the position output after calibration is normal without any sudden shift in position data. The code monotony value is measured as a 23-bit ST step at every 10-ns interval. The readout value is in 2's complement.

1. Unlock memory (Write Page 9/Bank 18, Address 0x00 = ABh).
2. Enable the code monotony measurement by writing Page 9/Bank 18, Address 0x06 = 01h.
3. Spin the spindle motor in a CW direction for >3 revolutions at a low speed, for example, 2 rpm to 60 rpm.
4. Read Page 9, Address 0x4F to 0x52 for the measured data. For BiSS-C, read Bank 19, Address 0x0F to 0x12.
5. End the code monotony measurement by writing Page 9/Bank 18, Address 0x06 = 00h.
6. Stop the motor. Repeat Steps 2 to 5 in a counter-clockwise (CCW) direction.

Figure 14: Code Monotony Self-Test Flowchart

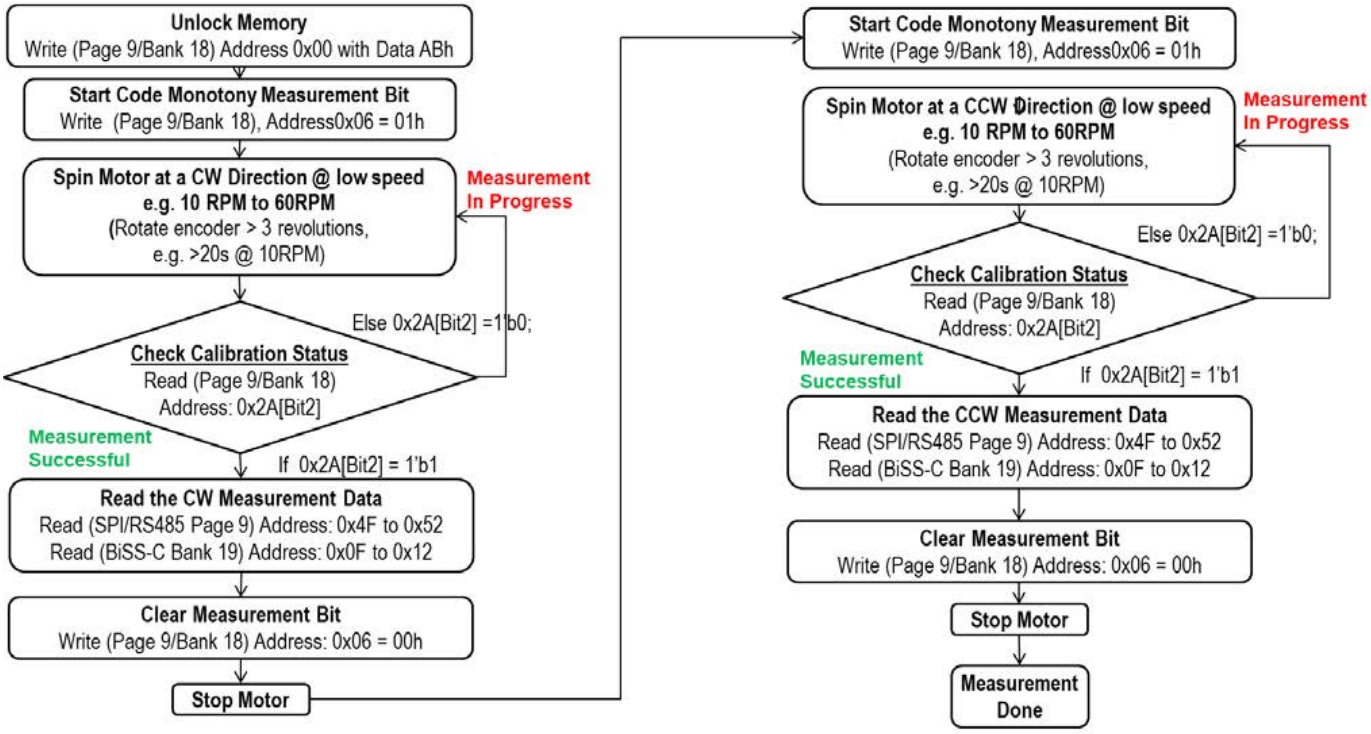


Table 19: Code Monotony Measurement Registers

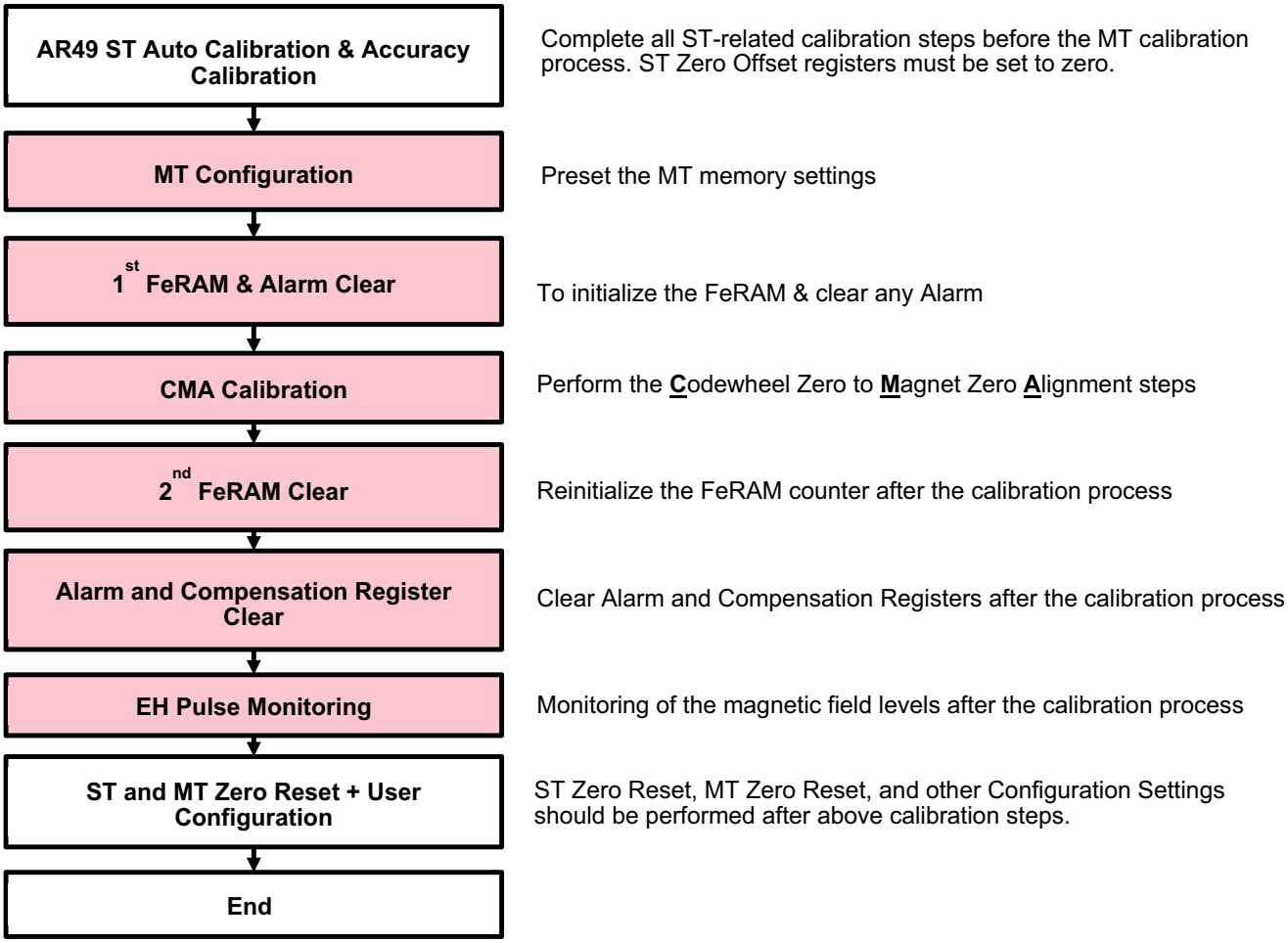
RS485	Address		BiSS-C	Address		Bit							
Page [dec]	[dec]	[hex]	Bank [dec]	[dec]	[hex]	7	6	5	4	3	2	1	0
9	6	06	18	6	06								CM_Test_En
	79	4F	19	15	0F	CM_Max[15:0]							
	80	50		16	10								
	81	51		17	11	CM_Min[15:0]							
	82	52		18	12								

Multi-Turn Calibration of the AR49-M49M Encoders

MT Calibration

For the MT option of the AR49-M49M encoders, it is compulsory to perform the MT calibration procedures after the encoder has been assembled. For the optimum results, the shield should also be assembled during this process.

Figure 15: AR49-M49M Encoder MT Calibration Flow



Pre-Set the MT Memory Settings

1. Motor condition: Static.
   a. Unlock Register Write.
   b. Write Address 0x7F to Data 09h (go to Page 9) or for BiSS-C: Write Address 0x40 to Data 12h (go to Bank 18).
   c. Write Address 0x00 to Data ABh (unlock level 1).
2. Trigger MT counter soft reset.
   a. Write Address 0x0F to Data 0Fh (trigger MT counter soft reset command). Wait 20 ms.
3. Set default MT configuration.
   a. Write Address 0x0A to Data 80h (MT counter test mode, Bit 7 set to High).

Table 20: MT Calibration Command and Related Registers

Standard SSI/SPI/ RS485			BiSS-C			Key AR49 Registers/Commands							
Page	Address		Bank	Address		Bit							
[dec]	[dec]	[hex]	[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0
9	6	06	18	6	06					CMA_ CCW_En	CMA_ CW_En	FeRAM_ Clear	
	08	08		08	08						VWC_ Trigger		XC_ Comp_ Clear
	10	0A		10	0A	MT_Test_ Mode							
	15	0F		15	0F	MT Counter Command[7:0]							
	43	2B		43	2B	MT_ Protocol_ Error	CMA_ Busy	CMA_ CCW_ Done	CMA_ CW_ Done	MT_ Counter_ Error	MT_ Counter_ Alarm	CMA_ Error	MT_ Sync_ Error
	48	30		48	30		MT[38:32]						
	49	31		49	31	MT[31:24]							
	50	32		50	32	MT[23:16]							
	51	33		51	33	MT[15:8]							
	52	34		52	34	MT[7:0]							
	62	3E		62	3E	CMA_Offset[15:8]							
	63	3F		63	3F	CMA_Offset[7:0]							
	66	42	19	2	02							MT_ MemErr	MT_ MagLO
	67	43		3	03	VWC Quality	XC_ Error	CMA_ Timeout	VWC_ Timeout	Speed_ VWC	Speed_ CMA	Speed_ MT	MT Error
	68	44		4	04	Alarm Trigger			DUT Ready				
	69	45		5	05			Reserved	Reserved	VWC Result Ready	CMA CCW Ready	CMA CW Ready	MT Ready
	70	46		6	06	EH Pulse VWC data; Average – 4 Sigma							
	71	47		7	07	EH Pulse VWC data – Mean							

First FeRAM and Alarm Clear

1. Motor condition: Static.
2. Unlock Register Write.
3. Trigger MT counter soft reset.
4. Set default MT configuration.
5. FeRAM clear.
   a. Write Address 0x06 to Data 02h (FeRAM clear command, Bit 1 set to High).
6. Read back 39 bits of the FeRAM MT value.
   a. Read back 39 bits value from Page 9/Bank 18 Address 0x30 to 0x34,
   b. Confirm its value is 0 ± 1 revolution.

Codewheel Zero to Magnet Zero Alignment (CMA) Calibration

1. Motor condition: Spin 100 rpm in the CW direction.
2. Unlock Register Write.
3. Trigger MT counter soft reset.
4. Set default MT configuration.
5. CMA clock wise calibration.
   a. Write Address 0x06 to Data 04h.
   b. Wait for at least 1.2 seconds (2 revolutions at the speed of 100 rpm).
   c. Read Address 0x2B. Expected data return 10h.
6. Motor condition: Spin 100 rpm in the CCW direction.
7. CMA counter clockwise calibration.
   a. Write Address 0x06 to Data 0Ch.
   b. Wait for at least 1.2 seconds (2 revolutions at the speed of 100 rpm).
   c. Read Address 0x2B. Expected data return 30h.
8. CMA completed. AR49 will automatically program the CMA value into the memory.
9. Power cycle and read back the AR49 CMA value and confirm it has been set.
   a. Read Address 0x3E and 0x3F. Expected data returned not equal to 00h.

Figure 16: CMA Calibration Direction Definition

Shaft/Bottom View

PCBA/Top View

Clockwise direction when looking toward the encoder shaft-end

Table 21: CMA Calibration Command and Related Registers

Standard SSI/SPI/ RS485			BiSS-C			Key AR49 Registers/Commands							
Page	Address		Bank			Bit							
[dec]	[dec]	[hex]	[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0
9	6	06	18	6	06					CMA_ CCW_En	CMA_ CW_En		
	10	0A		10	0A	MT_ Test_ Mode							
	43	2B		43	2B	MT_ Protocol_ Error	CMA_ Busy	CMA_ CCW_ Done	CMA_ CW_ Done	MT_ Counter_ Error	MT_ Counter_ Alarm	CMA_ Error	MT_ Sync_ Error
	62	3E		62	3E	CMA_Offset [15:8]							
	63	3F		63	3F	CMA_Offset [7:0]							

Second FeRAM Clear

1. Motor condition: Move 1 revolution, and then stop at AR49 ST position ~90 degrees.
2. Unlock Register Write.
3. Trigger MT counter soft reset.
4. Set default MT configuration.
5. FeRAM clear.
   a. Write Address 0x06 to Data 02h (FeRAM clear command, Bit-1 set to High).
6. Read back 39 bits of FeRAM MT value.
   a. Read back 39 bits value from Page 9/Bank 18 Address 0x30 to 0x34.
   b. Confirm that its value is 0 ± 1 revolution.

Table 22: EHMT Cross-Check Error Compensation and Related Registers

Standard SSI/SPI/ RS485			BiSS-C			Key AR49 Registers/Commands							
Page	Address		Bank	Address		Bit							
[dec]	[dec]	[hex]	[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0
9	08	08	18	08	08								XC_ Comp_ Clear
	34	22		34	22	Reserved			Temp_ Err	Mem_ Err	Config Code Err	STErr	MLS_ Err
	35	23		35	23	Reserved						Lis_Err	LED_ Err
	64	40	19	0	00	EHMT_XC_ERR_Compensation [15:8]							
	65	41		1	01	EHMT_XC_ERR_Compensation [7:0]							
	66	42		2	02	Reserved						MT_ MemErr	MT_ MagLO
	67	43		3	03	VWC Quality	XC_ Error	CMA_ Timeout	VWC_ Timeout	Speed_ VWC	Speed_ CMA	Speed_ MT	MT Error
	68	44		4	04	Alarm Trigger	Reserved		DUT Ready	Reserved			
	69	45		5	05	Reserved				VWC Result Ready	CMA CCW Ready	CMA CW Ready	MT Ready

Alarm and Compensation Register Clear

1. Motor condition: Static.
2. Unlock Register Write.
3. Execute XC_ERR compensation clear command as follows:
   a. Write Address 0x08 to Data 01h (XC compensation clear command)
4. Alarm clear.
   a. Write Address 0x02 to Data 04h (alarm clear command).
   b. Delay 100 ms.
5. Read back AR49 XC_ERR compensation value and confirm it has been cleared.
   a. Read Address 0x40 and 0x 41. Expected data return 00h.
6. Read Back AR49 and MT counter alarm status.
   a. Read Address 0x42 and 0x43. Expected data return 0000h.
   b. Read Address 0x44 and 0x45. Expected data return 1001h.
   c. Read Address 0x22 and 0x23. Expected data return 0000.

EH Pulse Voltage Monitoring

The AR49 has a built-in function to measure and monitor the EH pulse voltage level (VWC). Measurement must be conducted with the final encoder assembly inclusive of the external shield cover.

1. Unlock Register Write.
2. Set the default MT configuration.
3. Enable VWC monitoring self-check by writing Page 9/Bank 18 Address 0x08 = 04h.
4. Spin the spindle motor in the clockwise (CW) direction for >350 rotations at 3000 rpm.
5. Loop reading calibration status Page 9, Address 0x45 (BiSS-C Bank19, Address 0x05).
   a. If Bit[3] = 1b, the measurement is done.
6. End VWC monitoring self-check by writing Page 9/Bank 18, Address 0x08 = 00h.
7. Read Page 9, Address 0x46 to 0x47 (BiSS-C Bank19, Address 0x06 and 0x07) for the measured data.
8. Stop the motor. Repeat Steps 2 to 6 in the counter-clockwise (CCW) direction.
9. Clear the default MT configuration.

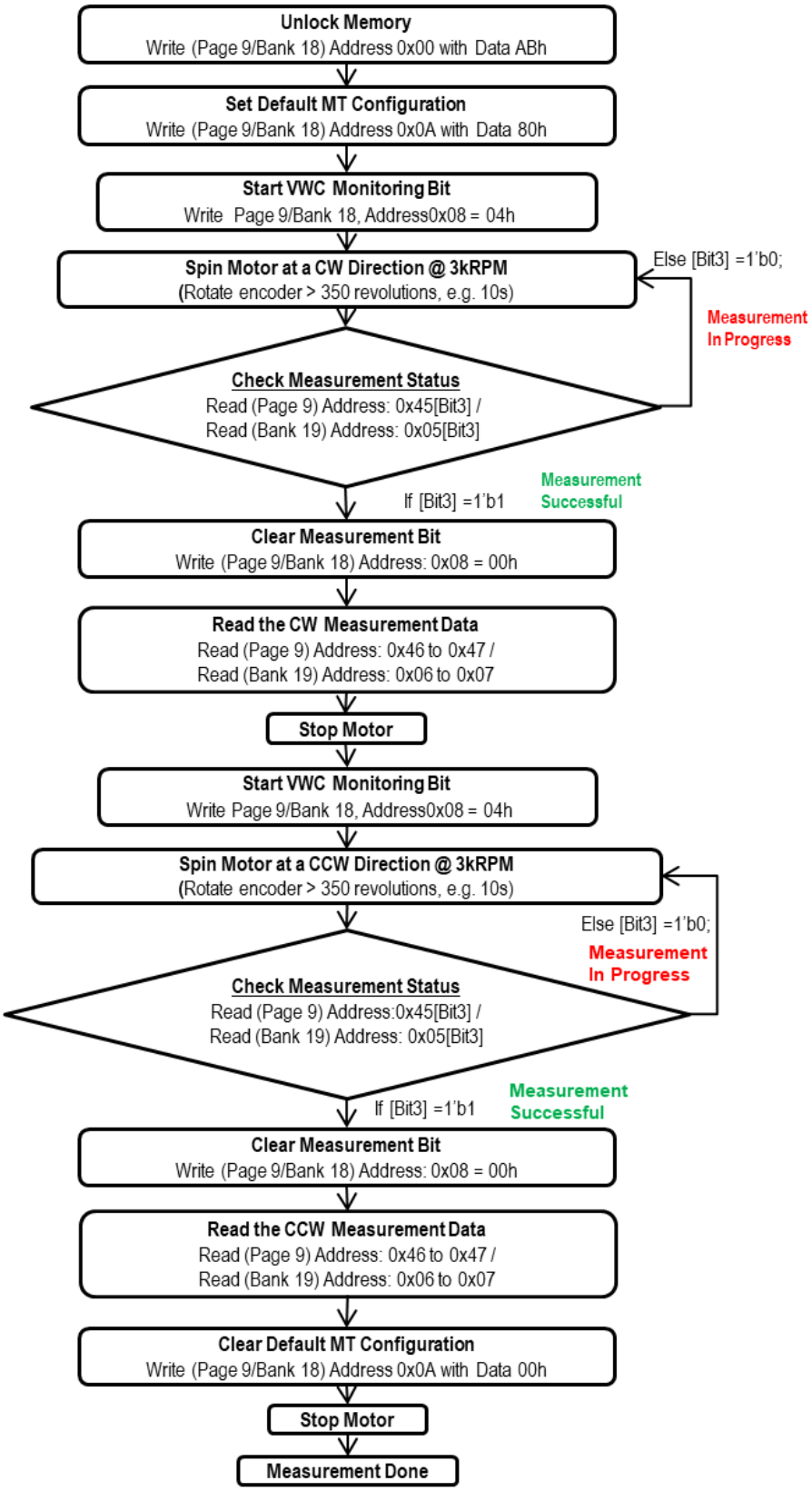
Table 23: EH Pulse Monitoring Measurement Registers

<table>
<tr><th colspan="3">SPI/RS485</th><th colspan="3">BiSS-C</th><th>Description</th><th colspan="8">Bit</th></tr>
<tr><th>Page</th><th colspan="2">Address</th><th>Bank</th><th colspan="2">Address</th><th></th><th colspan="8"></th></tr>
<tr><th>[dec]</th><th>[dec]</th><th>[hex]</th><th>[dec]</th><th>[dec]</th><th>[hex]</th><th></th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td rowspan="5">9</td><td>8</td><td>08</td><td>18</td><td>8</td><td>08</td><td>Command</td><td></td><td></td><td></td><td></td><td></td><td>Vwc_ Mon_ Trig</td><td></td><td></td></tr>
<tr><td>68</td><td>44</td><td rowspan="3">19</td><td>4</td><td>04</td><td rowspan="2">Status (Read Only)</td><td>Alarm Trigger</td><td></td><td></td><td>DUT Ready</td><td></td><td></td><td></td><td></td></tr>
<tr><td>69</td><td>45</td><td>5</td><td>05</td><td></td><td></td><td></td><td></td><td>VWC Result Ready</td><td></td><td></td><td>MT Ready</td></tr>
<tr><td>70</td><td>46</td><td>6</td><td>06</td><td rowspan="2">MT Counter VWC (Read Only)</td><td colspan="9">EH Pulse VWC data, Average – 4 Sigma (Target value: 53 to 100 decimal)</td></tr>
<tr><td>71</td><td>47</td><td>7</td><td>07</td><td colspan="9">EH Pulse VWC data – Mean (Target 56 to 100 decimal)</td></tr>
</table>

Table 24: EH Pulse Monitoring Target Specifications

Parameters	Conditions	Min.	Typ.	Max.	Unit
(Mean – 4σ)	Rotation speed 3000 revolutions/minute	5.3	—	10	V
Mean		5.6	—	10	V

Figure 17: VWC Monitoring Self Test Flowchart



General Specification of SPI 4-Wire Serial Communication

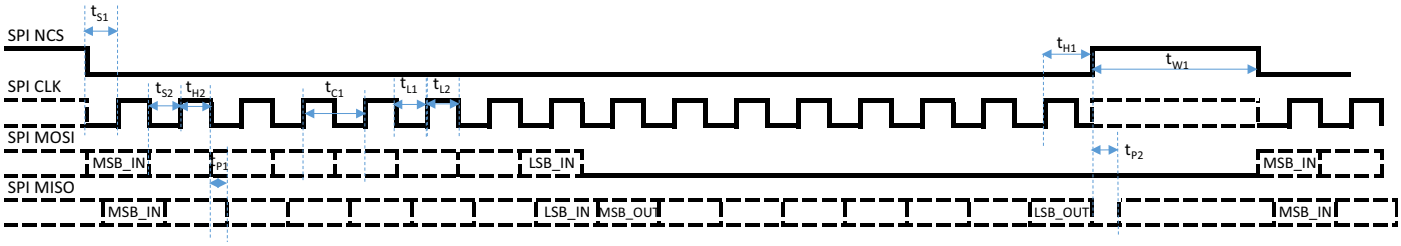
Overview of the 4-Wire Serial Peripheral Interface (SPI4)

Table 25: General Specification of SPI4 Serial Communication

Item	Specification	Note
Transmission type	Serial Peripheral Interface (SPI)	
Communication type	Single-ended	
Synchronization type	Synchronous	
Communication Baud rate	Up to 10.0 Mb/s	
Frame Length	Number of bits depending on operation	
Transmission Error Checking	6 bits CRC	$G(X) = X^6 + X^1 + 1$
	16 bits CRC	$G(X) = X^{16} + X^{15} + X^{12} + X^7 + X^6 + X^4 + X^3 + 1$

An SPI4 serial communication is established between the encoder (client) and the host (for example, a servo driver) in a single-ended transmission format. The encoder will carry out specific operations based on the command requests made by the host.

Figure 18: General Transmission Frames Format for SPI-4 Wires



NOTE:

- When NCS = 1, MISO = high-Z (to support multi-encoder bus mode).
- During the first 8 clocks, MISO always echoes the operation command received on the MOSI line (to support the multi-encoder bus mode).
- SPI Mode 0 and SPI Mode 3.are implemented.

Table 26: SPI4 Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
t_{C1}	Permissible Clock Cycle Time	100	—	—	ns
t_{L1}	Clock Signal Low Level Duration	50	—	—	ns
t_{L2}	Clock Signal High Level Duration	50	—	—	ns
t_{S1}	Setup Time: NCS lo before SCLK Low→High	50	—	—	ns
t_{H1}	Hold Time: NCS lo after SCLK Low→High	80	—	—	ns

Table 26: SPI4 Timing Specifications (Continued)

Symbol	Description	Min.	Typ.	Max.	Unit
t_{W1}	Wait Time: Between NCS Low→High and NCS High→Low	200	—	—	ns
t_{H2}	Hold Time: MOSI Stable after SCLK Low→High	20	—	—	ns
t_{S2}	Setup Time: MOSI Stable before SCLK Low→ High	15	—	—	ns
t_{P1}	Propagation Delay: MISO Stable after SCLK High→Low	—	51	—	ns
t_{P2}	Propagation Delay: MISO High Impedance after NCS Low→High	—	10	35	ns

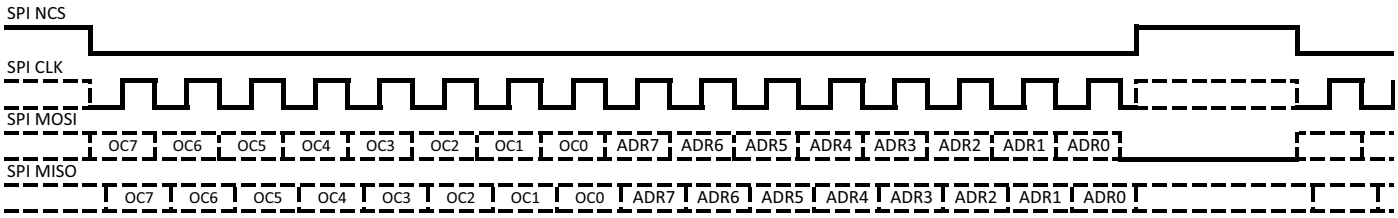
SPI4 Cyclic Redundancy Check Setting (CRC)

Table 27: SPI4 CRC Settings

Page	Address [hex]	Bit 7	6	5	4	3	2	1	0	Default Value	Description
7	25								SPI4_Ext_EN	00h	6bits CRC: “0” 16bits CRC: “1”
	26	SPI4 CRC [15:8]								00h	CRC Initial Value
	27	SPI4 CRC [7:0]								00h	

Encoder Read Out Frame Sets Format and Timing

Figure 19: Register Read Operation Diagram



When NCS is low, the communication line is activated and the data is sampled on the rising edge of SCK.

The MISO state turns to high impedance mode (hi-Z) when NCS is high. The transmission works over specific operation command (OC).

Table 28: SPI4 Operation Commands

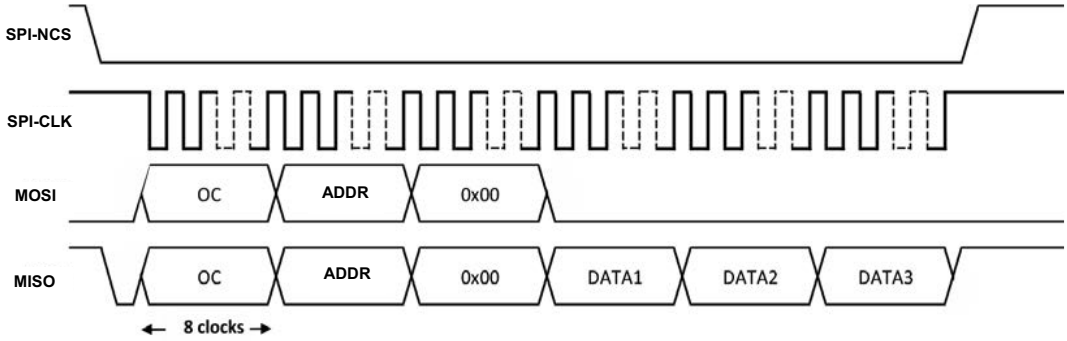
Operation Command (OC)	Description	Ports	CLK Bits															
			Byte 1	Byte 2							Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
0xB0	Activate (1 encoder)	MOSI	B0	1	0	0	0	0	0	RA0	PA0							
		MISO	B0	0	0	1	0	0	0	0	0							
	Activate (2 encoder)	MOSI	B0	1	0	0	0	RA0	PA0	RA1	PA1							
		MISO	B0	0	0	0	0	1	0	0	0							
0xA6	Position Read	MOSI	A6															
		MISO	A6	Position Data + nError + nWarning + CRC/Position Data + nError + nWarning + nsequence + CRC													…	
0x81	Register Read (Continuous)	MOSI	81	ADDRESS(ADDR)							00h							
		MISO	81	ADDRESS(ADDR)							00h	DATA1	DATA2	…				
0xCF	Register Write (Continuous)	MOSI	CF	ADDRESS(ADDR)							DATA1	DATA2	…					
		MISO	CF	ADDRESS(ADDR)							DATA1	DATA2	…					
0x9C	Read Status	MOSI	9C															
		MISO	9C	00h							ERR [7:0]	ERR [15:8]	ERR [23:16]	ERR [31:24]	WARN [7:0]	WARN [15:8]	WARN [23:16]	WARN [31:24]
0xD9	Write Command	MOSI	D9	COMMAND														
		MISO	D9	COMMAND														
0x97	Register Read (Single)	MOSI	97	ADDRESS(ADDR)														
		MISO	97	ADDRESS(ADDR)														
0xAD	Register Status/Data	MOSI	AD															
		MISO	AD	STATUS							DATA							
0xD2	Register Write (Single)	MOSI	D2	ADDRESS(ADDR)							DATA							
		MISO	D2	ADDRESS(ADDR)							DATA							

Memory Read Command

Use operation command (OC) 81h (continuous read on the current page of memory register) to read data from any register address in the ASIC chip. See Table 28 for the data streams sent on MOSI with OC 81h followed by the address of the first register to be read and a delay of 00h. These three bytes will reflect on the MISO line before sending out the register address's (ADDR) data (DATA1). As long as the CLK continues to be sent, consecutive register address's (ADDR+1) data (DATA2) is transmitted and so forth. This procedure continues until the clock ends.

Use operation command (OC) 97h followed by ADh to perform a single read data from any register address in the ASIC chip.

Figure 20: Memory Read Command with OC = 81h



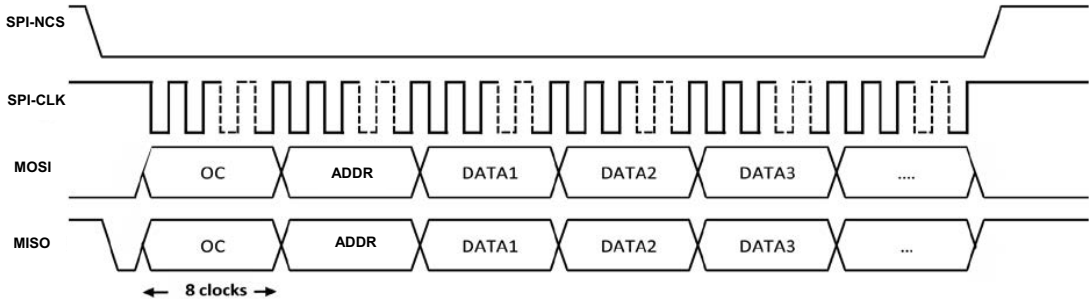
Memory Write Command

Use operation command (OC) CFh (continuous write on the current page of internal memory register) to write data into any register address in the ASIC chip. See Table 28 for the data streams sent on MOSI with OC = CFh followed by the address of the first register to be written and the data. With each data byte, the address of the register to be written is register address (ADDR+1). Data successfully received will be transmitted on MISO line.

Use operation command (OC) D2h followed by ADh to perform a single write data into any register address in the ASIC chip and retrieve back the written data.

WARNING! Do not perform a continuous write on an external EEPROM.

Figure 21: Memory Write Command with OC = CFh



Memory Read Status Command (Single – Status Description)

The following table describes the operation command (OC) ADh STATUS (STAT).

Table 29: Status Bits Descriptions

Bit	Name	Description
7	Error/SC_EN	Invalid operation command/Specific command enable
6:3	—	Reserved
2	Fail	Data request failed
1	Busy	Encoder busy
0	Valid	Data valid

NOTE: If the last OC received is D9h, STATUS Bit 7 = 1’b1 and the data value reflects the operation status.

SPI4 Operation Command

Use operation command (OC) D9h followed by the code shown in Table 30 to perform special tasks. Once the command is received, perform ADh to read back the status of the operation. The data value `FFh` indicates an error. The data value `00h` indicates the task is completed. The data value `Code` indicates the task is in progress. In the case of an overwritten operation, for example, 0x97h register read, perform the command operation 0x00h(NOP) to put the operation status back to buffer for 0xADh.

Table 30: SPI4 Specific Operation Command

Code	Name	Description
0x00	<NOP_OK>	<Return-code: last operation succeeded>.
0x10	REBOOT	Equivalent to power-on.
0x18	MT_RESYNC	Resynchronize with the external MT device.
0x19	MT_RESET	Clear FeRAM value.
0x20	SCLEAR	Clear the System Alarm registers.
0x80	MTST_PRESET	Set current position as MT = 0, ST = 0.
0x81	MT_PRESET	Set current position as MT = 0.
0xB4	AUTO_CAL_ALL1	Automatic calibrate analog + digital.
0xB5	AUTO_CAL_ALL2	Automatic calibrate analog + digital + accuracy.
0xFF	<NOP_FAIL>	<Return-code: last operation failed>.

SPI4 Position Read

Use operation command (OC) A6h to read the absolute position data from the ASIC chip. For nError (nE), nWarning (nW), CRC selections, refer to the CRC setting in Table 27. Position the latch at the first rising clock. nError and nWarning trigger 0 if any of the error triggered. Sequence counter (Seq Cnt) is the position read counter. For every consecutive position read request received by the encoder, the sequence counter value is increased by 1 (Seq Cnt = Seq Cnt + 1), until 63 counts are reached. The counter then rolls over to become 0 and restarts the counting. Single-turn bits (ST-bit) and multi-turn bits (MT-bit) are continuous bits with no zero bit patching. See the encoder resolution bits selection in Table 7.

Figure 22: SPI4 Position Read Command

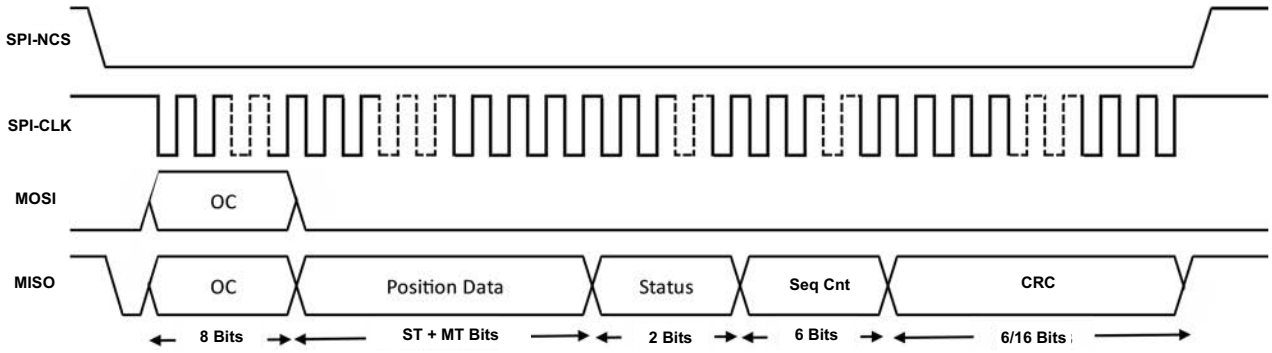


Table 31: Single-Turn Only Position Read

Operation Command (OC)	Description	Ports	1 Byte	<ST-Bit>	2 Bits		6 Bits	2 Bytes
0xA6(MT_OFF)	Position Read	MOSI	A6(8b)					
	--> format = Basic	MISO	A6(8b)	ST Pos	nE	nW	CRC (6b)	
	--> format = Extended	MISO	A6(8b)	ST Pos	nE	nW	Seq Cnt (6b)	CRC (16b)

Table 32: Multi-Turn + Single-Turn Position Read

Operation Command (OC)	Description	Ports	1 Byte	<MT-Bit>	<ST-Bit>	2 Bits		6 Bits	2 Bytes
0xA6	Position Read	MOSI	A6(8b)						
	--> format = Basic	MISO	A6(8b)	MT Pos	ST Pos	nE	nW	CRC (6b)	
	--> format = Extended	MISO	A6(8b)	MT Pos	ST Pos	nE	nW	Seq Cnt (6b)	CRC (16b)

Encoder Activation in a Chained or Bus Mode

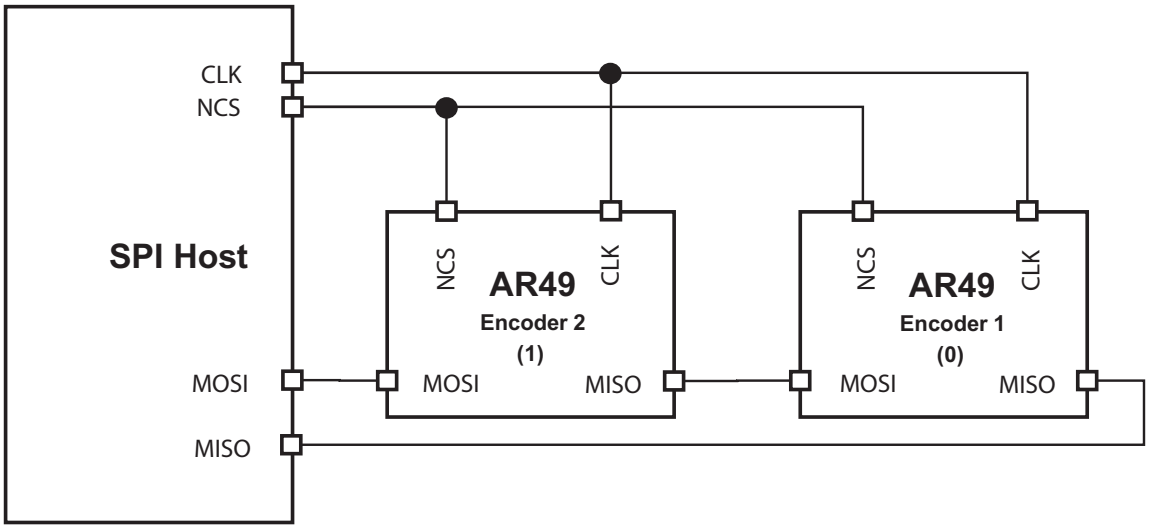
Use operation command (OC) B0h to activate encoders in a chained-type connection. Register data access (RAx) bit is enabled to access memory register in the encoder. Position data access (PAx) bit is enabled to access position data in the encoder.

NOTE: 1 = Enable; 0 = Disable.

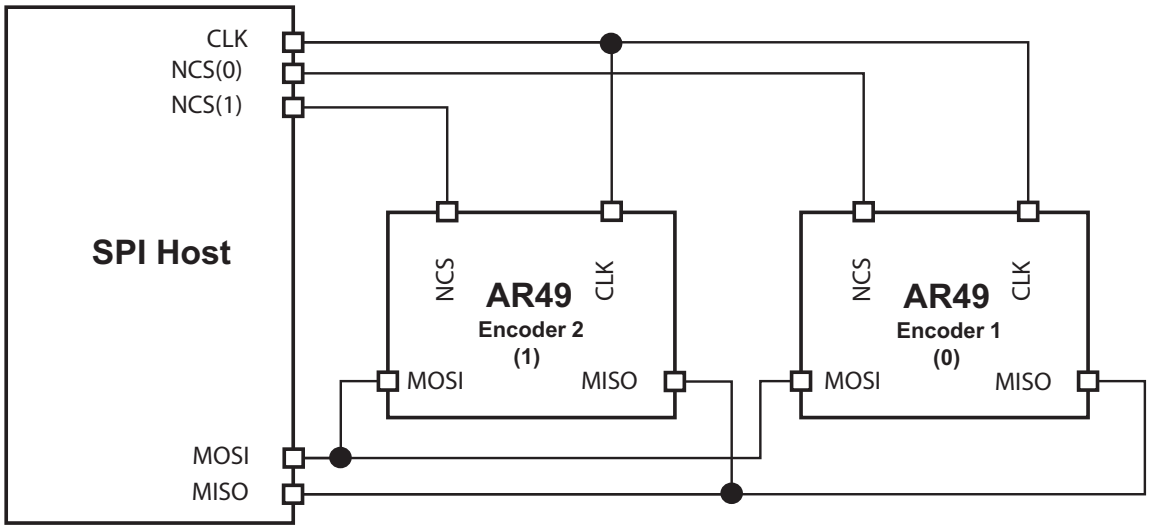
Table 33: Encoder Activation

OC	Description	Ports	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0xB0	Activate (1 encoder)	MOSI	B0								1	0	0	0	0	0	RA0	PA0
		MISO	B0								0	0	1	0	0	0	0	0
	Activate (2 encoders)	MOSI	B0								1	0	0	0	RA0	PA0	RA1	PA1
		MISO	B0								0	0	0	0	1	0	0	0

Figure 23: Chained or Bus Type Connection for Multi-Encoder



A Chain Type Connection for Multi-Encoder



A Bus Type Connection for Multi-Encoder

Table 34: Encoder Data Output Arrangement

Operation Command (OC)	Encoder 1								Encoder 2				
	Description	Ports	1 Byte	<S-Bit>	2 Bits		6 Bits	2 Bytes	<S-Bit>	2 Bits		6 Bits	2 Bytes
0xA6(MT_OFF)	Position Read	MOSI	A6(8b)										
	--> format = Basic	MISO	A6(8b)	ST Pos	nE	nW	CRC (6b)		ST Pos	nE	nW	CRC (6b)	
	--> format = Extended	MISO	A6(8b)	ST Pos	nE	nW	Seq Cnt (6b)	CRC (16b)	ST Pos	nE	nW	Seq Cnt (6b)	CRC (16b)

General Specification of RS485 Serial Communication

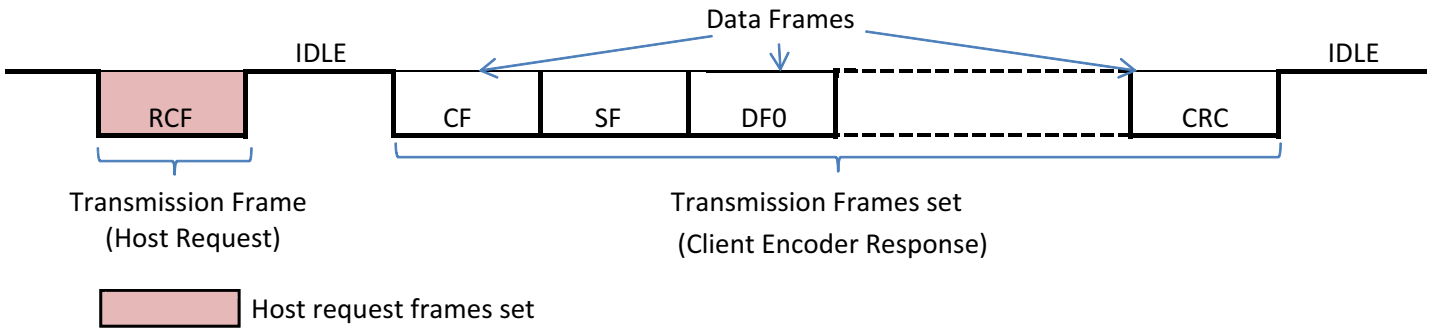
Overview of RS485 Communication

A one-to-one half-duplex serial communication is established between the client encoder and the host (for example, a servo driver). The communication is in a differential transmission format. The encoder will carry out specific operations based on the command requests made by the host. An acknowledgment of the command request received by the encoder is necessary before the encoder executes the requested operation. The acknowledgment is conditional on the valid verification of the start bit, information data field, and stop bit. Failing this checking, the encoder will not acknowledge and execute the received command request.

Table 35: General Specification of RS485 Serial Communication

Item	Specification	Note
Transmission Type	Differential Transceiver	
Communication Type	Half duplex	Recommended transceiver: ISL8485E or Equivalent
Transmission Code Type	Binary, Non-Zero Return (NRZ) code	
Synchronization Type	Asynchronous	
Communication Baud Rate	2.5 Mb/s, 5.0 Mb/s, and 10.0 Mb/s	
Frame Length	10 bits/Frame	
Transmission Error Checking	8 bits CRC	CRC equation $G(X) = X^8 + 1$ X = CRC0 ~ CRC7

Figure 24: General Transmission Frames Format on Half-Duplex Line



Start of transmission frames set: Upon detecting of the first logic of low state 0 on the transmission line after an idling state, and if the following 3 bits conform to the encoder address sync code, the encoder will acknowledge it as a valid request control field (RCF) and indicates the start of a transmission frame set. Otherwise, the encoder will continue to search for the next available logic of Low State 0.

End of transmission frames set: After the command frame is detected, if there is no start bit after the end bit of the last frame read, and no subsequent frame is detected, then the end of the transmission frame set is concluded.

Idle state: The Idle state indicates there is a space between each transmission frames set and subsequent transmission frames. At idling state, the logic of output in transmission line is kept to high state 1.

Encoder Readout Frame Sets Format and Timing

Figure 25: Encoder Position Data Readout Frames Set

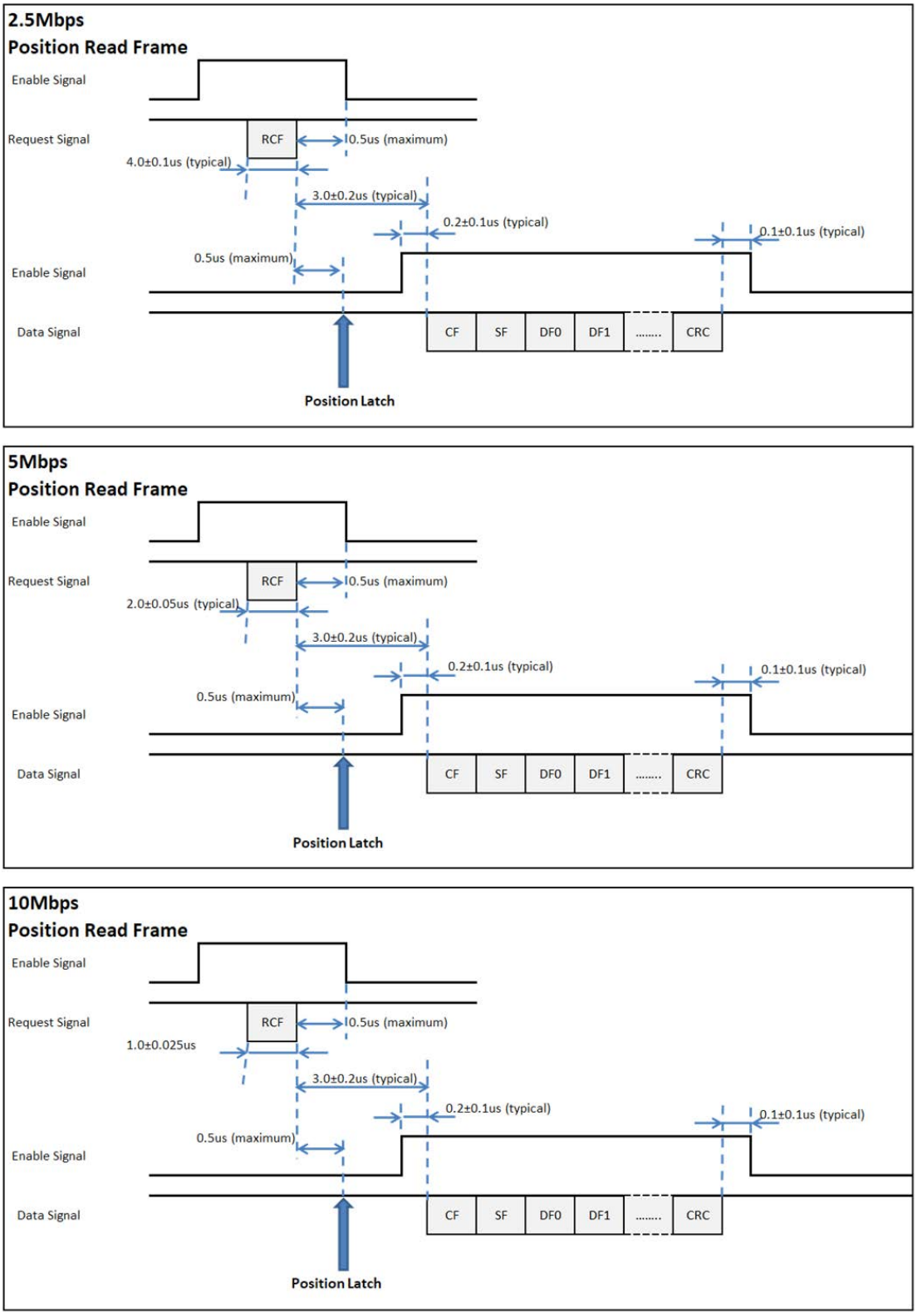
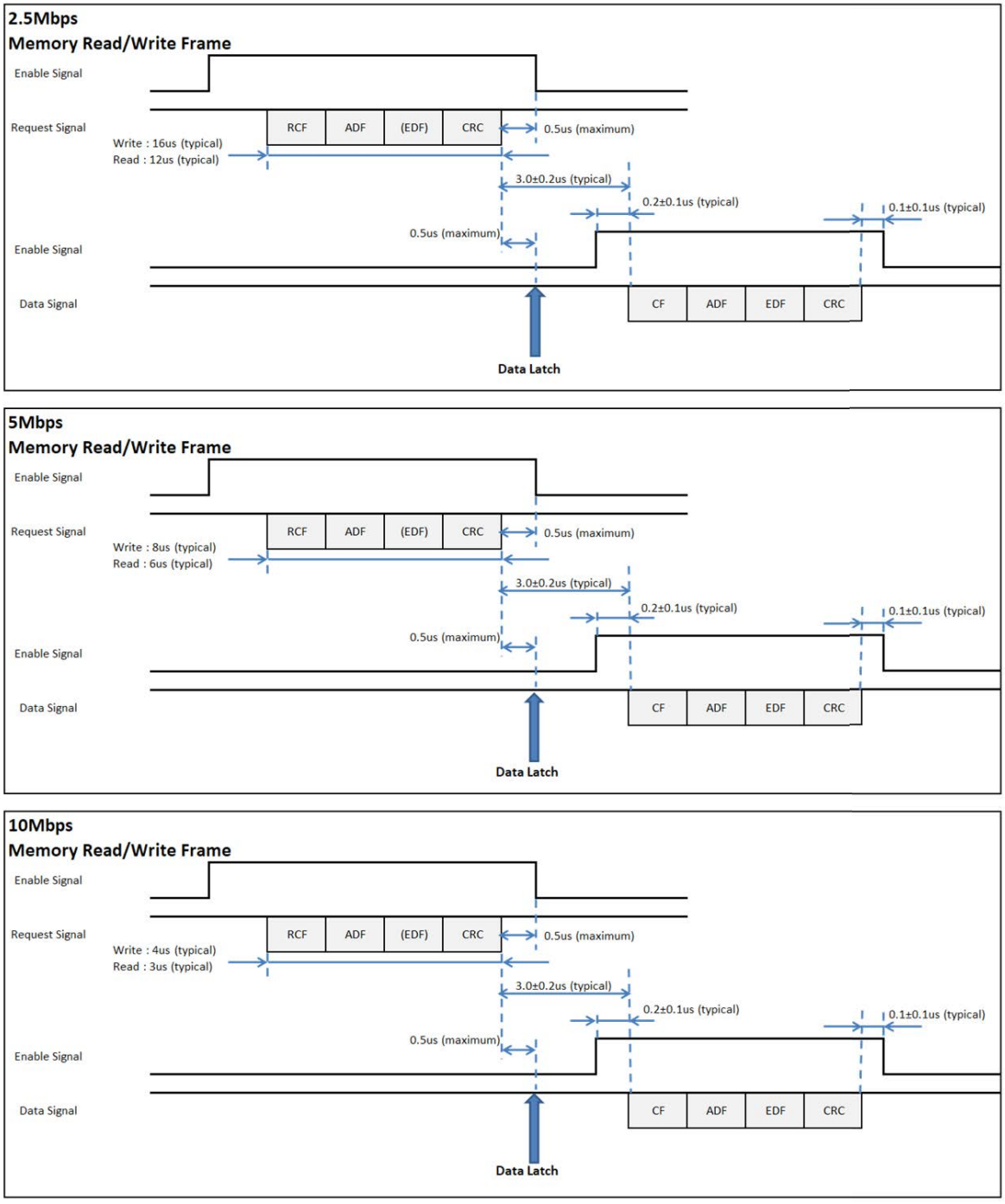


Figure 26: Encoder Memory Data Read and Write Frames Set



Encoder Position Data Readout Frame Sets

When the host issues a RCF frame request, the encoder will respond after 3.0 µs (typical) with encoder data frames set with the following contents:

- CF: Control field corresponds to the command frame issued by the host.
- SF: Status field.
- DF0~DF7: Encoder data field.
- CRC: Cyclic redundancy check (CRC) frame.

The encoder response data frame sets are dependent on the requested operation by the host (see Table 39).

Memory Data Readout Frames Set

Content of transmission frames:

- CF: Control field (same for both the host command and the encoder response).
- ADF: Address data field, indicates the memory location to read.
- EDF: Memory data field, contains the data read from memory.
- CRC: Cyclic redundancy check (CRC) checking.

Memory Data Write Frames Set

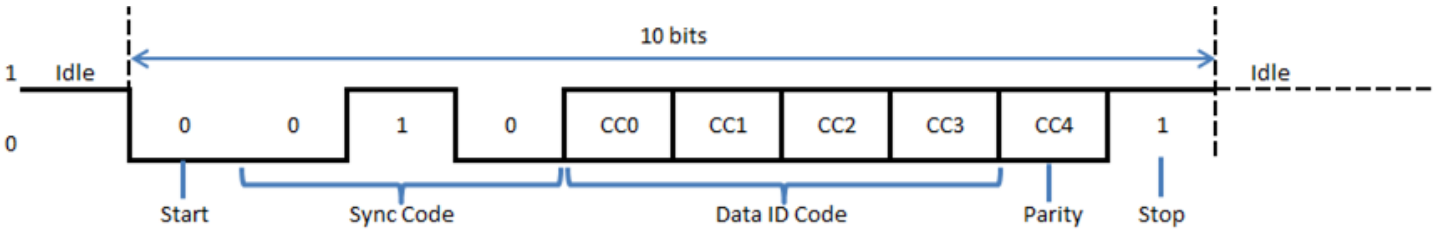
Content of transmission frames:

- CF: Control field (Same for both host command and encoder response).
- ADF: Address data field, indicate the memory location to write.
- EDF: Memory data field, contains the written data to memory.
- CRC: Cyclic redundancy check (CRC) checking.

Details Description of Data Frames

Control Field (CF)

Figure 27: Control Field Format



Contents of the CF frame:

- Start Bit: Indicates the start of a frame, always 0.
- Sync Code: Indicates a valid encoder address sync code has been issued, default is 010.
- Data ID: Combination of bits defining command instructions (see to Table 36 and Table 37).
- Parity Bit: Parity check bit for data ID (see Table 36).
- Stop Bit: Indicate the end of a frame, always 1.

RS485 Data ID and Client Encoder Operation Definition

Table 36: Encoder Operation Command Code Definition and Parity Bit

Encoder Operation	Data ID	Encoder Sync Code			Data ID Bits				Parity	HEX
		Bit 0	Bit 1	Bit 2	CC0	CC1	CC2	CC3	CC4	
Position or Encoder Info Read Command	0	0	1	0	0	0	0	0	0	02
	1	0	1	0	1	0	0	0	1	8A
	2	0	1	0	0	1	0	0	1	92
	3	0	1	0	1	1	0	0	0	1A
	4	0	1	0	0	0	1	0	1	A2
Memory Write Command	6	0	1	0	0	1	1	0	0	32
Alarm Clear Command	7	0	1	0	1	1	1	0	1	BA
Position Zero Reset Command	8	0	1	0	0	0	0	1	1	C2
Multi-Turn and Alarm Clear Command	C	0	1	0	0	0	1	1	0	62
Memory Read Command	D	0	1	0	1	0	1	1	1	EA

Description of Encoder Operation

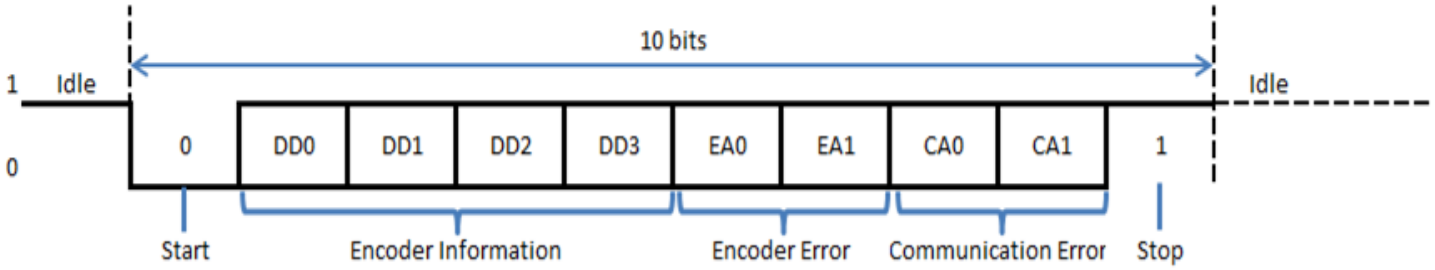
Table 37: Description of RS485 Encoder Operation for the 24-Bit ST Format

Operation	Data ID	Description of Operation
Position Read Command	0, 1, 2, 3, 4	Transmit Data ID code (Table 36) according to the list of data fields to the encoder.
Memory Write Command	6	8 bits of data to be written into a designated memory address of the user-accessible area.
Alarm Clear Command[a]	7	Consecutive 10x sending to perform alarm clear command.
Position Zero Reset Command[a]	8	Consecutive 10x sending to perform position zero reset command
Multi-turn and Alarm Clear Command[a]	C	Consecutive 10x sending to perform multi-turn and alarm clear command.
Memory Read Command	D	8 bits of data to be read from a designated memory address of the user-accessible area.

a. See Table 39 and Table 40 for the requirements of consecutive sending for the clear or reset commands.

Status Field (SF)

Figure 28: SF Frame Format



Content of SF frame:

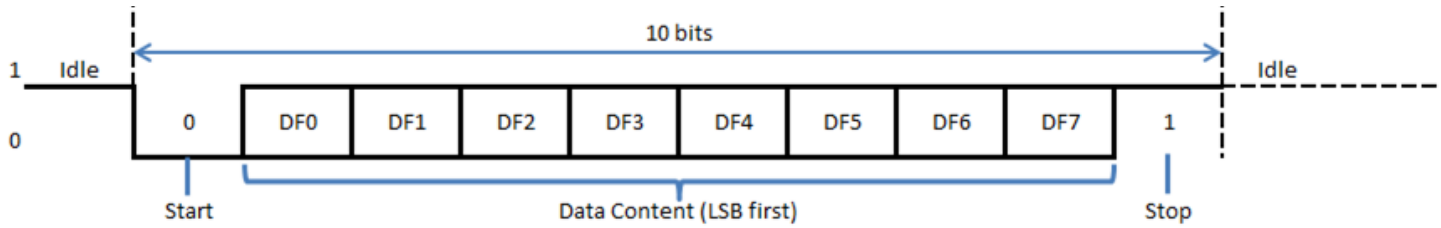
- Start Bit: Indicates the start of a frame, always 0.
- Encoder Information: Defined as 0000.
- Encoder Error: Returns with state 1 if an encoder error is detected.
- Stop Bit: Indicates the end of a frame, always 1.

Table 38: Status Field Description of Error Flags

Logic When Error Is Detected	Error Flag	Error Description
Encoder Error Bit 1	EA0	Encoder counting error.
	EA1	Multi-turn counting error.
Communication Error Bit 1	CA0	Parity error detected in host request frames set.
	CA1	End bit error detected in host request frames set.

Data Field (DF_n)

Figure 29: DF_n Frame Format



Content of DF_n frame:

- Start Bit: Indicates the start of frame, always 0.
- DF0~DF7: 8 bits data set with LSB first in sequence.
- End Bit: Indicate the end of frame, always 1.

Description of Data Frames with Respective Data ID

The AR49 encoder supports variants of RS485 output formats depending on the single-turn and multi-turn resolutions requirements. See Table 43 for the RS485 format settings.

RS485 Data Frames Format for 24-Bit ST and 24-Bit MT Output

This is the default RS485 format, which can transmit up to 3 bytes (24-bit) of ST data and 3 bytes (24-bit) of MT data.

Table 39: RS485 Data Frames Content with Respective Data ID for up to 24-bit Multi-Turn

ID	CF	SF	DF0	DF1	DF2	DF3	DF4	DF5	DF6	DF7	CRC	Remark	Frame Size
0	CF	SF	ABS0	ABS1	ABS2						Yes	Position Read Command	6
1	CF	SF	ABM0	ABM1	ABM2								6
2	CF	SF	ENID									Encoder Identification	4
3	CF	SF	ABS0	ABS1	ABS2	ENID	ABM0	ABM1	ABM2	ALMC		Position Read Command	11
4	CF	SF	ABS0	ABS1	ABS2	ENID	ABM0	ABM1	ABM2	TEMP			11
6	CF	ADF	EDF									Memory or Register Write Command	4
7	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to Perform Alarm Clear Command	6
8	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to Perform ST Zero Reset Command	6
C	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to Perform MT and Alarm Clear Command	6
D	CF	ADF	EDF									Memory or Register Read Command	4

NOTE:

- **ABSn**: Single-turn counts. LSB of the single-turn counts is located in ABS0, and MSB of the counts data is located in ABS2. Combining ABS0~ABS2 will provide a maximum total of 24 bits single-turn data.
- **ABMn**: Multi-turn counts. LSB of the multi-turn counts is located in ABM0, and MSB of the counts data is located in ABM2. Combining ABM0~ABM2 will provide a maximum total of 24 bits multi-turn data.
- **ENID**: The encoder single-turn bits identification in 8-bit format. For example, 23-bit output is set to 17h, and 24-bit output is set to 18h.
- **ALMC**: The encoder alarm data in 8-bit format. See Table 42.
- **TEMP:** The encoder temperature readout data in 8-bit format. See Table 18.

RS485 Data Frames Format for 25-Bit ST and 16-Bit MT Output

This is the alternative RS485 format, which can transmit up to 4 bytes (32-bit) of ST data and 2 bytes (16-bit) of MT data.

Table 40: RS485 Data Frames Content with up to 16-bit Multi-Turn Resolution

ID	CF	SF	DF0	DF1	DF2	DF3	DF4	DF5	DF6	DF7	CRC	Remark	Frame Size
2	CF	SF	ENID								Yes	Position Read Command.	4
3	CF	SF	ABS0	ABS1	ABS2	ENID	ABS3	ABM0	ABM1	ALMC			11
4	CF	SF	ABS0	ABS1	ABS2	ABS3							7
5	CF	SF	ABS0	ABS1	ABS2	ABS3	ABM0	ABM1					9
6	CF	ADF	EDF									Memory or Register Write Command.	4
7	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to Perform Alarm Clear Command.	6
8	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to Perform ST Zero Reset Command.	6
C	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to Perform MT and Alarm Clear Command.	6
D	CF	ADF	EDF									Memory or Register Read Command.	4

NOTE:

- **ABSn**: Single-turn counts. LSB of the single-turn counts is located in ABS0, and MSB of the counts data is located in ABS3. 7 bits LSB of STC0 are fixed to 0. Combining STC0~STC3 will provide a maximum total of 25 bits single-turn data. Combining ABS0~ABS3 will provide a maximum total of 25 bits single-turn data.
- **ABMn**: Multi-turn counts. LSB of the multi-turn counts is located in ABM0, and MSB of the counts data is located in ABM1. Combining ABM0~ABM1 will provide a maximum total of 16 bits multi-turn data.
- **ALMC**: Encoder alarm bits. See Table 42.
- **TEMP:** Encoder temperature readout bit.

Single-Turn Encoder Identification Setting

For the setting of the ENID value, the configuration is as listed in Table 41.

Table 41: ENID Setting

RS485			ENID								Default [hex]
Page	Address		Bit								
[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0	
7	1	01	ENID [7:0]								18h

The default value is set to 18h, referenced to the 24-bit single-turn resolution of the AR49 encoder ASIC.

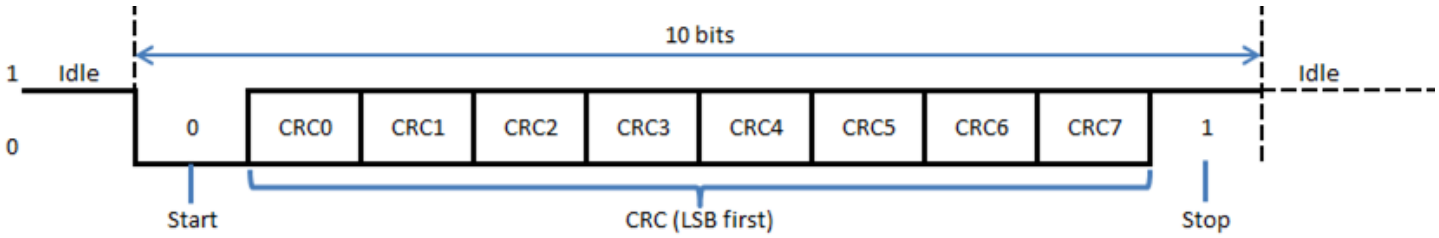
RS485 Encoder Alarm Definition

Table 42: ALMC Alarm Bits Definitions

Bit Value	ALMC Bit							
	DF7-0	DF7-1	DF7-2	DF7-3	DF7-4	DF7-5	DF7-6	DF7-7
0	No Error	No Error	No Error	No Error	No Error	No Error	N/A	N/A
1	MT Sync Error	Memory Error	ST Error	MT Counter Error	Lissajous /LED/ Temp Error	MT Error (EHMT Counter Err[0])		
Encoder Error Status	EA1	N/A	EA0	EA1	N/A	EA1		

Cyclic Redundancy Check Frame (CRC)

Figure 30: CRC Frame Format

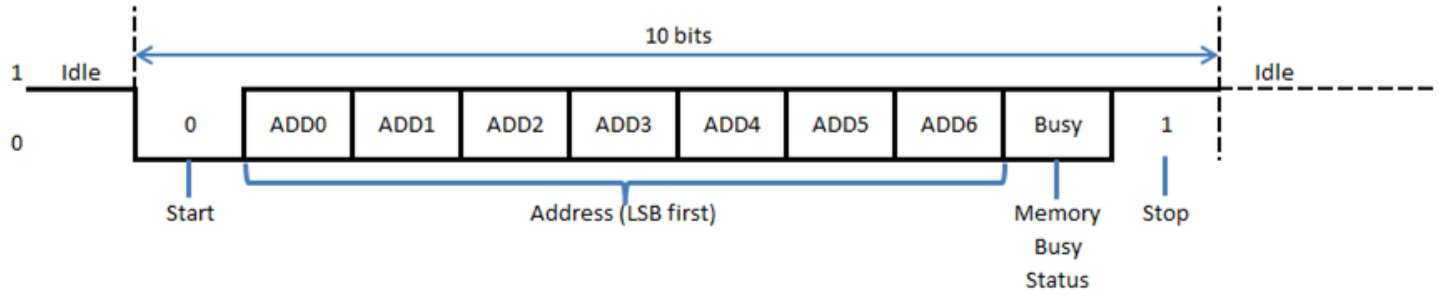


Content of CRC frame:

- Start Bit: Indicates the start of a frame, always 0.
- CRC0~CRC7: 8 bits CRC data set with LSB first in sequence. The CRC codes are generated per the equation of $G(X) = X^8 + 1$ (X = CRC0 ~CRC7).
- End Bit: Indicates the end of a frame, always 1.

Address Data Frame (ADF)

Figure 31: ADF Frame Format

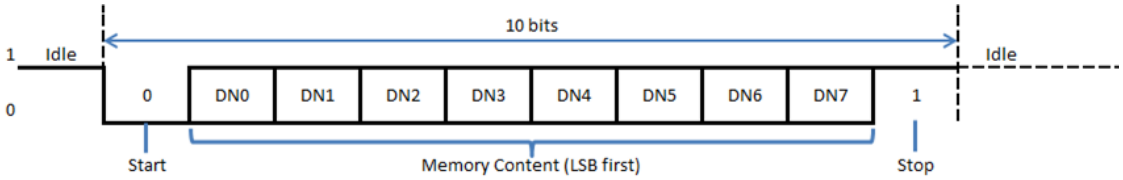


Content of ADF frame:

- Start Bit: Indicates the start of a frame, always 0.
- ADD0~ADD6: 7 bits memory address data set with LSB first in sequence.
- Busy: Memory access busy (MBSY) status flag.
- End Bit: Indicates the end of a frame, always 1.

Memory Data Frame (EDF)

Figure 32: EDF Frame Format



Content of EDF frame:

- Start Bit: Indicates the start of a frame, always 0.
- DN0~DN7: 8 bits memory data set with LSB first in sequence.
- End Bit: Indicates the end of a frame, always 1.

RS485 Encoder Configuration

The RS485 protocol settings, which is user configurable is listed in Table 43.

Table 43: RS485 Encoder Setting

Page [decimal]	Address [hex]	Bits	Parameter	Function	Value [binary]	Setting	Default Value [binary]
7	1D	7	Parity	Default Setting	0	0	0
		6	RS485 Data Format	Maximum ST Position Data	0	24-Bit	0
					1	25-Bit	
		5	Broadcast Mode Off	RS485 broadcast mode	0	Broadcast Mode	1
					1	Single Device	
		[4:3]	RS485 Baud Rate	Default = 2.5 Mb/s	00 01	2.5 Mb/s	00
					10	5.0 Mb/s	
					11	10 Mb/s	
		[2:0]	RS485 Encoder Address (Sync Code)	Encoder Address	000 001 010 011 :: 111	010 (Default for single device)	010

NOTE:

- Updating the RS485 settings requires the host to also issue the subsequent commands with the same changes made. Else, the communication between the host and the client encoder might fail.
- The memory program command is needed for the system area memory to be effective upon power cycle — applicable for changes to internal memory Pages 5 to 8.
- Perform the memory program command for changes to any of the affected banks before moving to other nonvolatile memory banks.
- Changes will be lost after a power cycle without a memory program command.

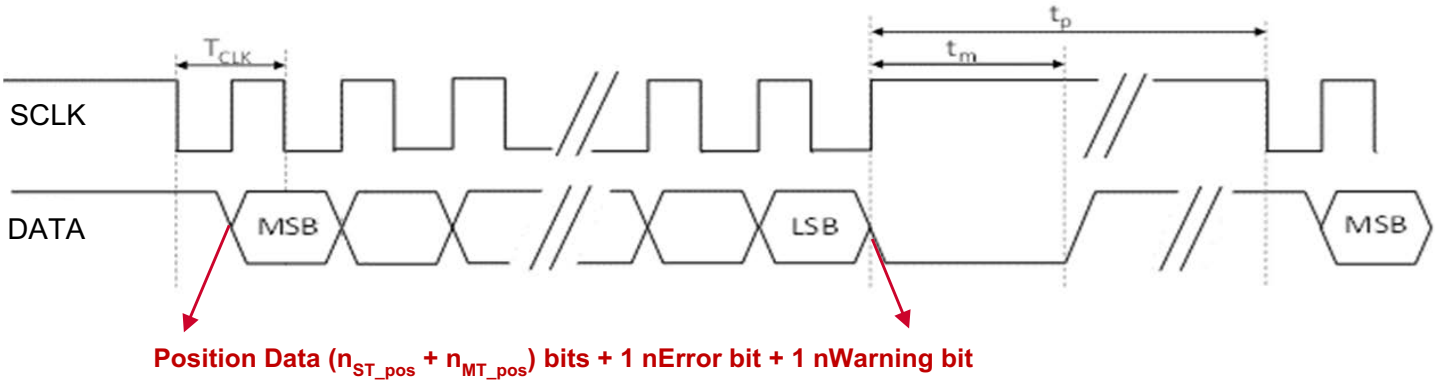
General Specification of Synchronous Serial Interface (SSI) Communication

A one-to-one single-ended/full-duplex serial communication is established between the encoder (client) and the host (for example, a servo driver). The communication can be a single-ended or differential transmission format. Synchronous data transmission is the data transmitted by synchronizing the transmission at the receiving and sending ends using a common clock. Data transmitted is adaptive to the number of clocks and bandwidth.

Table 44: SSI Protocol Specifications

SSI Communication Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Frequency	f_{CLK}	—	100	—	10,000	kHz
Clock Duty	DUT_{CLK}	—	—	50	—	%
Monoflop Time	t_m	—	—	—	20	µs
Pause Time	t_p	—	21	—	—	µs

Figure 33: SSI Data Field and Timing Diagram



MT[23:0]	ST[24:0]	Error[0]	Warning[0]

For the SSI option, the encoder calibration and device configuration are achieved by communicating in SPI mode during calibration.

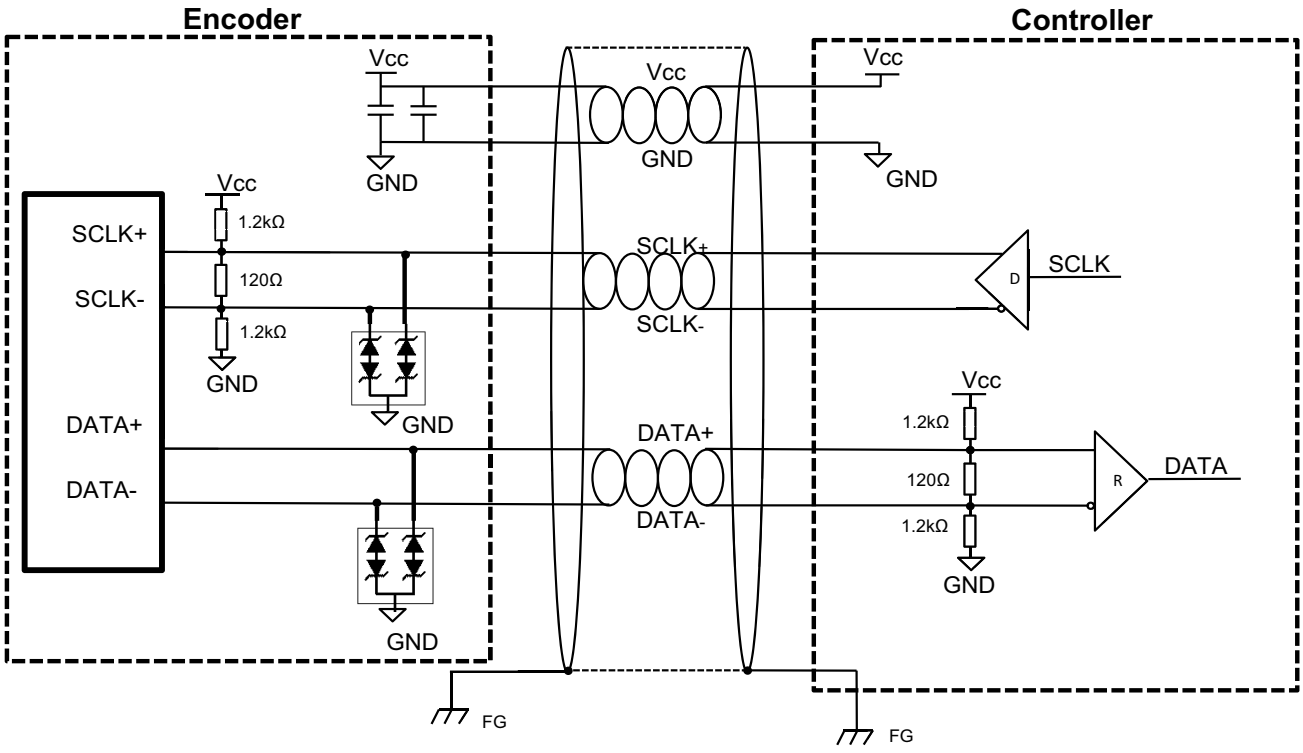
Table 45: Definition of SSI Encoder Alarm Output Bits

SSI Error Status [7:0]								
Option	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ST Only	N/A					ST Error | MLS Error	Memory Error	N/A
MT	N/A		MT Error (EHMT Counter Err[0])	N/A	MT Counter Error | MT Protocol Error | XC Error	ST Error | MLS Error	Memory Error	MT Sync Error
SSI Warning Status [7:0]								
ST or MT	N/A					Temp Error	Lissajous (Incremental) Error	LED Error

SSI 2-Wire Full-Duplex Connection

1. Provide the following encoder power supply:
   For the 5.0V supply, V_{CC} should be within the range of 4.5V ~ 5.5V.
2. For best noise immunity, use a twisted-pair shielded cable for connection to the servo driver.
3. To prevent undesirable signal reflection, terminate with a 120Ω resistor.
4. Terminate the shield wire to frame ground (FG) at both ends of the communication line.

Figure 34: Typical SSI Full-Duplex Connection



General Specification of BiSS-C Serial Communication

Table 46: General Specification of Serial Communication

Interface	Symbol	Recommended Circuit
Serial Clock	MA or SCLK	Transmitter (P/N: ISL3295E) or equivalent
Serial Data Output	SLO or DAT	Receiver (P/N: ISL3283E) or equivalent

BiSS-C Serial Interface

Table 47: BiSS-C Timing Characteristics

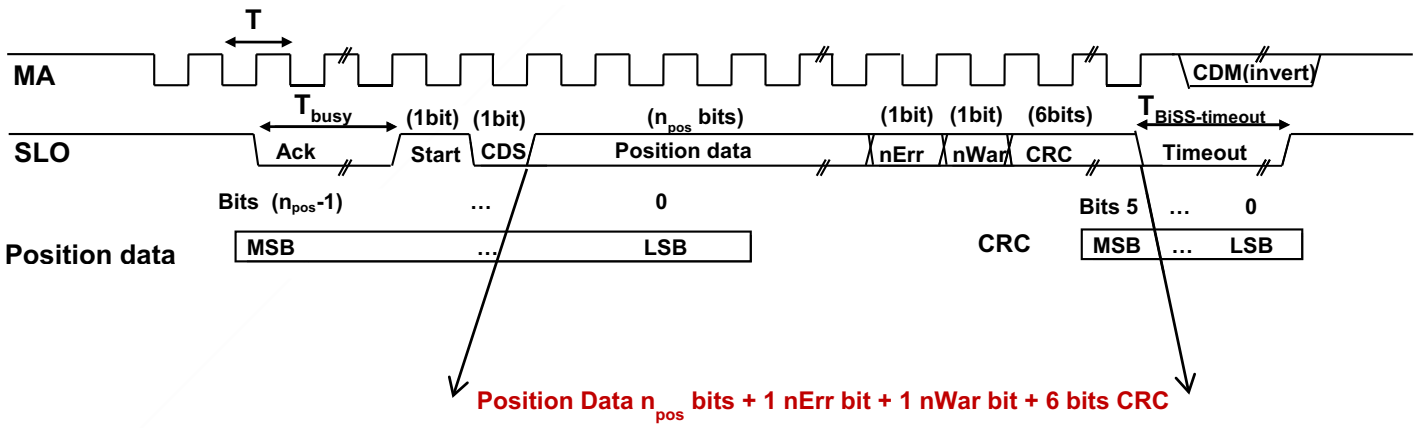
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
MA Frequency	f_{MA}	—	0.08	—	10	MHz	
MA Duty	DUT_{CLK}	—	—	50	—	%	
Busy	T_{busy}	f_{MA} = 5 MHz to 10 MHz	—	2/ f_{MA}	—	µs	a
		100 kHz ≤ f_{MA} ≤ 5 MHz	—	1/ f_{MA}	—		
Timeout	$t_{BiSS\text{-}timeout}$		1.5/ f_{MA}		5	µs	a
Frame to Frame	—	—	—	—	1	µs	
Encoder Initialization Time	—	—	—	500	—	ms	

a. Refer to Figure 35 for timing description.

BiSS-C Data Field

MT[23:0]	ST[24:0]	Error[0]	Warning[0]	CRC[5:0]

Figure 35: BiSS-C Interface Timing Diagram



NOTE:

- CRC Polynomial = Invert of ($X^6 + X^1 + X^0$).
- nErr bit is active low. (Combine all the error status and reflect in nErr bit.)
- nWar bit is active low. (Combine all the warning status and reflect in nWar bit.)
- Position data varies depending on single-turn and multi-turn resolution.

Table 48: BiSS-C Device Registers

Category	Description	Direct BiSS-C Register (hex)	Default Value (hex)
BiSS-C Device Information	BiSS EDS-Bank [7:0] [a]	41	00h
	BiSS Profile ID [15:0]	42	62h
		43	33h
	BiSS Serial Number [31:0] [b]	44	00h
		45	00h
		46	00h
		47	00h
	BiSS Device ID [47:0]	78	41h
		79	45h
		7A	18h
		7B	19h
		7C	80h
		7D	00h
	BiSS Manufacturer ID [15:0]	7E	41h
		7F	4Fh

a. No specific EDS Bank format is supported.

b. Only the two LSB bytes of the serial number data, in hex data are used, corresponding to the running serial numbers in the product label.

BiSS-C Client Register Description

Table 49: Definition of BiSS-C Encoder Status Bits and Clear Command

Address 72(48) – nErr, Error Status [7:0]								
Option	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ST Only	N/A					ST Error | MLS Error	Memory Error	N/A
EHMT	N/A		MT Error (EHMT Counter Err[0])	N/A	MT Counter Error | MT Protocol Error | XC Error	ST Error | MLS Error	Memory Error	MT Sync Error
Address 73(49) – nWar, Warning Status [7:0]								
N/A						Temp Error	Lissajous (Incremental) Error	LED Error
Address 74(4A) – Encoder Clear Command [a]; Bit2 = Alarm Clear, Bit1 = ST Zero Offset, Bit0 = MT Zero Offset								
N/A						Alarm Clear	ST Zero Offset	MT Zero Offset

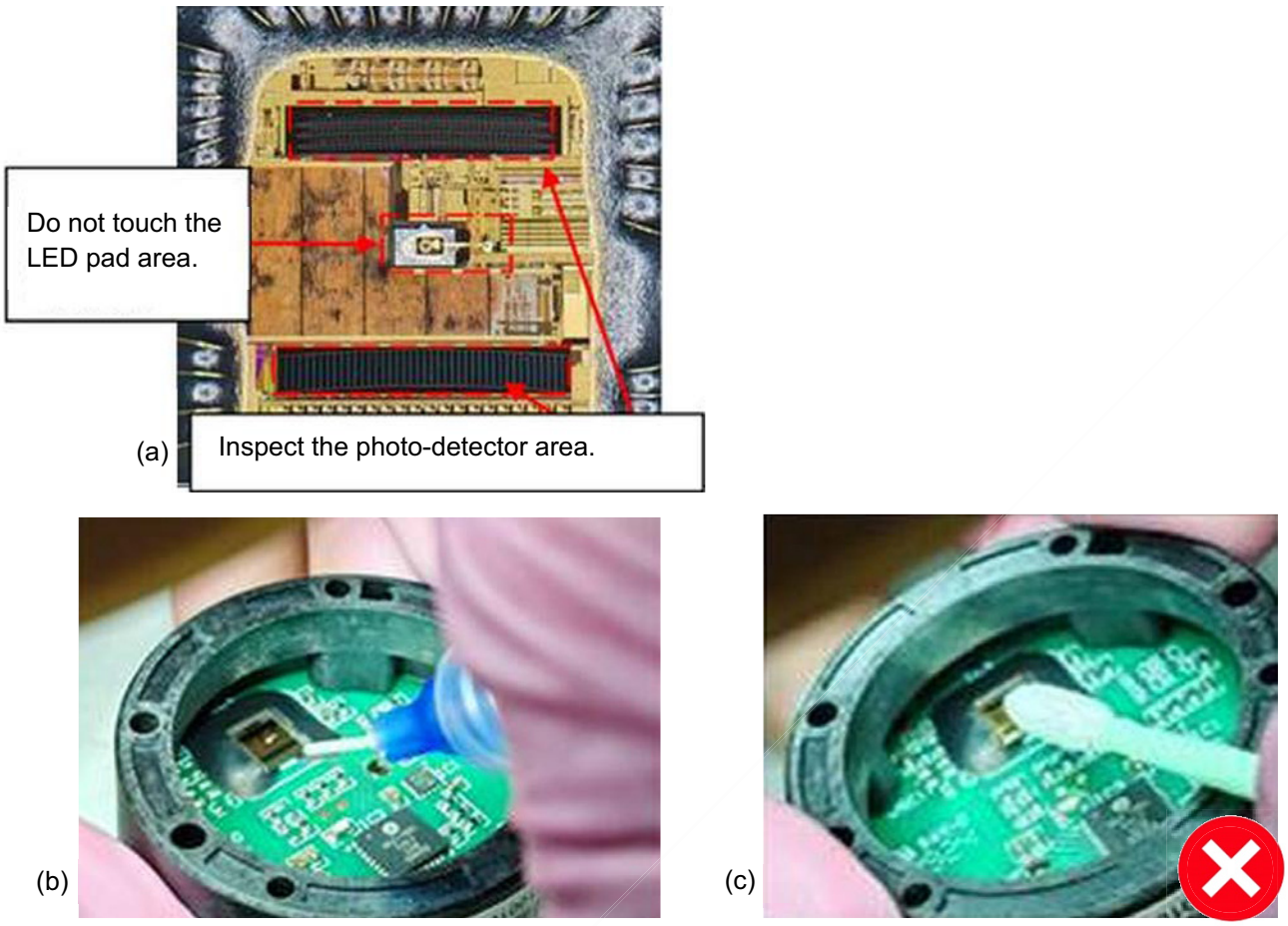
a. Write 1 to execute one time clear command. Only one command bit should be triggered for each time.

Trouble Shooting Guide

No.	Description	Causes	Counter Measure
1	No output	Encoder power supply too low	Check if Vcc versus ground potential is within 4.5V~5.5V,
		Poor connectivity between encoder connector to customer connector	Check the encoder connector and customer connector connectivity.
		Wrong wire connection assignment	Check the connector wire connection assignment.
		Detector IC faulty/shorted	Perform power cycle. If problem still exists, please consult factory.
		Transceiver faulty/shorted	Where applicable, ensure proper line terminating resistors are used.
		Wrong baud rate used for RS485	Check if the host and encoder are communicating at the correct baud rate.
		Wrong bit lengths used for BiSS-C communications	1. Ensure the host clock numbers are set accordingly to the encoder resolutions, 2. Follow the BiSS-C multi-cycle requirements for register access,
2	Encoder high current consumption (>200 mA at 25°C)	LED faulty/shorted	Check encoder PCBA to ensure no accidental damage to the LED,
		Detector IC faulty/shorted	Check the encoder connector and customer connector connectivity.
		Transceiver faulty/shorted	
3	XCErr triggered	Multi-turn block faulty	Ensure proper shielding and no exposure to a strong magnetic field source. Clear the alarm and power cycle after the disturbance source is removed.
4	MemoryErr triggered	Memory block faulty	
5	Multi-turn Counting Error triggered	Multi-turn block faulty	Ensure the MT calibration is done correctly.
6	LedErr triggered	LED faulty	
		Codewheel is blocked	Ensure no contaminations on the codewheel surface.
7	LisErr triggered	LED faulty	Clean the codewheel and perform a power cycle. If the problem still exists, consult factory.
		Single-turn block faulty	
		Codewheel issue	
8	MLSErr triggered	LED faulty	
		Single-turn block faulty	
		Codewheel issue	
9	Single-turn Counting triggered	Single-turn block faulty	
		Codewheel issue	

Cleaning of Codewheel and Encoder Module

Figure 36: Photo Detector Surface Inspection and Cleaning



NOTE:

- (a) Inspect the photo-detector area to ensure that there is no dust or oil/grease contamination.
- (b) Only use the air blower with a soft Teflon needle to blow away any dust particles on the photo-detector area.
- (c) Do not use a cleaning cotton bud/swab for cleaning the photo-detector area. Scratches to the dice surface might damage the encoder ASIC.

CAUTION! Do not touch the LED pad area with any cleaning instrument.

Dos and Don’ts

Do

1. Ensure a clean environment during installation.
2. Ensure that the encoder power supply is within 5V ± 10%.
3. Provide adequate protection from dust and moisture when using in a harsh environment.
4. Ensure that the connector-cable assembly follows the pin configuration, in accordance with the product data sheet.
5. Observe all ESD precautions when installing or handling of the encoder.
6. Ensure that the magnetic shield is designed in accordance with the recommendations in this application note.

Don’t

1. Do not overload the transceiver by using the wrong termination resistor.
2. Do not hammer the codewheel hub into the motor shaft during installation.
3. Do not reverse the power source polarity.
4. Do not operate the encoder under extreme temperatures over an extended time.
5. Do not place the magnet-hub in direct contact with the EH sensor.
6. Do not place the encoder module in close proximity to a strong magnet.

Packing Information

Table 50: Encoder Packing Information

Packing Unit	Quantity
Unit per tray	Maximum: 16 pieces
Unit per pizza box	Maximum: 32 pieces
Tray per pizza box	Maximum: 2 trays for 1 pizza box
Pizza box per carton box	Maximum: 6 pizza boxes

Figure 37: Example of the Encoder Module and Codewheel Packing within a Packaging Tray

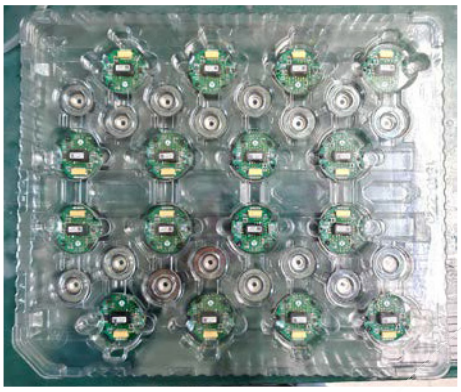


Figure 38: Packing Box and Carton Information

34 cm (L) x 28 cm (W) x 8 cm (H)

62 cm (L) x 34 cm (W) x 28 cm (H)

Accessories Information

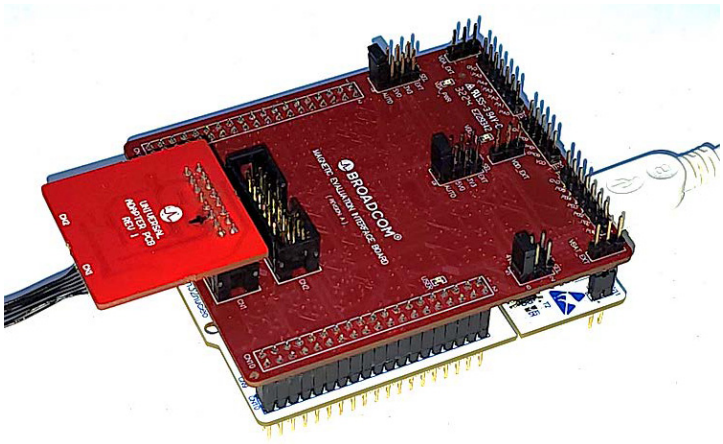
No.	Part Number	Description
1	AS20-C300	8-pin mating connector with 300-mm cable length, 100 pieces SPI.
2	AR49-M49-E01	Programming Kit (applicable for all protocol options). Contents: 1 unit of MCU based programming kit, 1 unit of USB cable for PC interface, DUT cable, and the associated programming software.
3	AR25-AC25	Accuracy Calibration Station for AR25/AR49 Series Rotary Reflective Encoder. Contents: Mechanical setup including servo motor control, high accuracy reference encoder, programming kits, associated cables assemblies (for PC interface, motor handler communication, DUT encoder connection), and the associated GUI programming software.

AR49-M49-E01 Programming and Calibration Kit

Broadcom offers a simple USB powered programming kit, together with a PC-based custom GUI program for users to perform the necessary calibration or to program in the desired encoder settings.

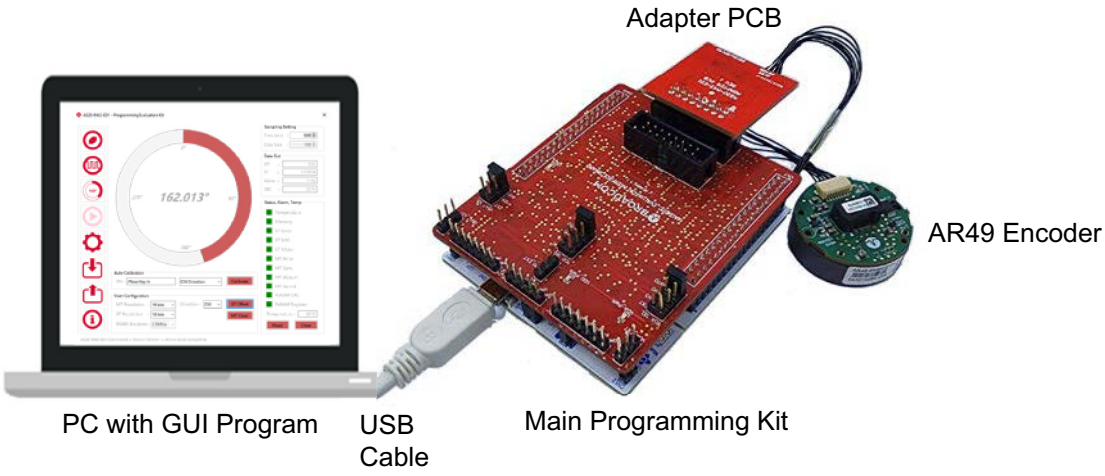
By connecting to the AR49-M49-E01 programming kit, users can communicate to the AR49 series encoders based on the communication protocol option of the DUT encoder.

Figure 39: AR49-M49-E01 Programming Kit with the Adapter Board Attached



CAUTION! The programming kit has exposed connector pins at both the top and bottom sides. Do not place the kit on top of a conductive surface.

Figure 40: AR49-M49-E01 Programming Kit Connection



The AR49 series encoder is connected to the AR49-M49-E01 Programming Kit via the dedicated adapter PCB. There are two 8-pin connectors on the adapter PCB for connection to the encoder depending on the protocol options. Only one of the connector should be connected one at a time, according to the protocol option.

Table 51: Pins Assignment on the AR49-M49-E01 Adapter PCB

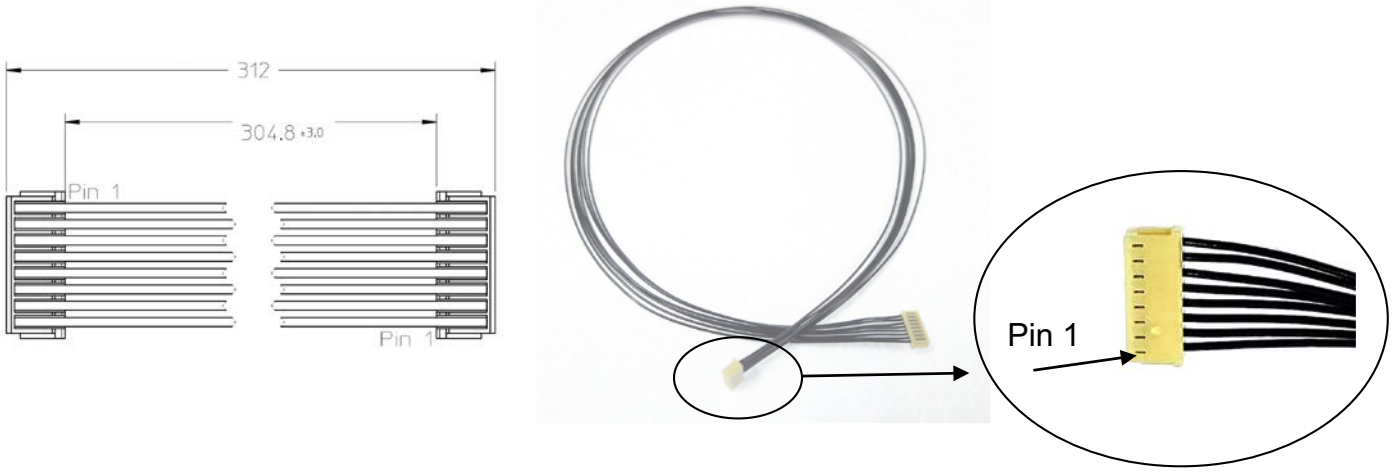
Pin No.	Connector1: SSI 2-Wire/BiSS-C/SPI 4-Wire	Connector 2: RS485
1	SEL1	NC
2	SEL0	NC
3	DATA-/SLO-/SPI-DIN/MOSI	DATA-
4	DATA+/SLO+/SPI-DO/MISO	DATA+
5	SCLK-/MA-/SPI-CLK	NC
6	SCLK+/MA+/SPI-NCS	NC
7	0V	0V
8	+5V	+5V

NOTE:

- Only one of the connectors should be connected one at a time, according to the protocol option.
- Pin 1 at the adapter PCB is connected to Pin 8 of the AR49 encoder, other pins are also reversed accordingly.
- The SSI option is configured via the shared SPI pins and setting the correct logic level to the SEL0 pin. SPI is enabled when SEL0 = Hi, while SSI is enabled when SEL0 = Lo. SEL1 = Lo by default.
- For SSI option, the SPI-CLK and SPI-NCS lines require a strong driver current to overcome the built-in 120Ω terminating resistance of the SSI SCLK lines. The programming kit has a buffer circuit included for this purpose.

AS20-C300 Cable Assembly

Figure 41: AS20-C300 Cable-Connector Assembly



NOTE:

- Dimensions are in millimeters.
- The 300-mm cable assembly has the mating connectors, 1.0-mm Pitch JST 08-SR, at both ends of the termination.

AR25-AC25 Accuracy Calibration System

The AR25-AC25 calibration system combines both the ST and MT signal calibration together with the position accuracy correction for the AR49 encoders.

The Once Around Correction (OAC) and Interpolation Error Correction (IEC) are performed on the AR49 encoder module. This is to reduce contributing factors such as motor shaft radial run-out, encoder codewheel to hub eccentricity, and mismatch in dimension tolerance between the hub's inner diameter to motor shaft. The AR49 OAC and IEC features compensate the mounting assembly and signal interpolation errors electronically.

This Accuracy Calibration Station is developed as a reference tool to enable customers to perform accuracy calibration on the AR49 encoder to the required optimum accuracy performance.

Figure 43 shows the graphical user interface of the programming software. The test list is defined by using a customizable test script file.

Figure 42: Overview of the Calibration System

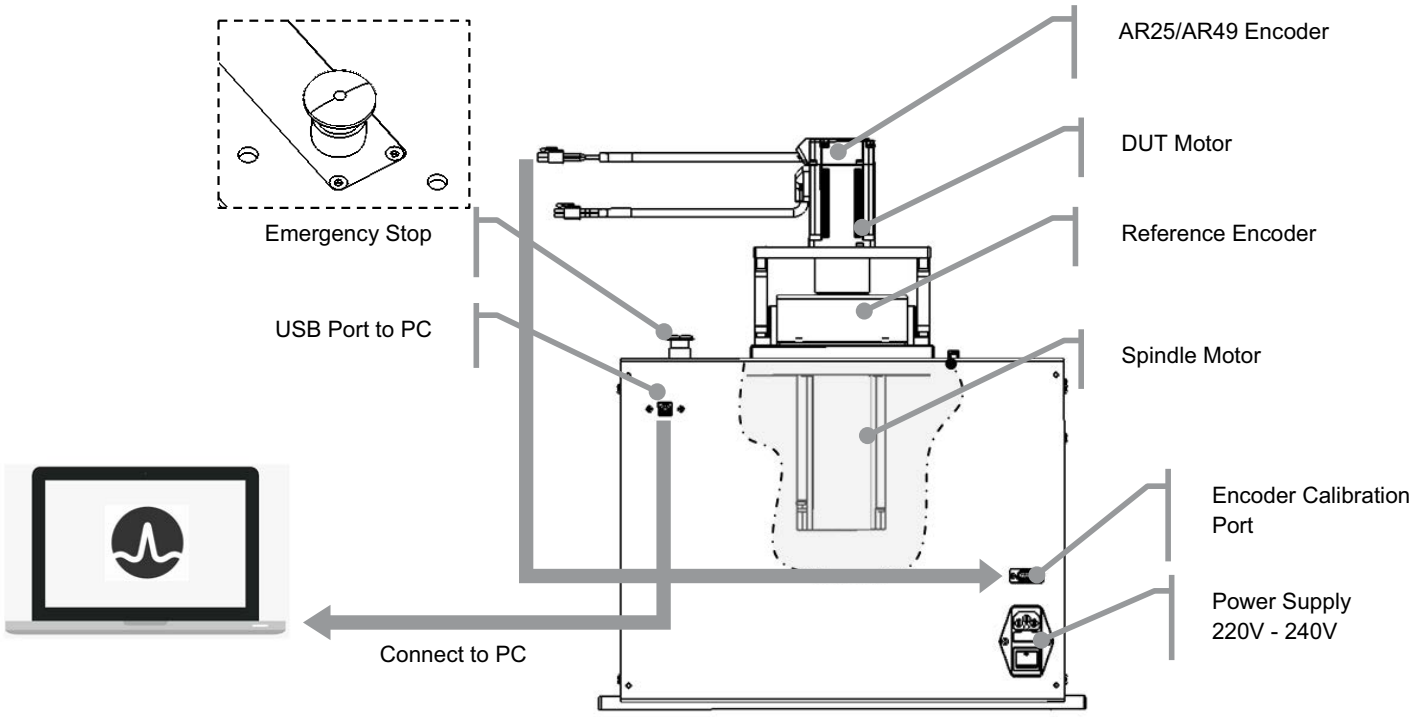


Figure 43: User Interface of the Calibration Software in Ready Mode