Ultra Low-Power 100 Mbps Ethernet Media Converter

GENERAL DESCRIPTION

The AL2100 is designed for media converter applications. It is intended for 100 Mbps Fast Ethernet fiber optic-to- twisted pair media converter designs. The device provides a PECL interface for use with media connectors such as the 1300 nm fiber optic module. The AL2100 is compatible with IEEE 802.3 100Base-FX and 100Base-TX standards.

The AL2100 provides additional functionality such as fault propagation, redundancy for fault-tolerant system design, and remote loopback for diagnostic support.

FEATURES

- Power supply: 2.5V
- 100 Mbps media converter: fiber-to-fiber or fiber-to-twisted pair
- Full duplex or half duplex
- Auto-negotiation on twisted pair PHY
- 48-pin TQFP
- Industrial temp (-40°C to +85°C)
- 0.25µm CMOS
- Fully compliant with IEEE 802.3 / 802.3u
- Baseline wander compensation
- Multifunction LED outputs
- HP auto-MDI/MDIX
- Diagnostic register
- Fault propagation
- Redundancy for fault tolerant system design

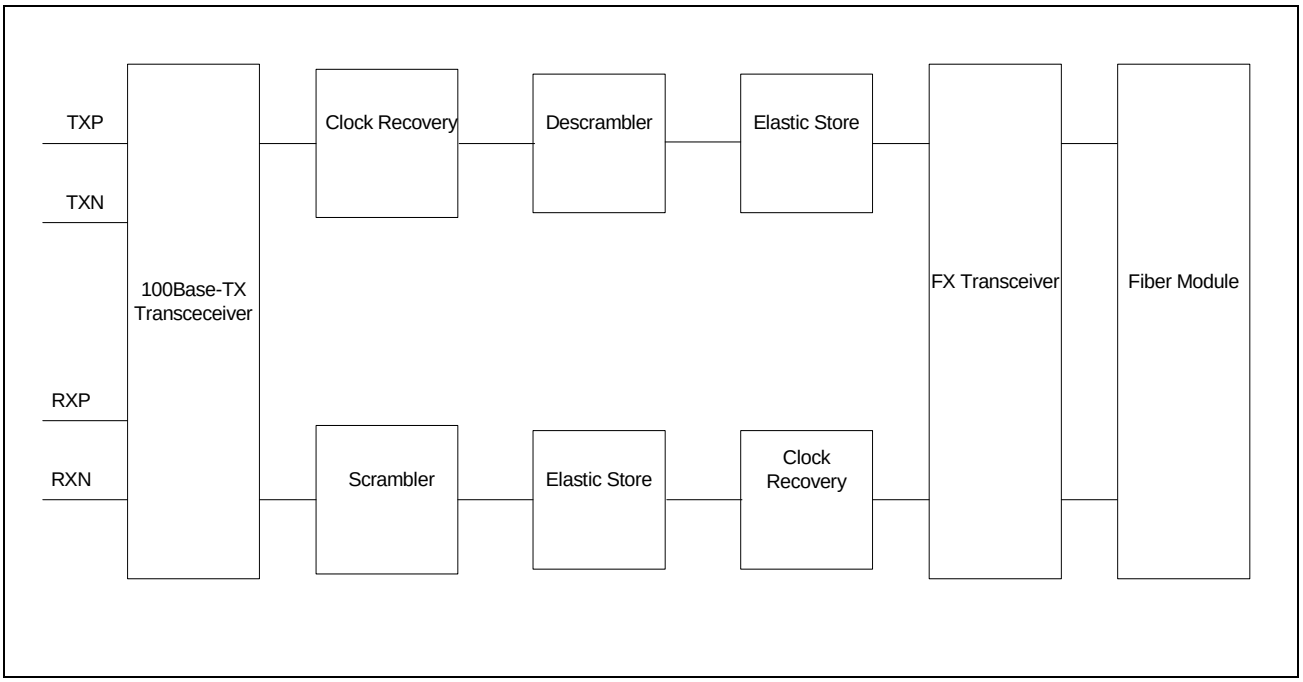

Figure 1: System Block Diagram

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REVISION HISTORY

Revision	*Date*	*Change Description*
AL2100-DS01-405-R	11/11/02	First revision
AL2100-DS00-R	2/22/02	Initial release

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The AL2100 (Figure 2) contains a physical layer interface (PHY) for 100BASE-TX and a PHY for 100BASE-FX networks. The PHY contains all the necessary functions such as elastic store, quantizer, and driver circuits to complete a media converter design. The device converts the MLT3 scrambled symbols from the twisted-pair (TP) input port into 4B5B NRZI encoded data, and transmits it over fiber media. The 4B5B NRZI encoded data from the fiber-input port is converted to a scrambled MLT3 symbol stream for TP transmission.

The device also supports far-end fault detection (fiber-only) and link status propagation. If any port is in a link-fail state, the device ceases to transmit data, and disables the appropriate output port. The device is transparent in regard to the connecting links. The media converter uses an elastic store to retime the received signal.

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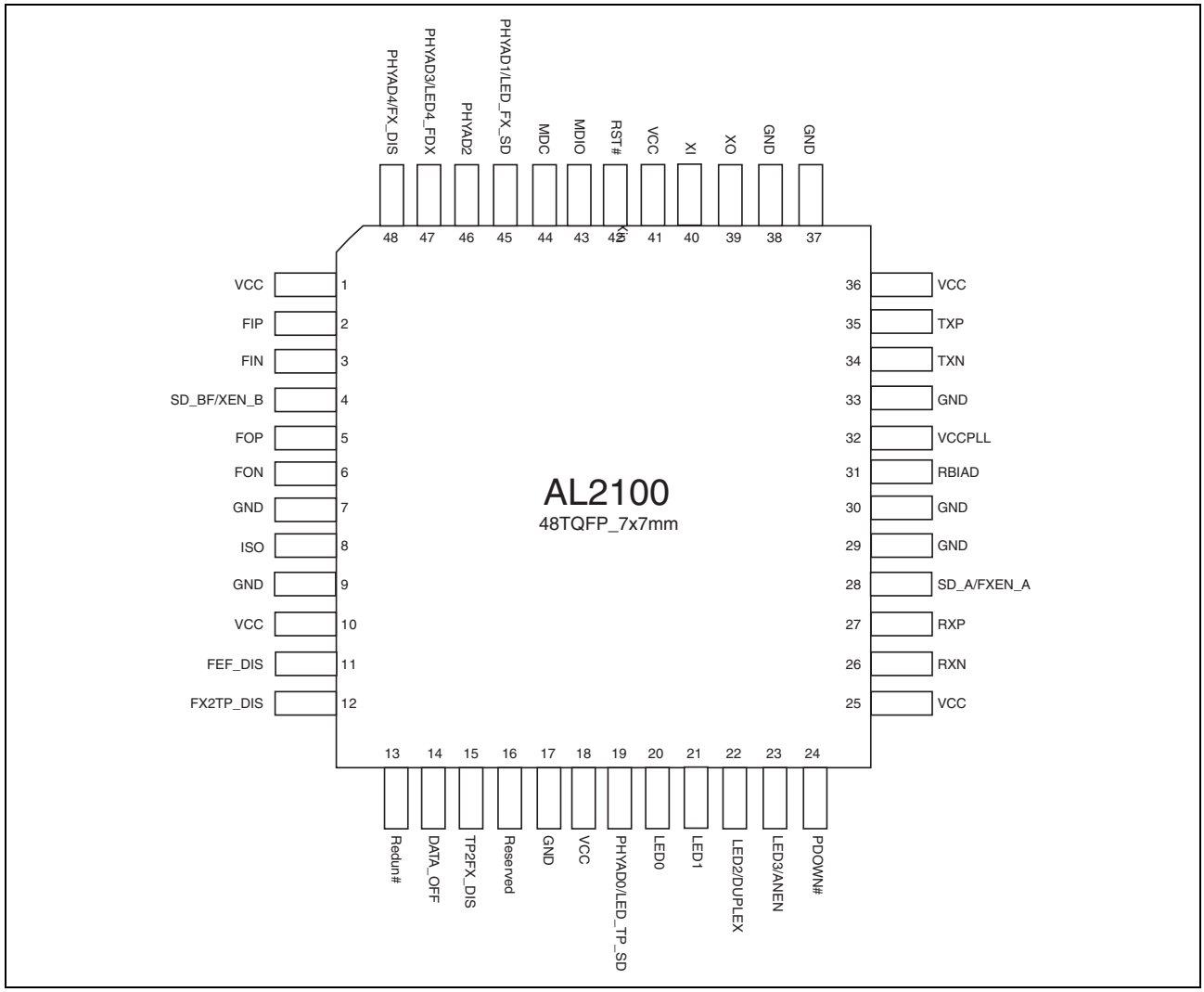


Figure 2: AL2100 Pin Out

Section 2: Pin Descriptions

Signal Types:

P = Power pin

G = Ground pin

AI = Analog Input pin

AO = Analog Output pin

D = Digital Pull-Down pin

U = Digital Pull-Up pin

$\overline{\text{OVERLINE}}$ = Active Low

B = Bi-directional digital pin

Table 1: Pin Descriptions

Name	*Number*	*Type*	*Description*
VCC	1	P	2.5V supply.
FIP	2	AI	FX PECL input +
FIN	3	AI	FX PECL input -
SD_B/FXEN_B	4	AI	SD_B/FXEN_B: multilevel threshold input. When the input level is 0V, the FX module is disabled. When the input is > 1V, the FX module is enabled, and this pin is used as the SD input with the PECL threshold.
FOP	5	AO	FX PECL output +
FON	6	AO	FX PECL output -
GNDFX	7	G	Ground.
GND	7	G	Ground.
ISO	8	BD	ISO (reset-read Input): pull high to isolate the TP PHY.
GND	9	G	Digital Ground.
VCC	10	P	2.5V supply.
FEF_DIS/Reserved	11	BD	FEF_DIS (reset-read input): pull high to disable the remote fault function in the fiber PHY, i.e. fiber-to-fiber fault propagation disable. Output function is reserved.
FX2TP_DIS/Reserved	12	BD	FX2TP_DIS (reset read Input): pull high to disable fiber-to-twisted-pair fault propagation. Output function is reserved.
$\overline{\text{REDUN}}$/Reserved	13	BD	$\overline{\text{REDUN}}$: redundancy function input. Input low to activate the chip; input high to put the chip in backup mode. For the primary chip, this pin is pulled low. For the secondary chip, this pin is connected to the DATA_OFF pin of the primary chip. Output function is reserved.
Reserved/DATA_OFF	14	BD	Input function is reserved. DATA_OFF: (output) high to put the secondary chip in backup mode. For the primary chip, this pin is connected to the $\overline{\text{REDUN}}$ of the secondary chip.
TP2FX_DIS/Reserved	15	BD	TP2FX_DIS (reset read Input): pull high to disable twisted pair-to-fiber fault propagation. Output function is reserved.
Reserved	16	BD	Input function is reserved. This pin is always pulled low.
GND	17	G	Ground.

Table 1: Pin Descriptions

Name	Number	Type	Description
VCC	18	P	2.5V supply.
PHYAD0/ LED_TP_SD	19	BU	PHYAD0 (reset read Input): pull high or low to set the PHY address bit 0 for serial management function. LED_TP_SD (output): indicates energy is detected on the twisted-pair input. The active level is the invert of the reset read value.
LED0	20	BU	Pull this pin high. LED0 (output): low active. The default behavior blinks when the twisted-pair port detects receive activity.
LED1	21	BU	Pull this pin high. LED1 (output): low active. The default behavior is ON when the twisted-pair port in link-up condition.
DUPLEX/LED2	22	BU	DUPLEX (reset read Input): sets the duplex capability for twisted-pair port auto-negotiation function. LED2 (output): the active value is the invert of the DUPLEX input level. The default behavior blinks when the fiber port detects receive activity.
ANEN/LED3	23	BU	ANEN (reset read input): auto-negotiation enable for the twisted pair port. LED3 (output): the active value is the invert of the ANEN input level. The default behavior is on when the link-up condition is detected on the fiber port, and blinks when the remote fault condition is detected on the fiber port.
$\overline{\text{PDOWN}}$	24	IU	$\overline{\text{PDOWN}}$ (low active input): pull low to put both TP and fiber ports into power-down mode. This is a regular input, not a reset read signal.
VCC	25	P	2.5V supply.
RXN	26	A	Receive – for TP port in MDI mode. Transmit – for TP port in MDIX mode.
RXP	27	A	Receive + for TP port in MDI mode. Transmit + for TP port in MDIX mode.
SD_A/FXEN_A	28	AI	SD_A/FXEN_A: (multithreshold input): pull low to disable the FX function on the twisted pair (TP) port. PECL input level to enable the FX function of the TP port. PECL high level to indicate the signal detect from the connected fiber module.
GND	29	G	Ground.
GND	30	G	Ground.
RBIAD	31	A	Bias resister connection. Connect to a 10K 1% resister to GND
VCCPLL	32	P	VCC for Analog Bias, PLL modules.
GND	33	G	Ground for transmit circuit.
TXN	34	A	Transmit – in MDI mode. Receive – in MDIX mode.
TXP	35	A	Transmit + in MDI mode. Receive + in MDIX mode.
VCC	36	P	2.5V supply.
GND	37	G	Ground
GND	38	G	Ground
XO	39	AO	XO (Output): crystal output.
XI	40	AI	XI (Input): crystal input. XI and XO pins are designed to connect to a 25 MHz, 50-PPM crystal. When using an oscillator, connect the XI pin to the oscillator, and leave the XO pin unconnected.
VCC	41	P	2.5V supply.
$\overline{\text{RST}}$	42	IU	Reset input is active low.

Table 1: Pin Descriptions

Name	*Number*	*Type*	*Description*
MDIO	43	BU	MDIO (input/output): management data I/O. This serial input/output pin is used to read from and write to the MII register. The data value on the MDIO pin is valid, and latched on the rising edge of MDC. This pin requires a 1 K Ohm resistor pull-up.
MDC	44	BD	MDC (Input): management data clock. The MDC clock input must be provided to allow serial management functions. This pin has a SCHMTT-trigger input.
PHYAD1/LED_FX_SD	45	BD	PHYAD1 (reset-read input): pull high or low to set PHY address bit 1 for serial management functions. LED_FX_SD (output): LED output for fiber signal detects. The active level is the invert of the reset read value.
PHYAD2/Reserved	46	BD	PHYAD2 (reset-read input): pull high or low to set PHY address bit 2 for serial management functions. Output function is reserved.
PHYAD3/LED4_FDX	47	BD	PHYAD3 (reset-read input): pull high or low to set PHY address bit 3 for serial management functions. LED4_FDX (output): The default behavior is on when the result of the auto-negotiation on the twisted pair port is full duplex. This LED pin is fully programmable. The active level is the invert of the reset read value.
PHYAD4/FX_DIS	48	BD	PHYAD4 (reset-read input): pull high or low to set PHY address bit 4 for serial management functions. FX_DIS (output): disable fiber output. The active level is the invert of the reset read value.

Section 3: Functional Description

The AL2100 contains a physical layer interface (PHY) for 100BASE-TX, and a PHY for 100BASE-FX networks. The PHY contains all the necessary functions, such as elastic store, quantizer, and driver circuits, to complete a media converter design. The device converts the MLT3 scrambled symbols from the twisted-pair (TP) input port into 4B5B NRZI encoded data, and transmits it over the fiber media. The 4B5B NRZI encoded data from the fiber-input port is converted to a scrambled MLT3 symbol stream for TP transmission.

The device also supports far-end fault detection (fiber-only), and links status propagation. If any port is in a link-fail state, the device cease transmitting data, and disables the appropriate output port. In essence, the device is transparent in regard to the connecting links. The media converter uses an elastic store to retime the received signal.

The AL2100 supports redundant link applications. A redundant link can be formed by either a switch with the 100BASE-FX transceiver that supports far-end fault signaling or two AL2100s. In the event of a link failure, the redundant link is automatically established.

100BASE-TX TO 100BASE-FX CONVERSION

The AL2100's 100BASE-TX receiver receives the scramble MLT3 signals, and passes them to the clock recovery circuit for data/clock extraction.The device de-scrambles the signals, and decodes them into an NRZ data stream. The signal is then passed through elastic-store circuitry for retiming. The resulting signal is converted into a serial NRZI data stream, and sent to the 100Base-FX transmitter.

100BASE-FX TO 100BASE-TX CONVERSION

The AL2100's 100BASE-FX receiver receives the NRZI data stream through the PECL receiver inputs, and passes them on to the clock recovery circuit for data/clock extraction. The device feeds the signals through elastic-store circuitry for retiming and encoding the NRZI data, and conversion to scramble MLT3 signals. The signals are sent to the 100BASE-TX transmitter.

FULL DUPLEX APPLICATION

The ideal function of a media converter chip provides a full-duplex transparent media link. The AL2100 supports full IEEE 802.3-compliant auto-negotiation functions. Auto-negotiation can be enabled to negotiate with the link partner for full-duplex applications.

ELASTIC STORE

The AL2100 provides an on-chip elastic store. With the elastic store in place, the device retimes the received signal, and removes jitter. In order to reduce the latency, preambles are inserted to the packet.

FAULT PROPAGATION

Three types of fault propagation are provided using the following logic:

```
TP_RCVR_ACTIVE = Wait_For_Link || TP_Link_Up;
TP_OUTPUT_EN = (FX_LINK_UP || FX2TP_DIS) && DATA_ENABLE;
FX_OUTPUT_EN = TP_RCVR_ACTIVE || TP2FX_DIS;
```

FIBER-TO-FIBER

This is the same as the remote fault function. When remote fault is disabled, the AL2100 disables the FX transmission if the received SD fails.

FIBER-TO-TWISTED PAIR

This operation can be controlled via the FX2TP_DIS signal. This signal is only defined in AL2100 normal operation mode, not in RMII testing mode. This is a reset read signal.

When this type of fault propagation is enabled, the failure of the FX link shuts down the twisted pair output.

TWISTED PAIR-TO-FIBER

This operation is controlled via the TP2FX_DIS signal. This signal is only defined in AL2100 normal operation mode. This is a reset read signal. When this type of fault propagation is enabled, the absence of receiving energy shuts down the fiber transmission to inform the fiber link partner about the link failure.

The AL2100 propagates idle signals from media-to-media. After reception of the idle signal (all ones), the device transmits an idle signal to the opposite ports, i.e. TP-to-fiber or fiber-to-TP. There are two types of link failure—receive or remote fault— also known as far-end fault.

TP Receive Link Failure

In the event of a TP-receive-link failure, the AL2100 ceases to transmit an idle signal to the fiber-optic driver. A valid TP link signal can be either a 10BASE-T link pulse or a 100BASE-TX idle signal.

Fiber Receive Link Failure

In the event of a fiber-receive-link failure, the AL2100 ceases to transmit an idle signal to the TP driver, and puts the driver into high-impedance mode. The device also sends a remote fault signal to the fiber-optic driver in addition to de-asserting the DATA_OFF signal.

TP Transmit Link Failure

In the event of a TP transmit link failure, the TP far-end transceiver ceases to transmit an idle signal, and starts transmitting FLP to the AL2100. Because the AL2100 does not understand FLP, it continues to transmit an idle signal to the fiber-optic driver.

Fiber Transmit Link Failure

In the event of a fiber-transmit-link failure, the far-end transceiver, with remote fault signaling capability, transmits the RF signal to the AL2100. As a result, the AL2100 performs two tasks: ceases to transmit an idle signal to the TP driver, and puts the driver into high-impedance mode,de-asserting the DATA_OFF signal.

REDUNDANT FUNCTION

```
FAULT_OUT = DATA_ENABLE && !FX_LINK;
```

The logic above uses the TP_RCVR_ACTIVE signal to gate the FX output. When the TP receiver is disconnected, it forces the FX side to drop the link, and causes the TP at the remote side to drop the link as well. When both sides receive activity in the TP side, the FX port on each side is enabled, and the link-up occurs. The link status of the FX port enables the TP output, and causes them to link up. The FX remote fault condition is generated by the standard FEF_DETECT state machine.

Three timers generate the TP_RCVR_ACTIVE signal. The first one is the activity_timer; the second one is the link_up_timer; the third is the tx_disable_timer. When using the activity_timer to determine whether there is a signal on the wire, start the link_up_timer, and wait for the AN to complete. If the link_up_timer expires, start the tx_disable_timer, and disable FX_OUPUT_EN and TX_OUTPUT_EN for a predefined period of time. See Figure 3 for more details.

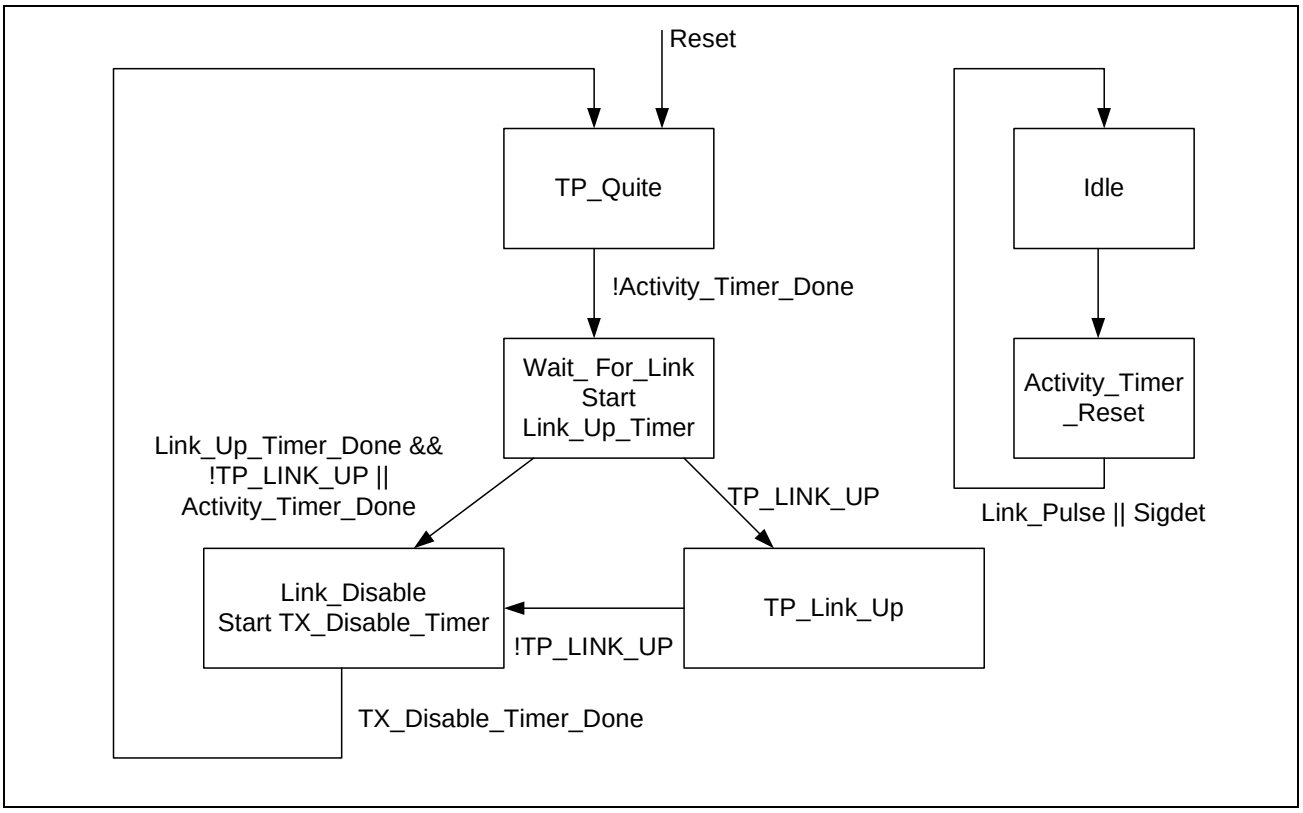


Figure 3: State Machine for Redundant Function

REDUNDANT LINK

The AL2100 supports redundant links through the use of the DATA_OFF and $\overline{\text{REDUN}}$ signals. The redundant link function is only available for the fiber port. An implementation of a redundant link is shown in Figure 4. The redundant link can also be configured with two fiber switch-ports, a far-end fault signaling support required, and two AL2100s.

There are two scenarios: either redundant link transmits a link fault or the receive link fault triggers the redundant link.

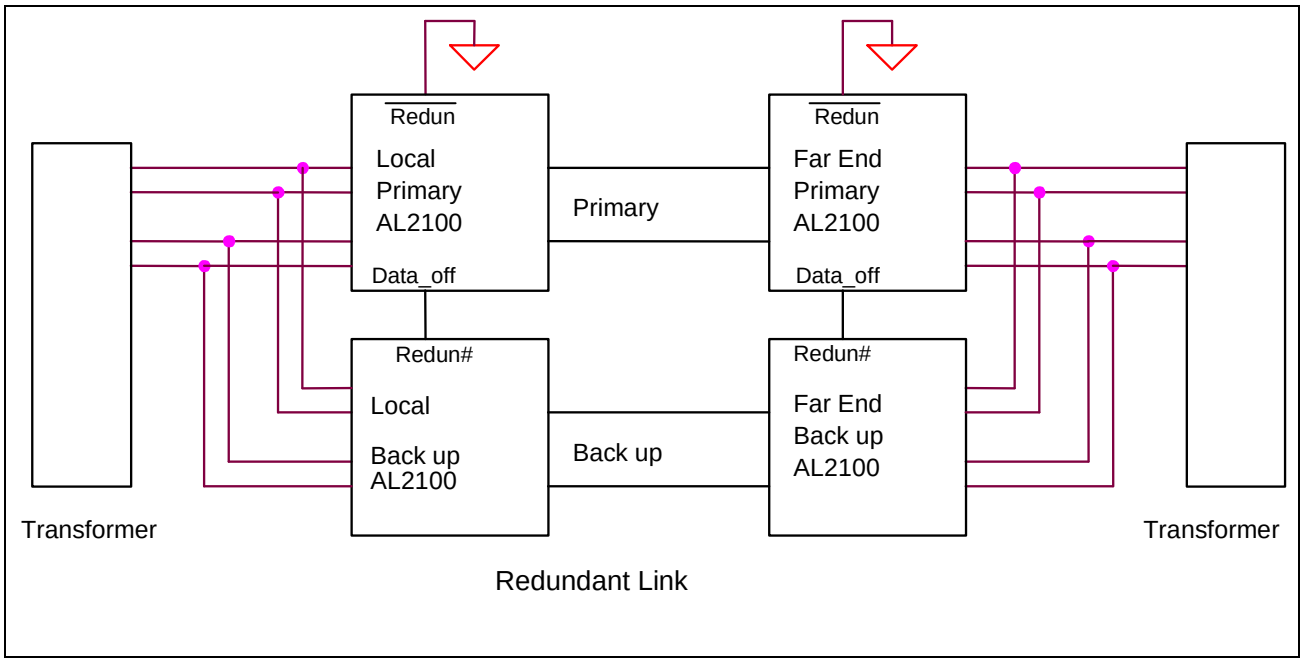


Figure 4: Redundant Link

RECEIVE LINK FAULT

In the event of a receive-link failure, the receiver goes into a link-down mode. The AL2100 takes the following actions:

- Starts transmitting the remote fault signal
- Puts the TXP and TXN pins in high-impedance mode
- De-asserts the DATA_OFF signal

The far-end primary transceiver is normally in a link-up state, and a back-up transceiver is in a link-fail state. During receive-link failure, the local AL2100 enables data transmission of the backup transceiver by asserting the $\overline{\text{REDUN}}$ signal. The backup AL2100 starts sending copies of the transmit signal. The primary far-end receiver that receives the RF signal enters the link-fail state. The back-up transceiver exits the link-fail state upon receiving a signal from the local AL2100, re-establishing the link. When the primary link is repaired, the $\overline{\text{REDUN}}$ is de-asserted.

TRANSMITS LINK FAULT

The 100BASE-FX specification provides a way to detect a transmit-link failure. Whenever a fiber receiver experiences a receive-link failure, it transmits a far-end fault signal. The far-end fault signal is indicated by the far-end fault IDLE signal (84

ones followed by a zero). When the AL2100 receives the far-end fault signal, it is notified by the far-end station that a transmit-fault occurred. The device goes into a link-down state, and takes the following actions:

- Puts the TXP and TXN pins in high-impedance mode
- De-asserts the DATA_OFF signal

The data transmission is assumed by the backup AL2100, and starts sending copies of the signals. Upon re-establishment of the primary fiber, DATA_OFF is asserted, and the backup data link is turned off.

LED INDICATORS

LED Output

All the LED pins in the AL2100 are multifunction I/Os. Their input is used in the reset-read operation for the secondary definition. All LED pins have internal pull-ups. The ON output value depends on the reset-read value of the LED pin. When the reset-read value is high, the default for all LED pins, the ON output value is low. When the reset read value is low, the ON output value is high.

Default LED formats are given in Table 2.

Table 2: LED Formats

LED	*Format*
LED0	RxAct_TP (Blink)
LED1	Link_TP (ON)
LED2	RxAct_FX (Blink)
LED3	Link_FX (ON) / Remote_Fault (Blink)
LED4	DUPLEX_TP (ON)

These LEDs can be configured into different modes. To configure the LEDs to work with other operation mode other than default mode, see ”LED Configuration” on page 10.

Note **LED connections and the source/sink current depend on the default setting.**

The AL2100 also support the following LEDs:

- LED4_FDX: default defined as full-duplex of auto-negotiation resulting on the TP port.
- LED_FX_SD: signal detects on Fiber PHY. This LED set by hardware pin 45 cannot be programmable.
- LED_TX_SD: receiving energy detects on the TP port. This LED is set by hardware pin 19, and cannot be programmable

LED CONFIGURATION

The LED interface is fully configurable via the common register setting. See Table 3.

Table 3: Events for LED Operation

Bit	*Events Description*
7	RxAct_FX
6	Link_FX
5	Link_TP
4	DUPLEX_TP
3	TxAct_TP
2	Remote_fault
1	N/A
0	RxAct_TP

Each LED has two 16-bit registers that define the operation. See "Common Registers" on page 27 for details.

SERIAL MANAGEMENT INTERFACE

MII management access is performed via pin MDC and MDIO. The MDC input pin is SCHMTT triggered to avoid noise on this bused signal.

The PHY's internal registers are accessible only through the MII 2-wire Serial Management Interface (SMI). MDC is a clock input to the PHY, which is used to latch in or out data and instructions for the PHY. The clock can run at any speed from DC to 25 MHz. MDIO is a bi-directional connection used to write instructions to, write data to, or read data from the PHY. Each data bit is latched either in or out on the rising edge of MDC. MDC is not required to maintain any speed or duty cycle, provided no half cycle is less than 20 ns, and that data is presented synchronous to MDC.

MDC and MDIO are a common signal pair to all PHYs on a design. Therefore, each PHY must have its own unique physical address. The physical address of the PHY is set by using the pins defined as PHYAD[4:0]. These input signals are strapped externally, and sampled as reset is negated. At idle, the PHY is responsible to pull the MDIO line to a high state. Therefore, a 1K Ohm resistor is required to connect the MDIO line to VCC.

PHY ADDRESSES

Two PHY addresses are taken under AL2100 mode. One is PHYAD [4:0], and the other is PHYAD [4:0] + 1. The first one is for twisted-pair PHY; the second is for fiber PHY.

The PHY addresses are set via the PHYAD4, PHYAD3, PHYAD2, PHYAD1, and PHYAD0 signals.

CLOCK SOURCE

The clock source for this chip is from the XI signal.

In normal operation mode (media converter), the XI signal is connected to a 25 Mhz, 50 PPM Oscillator or XI and XO signals are connected to a 25 MHz, 50 PPM Crystal.

POWER SOURCE

A single 2.5 V is supplied for all digital and analog operations.

100BASE-TWISTED PAIR PHY

GENERAL DESCRIPTION

The twisted pair PHY performs all of the physical layer interface functions for 100Base-TX full or half-duplex on CAT5 twisted pair cable. The 100Base-TX PHY performs encoder/decoder, link monitor, auto-negotiation selection, adaptive equalization, clock/data recovery, baseline wander correction, multimode transmitter, scrambler/descrambler, far-end fault (FEF), and auto-MDI/MDIX. It is fully compliant with the IEEE 802.3 and 803.3u standards.

ENCODER/DECODER

In 100Base-TX mode, the AL2100 transmits and receives data streams on twisted pair. When the MII transmit enable is asserted, nibble wide (4-bit) data from the transmit data pins is encoded into 5-bit code groups, and inserted into the transmit data stream. The 4B5B encoding is shown in the 4B/5B CODE-GROUP table. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start-of-stream delimiter (J/K codes), and appending an end-of-stream delimiter (T/R codes) to the end of packet. When the MII transmit error input is asserted during a packet, the error code group (H) is sent in place of the corresponding data code group. The transmitter repeatedly sends the idle code group between packets.

In 100Base-TX mode, the encode data stream is scrambled by a stream cipher block, and serialized and encoded into the MLT3 signal level. A multimode transmit DAC (digital to analog converter) is used to drive the MLT3 data onto twisted pair cable. Following are baseline wander correction, adaptive equalization, and clock/data recovery in 100Base-TX mode. The receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block, and deserialized and aligned into 5-bit code groups.

LINK MONITOR

In 100Base-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. The signal levels are qualified using squelch detect circuits. When no signal, or a certain valid signal, is detected on the receive pair for a minimum period of time, the link monitor enters the link-pass state, and the transmit and receive functions are enabled.

AUTO-NEGOTIATION/AUTO-NEGOTIATION SELECTION

Auto-negotiation selection is on the 100Base-T twisted-pair PHY only; it is not operating in 100Base-Fiber PHY.

In 100Base-TX mode, auto-negotiation can be enabled or disabled by hardware or software control. When the auto-negotiation function is enabled, the 100Base-TX PHY automatically chooses its mode of operation by advertising its abilities, and comparing them with those received from its link partner. The 100Base-TX PHY can be configured to advertise as 100Base-TX full-duplex or 100BaseTX half-duplex.

The default auto-negotiation mode is configured via a reset read value of LED3/ANEN, LED2/DUPLEX. The SPD100 signal is always defaulted to 1. When the SPD100 is set to 0, it is undefined, and the result is unexpected.

Table 4: SPD100 0 Settings

Register and Bit	*Name*	*Description*
Register 0, bit 13	Speed Select	1 = 100Mbps Set to 1 for normal operation. 0 is prohibited.
Register 0, bit 12	ANEN Enable	1 = Enable auto-negotiation 0 = Disable auto-negotiation
Register 0, bit 8	Duplex	The default value is !ANEN && DUPLEX
Register 4, bit 8 / Register 1, bit 14	100Base-TX Full Duplex	The default value of this bit is DUPLEX
Register 4, bit 7 / Register 1, bit 13	100Base-TX	The default value of this bit is ANEN ||!DUPLEX

ANALOG ADAPTIVE EQUALIZER

The analog adaptive equalizer removes inter-symbol interference (ISI) created by the transmission channel media. The PHY is designed to accommodate a maximum of 140 meters UTP CAT-5 cable. An AT&T 1061 CAT-5 cable of this length typically has an attenuation of 31dB at 100 MHz. A typical attenuation of 100-meter cable is 21dB. The worst case cable attenuation is around 24-26dB, as defined by TP-PMD specification. The amplitude and phase distortion from the cable cause ISI, which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pair cable. The equalizer has the ability to change its equalizer frequency response according to cable length. The equalizer tunes itself automatically for any cable, compensating for the amplitude and phase distortion introduced by the cable.

CLOCK RECOVERY

The equalized MLT-3 signal passes through the slicer circuit, and gets converted to NRZI format. The PHY uses a proprietary mixed-signal phase locked loop (PLL) to extract clock information from the incoming NRZI data. The extracted clock is used to retime the data stream, and set the data boundaries. The transmit clock is locked to the 25 MHz clock input, while the receive clock is locked to the incoming data streams. When initial lock is achieved, the PLL switches to the data stream, extracts the 125 MHz clock, and uses it for bit framing for the recovered data. The recovered 125 MHz clock is also used to generate the 25 MHz RX_CLK signal. The PLL requires no external components for its operation, and has high noise immunity and low jitter. It provides fast phase alignment, and locks to data in one transition. Its data/clock acquisition time after power-on is less than 60 transitions. The PLL can maintain lock on run-lengths of up to 60 data bits in the absence of signal transitions. When no valid data is present, i.e. when the SD is de-asserted, the PLL switches and locks onto TX_CLK. This provides a continuously running RX_CLK. At the PCS interface, the 5-bit data RXD[4:0] is synchronized to the 25 MHz RX_CLK.

BASELINE WANDER CORRECTION

A 100Base-TX data stream is not always DC balanced because the receive signal must pass through a transformer. The DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The 100Base-TX PHY automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reduces the chance of a receive symbol error.

Note **The baseline wander circuit is not required in 100Base-FX PHY.**

MULTI MODE TRANSMITTER

The multimode transmitter transmits MLT3 coded symbols in100Base-TX mode, NRZI coded symbols in 100Base-FX mode. It uses a current drive output, which is well balanced, and produces very low noise transmit signals. PECL voltage levels are produced with resistive terminations in 100base-FX mode.

STREAM CIPHER SCRAMBLER/DESCRAMBLER

In 100Base-TX mode, the transmit data stream is scrambled to reduce radiated emissions on the twisted pair cable. The data is scrambled by exclusive ORing the NRZ signal with the output of an 11-bit wide linear feed back shift register (LFSR), which produces a 2047-bit non repeating sequence. The scrambler reduces peak emission by randomly spreading the signal energy over the transmit frequency range, and eliminating peaks at certain frequencies.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle code groups.

The receiver does not attempt to decode the data stream unless the descrambler is locked. When locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization.

The receive data stream is expected to contain interpacket idle periods. If the descrambler does not detect enough idle code within 724 µs, it becomes unlocked, and the receive decoder is disabled. The descrambler is always forced into the unlock state when a link failure condition is detected.

Note **The stream cipher descrambler is not used in the 100Base-FX mode.**

HP-AUTO MDI/MDIX

This feature detects the required cable connection type straight through or crossed over, and makes corrections automatically.

100BASE FIBER PHY

The AL2100 includes a fiber PHY. It can transmit and receive data over fiber-optic cable when paired with an external fiber-optic line driver and receiver. In FX mode, the receive data stream differential PECL level is sampled from the fiber-optic receiver. NRZI decoding is used instead of MLT3. Baseline wander, adaptive equalization, and stream cipher descrambler functions are bypassed.

ENCODER/DECODER

The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the fiber PHY asserts the MII RXER signal. The fiber PHY also asserts RXER for several other error conditions that improperly terminate the data stream. While RXER is asserted, the receive data pins are driven with 4-bit code, indicating the type of error detected. The error codes are listed in Table 42 on page 31.

LINK MONITOR

In 100Base-FX mode, the external fiber-optic receiver performs the signal energy detection function, and communicates this information directly to the SD signal, pin 4.

CLOCK RECOVERY

The digital clock recovery creates all internal transmit and receive clocks. The transmit clock is locked to the 25 Mhz clock input, while the receive clock is lock to the incoming data stream. The clock recovery circuit optimized to MLT3, NRZI. The input data stream is sampled by the recovery clock, and fed synchronously to the adaptive equalizer.

TRANSMITTER

Serialized data bypasses the scrambler and 4B/5B encoder in FX mode. The output data is from the NRZI PECL signals. The PECL level signals are used to drive the fiber-transmitter.

FAR END FAULT (FEF)

Auto-negotiation provides the mechanism to inform the link partner that a remote fault has occurred. However, auto-negotiation is disabled in 100Base-FX applications. An alternative in-band signaling function (FEFI) is used to signal a remote fault condition.

FEFI is a stream of 84 consecutive 1s followed by one logic 0. This pattern is repeated three times.

A FEFI signals only under the following conditions:

- When no activity is received from the link partner
- When the clock recovery circuit detects a signal error or PLL lock error
- When the management entity sets the transmit FEF bit

TRANSMIT DRIVER

The transmit driver does not perform filtering. It uses a current drive output, which is well balanced, and produces a low noise PECL signal. PECL voltage levels are produced with resistive terminations.

Section 4: Register Descriptions

The first seven registers of the MII register set are defined by the MII specification. In addition to these required registers are several Altima Communications, Inc. specific registers. There are reserved registers and/or bits that are for Altima internal use only. The following standard registers are supported.

Note

Register numbers are in decimal format. The values are in hexadecimal (H) or binary format.

When writing to registers, it is recommended that a read/modify/write operation be performed because unintended bits can get set to unwanted states. This applies to all registers, including those with reserved bits.

Legend:

RW = Read and write access

SC = Self-clearing

LL = Latch low until cleared by reading

RO = Read-only

RC = Cleared on read

LH = Latch high until cleared by reading

100BASE-TX PHY REGISTERS

Table 5: Registers 0 through 31

Register	*Description*	*Default*
0	Control Register	3000
1	Status Register	6049
2	PHY Identifier 1 Register	0022
3	PHY Identifier 2 Register	5521
4	Auto-Negotiation Advertisement Register	0181
5	Auto-Negotiation Link Partner Ability Register	41E1
6	Auto-Negotiation Expansion Register	0005
7	Next Page Advertisement Register	2801
8-15	Reserved	XXXX
16	Interrupt Level Control Register	1800
17	Interrupt Control/Status Register is reserved because there is no hardware support.	0000
18,19	Reserved	XXXX
20	Cable Measurement Capability Register	XXXX
21	Receive Error Counter Register	0000
22-31	Reserved	XXXX

CONTROL REGISTER

Table 6: Register 0: Control Register Bit Description

Bit	Name	Description	Mode	Default
15	Reset	1 = PHY reset. This bit is self-clearing.	RW/SC	0
14	Loop back	1 = Enable loopback mode. This loops back TXD to RXD, and ignores all activity on the cable media. 0 = Normal operation.	RW	0
13	Speed Select	Set to 1 for normal operation; 0 is prohibited.	RW	1
12	ANEN Enable	1 = Enable auto-negotiation process (overrides 0.13 and 0.8) 0 = Disable auto-negotiation process. Mode selection is controlled via bit 0.8, 0.13 or through the mode pins.	RW	Set by ANEN
11	Power Down	1 = Power-down all blocks. While in the power-down state, the PHY responds to management transactions. Setting PDOWN, pin 24, to low has the same result. 0 = Normal operation.	RW	0
10	Isolate	1 = Electrically isolate the PHY from MII. PHY still responds to SMI. 0 = Normal operation.	RW	0
9	Restart ANEN	1 = Restart auto-negotiation process. 0 = Normal operation.	RW/SC	0
8	Duplex Mode	1 = Full duplex. 0 = Half duplex.	RW	Set by a mode pin
7	Collision Test	1 = Enable collision test, which issues the COL signal in response to the assertion of the TX_EN signal. Collision test is disabled when the PCSBP pin is high. Collision test is enabled regardless of the duplex mode. 0 = Disable COL test.	RW	0
6:0	Reserved		RW	0000000

STATUS REGISTER

Table 7: Register 1: Status Register Bit Description

Bit	Name	Description	Mode	Default
15	100Base-T4	Permanently tied to 0 indicates no 100BaseT4 capability.	RO	0
14	100Base-TX Full Duplex	1 = 100BaseTX full-duplex capable. 0 = Not 100BaseTX full-duplex capable.	RO	set by DUPLEX pin
13	100Base-TX Half Duplex	1 = 100BaseTX half-duplex capable. 0 = Not TX half-duplex capable.	RO	set by DUPLEX pin
12	10Base-T Full Duplex	1 = 10BaseT full-duplex capable. 0 = Not 10BaseT-full duplex capable.	RO	0
11	10Base-T Half Duplex	1 = 10BaseT half-duplex capable. 0 = Not 10BaseT half-duplex capable.	RO	0
10:7	Reserved		RO	0000
6	MF Preamble Suppression	The PHY is able to perform management transactions without an MDIO preamble. The management interface needs a minimum of 32 bits of preamble after reset.	RO	1

Table 7: Register 1: Status Register Bit Description

Bit	Name	Description	Mode	Default
5	ANEN Complete	1 = Auto-negotiation process completed. Registers 4, 5, and 6 are valid after this bit is set. 0 = Auto-negotiation process not complete.	RO	0
4	Remote Fault	1 = Remote fault condition detected. 0 = No remote fault. This bit remains set until it is cleared by reading Register 1.	RO/LH	0
3	ANEN Ability	1 = Able to perform auto-negotiation function; default value determined by ANEN pin. 0 = Unable to perform auto-negotiation function.	RO	set by ANEN pin
2	Link Status	1 = Link is established. If the link fails, this bit is cleared, and remains at 0 until the register is read again. 0 = Link has gone down.	RO/LL	0
1	Jabber Detect	1 = Jabber condition detect. 0 = No jabber condition detected.	RO/LH	0
0	Extended Capability	1 = Extended register capable. This bit is tied permanently to 1.	RO	1

PHY Identifier 1 Register

Table 8: Register 2: PHY Identifier 1 Register Bit Description

Bit	Name	Description	Mode	Default
15:0	OUI	Composed of the third through the 18th bits of the Organizationally Unique Identifier (OUI), respectively. See note below.	RO	0022(H)

Note

Based on an OUI of 0010A9 (hex)

PHY Identifier 2 Register

Table 9: Register 3: PHY Identifier 2 Register Bit Description

Bit	Name	Description	Mode	Default
15:10	OUI	Assigned to the 19th through 24th bits of the OUI. See Note below.	RO	010101
9:4	Model Number	Six bit manufacturer's model number.	RO	010010
3:0	Revision Number	4-bit manufacturer's revision number.	RO	0001

Note

Based on an OUI of 0010A9 (hex)

AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Table 10: Register 4: Auto-Negotiation Advertisement Register Bit Description

Bit	Name	Description	Mode	Default
15	Next Page	1 = Next Page enabled. 0 = Next Page disabled.	RW	0
14	Acknowledge	This bit is set internally after receiving three consecutive and consistent FLP bursts.	RO	0
13:11	Reserved			
10	FDFC	Full-Duplex Flow Control 1 = Advertise that the DTE (MAC) has implemented both the optional MAC control sublayer and the pause function as specified in Clause 31 and Annex 31B of 802.3u. 0 = MAC does not support flow control.		
9	100Base-T4	Technology not supported. This bit always 0	RO	0
8	100Base-TX Full Duplex	1 = 100BaseTX full-duplex capable. 0 = Not 100BaseTX full-duplex capable.	RW	set by DUPLEX pin
7	100Base-TX	1 = 100BaseTX half-duplex capable. 0 = Not TX half-duplex capable.	RW	set by DUPLEX pin
6	10Base-T Full Duplex	1 = 10BaseT full-duplex capable. 0 = Not 10BaseT full-duplex capable.	RW	0
5	10Base-T	1 = 10BaseT half-duplex capable. 0 = Not 10BaseT half-duplex capable.	RW	0
4:0	Selector Field	Protocol Selection [00001] = IEEE 802.3.	RO	00001

AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER/LINK PARTNER NEXT PAGE MESSAGE

Table 11: Register 5: Auto-Negotiation Link Partner Ability Register/Link Partner Next Page Message Bit Description

Bit	Name	Description	Mode	Default
15	Next Page	1 = Link partner desires Next Page transfer. 0 = Link partner does not desire Next Page transfer.	RO	0
14	Acknowledge	1 = Link Partner acknowledges reception of FLP words. 0 = Not acknowledged by Link Partner.	RO	0
13:10	Reserved			
9	100Base-T4	1 = 100BaseT4 supported by Link Partner. 0 = 100BaseT4 not supported by Link Partner.	RO	0
8	100Base-TX Full Duplex	1 = 100BaseTX full-duplex supported by Link Partner. 0 = 100BaseTX full-duplex not supported by Link Partner.	RO	0
7	100Base-TX	1 = 100BaseTX half-duplex supported by Link Partner. 0 = 100BaseTX half-duplex not supported by Link Partner.	RO	0
6	10Base-T Full Duplex	1 = 10Mbps full-duplex supported by Link Partner. 0 = 10Mbps full-duplex not supported by Link Partner.	RO	0
5	10Base-T	1 = 10Mbps half-duplex supported by Link Partner. 0 = 10Mbps half-duplex not supported by Link Partner.	RO	0
4:0	Selector Field	Protocol Selection [00001] = IEEE 802.3.	RO	00001

Note **When this register is used as Next Page Message, the bit definition is the same as Register 7.**

AUTO-NEGOTIATION EXPANSION REGISTER

Table 12: Register 6: Auto-Negotiation Expansion Register Bit Description

Bit	Name	Description	Mode	Default
15:5	Reserved		RO	0
4	Parallel Detection Fault	1 = Fault detected by parallel detection logic. This fault is due to more than one technology detecting a concurrent link-up condition. This bit can only be cleared by reading Register 6, using the management interface. 0 = No fault detected by parallel detection logic.	RO/ LH	0
3	Link Partner Next Page Able	1 = Link Partner supports next page function. 0 = Link Partner does not support next page function.	RO	0
2	Next Page Able	Next page is supported.	RO	1
1	Page Received	This bit is set when a new link code word has been received into the Auto-Negotiation Link Partner Ability Register. This bit is cleared upon a read of this register.	RC	0
0	Link Partner ANEN-Able	1 = Link partner is auto-negotiation capable. 0 = Link partner is not auto-negotiation capable.	RO	0

AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER

Table 13: Register 7: Auto-Negotiation Next Page Transmit Register Bit Description

Bit	Name	Description	Mode	Default
15	NP	1 = Another Next Page desired. 0 = No other Next Page Transfer desired.	RW	0
14	Reserved		RO	0
13	MP	1 = Message page. 0 = Unformatted page.	RW	1
12	ACK2	1 = Complies with message. 0 = Does not comply with message.	RW	0
11	TOG_TX	1 = Previous value of transmitted link code word equals 0. 0 = Previous value of transmitted link code word equals 1.	RW	0
10:0	CODE	Message/Unformatted Code Field.	RW	

DIAGNOSTIC REGISTER

Table 14: Register 18: Diagnostic Register Bit Description

Bit	Name	Description	Mode	Default
15:13	Reserved		RW	0
12	Force link pass TX	1 = Enable Force Link at 100 Base-T. 0 = Disable.	RW	0
11	DPLX	This bit indicates the result of the auto-negotiation for duplex. 1 = Full duplex. 0 = Half duplex.	RO	set by pin
10	Speed	This bit indicates the result of the auto-negotiation for speed. 1 = 100Base-T. 0 = 10Base-T.	RO	1
9	RX_PASS	In 100BT mode, this bit indicates that the valid signal was received but not necessarily locked onto.	RO	0
8	RX_LOCK	This bit indicates that the receive PLL has locked onto the received signal for the selected speed of operation (100Base-TX). This bit is set whenever a cycle-slip occurs, and remains set until it is read.	RO/RC	0
7:0	Reserved		RO	0

POWER/LOOPBACK REGISTER

Table 15: Register 19: Power/Loopback Register Bit Description

Bit	Name	Description	Mode	Default
14:7	Reserved		RW	00000000
6	Reserved		RW	0
5	Disable watch dog timer for decipher	1 = Disable watchdog timer. 0 = Enable watchdog timer.	RW	0
4	Low Power Mode disable	1= Disable advance power saving mode. 0= Enable advance power saving mode.	RW	0
3	Enable digital loopback	1 = Enable digital loopback. 0 = Disable digital loopback.	RW	0
2	Reserved	Reserved	RW	0
1	Reserved	Reserved.	RW	0
0	Reserved	Reserved.	RW	0

CABLE MEASUREMENT CAPABILITY REGISTER

Table 16: Register 20: Cable Measurement Capability Register Bit Description

Bit	Name	Description	Mode	Default
15	Reserved		RW	1
14	Reserved	1 = Turn on. 0 = Turn off.	RW	1
13:9	Reserved		RO	0

Table 16: Register 20: Cable Measurement Capability Register Bit Description

Bit	Name	Description	Mode	Default
8	Adaptation disable	1 = Turn on adaptation disable mode. 0 = Turn off. To set the value of 20.7:4, turn on 20.8, and turn off 20.14, or this PHY rejects to receive packets.	RW	0
7:4	Cable measurement capability	These bits can be used as a cable length indicator. The bits are incremented from 0000 to 1111 with an increment of approximately 10 meters. The equivalent is 0 to 32dB with an increment of 2dB at 100 MHz. The value is a read back from the equalizer; the measured value is not absolute.	RW	X
3:0	Reserved		RO	XXXX

Receive Error Counter

Table 17: Register 21: Receive Error Counter Bit Description

Bit	Name	Description	Mode	Default
15:0	RX_ER Counter	Count receive error events.	RO	0

Power Management Register

Table 18: Register 22: Power Management Register Bit Description

Bit	Name	Description	Mode	Default
15:14	Reserved		RO	00
13	PD_PLL	1 = Power down PLL circuit.	RO	X
12	PD_EQUAL	1 = Power down equalizer circuit.	RO	X
11	PD_BT_RCVR	1 = Power down 10 base T receiver.	RO	X
10	PD_LP	1 = Power down link pulse receiver.	RO	X
9	PD_EN_DET	1 = Power down energy detect circuit.	RO	X
8	PD_FX	1 = Power down FX circuit.	RO	X
7:6	Reserved		RW	00
5	MSK_PLL	0 = Force power up PLL circuit.	RW	X
4	MSK_EQUAL	0 = Force power up equalizer circuit.	RW	X
3	MSK_BT_RCVR	0 = Force power up 10 base T receiver.	RW	X
2	MSK_LP	0 = Force power up link pulse receiver.	RW	X
1	MSK_EN_DET	0 = Force power up energy detect circuit.	RW	X
0	MSK_FX	0 = Force power up FX circuit	RW	X

OPERATION MODE REGISTER

Table 19: Register 23: Operation Mode Register Bit Description

Bit	Name	Description	Mode	Default
15:14	Reserved			
13	Reserved			
12	Reserved			
11	Scramble disable	1 = Disable scrambler data. 0 = Enable scrambler data.	RW	0
10	Reserved		RW	0
9	Pcsbp	1 = Enable PCS bypass mode. 0 = disable PCS bypass mode.	RW	0
23:8	Reserved		RW	0
7:6	Reserved			
5	Reserved		RO	0
4:0	Reserved		RO	XXXXX

CRC FOR RECENT RECEIVED PACKET

Table 20: Register 24: CRC for Recent Received Packet Bit Description

Bit	Name	Description	Mode	Default
15:0	CRC16	CRC16 value displayed. For system level test purpose.	RC	0000H

100BASE-FX PHY REGISTERS

Table 21: 100Base-FX PHY Registers

Register	Name	Address
0	Control Register	2100
1	Status Register	7849
2	PHY Identifier 1 Register	0022
3	PHY Identifier 2 Register	5523
4-20	Reserved	XXXX
21	Receive Error Counter Register	0000
22-31	Reserved	XXXX

CONTROL REGISTER

Table 22: Register 0: Control Register Bit Description

Bit	Name	Description	Mode	Default
15	Reset	1 = PHY reset. This bit is self-clearing.	RW/SC	0
14	Loopback	1 = Enable loopback mode. This loops back TXD to RXD, and ignores all the activity on the cable media. 0 = Normal operation.	RW	0
13	Speed Select	1 = 100Mbps. Default is always = 1. This bit set to 0 is undefined.	RW	1
12	ANEN Enable	1= N/A 0= Disable auto-negotiation. This bit is always set to 0 in FX PHY.	RW	0
11	Power Down	1 = Power down. All blocks except for SMI are turned off. Setting the PWRDN pin to high achieves the same result. 0 = Normal operation.	RW	0
10	Isolate	1 = Electrically isolate the PHY from MII. PHY is still able to response to SMI. 0 = Normal operation.	RW	0
9	Restart ANEN	1 = Restart auto-negotiation process. 0 = Normal operation.	RW/SC	0
8	Duplex Mode	1 = Full duplex. 0 = Half duplex.	RW	set by DUPLEX pin
7	Collision Test	1 = Enable collision test, which issues the COL signal in response to the assertion of the TX_EN signal. Collision test is disabled when PCSBP pin is high. Collision test is enabled regardless of the duplex mode. 0 = Disable COL test.	RW	0
6:0	Reserved		RW	0000000

STATUS REGISTER

Table 23: Register 1: Status Register Bit Description

Bit	Name	Description	Mode	Default
15	100Base-T4	Permanently tied to 0 indicates no 100BaseT4 capability.	RO	0
14	100Base-TX Full Duplex	1 = 100BaseTX full-duplex capable. 0 = Not 100BaseTX full-duplex capable.	RO	1
13	100Base-TX Half Duplex	1 = 100BaseTX half-duplex capable. 0 = Not TX half-duplex capable.	RO	1
12	10Base-T Full Duplex	1 = 10BaseT full-duplex capable. 0 = Not 10BaseT full-duplex capable.	RO	0
11	10Base-T Half Duplex	1 = 10BaseT half-duplex capable. 0 = Not 10BaseT half-duplex capable.	RO	0
10:7	Reserved		RO	0000
6	MF Preamble Suppression	The PHY is able to perform management transaction without MDIO preamble. The management interface needs a minimum of 32 bits of preamble after reset.	RO	1
5	ANEN Complete	1 = Auto-negotiation process completed. Registers 4, 5, 6 are valid after this bit is set. 0 = Auto-negotiation process not complete.	RO	0
4	Remote Fault	1 = Remote fault condition detected. 0 = No remote fault. This bit remains set until it is cleared by reading Register 1.	RO/LH	0
3	ANEN Ability	1 = Able to perform auto-negotiation function; default value determined by ANEN pin. 0 = Unable to perform auto-negotiation function.	RO	1
2	Link Status	1 = Link is established. If link fails, this bit is cleared, and remains at 0 until register is read again. 0 = Link has gone down.	RO/LL	0
1	Jabber Detect	1 = Jabber condition detect. 0 = No jabber condition detected.	RO/LH	0
0	Extended Capability	1 = Extended register capable. This bit is tied permanently to 1.	RO	1

PHY IDENTIFIER 1 REGISTER

Table 24: Register 2: PHY Identifier 1 Register Bit Description

Bit	Name	Description	Mode	Default
15:0	OUI*	Composed of the third through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0022(H)

Note

Based on an OUI is 0010A9 (hex).

PHY Identifier 2 Register

Table 25: Register 3: PHY Identifier 2 Register Bit Description

Bit	Name	Description	Mode	Default
15:10	OUI	Assigned to Bits 19 through 24 of the OUI.	RO	010101
9:4	Model Number	6-bit manufacturer's model number.	RO	010010
3:0	Revision Number	4-bit manufacturer's revision number.	RO	0001

Note

Based on an OUI of 0010A9 (Hex).

When this register is used as Next Page Message, the bit definition is the same as Register 7.

Receive Error Counter

Table 26: Register 21: Receive Error Counter Bit Description

Bit	Name	Description	Mode	Default
15:0	RX_ER Counter	Count receive error events.	RO	0

Power Management Register

Table 27: Register 22: Power Management Register Bit Description

Bit	Name	Description	Mode	Default
15:14	Reserved		RO	00
13	PD_PLL	1 = Power down PLL circuit.	RO	X
12	PD_EQUAL	1 = Power down equalizer circuit.	RO	X
11	Reserved		RO	X
10	PD_LP	1 = Power down link pulse receiver.	RO	X
9	PD_EN_DET	1 = Power down energy detect circuit.	RO	X
8	PD_FX	1 = Power down FX circuit.	RO	X
7:6	Reserved		RW	00
5	MSK_PLL	0 = Force power up PLL circuit.	RW	X
4	MSK_EQUAL	0 = Force power up equalizer circuit.	RW	X
3	Reserved		RW	X
2	MSK_LP	0 = Force power up link pulse receiver.	RW	X
1	MSK_EN_DET	0 = Force power up energy detect circuit.	RW	X
0	MSK_FX	0 = Force power up FX circuit.	RW	X

OPERATION MODE REGISTER

Table 28: Register 23: Operation Mode Register Bit Description

Bit	Name	Description	Mode	Default
15:14	Reserved			
13	Clk_rclk_save	1 = Set rclk save mode. Rclk shuts off after 64 cycles of each packet.		0
12	Reserved			
11	Scramble disable	1 = Disable scrambler	RW	1
10	Reserved		RW	0
9	Pcsbp	1 = Enable PCS bypass mode.	RW	0
23:8	Reserved		RW	0
7:6	Reserved			
5	Reserved		RO	0
4:0	Reserved		RO	XXXXX

CRC FOR RECENT RECEIVED PACKET

Table 29: Register 24: CRC for Recent Received Packet Bit Description

Bit	Name	Description	Mode	Default
15:0	CRC16	CRC16 value displayed. For system level test purposes.	RC	0000H

COMMON REGISTERS

The following registers are mapped to Registers 28 through 31 on the TP PHY. Register 28[15:12] is used as a page select. There are multiple pages of Registers 29 through 31, depending on the value of Register 28[15:12].

MODE CONTROL REGISTER

Table 30: Common Register 0: Mode Control Register (Map to TP_PHY, Reg. 28) Bit Description

a.28.15:12	Page Selection	Select multiple common register pages.	RW	0000
a.28.11:7	Reserved		RO	0000
a.28.6	Reserved		RO	1
a.28.5	Reserved		RO	0
a.28.4	Reserved		RO	0
a.28.3	Reserved		RW	0
a.28.2	Act select	Act event select. 0 = Receive activity. 1 = TX or RX activity.	RW	1
a.28.1	Reserved		RO	0
a.28.0	Reserved		RO	0

COMMON REGISTER 1, 2, AND 3

Common Registers 1, 2, and 3 are reserved.

LED BLINK RATE REGISTER 4

Table 31: Common Register 4: LED Blink Rate (Map to TP_Phy, Reg. 29, Page 1 a28 [15:12] = 0001) Bit Description

Bit	Name	Description	Mode	Default
A1.29.15:8	Reserved	Reserved	RO	00000000
A1.29.7:0	Blink Rate	Set LED blink rate. The blink rate is this number times 16 ms. Default is 256 ms.	RW	00010000

LED0 SETTING1 REGISTER 5

The default operation for LED0 is BLINK on TP RX_ACT. The default operation for LED5 is BLINK when Remote loopback packet is received.

Table 32: Common Register 5: LED0 Setting1 (Map to TP_Phy, Reg 30, Page 1 a28[15:12] = 0001) Bit Description

Bit	Name	Description	Mode	Default
A1.30.15:13	Reserved		R	000
A1.30.12	Force LED On	Force LED0 On.	RW	0
A1.30.11:9	Reserved		R	000
A1.30.8	Force LED Off	Force LED0 Off.	RW	0
A1.30.7:0	Msk Blink	Blink mask. When the bits are set to 1, the corresponding event causes the led to blink.	RW	00000001

LED0 SETTING2 REGISTER 6

Table 33: Common Register 6: LED0 Setting2 (Map to TP_Phy, Reg. 31, Page 1 a28 [15:12] = 0001) Bit Description

Bit	Name	Description	Mode	Default
A1.31.15:8	Msk On	On mask. When the bits are set to one, corresponding events cause the LED to turn on.	RW	00000000
A1.31.7:0	Msk Off	Off mask. When the bits are set to 1, corresponding events cause the led to turn off	RW	00000000

LED1 SETTING1 REGISTER 7

The default operation for LED1 is ON on TP_LINK.

Table 34: Common Register 7: LED1 Setting1 (Map to TP_Phy, Reg. 29, Page 2 a28 [15:12] = 0010) Bit Description

Bit	Name	Description	Mode	Default
A2.29.15:13	Reserved	Reserved	R	000
A2.29.12	Force LED On	Force LED1 On.	RW	0

Table 34: Common Register 7: LED1 Setting1 (Map to TP_Phy, Reg. 29, Page 2 a28 [15:12] = 0010) Bit Description

Bit	Name	Description	Mode	Default
A2.29.11:9	Reserved	Reserved	R	000
A2.29.8	Force LED Off	Force LED1 Off	RW	0
A2.29.7:0	Msk Blink	Blink mask. When the bits are set to one, corresponding events cause the LED to blink.	RW	00000000

LED1 SETTING2 REGISTER 8

Table 35: Common Register 8: LED1 Setting2 (Map to TP_Phy, Reg. 30, Page 2 a28 [15:12] = 0010) Bit Description

Bit	Name	Description	Mode	Default
A2.30.15:8	Msk On	On mask. When the bits are set to 1, corresponding events cause the LED to turn on.	RW	00100000
A2.30.7:0	Msk Off	Off mask. When the bits are set to 1, corresponding events cause the LED to turn off.	RW	0000

LED2 SETTING1 REGISTER 9

The default operation for LED2 is BLINK on RxAct_FX.

Table 36: Common Register 9: LED2 Setting1 (Map to TP_Phy, Reg. 31, Page 2 a28 [15:12] = 0010) Bit Description

Bit	Name	Description	Mode	Default
A2.31.15:13	Reserved	Reserved	R	000
A2.31.12	Force LED On	Force LED2 On.	RW	0
A2.31.11:9	Reserved	Reserved	R	000
A2.31.8	Force LED Off	Force LED2 Off.	RW	0
A2.31.7:0	Msk Blink	Blink mask. When the bits are set to 1, corresponding events cause the LED to blink	RW	10000000

LED2 SETTING2 REGISTER 10

Table 37: Common Register 10: LED2 Setting2 (Map to TP_Phy, Reg. 29, Page 3 a28 [15:12] = 0011) Bit Description

Bit	Name	Description	Mode	Default
A3.29.15:8	Msk On	On mask. When the bits are set to 1, corresponding events cause the LED to turn on.	RW	00000000
A3.29.7:0	Msk Off	Off mask. When the bits are set to 1, corresponding events cause the LED to turn off.	RW	00000000

LED3 Setting1 Register 11

The default operation for LED3 is ON on FX_LINK, BLINK on Remote_fault.

Table 38: Common Register 11: LED3 Setting1 (Map to TP_Phy, Reg. 30, Page 3 a28 [15:12] = 0011) Bit Description

Bit	Name	Description	Mode	Default
A3.30.15:13	Reserved		R	000
A3.30.12	Force LED On	Force LED3 On.	RW	0
A3.30.11:9	Reserved		R	000
A3.30.8	Force LED Off	Force LED3 Off.	RW	0
A3.30.7:0	Msk Blink	Blink mask. When the bits are set to 1, corresponding events cause the LED to blink	RW	00000100

LED3 Setting2 Register 12

Table 39: Common Register 12: LED3 Setting2 (Map TP_Phy, Reg. 31, Page 3 a28 [15:12] = 0011) Bit Description

Bit	Name	Description	Mode	Default
A3.31.15:8	Msk On	On mask. When the bits are set to 1, corresponding events cause the LED to turn on	RW	01000000
A3.31.7:0	Msk Off	Off mask. When the bits are set to 1, corresponding events cause the LED to turn off.	RW	00000000

LED4 Setting1 Register 13

The default operation for LED4 is ON when the result of auto negotiation on twisted pair port is full duplex.

Table 40: Common Register 13: LED4 Setting1 (Map to TP_Phy, Reg 29, Page 4 a28 [15:12] = 0100) Bit Description

Bit	Name	Description	Mode	Default
A4.29.15:13	Reserved		R	000
A4.30.12	Force LED On	Force LED4 On.	RW	0
A4.29.11:9	Reserved		R	000
A4.29.8	Force LED Off	Force LED4 Off.	RW	0
A4.29.7:0	Msk Blink	Blink mask. When the bits are set to 1, corresponding events cause the LED to blink	RW	00000000

LED4 Setting2 Register 14

Table 41: Common Register 14: LED4 Setting2 (Map TP_Phy, Reg 30, Page 4 a28[15:12] = 0100) Bit Description

Bit	Name	Description	Mode	Default
A4.30.15:8	Msk On	On mask. When the bits are set to 1, corresponding events cause the LED to turn on.	RW	00010000
A4.30.7:0	Msk Off	Off mask. When the bits are set to 1, corresponding events cause the LED to turn off.	RW	00000000

Section 5: 4B/5B Code-Group Table

Table 42: 4B/5B Code-Group Table

Symbol Name	4B Code	5B Code	Description
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F
Idle and Control Code			
I	0000	11111	Idle
J	0101	11000	Start of stream delimiter, part 1 of 2; always use in pair with K symbol.
K	0101	10001	Start of stream delimiter, part 2 of 2; always use in pair with J symbol.
T	Undefined	01101	End of stream delimiter, part 1 of 2; always use in pair with R symbol.
R	Undefined	00111	End of stream delimiter, part 2 of 2; always use in pair with T symbol.
Invalid Code			
H	Undefined	00100	Transmit Error; used to send HALT code-group
V	Undefined	00000	Invalid code
V	Undefined	00001	Invalid code
V	Undefined	00010	Invalid code
V	Undefined	00011	Invalid code
V	Undefined	00101	Invalid code
V	Undefined	00110	Invalid code
V	Undefined	01000	Invalid code
V	Undefined	01100	Invalid code
V	Undefined	10000	Invalid code
V	Undefined	11001	Invalid code

Section 6: SMI Read/Write Sequence

Table 43: SMI Read/Write Sequence

	Preamble (32 Bits)	*Start (2 Bits)*	*OpCode (2 Bits)*	*PHYAD (5 Bits)*	*REGAD (5 Bits)*	*Turn Around (2 Bits)*	*Data (16 Bits)*	*Idle*
Read	1…1	01	10	AAAAA	RRRRR	Z0	D…D	Z
Write	1…1	01	01	AAAAA	RRRRR	10	D…D	Z

Section 7: Electrical Specifications

The following electrical characteristics are design goals rather than characterized numbers.

Absolute Maximum Ratings

Table 44: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage	VCC	GND-0.3	2.625	V
Storage Temperature	Ts	-40	+125	°C
Electrostatic Discharge	VESD		1000	V

Recommended Operating Conditions

Table 45: Recommended Operating Conditions

Parameter	Symbol	Pin	Operating Mode	Min	Max	Units
Supply Voltage	VCC	VCC		2.375	2.625	V
High-Level Input Voltage	V_{IH}	All Digital Inputs		2		V
Low-Level Input Voltage	V_{IL}	All Digital Inputs			0.8	V
PECL Low-Level Input Voltage	V_{IL}	SD	100BaseFX		1.7	V
PECL High-Level Input Voltage	V_{IH}	SD	100BaseFX	2.2		V
Differential Input Voltage	V_{IDIFF}	FIP/FIN	100BaseFX	1.4	1.8	V
Common Mode Input Voltage	V_{ICM}	RXP/RXN	100BaseTX	1.8	VCC	V
Common Mode Input Voltage	V_{ICM}	FIP/FIN	100BaseFX	1.8	2.2	V
Ambient Operating Temperature	T_A			-40	+85	°C

Electrical Characteristics

Table 46: Electrical Characteristics

Parameter	Symbol	Pins	Conditions	Min	Max	Units
Supply Current	I_{CC}	VCC,VCCPLL	VCC= 2.5v +/- 5%		154	mA
Supply Current Power Down Mode	I_{CC}	VCC,VCCPLL	100BASE-TX 100BASE-FX		20	mA
High-Level Output Voltage	V_{OH}	All Digital Outputs	I_{OH} = -4mA VCC= 2.5v +/- 5%	2		V
High-Level Output Voltage	V_{OH}	TXP/TXN	Driving Load Magnetic Module		VCC+1.5	V
Low-Level Output Voltage	V_{OL}	All Digital Outputs			0.4	V

Table 46: Electrical Characteristics (Cont.)

Parameter	*Symbol*	*Pins*	*Conditions*	*Min*	*Max*	*Units*
Low-Level Output Voltage	V_{OL}	TXP/TXN	Driving Load Magnetic Module	VCC-1.5		
Differential Output Voltage	V_{ODIFF}	FOP/FON	100BASE-FX	1.4	1.8	V
Input Current	I_I	Digital Inputs w/Pull-Up Resistor	V_I = VCC		+200	µA
Input Current	I_I	All Other Digital inputs	VCC ≥ V_I ≥ GND		±100	µA
Bias Voltage	V_{BIAS}	RBIAD		1.18	1.30	V

Section 8: Timing and AC Characteristics

CLOCK TIMING

Table 47: Clock Timing

Parameter	Symbol	Min	Typ	Max	Units
XTAL Input Cycle Time	CK_CYCLE		40		ns
XTAL Input High/Low Time	CK_HI CK_LO		20		ns
XTAL Input Rise/Fall Time	CK_EDGE			4	ns

RESET TIMING

Table 48: Reset Timing

Parameter	Symbol	Min	Typ	Max	Units
Reset Pulse Length Low Period with Stable XTAL Input	RESET_LEN	1			µs
Activity after end of reset	RESET_WAIT	1			second

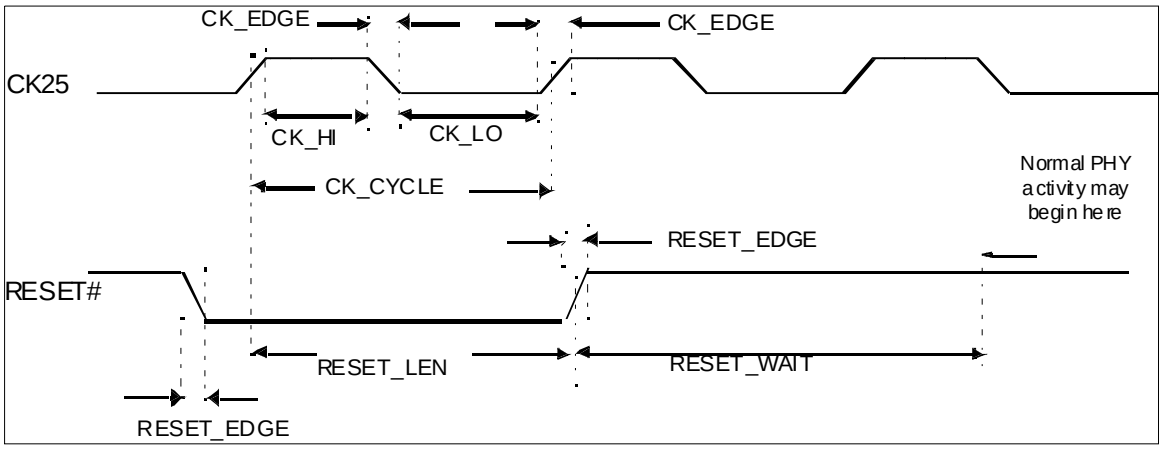


Figure 5: Reset Timing

MANAGEMENT DATA INTERFACE TIMING

Table 49: Management Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
MDC Cycle Time	MDC_CYCLE	40			ns
MDC High/Low		20			ns
MDC Rise/Fall Time	MDC_RISE MDC_FALL			10	ns
MDIO Input Setup Time to MDC Rising	MDIO_SETUP	10			ns
MDIO Input Hold Time from MDC Rising	MDIO_HOLD	10			ns
MDIO Output Delay from MDC Rising	MDIO_DELAY	0		30	ns

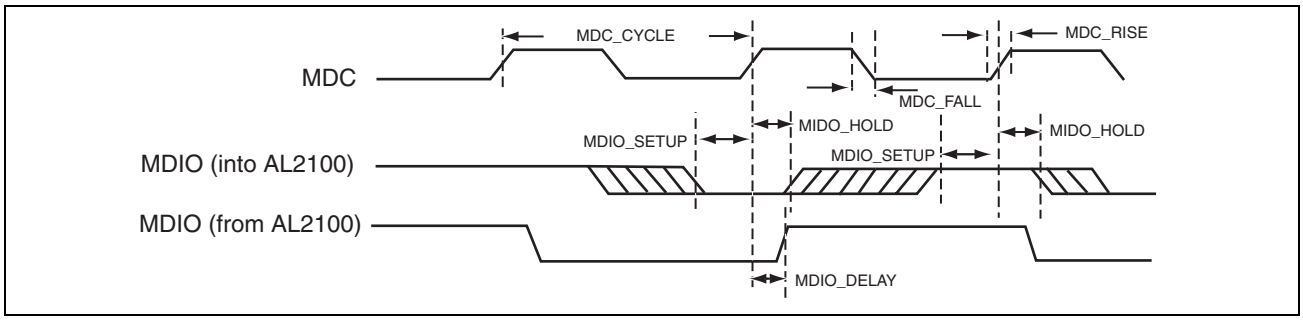


Figure 6: Management Interface Timing

Section 9: TX Application Termination

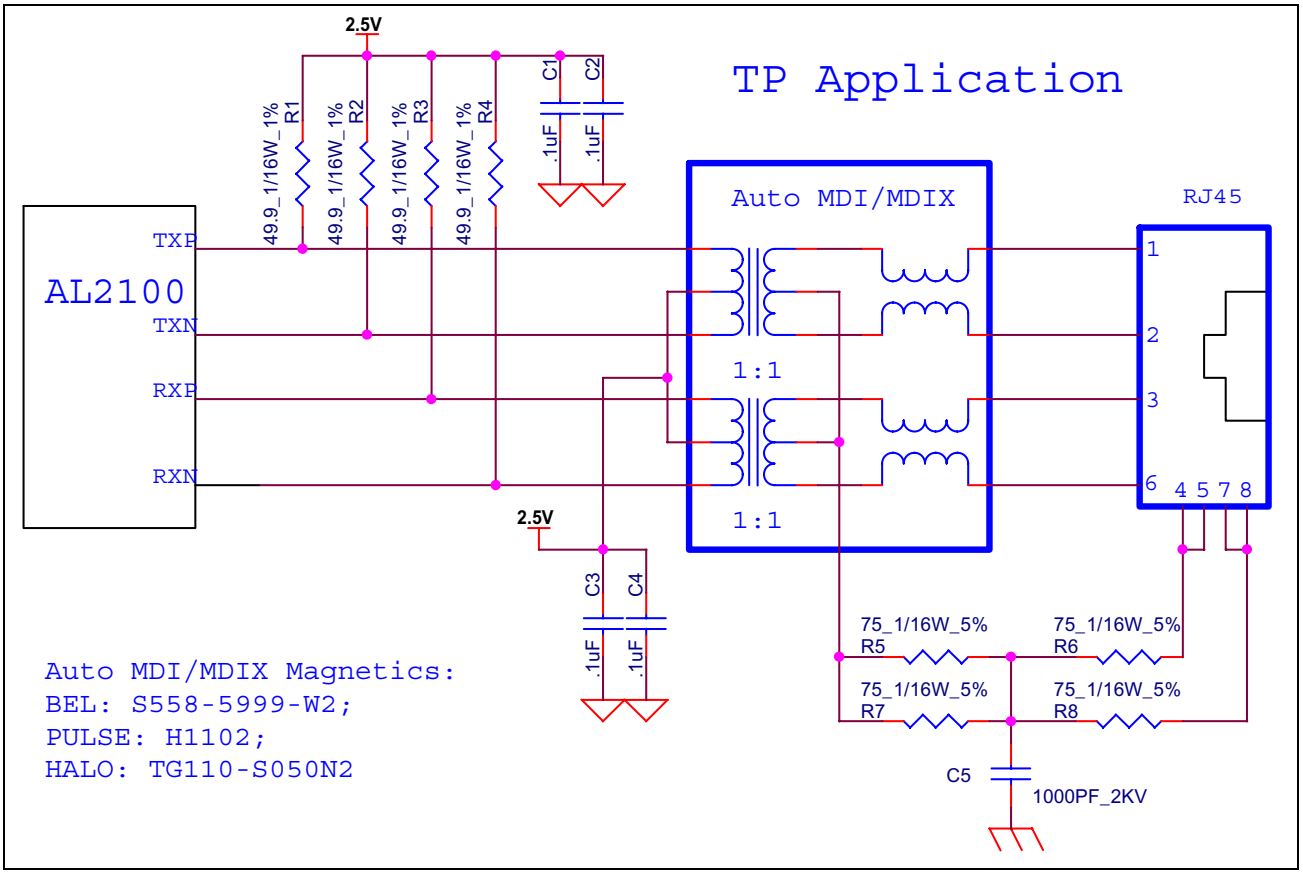


Figure 7: TX Application

Section 10: FX Application Termination

Please contact Altima Communications, Inc. for the latest component value recommendation.

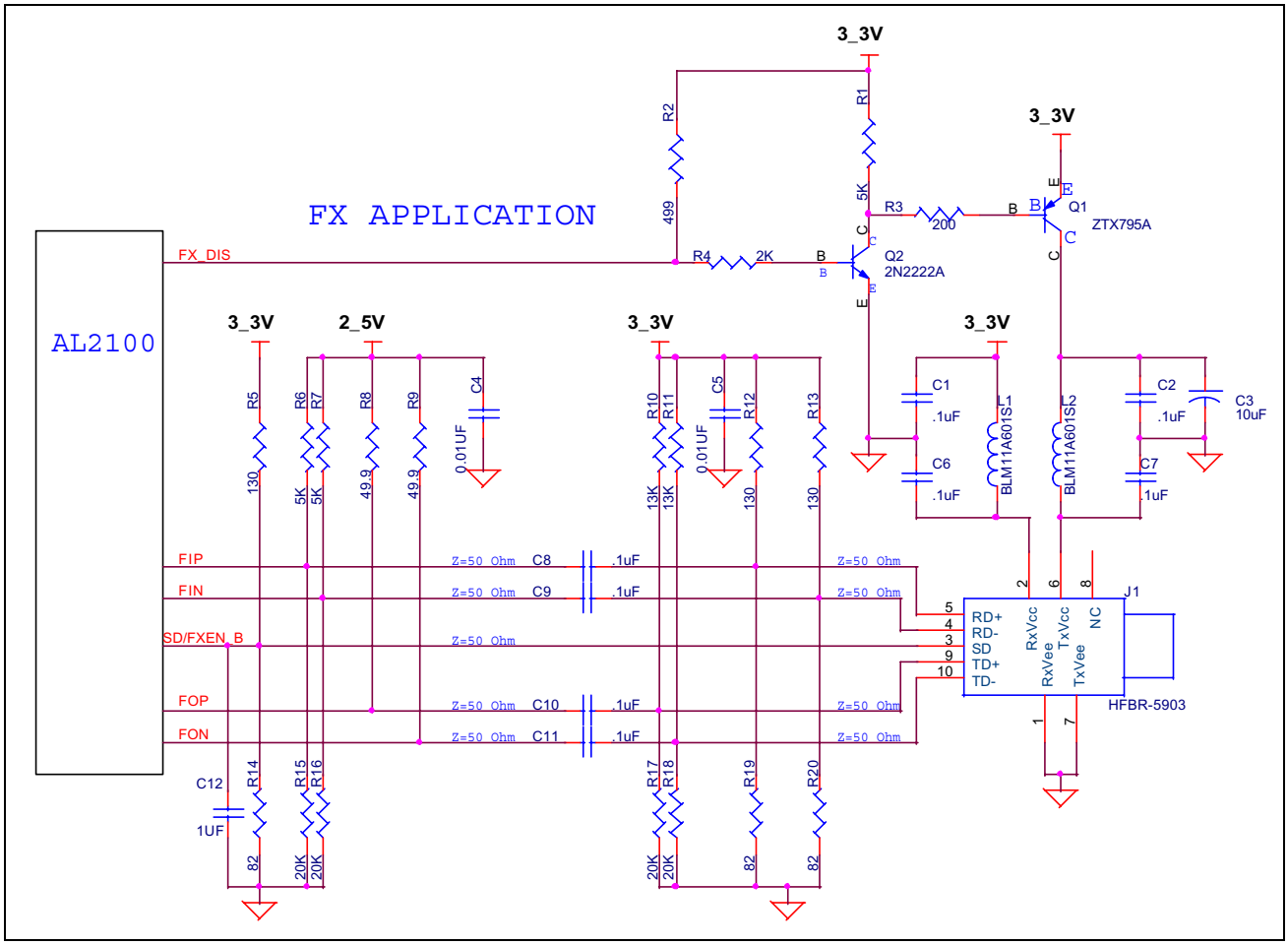


Figure 8: FX Application

Section 11: Power and Ground Filtering

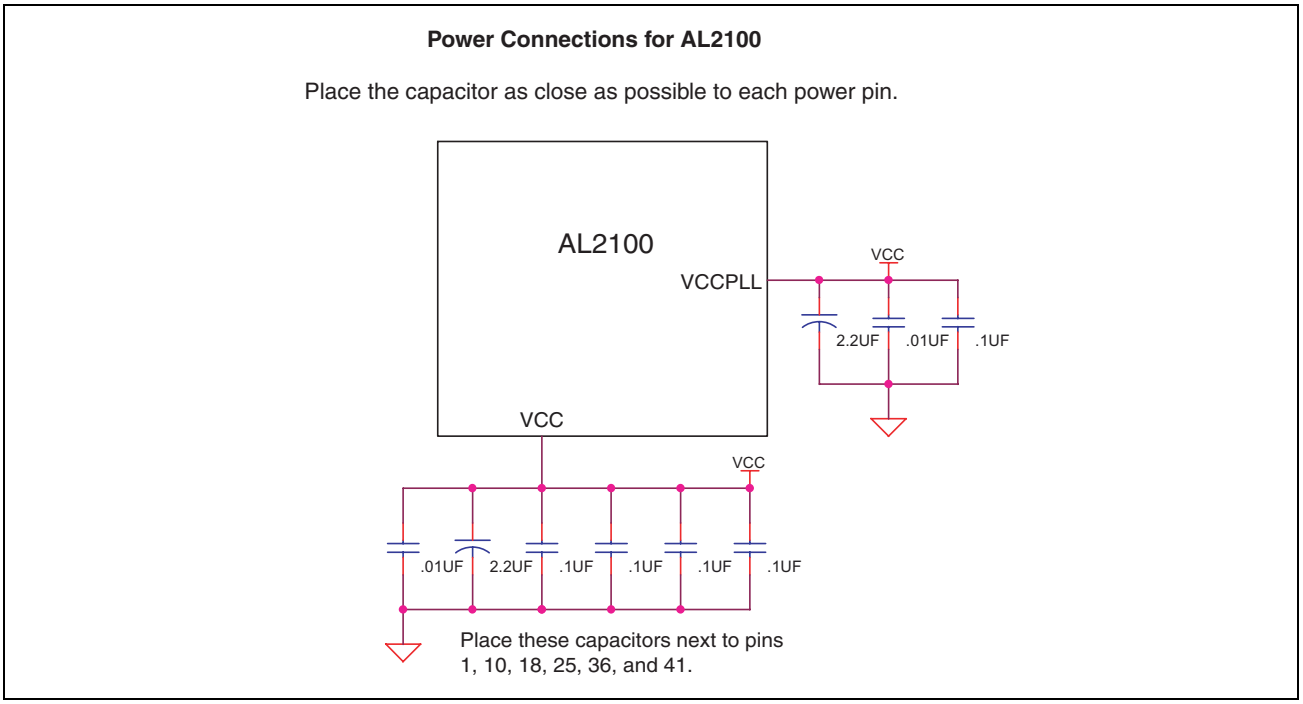
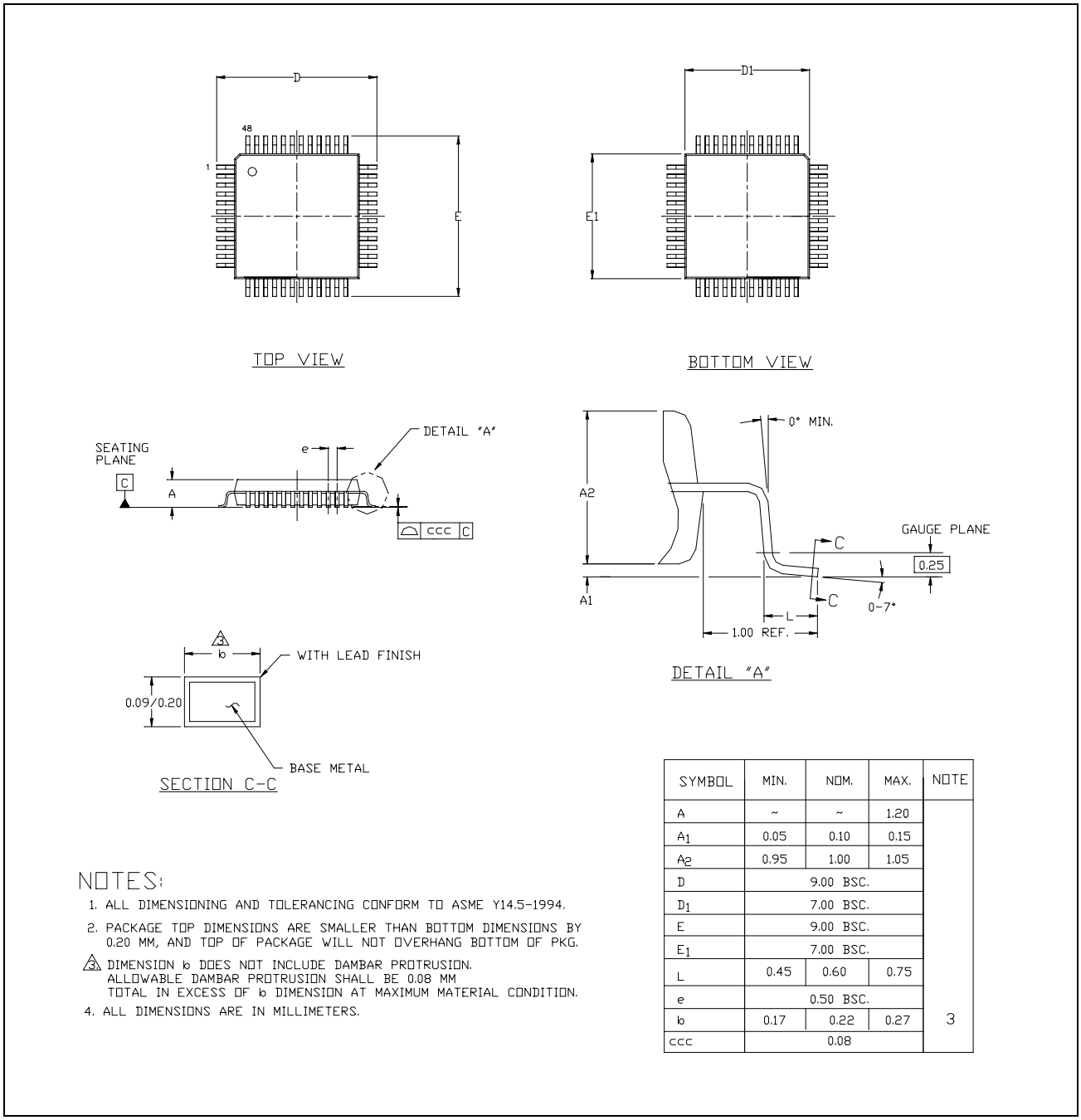


Figure 9: Power and Ground Filtering

Section 12: Package Dimensions (48-Pin TQFP)



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-1994.
2. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS BY 0.20 MM, AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PKG.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MIN.	NOM.	MAX.	NOTE
A	~	~	1.20	
A_1	0.05	0.10	0.15	
A_2	0.95	1.00	1.05	
D		9.00 BSC.		
D_1		7.00 BSC.		
E		9.00 BSC.		
E_1		7.00 BSC.		
L	0.45	0.60	0.75	
e		0.50 BSC.		
b	0.17	0.22	0.27	3
ccc		0.08		

Figure 10: Quad Flat Pack Outline (7 x 7 mm)

Section 13: Thermal Characteristics

Table 50: Thermal Characteristics

Airflow (Feet/Minute)	*0*	*100*	*200*	*400*	*600*
Theta JA (°C/W)	53.9 °C/W	51.2 °C/W	50 °C/W	48.6 °C/W	47.5 °C/W

Table 51: Maximum Junction Temperature

	Theta JC
Theta JC (°C/W) at Max Junction Temperature of 125 °C	24.7 °C/W

Section 14: Ordering Information

Part Number	*Package*	*Ambient Temperature*
AL2100KQT	48TQFP	0° to 70° C
AL2100IQT	48TQFP	-40° to 85° C

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