APPLICATION NOTE

AL2100

Media Converter

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AL2100-AN100-R
10/02/02

REVISION HISTORY

Revision	*Date*	*Change Description*
AL2100-AN100-R	10/02/02	Initial release.

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AL2100 Overview

The AL2100 is designed for media converter applications. It is intended for 100 Mbps Fast Ethernet fiber optic-to-twisted pair media converter designs. The device provides a PECL interface for use with media connectors such as the 1300 nm fiber optic module. The AL2100 is compatible with IEEE 802.3 100Base-FX and 100Base-TX standards.

The AL2100 also provides additional functionality such as fault propagation and redundancy for fault-tolerant system design.

This application note should be read in conjunction with the latest version of the AL2100 data sheet (document *AL2100-DSxx-R*). The AL2100 is available in a 48-pin 7mm^2 TQFP package (see the datasheet for ordering information).

Note **The AL2100 is not suitable for applications that run at 5.0V.**

2.5V Power Supply

The AL2100 power supply is summarized as follows:

- The AL2100 operates at 2.5V ±5%.
- The AL2100 digital inputs and output are 3.3V tolerant and can accept 3.3V CMOS logic levels.
- The AL2100 is not 5V tolerant.

To clarify the purpose of the power pin types, each type is listed and defined in Table 1.

Table 1: Power Pins

Pin Name	*PIN#*	*Description*
VCC	1, 10, 18, 25, 36	Connect to 2.5V power supply.
VCCPLL	32	VCC for analog Bias, PLL module. Connect to 2.5V power supply.
GND	7, 9, 17, 29, 30, 33, 37, 38	Connect to Ground plane.

INTERNAL PULL-UPS AND PULL-DOWNS

This section lists those inputs, or combination of inputs and outputs, that include internal resistive pull-ups or pull-downs. The value of each pull-up and pull-down is approximately 100KΩ (±20%).

The I/O pins listed in Table 2 have very weak pull-ups or pull-downs and are required to have external 5 KΩ-10 KΩ resistors to pull-up or pull-down these pins.

Table 2: Pull-ups and Pull-downs

Pin Name	*Internal Default*	*Need External Pull-down*	*Need External Pull-up*
ISO	Pull-down	Normal operation mode	Isolate mode
FEF_DIS	Pull-down	Normal operation mode	Disable FEF
FX2TP_DIS	Pull-down	Normal operation mode	Disable Fiber to TP Fault Propagation
REDUN#	Pull-down	Normal operation mode	Put the chip in Backup mode
TP2FX_DIS	Pull-down	Normal operation mode	Disable TP to Fiber Fault Propagation
PHYAD0	Pull-up	Set PHY address bit 0 to 0	Set PHY address bit 0 to 1
LED0	Pull-up	N/A	Always pull-up
LED1	Pull-up	N/A	Always pull-up
DUPLEX/LED2	Pull-up	Half Duplex	Normal operation mode
ANEN/LED3	Pull-up	Disable Auto-neg	Normal operation mode
PDOWN#	Pull-up	Power Down	Normal operation mode
RST#	Pull-up	Reset	Normal operation mode
MDIO	Pull-up	N/A	Normal operation mode (use 1 KΩ to pull-up)
MDC	Pull-down	Normal operation mode	N/A
PHYAD[4:1]	Pull-down	Set PHY address bit [4:1] to 0000	Set PHY address bit [4:0] to 1111

25 MHz Reference Clock

The AL2100 device accepts a 25 MHz reference clock from either a low cost crystal circuit (e.g., parallel resonance operating in the fundamental mode) or a single ended clock source (e.g., a 50 ppm self-contained oscillator or buffered system clock). See Figure 1 for the clock connection requirements.

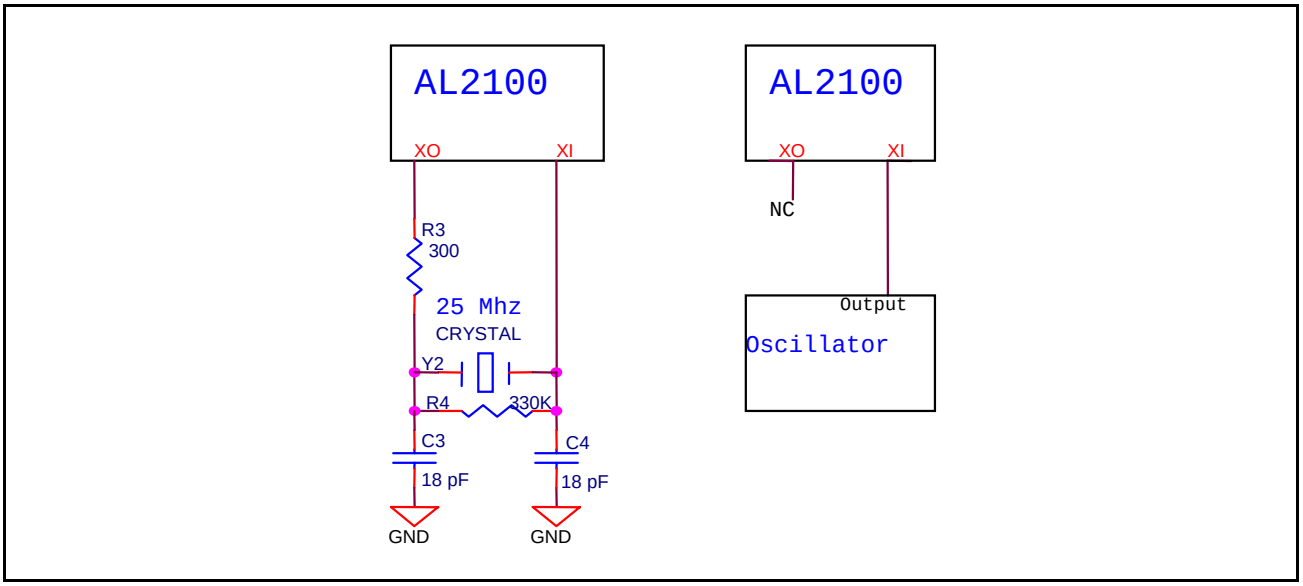


Figure 1: Reference Clock Connections

For stand-alone crystal applications, Broadcom recommends the crystal be located as close to the XI (crystal input) and XO (crystal output) pins of the AL2100 as possible to minimize stray capacitance due to excessive trace routing that could interfere with crystal start-up as well as clock stability.

Broadcom also recommends the use of a crystal rated for a total load capacitance of 18 pF. A calculation for deriving the approximate load capacitance is as follows:

$$((C_{L1} \times C_{L2})/(C_{L1} + C_{L2})) + C_s$$

where:

- C_{L1} x C_{L2} are the actual load capacitors connected to either side of the crystal.
- C_s is the sum of the stray capacitance and input pin capacitance of the PHY device.

Assuming load caps of 18 pF each and a total stray + parasitic capacitance of approximately 9 pF, the above equation yields a total load capacitance of around 18 pF. The load capacitor values may need to be adjusted from the example above to account for variations in parasitic capacitance or crystal specification.

For applications using a crystal-based oscillator or buffered system clock, the XI input should be used and the XO pin can remain unconnected. The input voltage swing of the reference clock must be no greater than3.3v.

The electrical specifications recommended for the oscillator clock or crystal source are listed in Table 3.

Table 3: Clock Source Recommended Electrical Specifications

	Oscillator Module	*Crystal*
Frequency	25.00000 MHz	25.00000 MHz
Tolerance (Includes initial accuracy, aging and stability over temperature)	± 50 ppm	± 50 ppm
Duty Cycle	50% ± 14%	
Edge Rate	1 ns to 4 ns (10% to 90%)	
Voltage Swing	2.5V maximum	
Mode		Parallel Resonant
Load Capacitance		18 pF
Aging	5 ppm per year, maximum	5 ppm per year, maximum
Stability over Temperature	± 10 ppm	± 10 ppm

The following clock devices exhibit good performance in a variety of Broadcom's evaluation platforms.

- Oscillator: GED part number LM20001E/DI-25.000M (G-ED, San Marcos, CA, (760) 591-4170)
- Oscillator: Epson Electronics part
- Crystal: Epson part number MA-506-25.000M-C2 (http://www.epson-electronics.de/download/downcrys.htm)
- Crystal: Digi-Key part number SE2639CT-ND
- Crystal: Ecliptek part# EC1SM-25.000

RBIAD

The 100Base-TX transmit amplitudes can be directly controlled by adjusting the amount of current allowed to flow from the RBIAD pin to GND. It is recommended that in order to verify proper transmit signal amplitude for a given design, an initial value of 10 KΩ (1%) be used for the external RBIAD resistor.

A 1% change in RBIAD current results in a 1% change in transmit amplitude at the TXP/TXN outputs. Increasing the value of the RBIAD resistor results in a proportional decrease in transmit amplitude.

Note **The transmit signal amplitude can be affected by magnetics insertion loss as well as stray capacitance in the front-end design. Therefore, it is important to quantify these additional possible sources of attenuation and adjust the value of the RBIAD resistor accordingly to compensate.**

100BASE-FX

The AL2100 supports 100BASE-FX operation via the SD, FXIP/FXIN, and FXOP/FXON pins. The connection diagrams in Figure 2 illustrate the proper termination and level shifting required to interface the AL2100 to a 3.3V fiber transceiver.

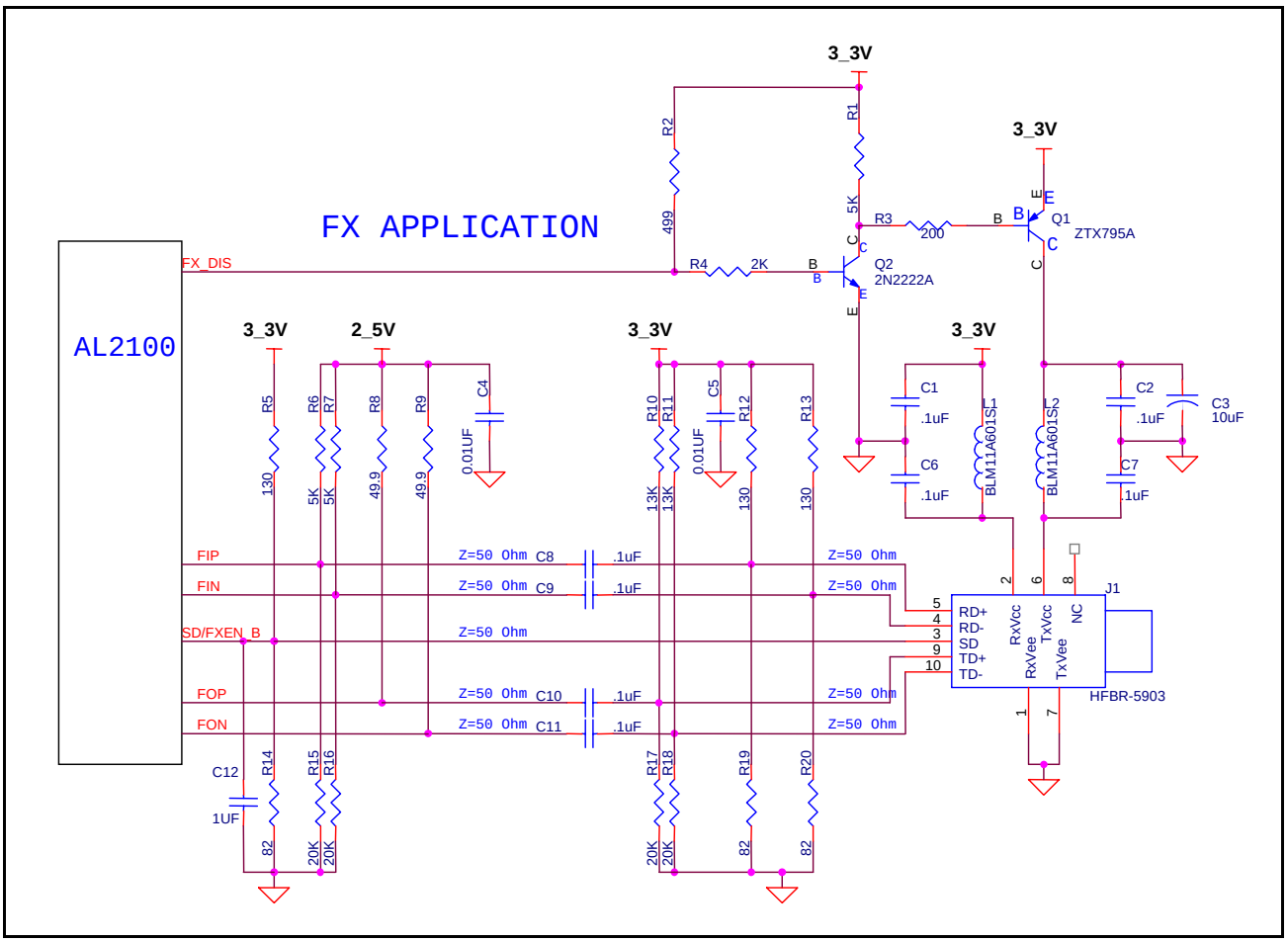


Figure 2: Fiber Connection

Note

Figure 2 illustrates only the termination scheme for the 100BASE-FX interface. Refer to the fiber transceiver manufacturer's guidelines for transceiver power supply connection and filtering.

The FOP/FON and FIP/FIN signal traces between the PHY and fiber transceiver should each be routed with a characteristic impedance of 50Ω (100Ω differential) to match the termination network impedance given in Figure 2.

The SD traces do not require special impedance considerations due to the static nature of signal detect.

Configuring the AL2100 100Base-FX operation is accomplished simply by connecting the SD input to a 100Base-FX compliant transceiver and by setting the potential of the pin as shown in Figure 2. Agilent manufactures high quality 100BASE-FX transceivers. The Agilent fiber module part# HFBR-5903.

The following are 100Base-FX layout considerations:

- **SD pin**: Assuming the use of a 3.3V fiber transceiver, take care to level shift the SD signal from the fiber transceiver to the AL2100 properly. As with any interface, trace lengths should be kept to a minimum wherever possible. The FX module is disabled when the SD input level is 0v. The FX mode is enable when the input is >1V and the SD pin is used as signal detect input with the PECL threshold.
- **FIP/FIN pin**: The FIP/FIN inputs of the AL2100 are internally biased and typical 3.3V fiber transceivers normally source PECL with a center of the voltage swing of approximately 2.0V. Additionally, if the system layout requires that the FIP/FIN trace lengths are more than approximately one inch, take care to set up the termination to account for transmission line effects as well (as indicated in Figure 2).
- **FOP/FON pin**: The AL2100 employs current-sink outputs to transmit the 100Base-FX signaling to the fiber transceiver, so a special level shifting and impedance matching termination network must be implemented. The slight mismatch in the final voltage divider for the FOP versus FON ensures that the FOP/FON input of the fiber transceiver will not switch due to noise that might be present when the AL2100 is quiet.

AUTO-MDI/MDIX

In most 10/100Base-TX connections, one end of the link is configured as an MDI (Medium Dependent Interface) crossover so that each transceiver's transmitter is connected to the other's receiver. This allows the end user to install straight-through cables. However, there are many instances where cross-over cables are required and this has caused significant confusion and downtime in the field. The AL2100 contains the ability to perform Auto-MDI/MDIX crossover on chip, thus eliminating the need for crossover cables or cross- wired (MDIX) ports.

During auto-negotiation and 100BASE-TX operation, the AL2100 normally transmits on TXP/TXN and receives on RXP/RXN. When connected via a straight-through cable to another device that does not perform the Auto-MDI/MDIX crossover, the AL2100 automatically switches its transmitter to RXP/RXN and its receiver to TXP/TXN to communicate with the remote device. If two devices are connected that both have Auto-MDI/MDIX crossover capability, then a random algorithm determines which end performs the crossover function.

The Auto-MDI/MDIX crossover feature is a function of auto-negotiation. If the AL2100 is configured not to perform Auto-Negotiation, the feature does not work and a specific cable is required to ensure the transmitter at one end of the cable is connected with the receiver at the other end of the cable. This feature is enabled by default and cannot be disabled.

Specific magnetics and cable termination issues must be considered when using the AL2100 in Auto-MDI/MDIX mode. See "Magnetics" on page 7 for further detail.

MAGNETICS

One important restriction in pairing magnetics with the AL2100 relates to the ordering of isolation transformer and common mode choke in the transmit signal path (and receive signal path when Auto-MDI/MDIX is enabled). The transmit output signal from the AL2100 must be connected to the isolation transformer first, followed by the common mode choke (as shown in Figure 3).

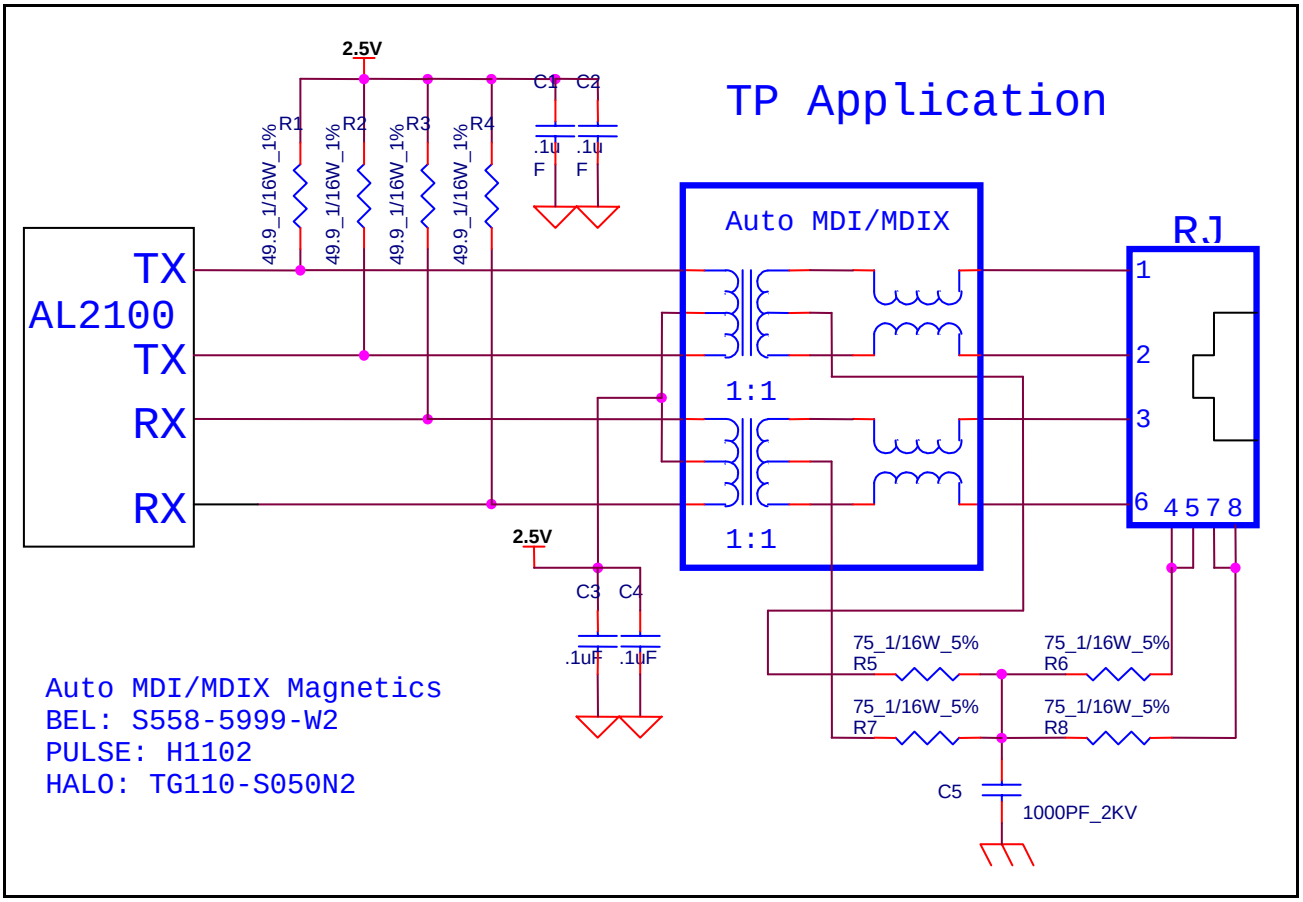


Figure 3: Twisted Pair Connection

The following list includes recommended single channel magnetics components from various vendors for use with the AL2100. The use of these magnetics is recommended regardless of whether Auto-MDI/MDIX is enabled.

- Bel: S558-5999-W2 (Single)
- Pulse Engineering: H1102 (Single)
- Halo: TG110-S050N2 (single), TG110-LC50N2 (single).

Figure 3 illustrates specific magnetics interconnect and differential cable termination requirements for applications that use Auto-MDI/MDIX.

LED OPERATION

LEDS CONNECTION

The LEDs can be pull-up to 2.5V or 3.3V. It is recommended to limit the LED current below 10 mA per LED. Choice of the current limiting resistor value is importance to ensure desired LEDs brightness (typically 150 Ohm for 2.5V connection). The LED[4:0] default function is shown in Table 4.

Table 4: LEDs Default Function

LEDs	*Function*	*Display*
LED0	RxAct_TP	Blink
LED1	Link_TP	ON
LED2	Rx_Act_FX	Blink
LED3	Link_FX	ON
LED4	Duplex_TP	ON
LED_FX_SD	Signal detect FX	ON
LED_TX_SD	Receiving energy detect TP	ON

CONFIGURE LEDS INTO DIFFERENT MODES

LED [4:0] can be configured into different modes. Each LED has two 16 bits register to define its operation (see Common Register and LED Event Table in the datasheet for the details).

Table 5 is an example of how to configure LED0 to turn ON when there is a link up and Blinking when there is receive activity at TP PHY. The default LED0 is blink when TP RX_ACT is true and now we add LED0 turn ON when there is a link up at TP PHY.

Table 5: Example: Configuring LED0 into TP_Link and Transmit Activity

Step	*Setting Register*	*Purpose*
1	a28[15:12] = 0001	Map to TP_Phy, Reg 31, Page 1.
2	A1.31[15:8] = 00100000	Set LED0 to turn ON when there is a TP link up.
3	A1.30[7:0] = 00000001	Set LED0 to blink when there is receive activity on TP PHY.

FAULT PROPAGATION

Three types of fault propagation are provided.

FIBER TO FIBER (FX2FX)

The Fiber to Fiber (FX2FX) fault propagation is illustrated in Figure 4.

- When function FEF (Far End Fault) is enabled (pin 11 pulled down):
  If Fiber side Receive signal failure, the AL2100 will:
  - Transmit Far End Fault (FEF) pattern to Fiber Far End Link Partner.
  - DATA_OFF signal de-assert.
- When function FEF is disabled (pin 11 pulled up):
  - Not transmit FEF pattern.
  - Stop transmitting idle signal.

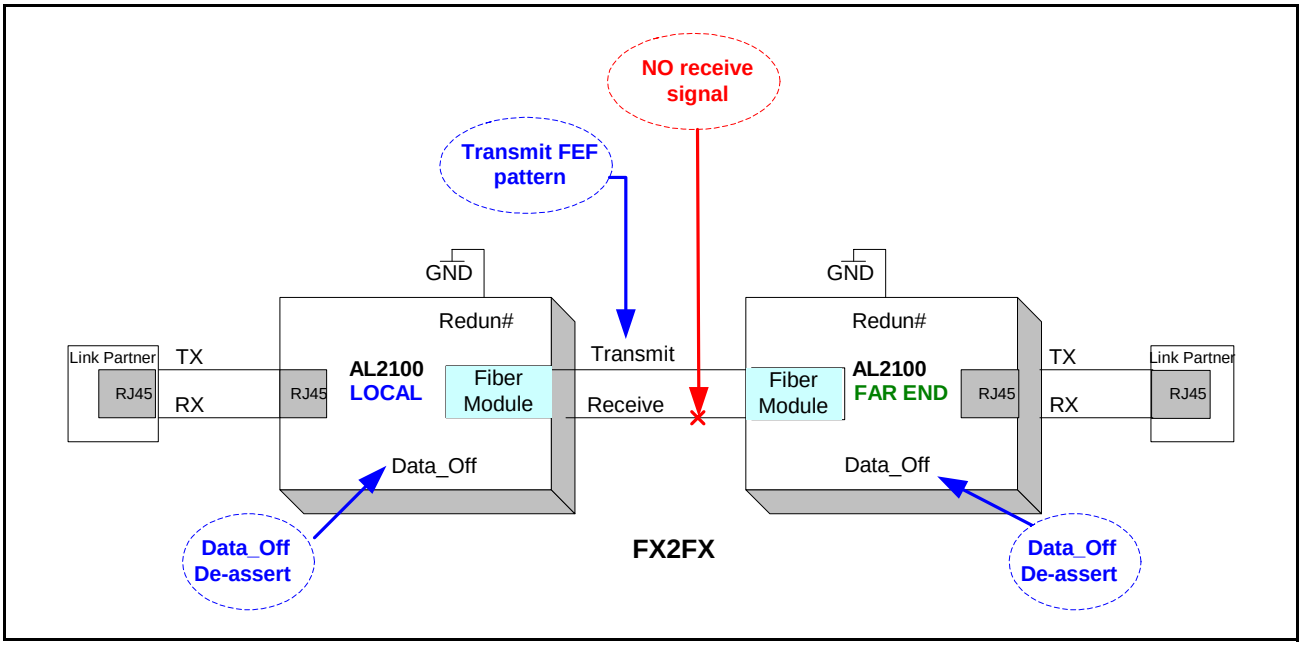


Figure 4: Fiber to Fiber Fault Propagation (FX2FX)

FIBER TO TWISTED PAIR (FX2TP)

The Fiber to Twisted Pair (FX2TP) fault propagation is illustrated in Figure 5.

- When FX2TP_DIS signal (pin12) is pulled down:
  If the fiber side receives the Failure signal or loss of link, AL2100 will:
  - DATA_OFF signal de-assert.
  - Stop transmitting the idle signal to the TP driver and put the driver into high-impedance mode.
  - Make TP (Twisted Pair) side drop link
- When the FX2TP_DIS signal is disabled (pin12 pulled up):
  If the fiber side receives Link Failure or Transmit Link Failure:
  - TP side is not effected by FX side.

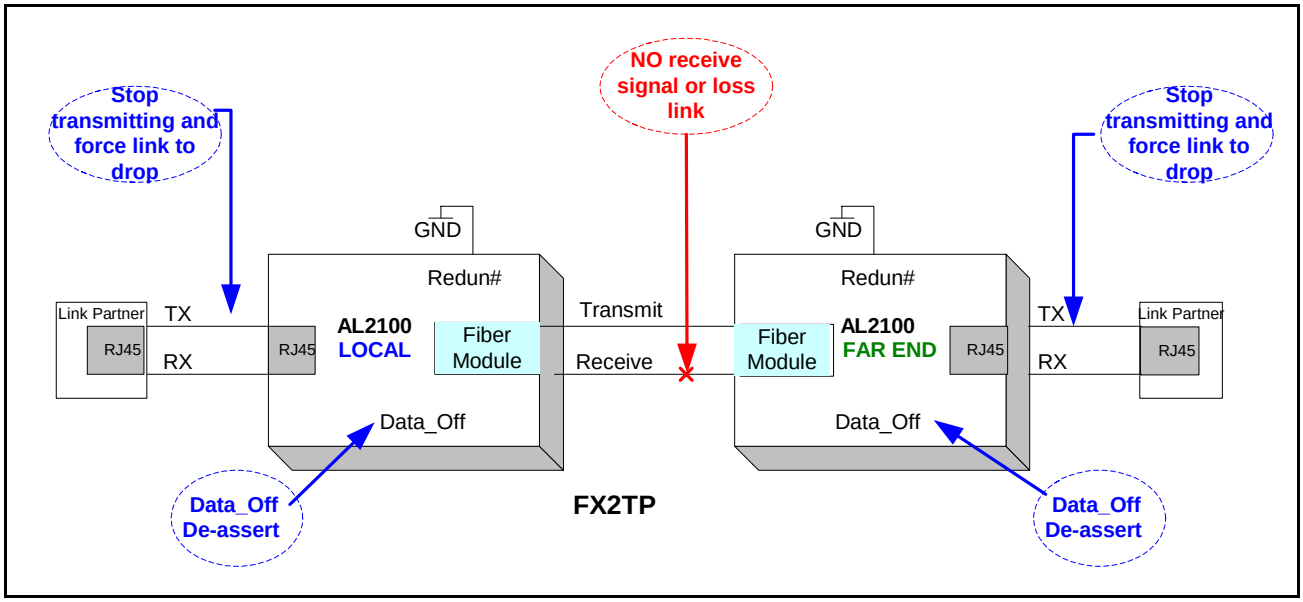


Figure 5: Fiber to Twisted Pair Propagation (FX2TP)

TWISTED PAIR TO FIBER (TP2FX

The Twisted Pair to Fiber (TP2FX) fault propagation is illustrated in Figure 6.

- When TP2FX_DIS signal (pin15) is pulled down:
  If TP side has Link Failure, the AL2100 will:
  - Stop transmitting an idle signal to the fiber-optic driver.
  - Make Fiber side drop Link.
- When TP2FX_DIS signal is disabled (pin15 pulled up):
  If the TP side has Link Failure.
  - FX side is not effected by the TP side.

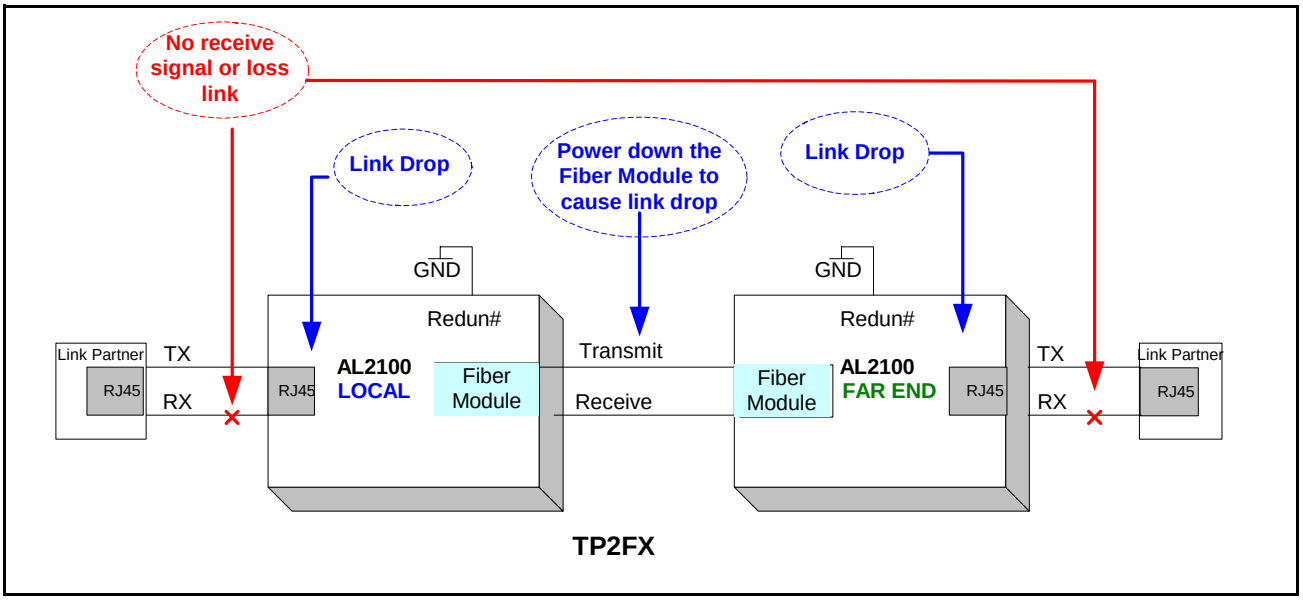


Figure 6: Twisted Pair to Fiber Fault Propagation (TP2FX)

REDUNDANT LINK

This function allows the network system to reduce the down time when the local system loses connection with far end system. The backup system automatically enters the link up state when the primary system is in repair and starts transmitting and receiving data from the local to far end (see Figure 7).

Whenever there is a loss of link between Local Primary Fiber and Far-End Primary Fiber, both the Local Primary transceiver and Far-End Primary transceiver:

- Start transmitting the remote fault signal.
- Enter the link-down state.
- Put the TXP/N pins in high-impedance mode.
- DATA_OFF signal De-Assert.

Both the Back-up Local transceiver and Back-up Far-End transceiver:

- Enter the link-up state and perform transmit and receive data.

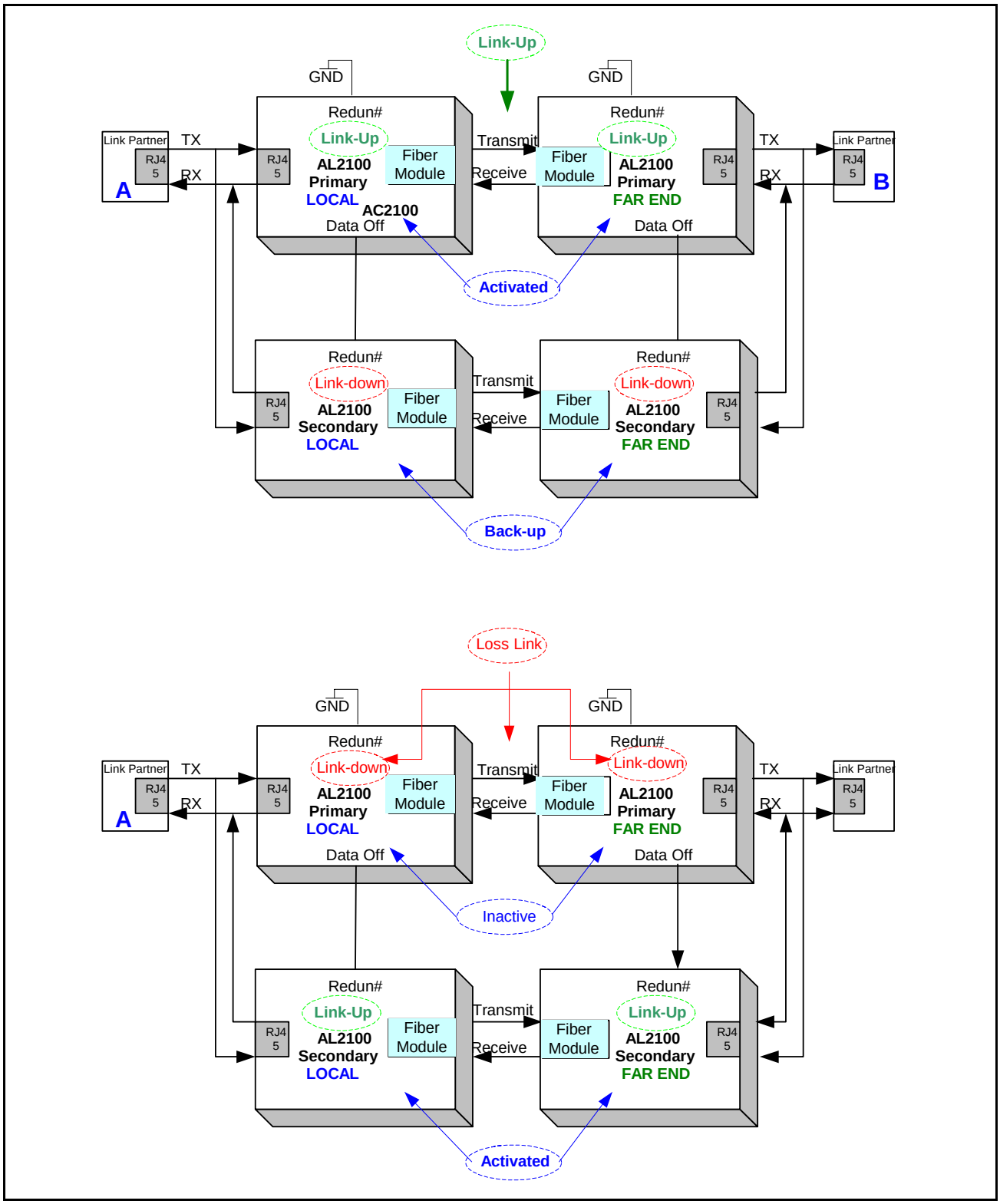
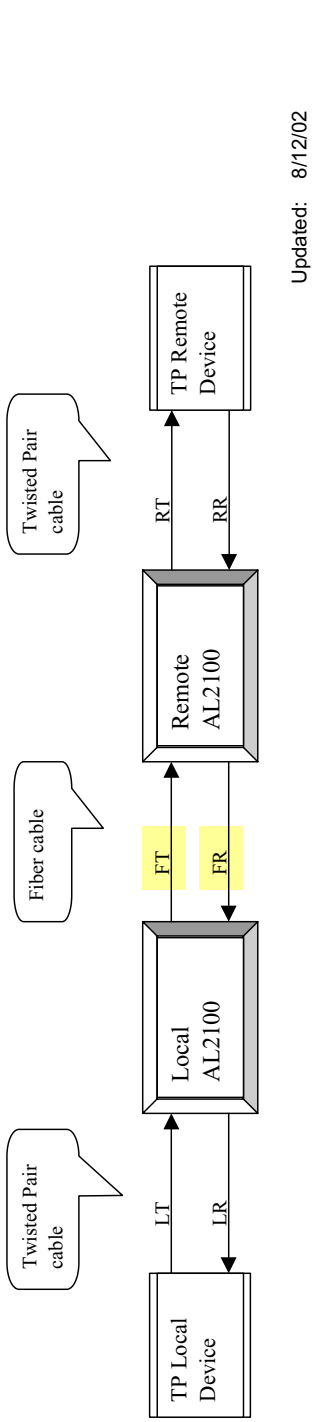


Figure 7: Redundant Link Function

LEDs Behavior

The behavior of the LEDs is shown in Figure 8 for the following conditions:

- When the fiber cable is disconnect while the Link Partner is in Force mode.
- When the fiber cable is disconnected while the Link Partner is in Auto-Neg mode.
- When the TP cable of the Local Link Partner is disconnected.
- When the TP cable of the Remote Link Partner is disconnect.



Updated: 8/12/02

TP Local and TP Remote Link Partner is in auto-neg mode:

	TP Local Device	Local AL2100							Remote AL2100							TP Remote
		TP side				FX side			TP side				FX side			
	Link LED	LED0 RX_TP	LED1 Link_TP	LED4 Duplex_TP	LED TP_SD	LED2 RX_FX	LED3 Link_FX/ Fault_FX	LED FX_SD	LED0 RX_TP	LED1 Link_TP	LED4 Duplex_TP	LED TP_SD	LED2 RX_FX	LED3 Link_FX/ Fault_FX	LED FX_SD	Link LED
TP Local disconnect	Off	Off	Off	Off	Off	Off	Blink	Blink	Blink	Blink	Blink	Blink	Blink	Blink	Blink	Blink
Fiber cable disconnect	Off	Blink	Blink	Blink	Blink	Off	Off	Off	Blink	Blink	Blink	Blink	Off	Off	Off	Off
TP Remote disconnect	Blink	Blink	Blink	Blink	Blink	Blink	Blink	Blink	Off	Off	Off	Off	Off	Blink	Blink	Off

TP Local and TP Remote Link Partner is in Forced 100Mbps mode:

	TP Local Device	Local AL2100							Remote AL2100							TP Remote
		TP side				FX side			TP side				FX side			
	Link LED	LED0 RX_TP	LED1 Link_TP	LED4 Duplex_TP	LED TP_SD	LED2 RX_FX	LED3 Link_FX/ Fault_FX	LED FX_SD	LED0 RX_TP	LED1 Link_TP	LED4 Duplex_TP	LED TP_SD	LED2 RX_FX	LED3 Link_FX/ Fault_FX	LED FX_SD	Link LED
TP Local disconnect	Off	Off	Off	Off	Off	Off	Blink	**ON**	Off	**ON**	Off	**ON**	Blink	Blink	Blink	Blink
Fiber cable disconnect	Off	Off	**ON**	Off	**ON**	Off	Off	Off	Off	**ON**	Off	**ON**	Off	Off	Off	Off
TP Remote disconnect	Blink	Off	**ON**	Off	**ON**	Blink	Blink	Blink	Off	Off	Off	Off	Off	Blink	**ON**	Off

Figure 8: LED Behavior

GENERAL LAYOUT NOTES

When determining component placement and routing for an AL2100 based design, the following recommendations help optimize system design and performance.

ANALOG RELATED PASSIVE COMPONENT PLACEMENT

Relative component placement across the analog side of the AL2100 (pins 17 through 32) is critical and should be addressed with the following priorities in mind:

- Power supply filter components should be placed first and located closest to the PHY (highest priority).
- Transmit termination resistors should be placed as close as possible to the TXP/TXN pins of the PHY.
- Receive termination network should be placed as close as possible to the RXP/RXN pins of the PHY.

TXP/TXN TRACE ROUTING

When routing the TXP/TXN signal traces from the PHY to the 1:1 transformer, the traces should be routed adjacent to a ground plane for controlled characteristic impedance. Broadcom recommends that the TXP and TXN signal traces be routed with matched length (i.e., as short as possible) and with a characteristic differential impedance of 100 ohms.

RXP/RXN TRACE ROUTING

The RXP and RXN traces, which connect the receive transformer to the PHY, should be routed with a differential characteristic impedance of 100 ohms and should be routed adjacent to a ground plane. Again, matched trace length is important.

REFERENCE CLOCK

If the design requires a low cost crystal, minimize trace length from the crystal to the XO (crystal output) and XI (crystal input) pins of the AL2100. This will help minimize stray capacitance and noise pick-up that might otherwise affect the reference clock integrity. In a worst case scenario, too much parasitic capacitance or inductance in the crystal traces could cause the crystal to suffer from start-up problems or instability.

When using a single-ended reference clock, it is usually best to series terminate at the clock source to ensure optimal signal integrity at the input to the AL2100.

MAGNETICS TO RJ45

Broadcom recommends that properly-grounded (i.e., usually to the chassis ground) shielded RJ45 media connectors are used to control EMI emissions.

When routing the transmit and receive pairs between magnetics and the RJ45, it is recommended that an inner layer or layers be used. The outer layers (top and bottom) can then be dedicated to chassis ground in the area between the magnetics and the RJ45. This will help isolate the sensitive analog signals from external noise sources, as well as help reduce EMI emissions. See Figure 9 on page 16.

CHASSIS GROUND

When planning the placement of chassis ground in the layout, it is always beneficial to consider placing at least two component pads (1206 size) across the void between chassis ground and system ground (see Figure 9).These component pads may be stuffed with a variety of components to reduce EMI emissions. Installing capacitors or leaving these pads unpopulated are options to be considered. These options can provide substantial flexibility when attempting to control EMI emissions.

BOARD LAYER ALLOCATION

Figure 9 illustrates one option for board layer allocation. The figure gives an example based on a single VCC and single ground plane. Of course, some applications will require a second VCC plane in order to accommodate a second power rail.

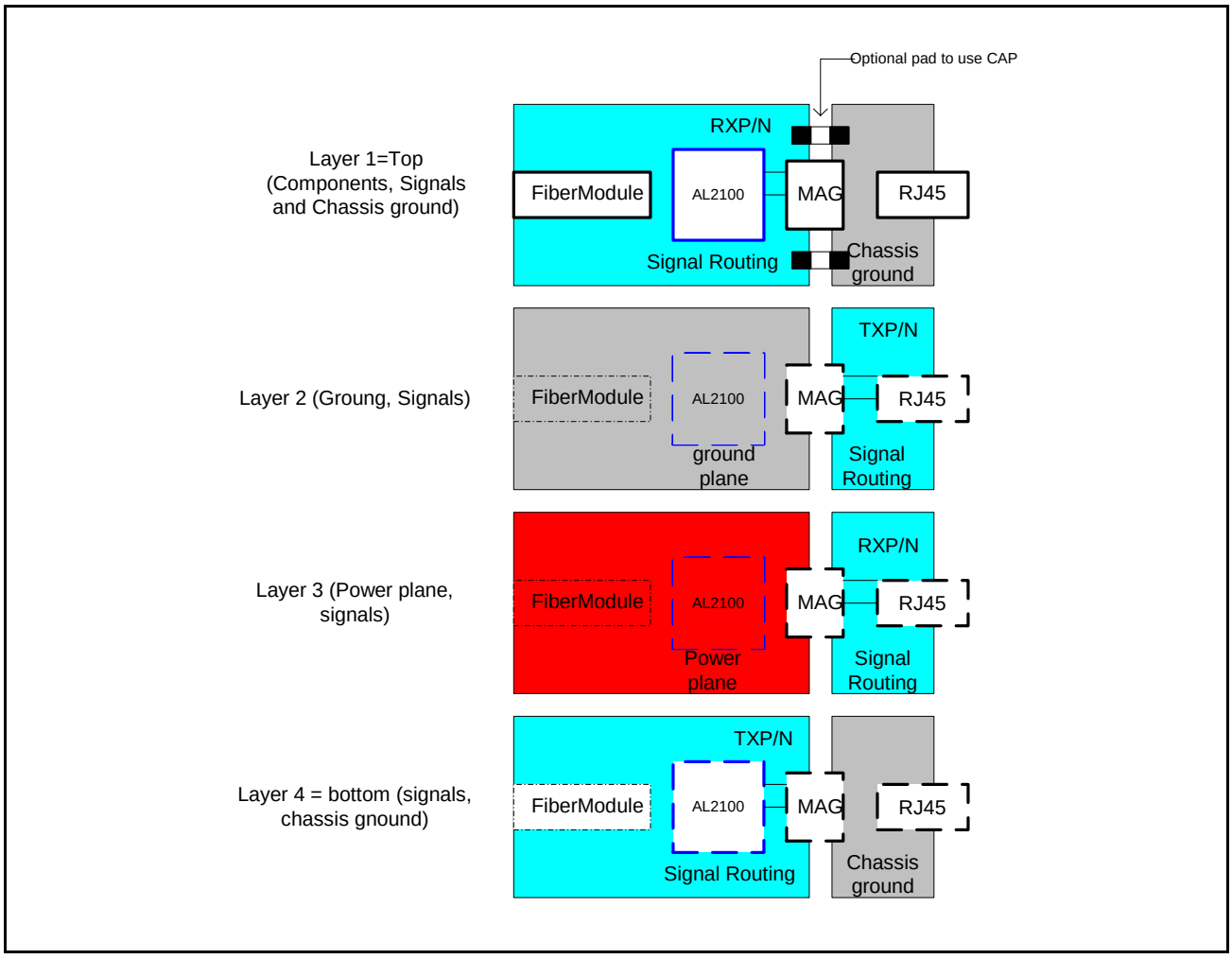


Figure 9: Board Layer Allocation

POWER SUPPLY FILTER COMPONENTS

Always place power supply filter components as close as possible to the recommended pins (see Figure 10) in order to maximize the filtering effects. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it via copper trace. Instead make the connection directly to the associated planes with vias.

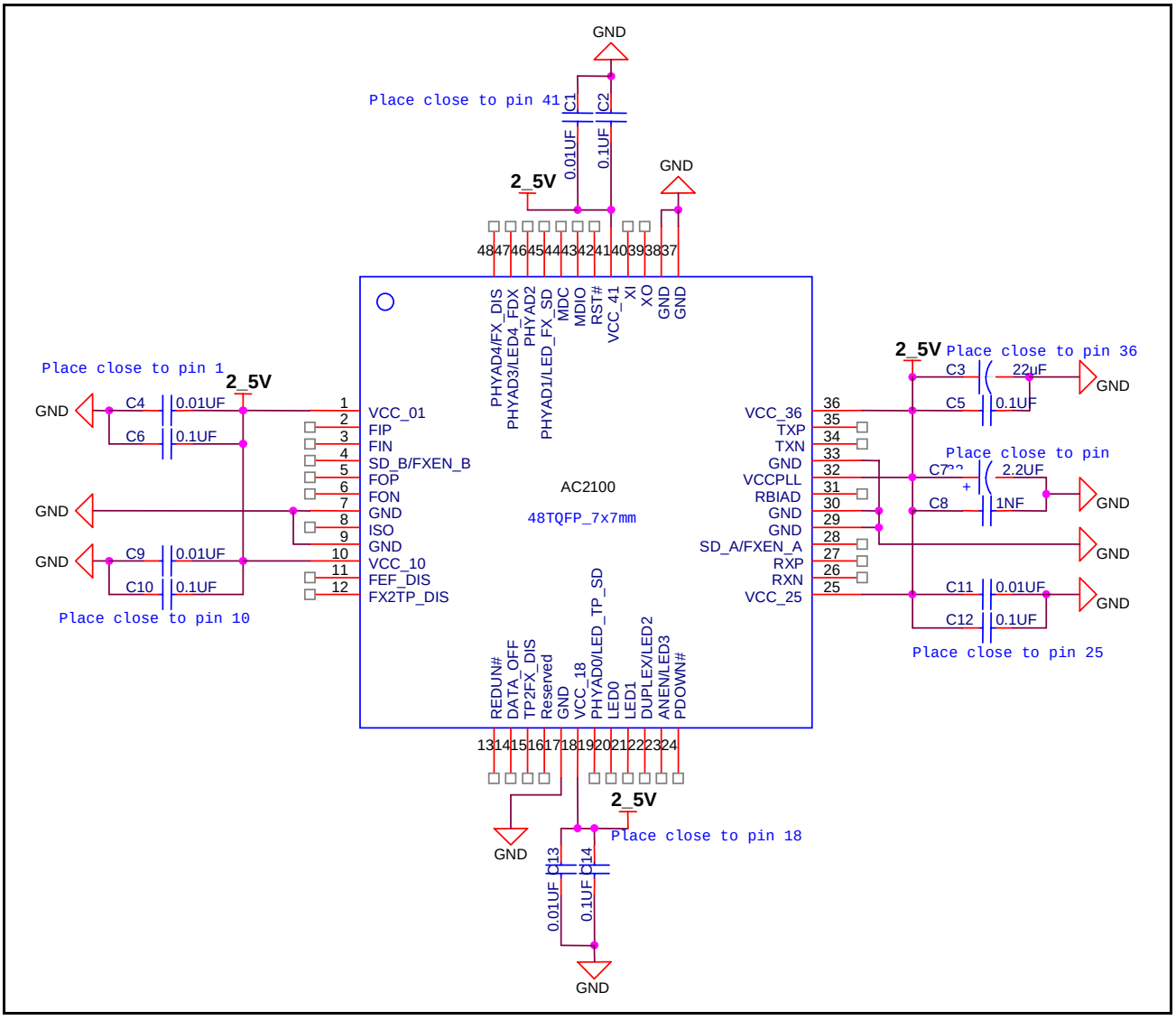


Figure 10: AL2100 Relative Placement of Filter Components

THERMAL INFORMATION

This section includes basic thermal information pertaining to the AL2100KPT package types. Table 6 provides the thermal data Theta-J_A versus Airflow.

Table 6: AL2100KPB Theta-J_A vs. Airflow

48 TQFP Package	***Air Flow (feet per minute)***				
	0	***100***	***200***	***400***	***600***
Theta-JA(C/W)	53.9	51.2	50	48.6	47.5

Theta-J_C for this package is given as 24.7 ^{o}C/W. Additionally, the AL2100KQT is designed for and rated for a maximum Junction Temperature of 125 ^{o}C.

AL2100 REFERENCE SCHEMATIC

- See Figure 11: “AL2100 Reference Schematic (page 1 of 2),” on page 19.
- See Figure 12: “AL2100 Reference Schematic (page 2 of 2),” on page 20.

AL2100 BILL OF MATERIAL FOR REFERENCE SCHEMATIC

- See Figure 13: “AL2100 Bill of Material for Reference Schematic (page 1 of 3),” on page 21.
- See Figure 14: “AL2100 Bill of Material for Reference Schematic (page 2 of 3),” on page 22.
- See Figure 15: “AL2100 Bill of Material for Reference Schematic (page 3of 3),” on page 23.

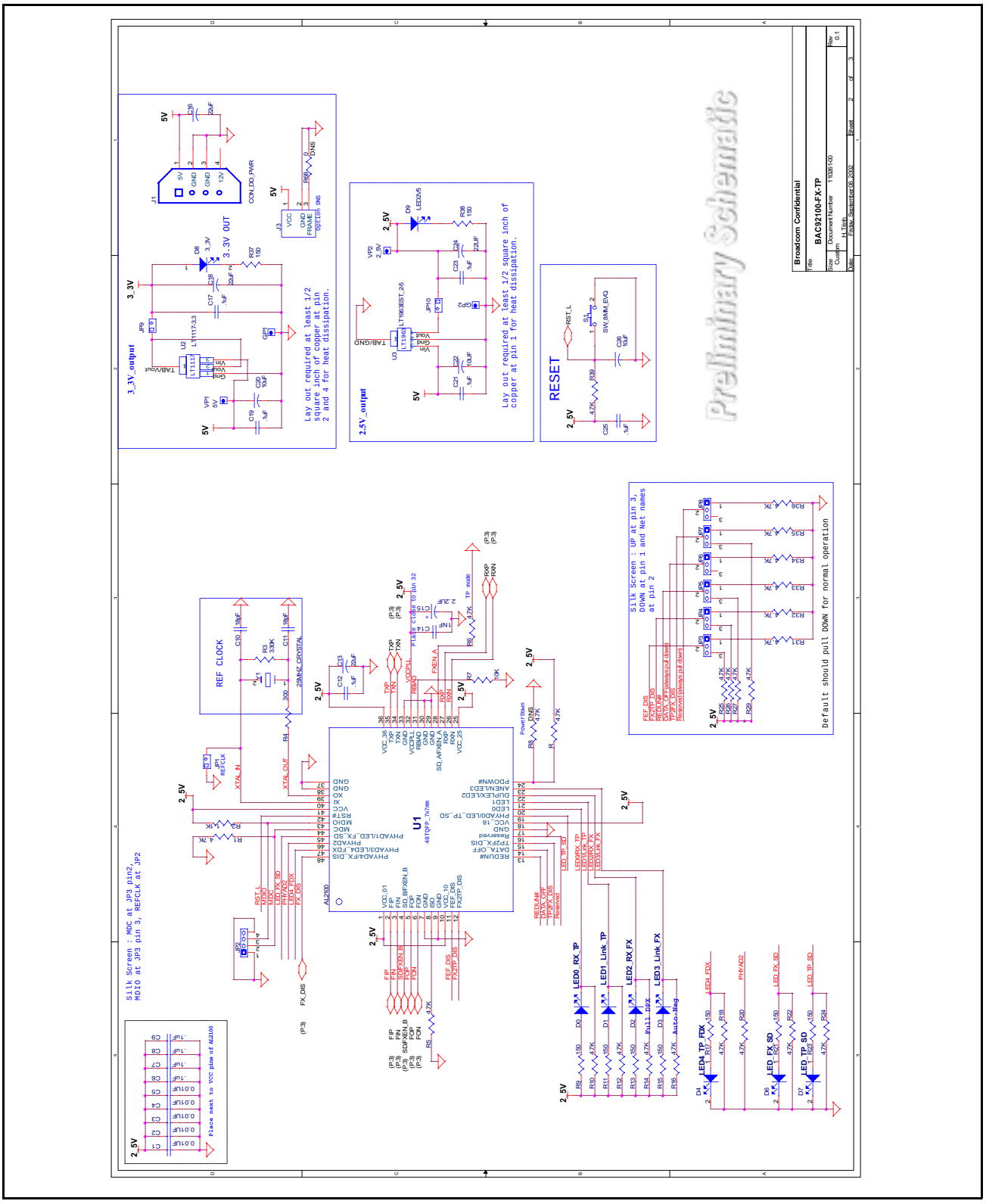


Figure 11: AL2100 Reference Schematic (page 1 of 2)

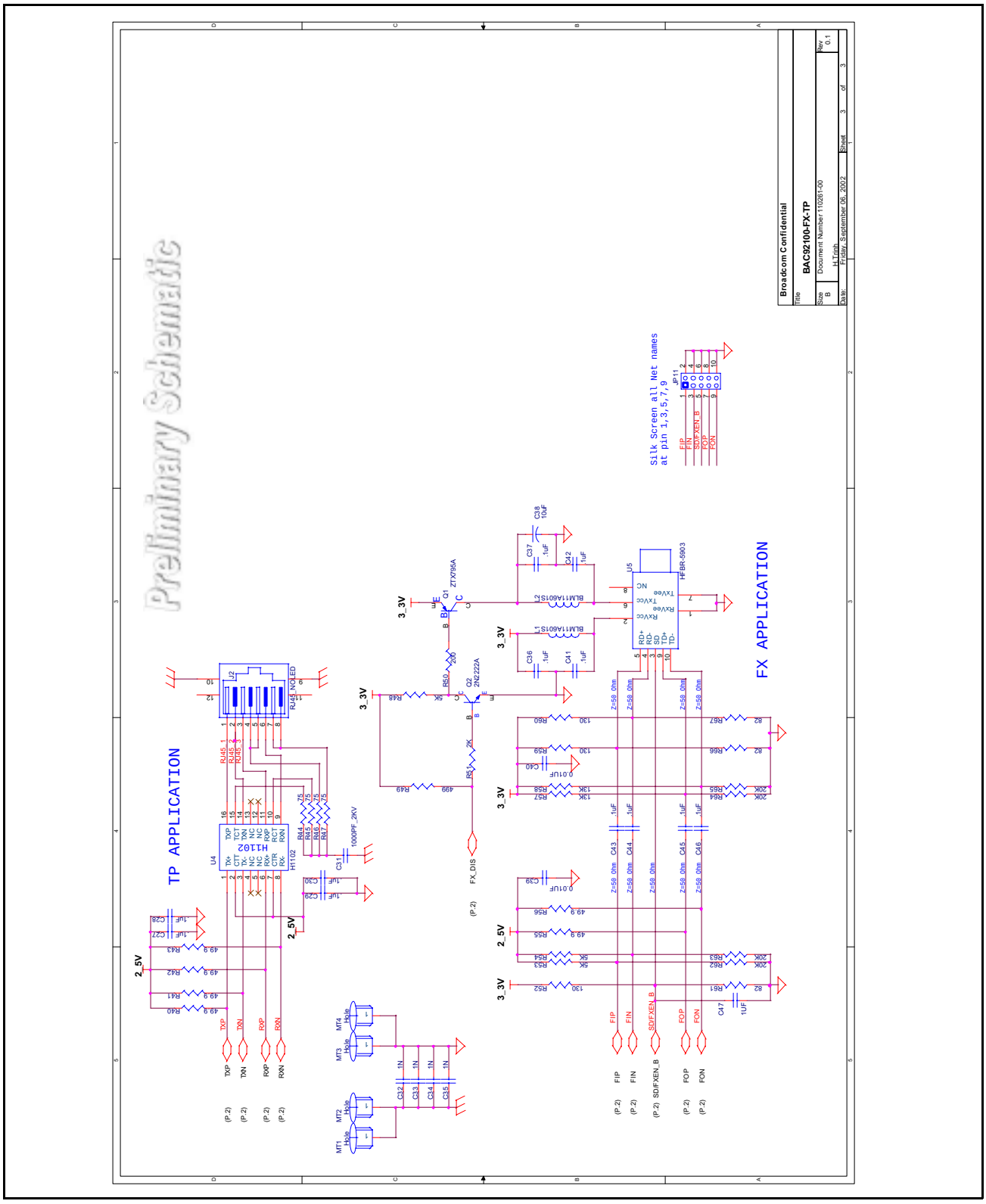
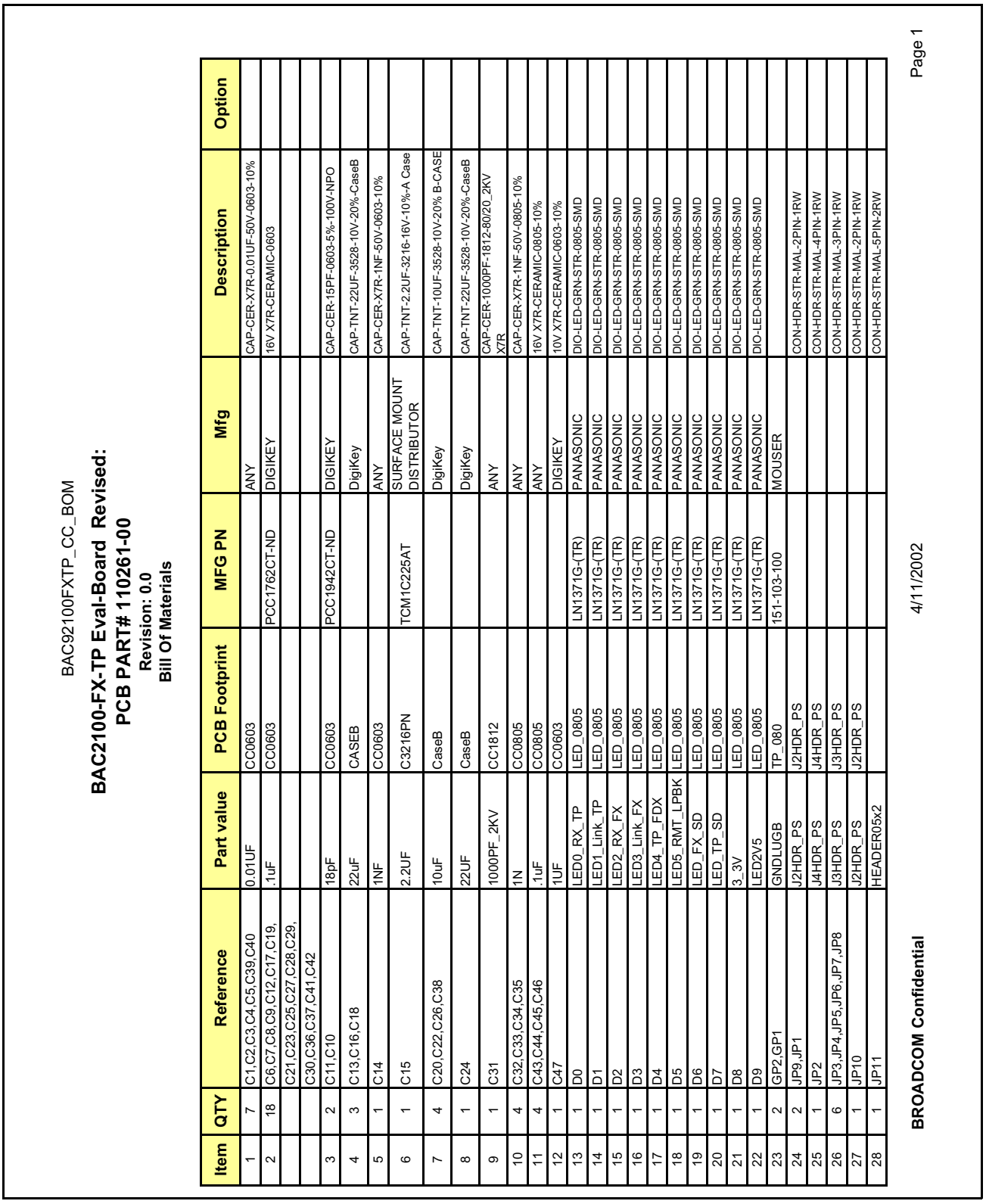


Figure 12: AL2100 Reference Schematic (page 2 of 2)



BAC92100FXTP_CC_BOM

BAC2100-FX-TP Eval-Board Revised:
PCB PART# 110261-00
Revision: 0.0
Bill Of Materials

Item	QTY	Reference	Part value	PCB Footprint	MFG PN	Mfg	Description	Option
1	7	C1,C2,C3,C4,C5,C39,C40	0.01UF	CC0603		ANY	CAP-CER-X7R-0.01UF-50V-0603-10%	
2	18	C6,C7,C8,C9,C12,C17,C19,	.1uF	CC0603	PCC1762CT-ND	DIGIKEY	16V X7R-CERAMIC-0603	
		C21,C23,C25,C27,C28,C29,						
		C30,C36,C37,C41,C42						
3	2	C11,C10	18pF	CC0603	PCC1942CT-ND	DIGIKEY	CAP-CER-15PF-0603-5%-100V-NPO	
4	3	C13,C16,C18	22uF	CASEB		DigiKey	CAP-TNT-22UF-3528-10V-20%-CaseB	
5	1	C14	1NF	CC0603		ANY	CAP-CER-X7R-1NF-50V-0603-10%	
6	1	C15	2.2UF	C3216PN	TCM1C225AT	SURFACE MOUNT DISTRIBUTOR	CAP-TNT-2.2UF-3216-16V-10%-A Case	
7	4	C20,C22,C26,C38	10uF	CaseB		DigiKey	CAP-TNT-10UF-3528-10V-20% B-CASE	
8	1	C24	22UF	CaseB		DigiKey	CAP-TNT-22UF-3528-10V-20%-CaseB	
9	1	C31	1000PF_2KV	CC1812		ANY	CAP-CER-1000PF-1812-80/20_2KV X7R	
10	4	C32,C33,C34,C35	1N	CC0805		ANY	CAP-CER-X7R-1NF-50V-0805-10%	
11	4	C43,C44,C45,C46	.1uF	CC0805		ANY	16V X7R-CERAMIC-0805-10%	
12	1	C47	1UF	CC0603		DIGIKEY	10V X7R-CERAMIC-0603-10%	
13	1	D0	LED0_RX_TP	LED_0805	LN1371G-(TR)	PANASONIC	DIO-LED-GRN-STR-0805-SMD	
14	1	D1	LED1_Link_TP	LED_0805	LN1371G-(TR)	PANASONIC	DIO-LED-GRN-STR-0805-SMD	
15	1	D2	LED2_RX_FX	LED_0805	LN1371G-(TR)	PANASONIC	DIO-LED-GRN-STR-0805-SMD	
16	1	D3	LED3_Link_FX	LED_0805	LN1371G-(TR)	PANASONIC	DIO-LED-GRN-STR-0805-SMD	
17	1	D4	LED4_TP_FDX	LED_0805	LN1371G-(TR)	PANASONIC	DIO-LED-GRN-STR-0805-SMD	
18	1	D5	LED5_RMT_LPBK	LED_0805	LN1371G-(TR)	PANASONIC	DIO-LED-GRN-STR-0805-SMD	
19	1	D6	LED_FX_SD	LED_0805	LN1371G-(TR)	PANASONIC	DIO-LED-GRN-STR-0805-SMD	
20	1	D7	LED_TP_SD	LED_0805	LN1371G-(TR)	PANASONIC	DIO-LED-GRN-STR-0805-SMD	
21	1	D8	3_3V	LED_0805	LN1371G-(TR)	PANASONIC	DIO-LED-GRN-STR-0805-SMD	
22	1	D9	LED2V5	LED_0805	LN1371G-(TR)	PANASONIC	DIO-LED-GRN-STR-0805-SMD	
23	2	GP2,GP1	GNDLUGB	TP_080	151-103-100	MOUSER		
24	2	JP9,JP1	J2HDR_PS	J2HDR_PS			CON-HDR-STR-MAL-2PIN-1RW	
25	1	JP2	J4HDR_PS	J4HDR_PS			CON-HDR-STR-MAL-4PIN-1RW	
26	6	JP3,JP4,JP5,JP6,JP7,JP8	J3HDR_PS	J3HDR_PS			CON-HDR-STR-MAL-3PIN-1RW	
27	1	JP10	J2HDR_PS	J2HDR_PS			CON-HDR-STR-MAL-2PIN-1RW	
28	1	JP11	HEADER05x2				CON-HDR-STR-MAL-5PIN-2RW	

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Figure 13: AL2100 Bill of Material for Reference Schematic (page 1 of 3)

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			CON_DD_PWR	HEADER_PWR	15-24-4157	MOLEX	MOLEX-PWRHEADER-5PINS-250V-10A	
29	1	J1	CON_DD_PWR	HEADER_PWR	15-24-4157	MOLEX	MOLEX-PWRHEADER-5PINS-250V-10A	
30	1	J2	RJ45_NOLED	RJ_45			RJ45-NOLED-SHIELD	
31	2	L2,L1	BLM11A601S	LC0603	BLM11A601S	MURATA ELECTRONICS NORTH	IND-FB-200MA-600@100MHZ-0603	
32	4	MT1,MT2,MT3,MT4	Hole	MTG_125				DNS
33	1	Q1	ZTX795A	TO92			TRS-GP-ZTX795A-TO92-PNP 140V 0.5A 100HFE	
34	1	Q2	2N2222A	TO18	2N222A	PHILIPS	TRS-GP-2N2222-TO18-NPN 40V 150MA 100HFE	
35	24	R1,R5,R6,R10,R12,R14,R16,	4.7K	RC0603		ANY	RES-THK-4.7K-5%-1/16W-0603	
		R18,R20,R22,R24,R25,R26,						
		R27,R28,R29,R30,R31,R32,						
		R33,R34,R35,R36,R39						
36	1	R2	1.1K	RC0603		ANY	RES-THK-1.1K-0603-1%-63MW	
37	1	R3	330K	RC0603	RM73B1JT334J	Eric Electronic	RES-THK-330K-0603-5%-63MW	DNS
38	1	R4	300	RC0603		ANY	RES-THK-300-0603-5%-63MW	
38.a	1	R50	200	RC0603		ANY	RES-THK-200-0603-5%-63MW	
39	1	R7	10K	RC0603		DigiKey (Genr)	RES-THK-10K-0603-1%-63MW	
40	1	R8	4.7K	RC0603		ANY	RES-THK-4.7K-5%-1/16W-0603	DNS
41	10	R9,R11,R13,R15,R17,R19,	150	RC0603		ANY	RES-THK-150-5%-1/16W-0603	
		R21,R23,R37,R38						
42	6	R40,R41,R42,R43,R55,R56	49.9	RC0603		ANY	RES-THK-49.9-1/16W-0603-1%	
43	4	R44,R45,R46,R47	75	RC0603		ANY	RES-THK-75-0603-1%-63MW	
44	3	R48,R53,R54	5K	RC0603			RES-THK-5K-1%-1/16W-0603	
45	1	R49	499	RC0603			RES-THK-499-1%-1/16W-0603	
46	1	R51	2K	RC0603		Any	RES-THK-2K-0603-5%-63MW	
47	3	R52,R59,R60	130	RC0603			RES-THK-130-1%-1/16W-0603	
48	2	R57,R58	13K	RC0603			RES-THK-13K-1%-1/16W-0603	
49	3	R61,R66,R67	82	RC0603		ANY	RES-THK-82-1%-1/16W-0603	
50	4	R62,R63,R64,R65	20K	RC0603		ANY	RES-THK-20K-1%-1/16W-0603	
51	1	S1	SW_8MM_EVQ	SW_8MM_EVQ	P8029SCT	DigiKey		
52	1	U1	AL2100	QFP7X7_48		Broadcom	atest revision	
53	1	U2	LT1117-3.3	SOT223			IC-LGC-LT1117-3.3V-SOT223 LINEAR REG 500MA 3.3V	
54	1	U3	LT1963EST_2-5	LT1963_SOT223	LT1963EST-2.5	Linear Tech		
55	1	U4	H1102	SO16W	H1102	PULSE	Auto MDI/MDIX-XFM-1to1-Pulse-SO16W H1102	
56	1	U5	HFBR-5903	HFBR5903	HFBR-5903	Agilent	Fiber-Module-HFBR5903-Agilent-TH	
57	1	VP1	5V	TP_080			CON-PIN-TEST-RED	
58	1	VP2	2_5V	TP_080			CON-PIN-TEST-RED	

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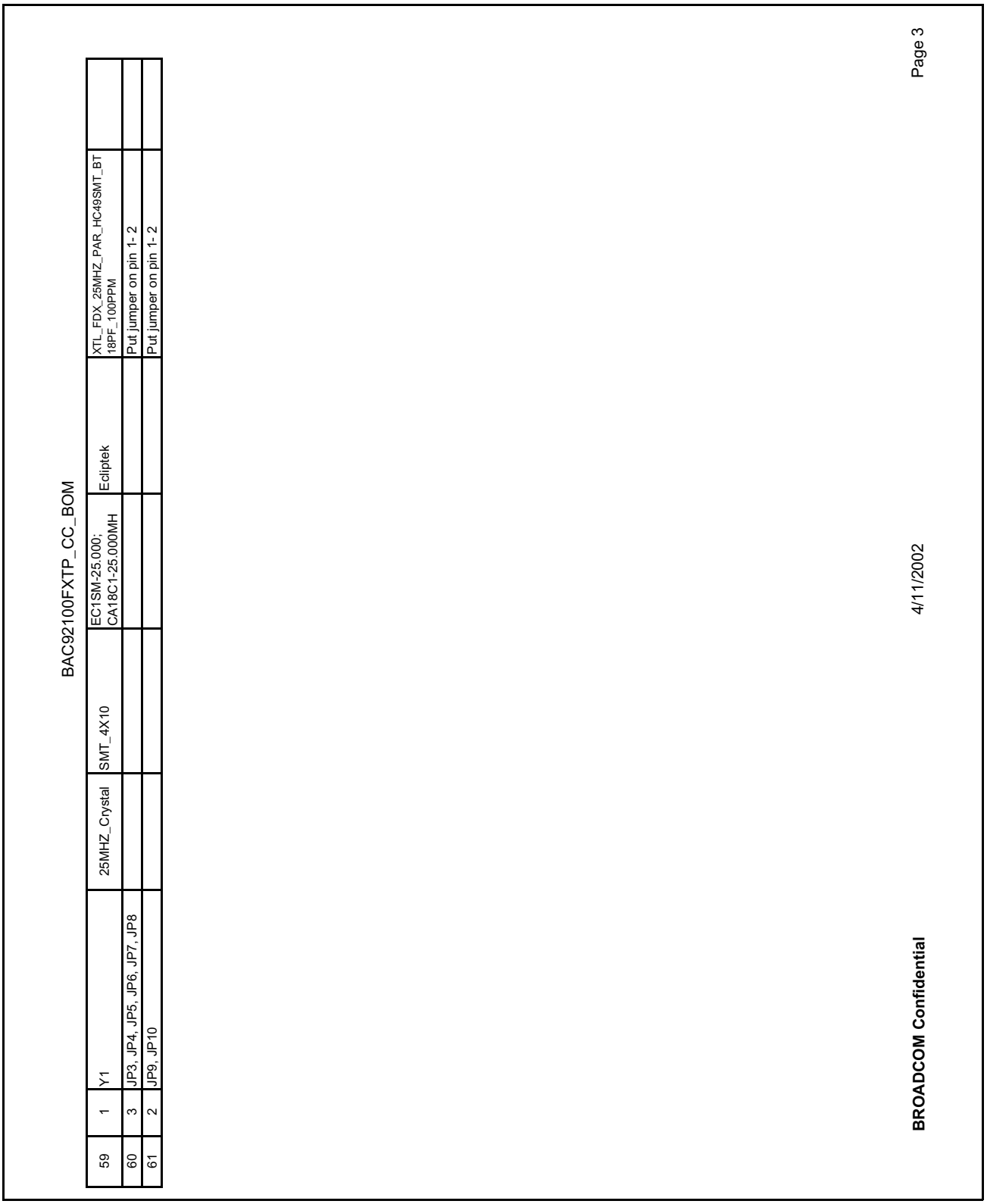

Figure 15: AL2100 Bill of Material for Reference Schematic (page 3of 3)

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