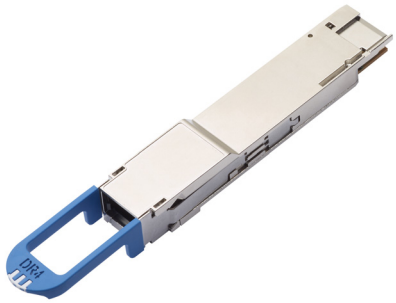
BROADCOM®

Data Sheet

AFCT-91DRDSZ

QSFP-DD Pluggable, Fiber-Optics Module 400G DR4, 500m SMF Ethernet Applications 8 × 50-Gb/s Electrical, 4 × 100-Gb/s Optical MPO Connector



Description

The Broadcom® AFCT-91DRDSZ is a fiber-optic, pluggable QSFP-DD transceiver for 400-gigabit Ethernet applications. This transceiver module is intended for Ethernet communication links over 500m of single-mode fiber optic (SMF) cable. The transceiver converts eight electrical data lanes at 53.125 Gb/s (PAM4 encoded) at the host system into four high-speed optical lanes at 106.25 Gb/s (PAM4 encoded) on the line side for an aggregated link bandwidth of 400 Gb/s. The optical interface includes four transmit data lanes and four receive data lanes using a signal carrier wavelength of 1310 nm in a DR4 configuration, intended for use with connectorized parallel 4+4 fiber cabling. Each electrical lane conforms to the IEEE 802.3-2018 400GAUI-8 interface with host KP FEC.

The AFCT-91DRDSZ mechanical form factor is high-density, conforming to the QSFP-DD MSA (Type 2 housing) with a 76-contact electrical edge-type connector, and has a conventional MPO-12 optical receptacle. The pull tab facilitates insertion and extraction of these transceivers in high-density faceplate configurations. This module incorporates Broadcom integrated circuit and Silicon Photonics Chiplet in Package (SCIP) technology providing an interconnect solution with reliable performance and low power.

Part Number Ordering Options

400-Gigabit Ethernet Transceiver	AFCT-91DRDSZ
Host Compliance Board	AFCT-91HCB
Module Compliance Board	AFCT-91MCB

Features

- 400G link distances up to 500m SMF
- Electrically compliant to IEEE 400GbE electrical specification 802.3-2018 (Annex 120E, 400GAUI-8) with host KP FEC
- Optically compliant to IEEE 802.3-2018 (Clause 124, 400GBASE-DR4)
- QSFP-DD MSA Specification-compliant (CMIS 5.0)
- Class 1 Eye Safety
- Pull tab: Ease of transceiver insertion and extraction
- 0°C to 70°C case temperature operating range
- Silicon photonics technology: DFB laser transmitter, Mach-Zehnder modulator, and integrated photo detector
- Hot-pluggable QSFP-DD transceiver for ease of installation and servicing
- Two-wire serial (TWS) interface with digital monitoring and maskable interrupts for expanded functionality

Applications

- 400-gigabit Ethernet interconnects
- Datacom/telecom switch and router connections
- Data aggregation and backplane applications
- Proprietary protocol and density applications

Module and Label

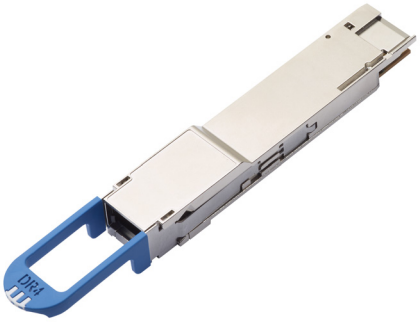
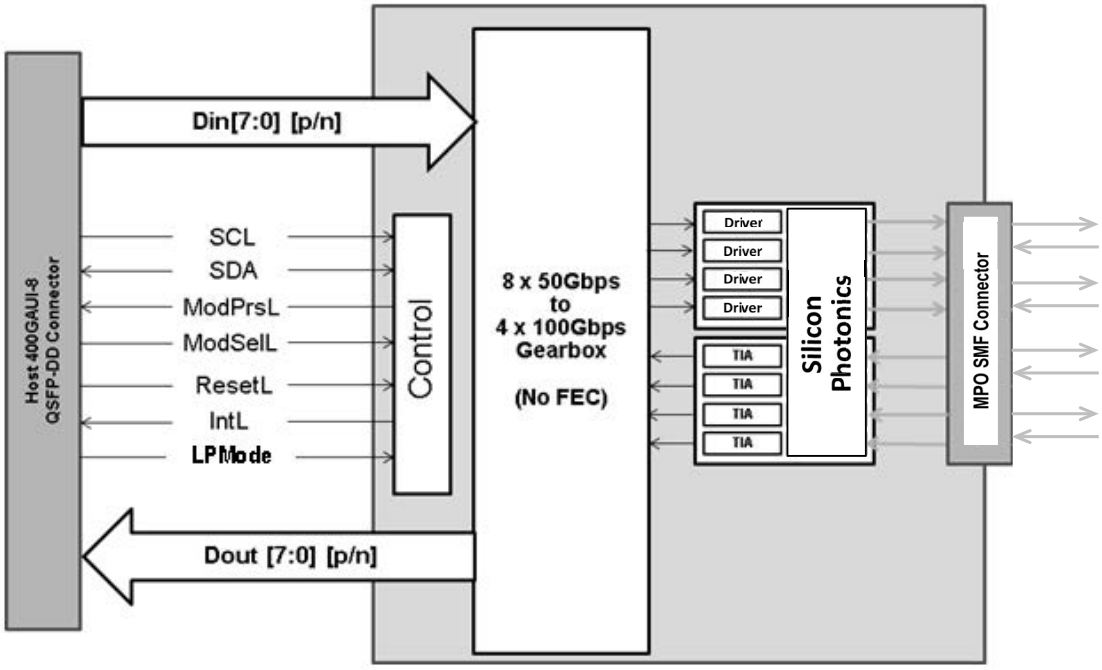


Figure 1: Transceiver Block Diagram



Transmitter

The optical transmitter portion of the transceiver (refer to Figure 1) incorporates an 8 × 50-Gb/s 400GAUI-8 compliant electrical input with equalization (EQ) block, integrated electrical multiplexer, silicon photonics, DFB lasers, Mach-Zehnder modulators, drivers, and diagnostic monitors. The transmitter is designed for EN 60825 and CDRH Class 1 eye safety compliance. The Tx input buffer provides 400GAUI-8 compliant differential inputs, presenting a nominal differential input impedance of 100Ω. AC-coupling capacitors are located inside the QSFP-DD module and are not required on the host board. For module control and interrogation, the control interface (LVTTL compatible) incorporates a two-wire serial (TWS) interface of clock and data signals.

Receiver

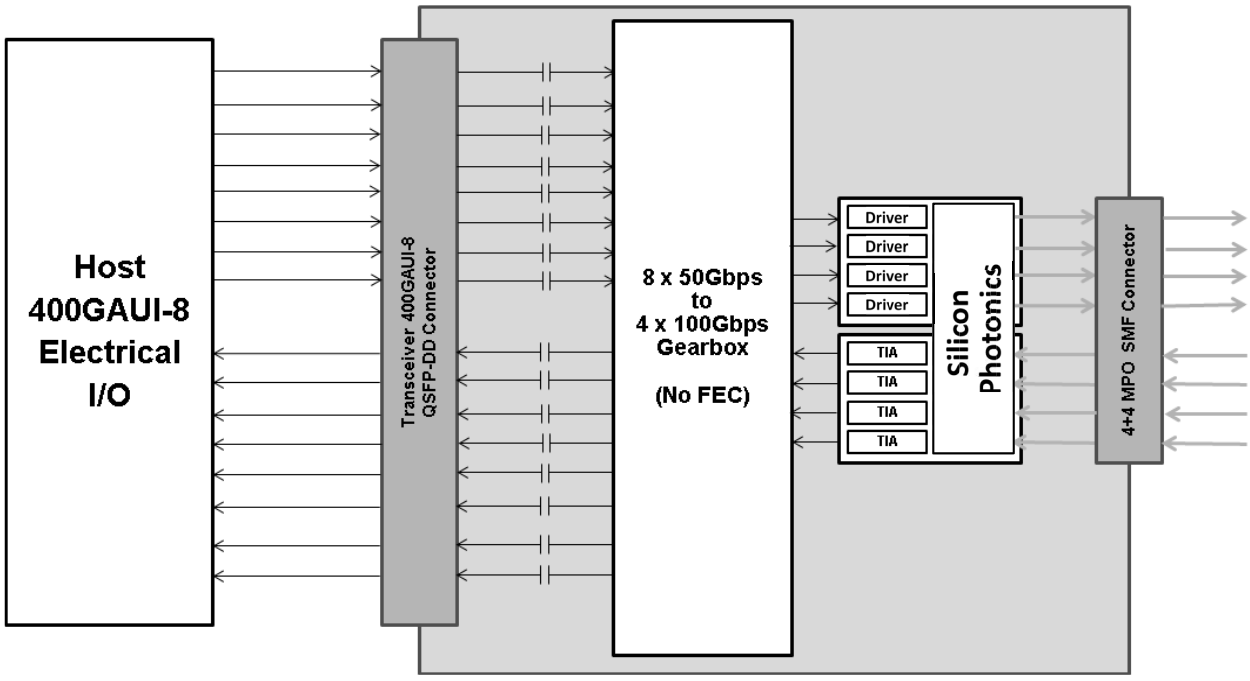
The optical receiver portion of the transceiver (refer to Figure 1) incorporates silicon photonics with integrated photo detectors, transimpedance amplifiers (TIAs), integrated demultiplexer, and 8 × 50 Gb/s 400GAUI-8 compliant electrical output blocks. The Rx Output Buffer provides 400GAUI-8 compliant differential outputs for the high-speed electrical interface presenting nominal single-ended output impedances of 50Ω to AC ground and 100Ω differentially that should be differentially terminated with 100Ω. AC-coupling capacitors are located inside the QSFP-DD module and are not required on the host board.

The optical outputs or electrical outputs squelch for loss of input signals (squelch disable is not implemented) and are disabled with channel deactivation through TWS interface. To reduce the need for polling, a hardware interrupt signal INTL is provided to inform hosts of an assertion of LOS or LOL.

High-Speed Electrical Signal Interface

Figure 2 shows the interface between an ASIC/SerDes and the QSFP-DD module. The high-speed signal lines are internally AC coupled, and the electrical inputs are internally terminated to 100Ω differential. All transmitter and receiver electrical channels are compliant to module 400GAUI-8 specifications per IEEE 802.3 Annex 120E.

Figure 2: Application Reference Diagram



Control Signal Interface

The module has the following low-speed signals for control and status: ModSelL, LPMode, ResetL, ModPrsL, and IntL. In addition, an industry-standard TWS is scaled for 3.3V LVTTL. It is implemented as a target device. Signal and timing characteristics are further defined in Control Interface and Memory Map.

The registers of the serial interface memory are defined in Control Interface and Memory Map.

Digital Diagnostic Monitoring

The information provides opportunity for predictive failure identification, compliance prediction, fault isolation, and component monitoring.

Predictive Failure Identification – The diagnostic information allows the host system to identify potential link problems. When identified, a *failover* technique isolates and replaces suspect devices before system uptime is impacted.

Compliance Prediction – The real-time diagnostic parameters can be monitored to alert the system when operating limits are exceeded and compliance cannot be ensured. As an example, the real-time average receiver optical power can assess the compliance of the cable plant and remote transmitter.

Fault Isolation – The diagnostic information allows the host to pinpoint the location of a link problem and accelerate system servicing and minimize downtime.

Component Monitoring – As part of host system qualification and verification, real-time transceiver diagnostic information is combined with system-level monitoring to ensure performance and operating environment are meeting application requirements.

Digital diagnostic monitoring for the following attributes is implemented:

- **Transceiver Module Temperature**
  Represents the module case temperature (lower page 00h bytes 14 to 15).
- **Transceiver Module Power Supply**
  Reports the module +3.3V supply voltage (lower page 00h bytes 16 to 17).
- **Transmitter Output Power**
  Reports the average output optical power for each transmitter channel (upper page 11h bytes 154 to 155 for channel 1, bytes 156 to 157 for channel 2, bytes 158 to 159 for channel 3, bytes 160 to 161 for channel 4).
- **Transmitter Laser Bias Current**
  Reports the DC laser bias current for each transmitter channel (upper page 11h bytes 170 to 171 for channel 1, bytes 172 to 173 for channel 2, bytes 174 to 175 for channel 3, bytes 176 to 177 for channel 4).
  The bias current increment value of 2 µA is to be scaled by the multiplier specified in upper page 01h byte 160 bits 4:3 (00b = multiply x 1; 01b = multiply x 2; 10b = multiply x 4; 11b = reserved). This multiplier also applies to the increment value for the bias current alarm and warning thresholds.
- **Receiver Input Power**
  Reports the average input optical power for each receiver channel (upper page 11h bytes 186 to 187 for channel1, bytes 188 to 189 for channel 2, bytes 190 to 191 for channel 3, bytes 192 to 193 for channel 4).

Table 1: Module DMI Accuracy

Temperature	± 3	°C
Power Supply Voltage	± 0.1	V
TX Output Power[a]	± 3	dB
TX Laser Bias Current	± 10	%
RX Input Power[a]	± 3	dB

a. Over an optical range of (–3 dBm, +4 dBm) per channel.

All diagnostic monitor attributes are 2-byte fields. To maintain coherency, the host must access these with single 2-byte read sequences.

For each monitored attribute, alarm and warning thresholds are established. Flags are set and interrupts generated when the attributes are outside the thresholds. All flags are latched and remain set even if the condition initiating the flag clears. A mask bit that can be set to prevent assertion of interrupt for each individual attribute exists for every monitor flag. Entries in the mask fields are volatile.

Regulatory and Compliance Issues

Various standard and regulations apply to the modules. These include eye-safety, EMC, ESD, and RoHS. Refer to Regulatory Compliance for details regarding these and component recognition. Note that the transmitter module is a Class 1 laser product. Refer to the Regulatory Compliance Table for details.

Package Outline

The module is designed to meet the package outline defined in the QSFP-DD MSA specification. Refer to Package Outline for details.

Handling and Cleaning

The transceiver module can be damaged by exposure to current surges and over voltage events. Take care to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Wave soldering, reflow soldering, and aqueous wash process with the modules on board are not recommended. Observe normal handling precautions for electrostatic discharge sensitive devices.

Each module is supplied with an inserted port plug for protection of the optical ports. Ensure that this plug is always in place whenever a fiber cable is not inserted.

The optical connector includes recessed elements that are exposed whenever a cable or port plug is not inserted. Prior to insertion of a fiber-optic cable, clean the cable end to avoid contamination from the cable plug. The port plug ensures that the optics remain clean and no additional cleaning should be needed. In the event of contamination, use standard MPO port cleaning methods. Use dry nitrogen or clean dry air at less than 20 psi to dislodge the contamination. Do not use liquids.

Absolute Maximum Ratings

Stress in excess of any of the individual absolute maximum ratings can cause immediate catastrophic damage to the module even if all other parameters are within recommended operating conditions. Do not assume that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the absolute maximum ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	–40	85	°C	—
3.3V Power Supply Voltage	V_{CC}	–0.5	3.6	V	—
Data Input Voltage – Single Ended	—	–0.5	V_{CC} + 0.5	V	—
Data Input Voltage – Differential	$\|V_{DIp} – V_{DIn}\|$	—	0.8	V	a
Control Input Voltage	Vi	–0.5	V_{CC} + 0.5, 3.6	V	—
Control Output Current	I_O	–20	20	mA	—
Relative Humidity	RH	5	95	%	—

a. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input should be at least 1600 mV peak-to-peak differential.

Recommended Operating Conditions

Recommended operating conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the recommended operating conditions, reliability is not implied, and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Case Temperature	T_C	0	—	70	°C	a
3.3V Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Electrical Signal Rate per Channel (PAM Encoded)	—	—	26.5625	—	GBd	b
Optical Signal Rate per Channel (PAM Encoded)	—	—	53.125	—	GBd	c
Power Supply Noise	—	—	—	66	mVpp	d
Receiver Differential Data Output Load	—	—	100	—	Ω	—
Fiber Length (9-µm SMF)	—	2	—	500	m	e

a. The position of case temperature measurement is shown in Figure 7. Avoid continuous operation at the maximum recommended operating case temperature to not degrade reliability.

b. ± 100 ppm. 400GAUI-8 operation with host-generated FEC. The AFCT-91DRDSZ must receive precoded FEC signals from the host ASIC.

c. ± 100 ppm. 400G DR4 operation with host-generated FEC. The AFCT-91DRDSZ must receive precoded FEC signals from the host ASIC.

d. Power supply noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels, including peak-to-peak noise, are limited to the recommended operating range of the associated power supply. Refer to Figure 6 for the reference power supply filter.

e. 9-µm SMF (minimum). The maximum link distance is based on an allocation of 1 dB of attenuation and 3 dB total connection and splice loss. The loss of a single connection should not exceed 0.5 dB.

General Electrical Characteristics

The following characteristics are defined over the recommended operating conditions unless otherwise noted. For control signal timing including ModSelL, LPMode, ResetL, ModPrsL, IntL, SCL, and SDA, refer to Control Interface and Memory Map.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Transceiver Power Consumption	—	—	—	12	W	Power Class 6
Transceiver Power Supply Current, Total	—	—	—	3463	mA	—
AC-Coupling Capacitors (Internal)	—	—	0.1	—	µF	—

High-Speed Electrical Input Characteristics

From 400GAUI-8, IEEE 802.3 Annex 120E. The following characteristics are defined over the recommended operating conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Unit	Notes/Conditions
Signaling Rate, Per Lane (PAM4 encoded)	TP1	—	26.5625	—	GBd	±100 ppm
Differential Peak-to-Peak Input Voltage Tolerance	TP1a	900	—	—	mV	—
Differential Input Return Loss, Minimum	TP1	—	Eq 83E-5	—	dB	IEEE 802.3
Differential to Common-Mode Input Return Loss, Minimum	TP1	—	Eq 83E-6	—	dB	IEEE 802.3
Differential Termination Mismatch	TP1	—	—	10	%	—
Module Stressed Input Test	TP1a	—	120E.3.4.1	—	—	IEEE 802.3[a]
Single-Ended Voltage Tolerance Range	TP1a	–0.4	—	3.3	V	—
DC Common-Mode Output Voltage	TP1	–0.35	—	2.85	V	[b]

a. Meets BER specified in IEEE 802.3 annex 120E.1.1.

b. DC common-mode voltage is generated by the host. The specification includes effects of ground offset voltage.

Parameter	Value	Unit	Notes/Conditions
Module Stressed Input Test	—	—	[a]
ESMW (Eye Symmetry Mask Width)	0.22	UI	—
Eye Width	0.22	UI	—
Applied Peak-to-Peak Sinusoidal Jitter	Table 120E-6	—	IEEE 802.3
Eye Height	32	mV	—

a. Module stressed input tolerance is measured using the procedure defined in IEEE 802.3 annex 83E.3.4.1.1.

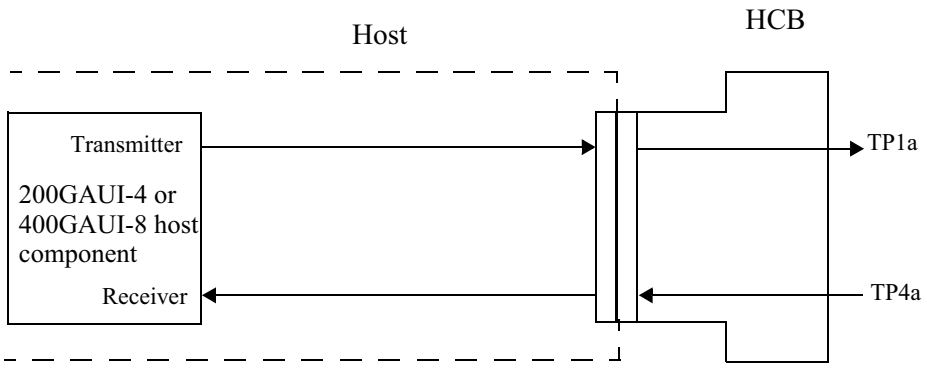
Parameter	Test Point	Min.	Typ.	Max.	Unit	Notes/Conditions
Electrical Input LOS Assert Threshold, Differential Peak-to-Peak Voltage Swing	ΔVdi pp los	70	—	—	mVpp	—
LOS Hysteresis	—	0.5	—	4	dB	[a]

a. LOS hysteresis is defined as 20*Log(LOS Deassert Level / LOS Assert Level).

Module Input Electrical Characteristics

Test Point	Description
TP0	Host ASIC transmitter output at the ASIC package pin on a DUT board.
TP1	Input to the module compliance board through the mated module compliance board and the module connector. Tests module input.
TP1A	Host ASIC transmitter output across the host board and the host edge card connector at the output of the host compliance board.
TP2	Optical transmitter output as measured at the end of a 2m to 5m patch cord mated to the optical module.
TP3	Optical test point as measured at the end of an optical fiber cable; closest test point to the presumed optical receiver input.
TP4	Module output through the mated module and the host edge card connector through the module compliance board.
TP4A	Input to the host compliance board through the mated host compliance board and the host edge card connector. Tests host input.
TP5	Input to host ASIC.

Figure 3: IEEE 802.3 400GAUI-8 Compliance Points TP1a, TP4a



The reference receiver measures the eye width and the eye height. The reference receiver includes a selectable continuous time linear equalizer (CTLE), which is described by Equation (IEEE 802.3 120E-2) with coefficients (IEEE 802.3 Table 120E-2).

$$H(f) = \frac{GP_1P_2P_{LF}}{Z_1Z_{LF}} \times \frac{j2\pi f + Z_1}{(j2\pi f + P_1)(j2\pi f + P_2)} \times \frac{j2\pi f + Z_{LF}}{j2\pi f + P_{LF}}$$

where:

H(f)	is the CTLE transfer function, *f* is the frequency in GHz
G	is the CTLE gain
P_1, P_2	are the CTLE poles in Grad/s
Z_1	is the CTLE zero in Grad/s
P_{LF}	is the low frequency CTLE pole in Grad/s
Z_{LF}	is the low frequency CTLE zero in Grad/2
j	is the square root of –1
f	is the frequency in GHz

Reference CTLE Coefficients (Table 120E-2 IEEE 802.3)

26.5625 GBd						
Peaking (dB)	**G**	**$P_1/2\pi$ (GHz)**	**$P_2/2\pi$ (GHz)**	**$Z_1/2\pi$ (GHz)**	**$P_{LF}/2\pi$ (GHz)**	**$Z_{LF}/2\pi$ (GHz)**
1	0.891251	26.5625	14.1	9.463748	1.2	1.2
1.5	0.841395	26.5625	14.1	9.248465	1.2	1.15
2	0.794328	26.5625	14.1	9.069645	1.2	1.1
2.5	0.749894	26.5625	14.1	8.640319	1.2	1.075
3	0.707946	26.5625	14.1	8.255665	1.2	1.05
3.5	0.668344	26.5625	14.1	7.906766	1.2	1.025
4	0.630957	26.5625	14.1	7.58765	1.2	1
4.5	0.595662	26.5625	14.1	7.076858	1.2	1
5	0.562341	26.5625	14.1	6.614781	1.2	1
5.5	0.530884	26.5625	14.1	6.193091	1.2	1
6	0.501187	26.5625	14.1	5.805801	1.2	1
6.5	0.473151	26.5625	14.1	5.448395	1.2	1
7	0.446684	26.5625	14.1	5.117337	1.2	1
7.5	0.421697	26.5625	14.1	4.809777	1.2	1
8	0.398107	26.5625	14.1	4.523367	1.2	1
8.5	0.375837	26.5625	14.1	4.256129	1.2	1
9	0.354813	26.5625	14.1	4.006377	1.2	1

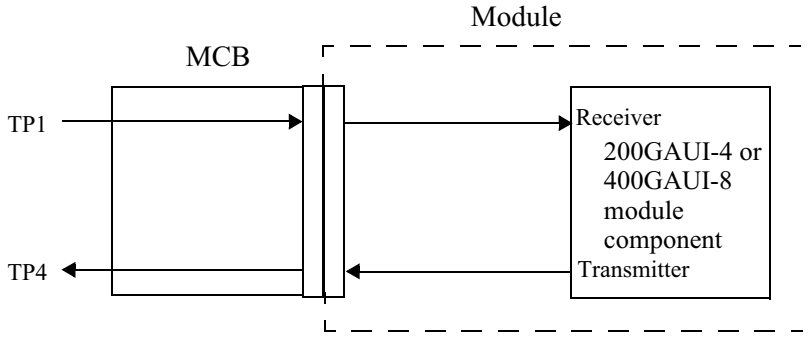
High-Speed Electrical Output Characteristics

From 400GAUI-8, IEEE 802.3 Annex 120E. The following characteristics are defined over the recommended operating conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Unit	Notes/Conditions
Signaling Rate, Per Lane PAM4 Encoded	TP4	—	26.5625	—	GBd	±100 ppm
AC Common-Mode Output Voltage (RMS)	TP4	—	—	17.5	mV, rms	—
Differential Peak-to-Peak Output Voltage	TP4	—	—	900	mV	—
Near-End Eye Symmetry Mask Width (ESMW)	TP4	0.265	—	—	UI	—
Near-End Eye Height, Differential	TP4	70	—	—	mV	—
Far-End Eye Symmetry Mask Width (ESMW)	TP4	0.2	—	—	UI	—
Far-End Eye Height, Differential	TP4	30	—	—	mV	—
Far-End Pre-Cursor ISI Ratio	TP4	–4.5	—	2.5	%	—
Differential Output Return Loss, Minimum	TP4	—	Eq 83E-2	—	dB	IEEE 802.3
Common to Differential Mode Conversion Return Loss, Minimum	TP4	—	Eq 83E-3	—	dB	IEEE 802.3
Differential Termination Mismatch	TP4	—	—	10	%	—
Transition Time, 20% to 80%	TP4	9.5	—	—	ps	—
DC Common-Mode Voltage	TP4	–0.35	—	2.85	V	a

a. DC common-mode voltage is generated by the host. The specification includes effects of ground offset voltage.

Figure 4: IEEE 802.3 400GAUI-8 Compliance Points TP1, TP4



High-Speed Optical Transmitter Characteristics

From 400GBASE-DR4, IEEE 802.3 Clause 124. The following characteristics are defined over the recommended operating conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Unit	Notes/Conditions
Signaling Rate, Per Lane PAM4 Encoded	—	—	53.125	—	GBd	± 100 ppm
Lane Center Wavelength	TP2	1304.5	1310	1317.5	nm	—
Side Mode Suppression Ratio (SMSR)	TP2	30	—	—	dB	—
Average Launch Power, Each Lane	TP2	–2.9	—	+4.0	dBm	a
Outer Optical Modulation Amplitude (OMA), Each Lane	TP2	–0.8	—	+4.2	dBm	b
Launched Power in OMA_{outer} – TDECQ, Each Lane	TP2	–2.2	—	—	dBm	—
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), Each Lane	TP2	—	—	3.4	dB	—
Extinction Ratio, Each Lane	TP2	3.5	—	—	dB	—
$RIN_{21.4}OMA$	TP2	—	—	–136	dB/Hz	—
Optical Return Loss Tolerance	TP2	—	—	21.4	dB	—
Transmitter Reflectance	TP2	—	—	–26	dB	c
Average Launch Power of OFF Transmitter, Each Lane	TP2	—	—	–15	dBm	d

a. Average launch power, each lane (min.) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

b. Even if the TDECQ < 1.4dB, the OMA_{outer}(min) must exceed these values.

c. Transmitter reflectance is defined looking into the transmitter.

d. Under all transmitter lanes disabled condition only.

High Speed-Optical Receiver Characteristics

From 400GBASE-DR4, IEEE 802.3 Clause 124. The following characteristics are defined over the recommended operating conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Unit	Notes/Conditions
Signaling Rate, Per Lane PAM4 Encoded		—	53.125	—	GBd	± 100ppm
Lane Center Wavelength	TP3	1304.5	1310	1317.5	nm	—
Damage Threshold	TP3	+5.0	—	—	dBm	a
Receiver Average Power, Each Lane	TP3	–5.9	—	+4.0	dBm	b
Receiver Optical Modulation Amplitude (OMA_{outer}), Each Lane	TP3	max(–3.9, SECQ–5.3)	—	+4.2	dBm	c
Receiver Reflectance	TP3	—	—	–26	dB	—
Receiver Stressed Sensitivity OMA_{outer}, Each Lane	TP3	—	—	–1.9	dBm	d
Conditions of Stressed Receiver Sensitivity	TP3	—	—	—	—	e
Stressed Eye Closure (SECQ), Lane under Test	TP3	—	3.4	—	dB	—
OMA_{outer} of Each Aggressor Lane	TP3	—	4.2	—	dBm	—
LOS Assert – AVG	TP3	–15	—	—	dBm	—
LOS De-Assert – AVG	TP3	—	—	–5.9	dBm	—
LOS Hysteresis	TP3	0.5	—	—	dB	—

a. The receiver should be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.

b. Average receive power, each lane (min.) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

c. Receiver sensitivity (OMA_{outer}), each lane (max.) expressed as the minimum receiver power is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.

d. Measured with conformance test signal at TP3 (IEEE 802.3, Clause 124.8.9) for the BER specified in Clause 124.1.1.

e. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Regulatory Compliance

The AFCT-91DRDSZ complies with all applicable laws and regulations as detailed in the Regulatory Compliance Table. Certification level is dependent on the overall configuration of the host equipment. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

The AFCT-91DRDSZ is compatible with ESD levels found in typical manufacturing and operating environments as described in the Regulatory Compliance Table. In the normal handling and operation of optical transceivers, ESD is of concern in two circumstances.

The first case is during handling of the transceiver prior to insertion into a QSFP-DD compliant cage. To protect the device, it is important to use normal ESD handling precautions. These include use of grounded wrist straps, workbenches, and floor wherever a transceiver is handled.

The second case to consider is static discharges to the exterior of the host equipment chassis after installation. If the optical interface is exposed to the exterior of the host equipment cabinet, the transceiver may be subject to system level ESD requirements.

Electromagnetic Interference (EMI)

Equipment incorporating multi-gigabit transceivers is typically subject to regulation by the FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. The AFCT-91DRDSZ compliance to these standards is detailed in the Regulatory Compliance Table. The metal housing and shielded design of the AFCT-91DRDSZ minimizes the EMI challenge facing the equipment designer.

Flammability

The AFCT-91DRDSZ optical transceiver is made of metal and high strength, heat-resistant, chemical-resistant and UL94V-0 flame-retardant plastic.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JS-001-2017)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	EN61000-4-2, Criterion B	When installed in a properly grounded housing and chassis the units are subjected to 15-kV air discharges during operation and 8-kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15, CENELEC EN55022 (CISPR 22A), VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing 	Class 1 Laser Product Complies with FDA performance standards for laser products except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019. (IEC) EN 62368-1:2014+A11 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number: 2211516-000 TUV File: R 50556376 0001 CB File: JPTUV-138618
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E484615 UL-CA-2234877-0
RoHS Compliance	—	Less than 1000 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls (PPB), and polybrominated biphenyl ethers (PBDE).

QSFP-DD Module Pins

Figure 5: QSFP-DD Module Pin Layout

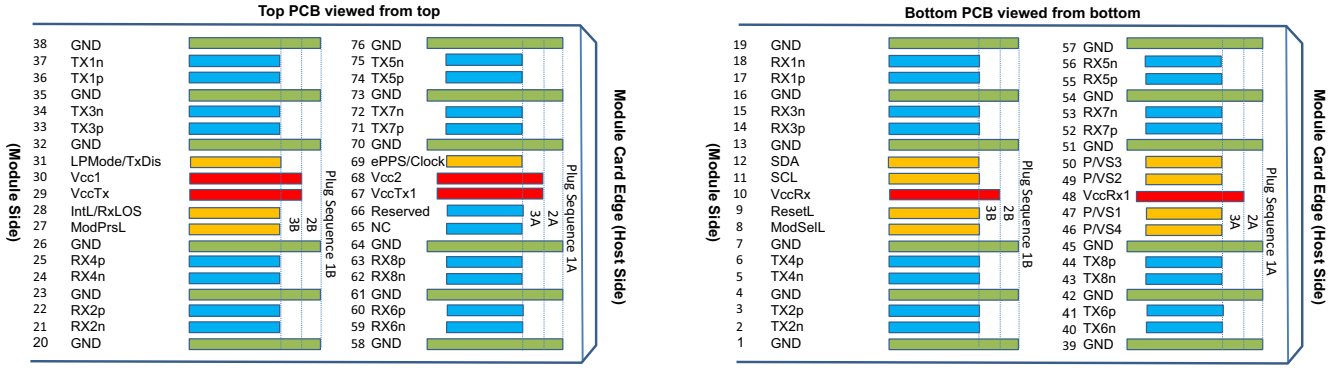


Table 2: QSFP-DD Module Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1	—	GND	Ground	1B	a
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	b
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	b
4	—	GND	Ground	1B	a
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	b
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	b
7	—	GND	Ground	1B	a
8	LVTTL-I	ModSelL	Module Select. When held low by the host, the module responds to TWS serial communication commands.	3B	—
9	LVTTL-I	ResetL	Module Reset. The ResetL signal is pulled up to V_{CC} in the QSFP-DD module.	3B	—
10	—	V_{CC} Rx	+3.3V Power Supply Receiver	2B	c
11	LVCMOS-I/O	SCL	TWS Interface Clock. Requires pull-up resistor to 3.3V on the host board.	3B	—
12	LVCMOS-I/O	SDA	TWS Interface Data. Requires pull-up resistor to 3.3V on the host board.	3B	—
13	—	GND	Ground	1B	a
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	b
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	b
16	—	GND	Ground	1B	a
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	b
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	b
19	—	GND	Ground	1B	a
20	—	GND	Ground	1B	a
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	b

Table 2: QSFP-DD Module Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	b
23	—	GND	Ground	1B	a
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	b
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	b
26	—	GND	Ground	1B	a
27	LVTTL-O	ModPrsL	Module Present. Requires pull-up resistor to 3.3V on the host board. Module Present is pulled low in the module.	3B	—
28	LVTTL-O	IntL	Interrupt. The IntL signal is an open collector output and must be pulled to host supply voltage (3.3V) on the host board.	3B	—
29	—	V_{CC} Tx	+3.3V Power Supply	2B	c
30	—	V_{CC}1	+3.3V Power Supply	2B	c
31	LVTTL-I	LPMode	Low Power Mode. LPMode is pulled up to V_{CC} in the module.	3B	—
32	—	GND	Ground	1B	a
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	b
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	b
35	—	GND	Ground	1B	a
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	b
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	b
38	—	GND	Ground	1B	a
39	—	GND	Ground	1A	a
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	b
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	b
42	—	GND	Ground	1A	a
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	b
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	b
45	—	GND	Ground	1A	a
46	—	NC	No Connect	3A	—
47	—	NC	No Connect	3A	—
48	—	V_{CC} Rx1	+3.3V Power Supply Receiver	2A	c
49	—	NC	No Connect	3A	—
50	—	NC	No Connect	3A	—
51	—	GND	Ground	1A	a
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	b
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	b
54	—	GND	Ground	1A	a
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	b
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	b

Table 2: QSFP-DD Module Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
57	—	GND	Ground	1A	a
58	—	GND	Ground	1A	a
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	b
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	b
61	—	GND	Ground	1A	a
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	b
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	b
64	—	GND	Ground	1A	a
65	—	NC	No Connect	3A	—
66	—	NC	No Connect	3A	—
67	—	V_{CC} Tx1	+3.3V Power Supply	2A	c
68	—	V_{CC}2	+3.3V Power Supply	2A	c
69	—	NC	No Connect	3A	—
70	—	GND	Ground	1A	a
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	b
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	b
73	—	GND	Ground	1A	a
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	b
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	b
76	—	GND	Ground	1A	a

a. GND is the symbol for signal supply (power) common for the QSFP-DD module. All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

b. For all Tx and Rx high-speed differential inputs/outputs, there are 0.1-µF AC-coupling capacitors located inside the QSFP-DD module, and they are not required on the host board.

c. V_{CC} Rx, V_{CC}1, and V_{CC} Tx are the receiver and transmitter power supplies and should be applied concurrently.

Figure 6: Reference Power Supply Filter

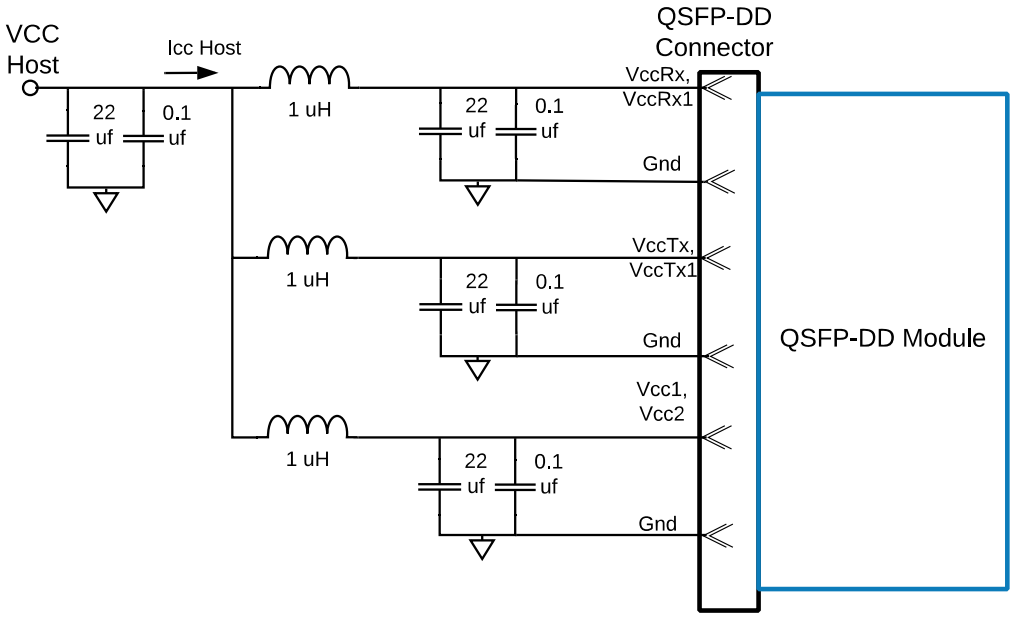
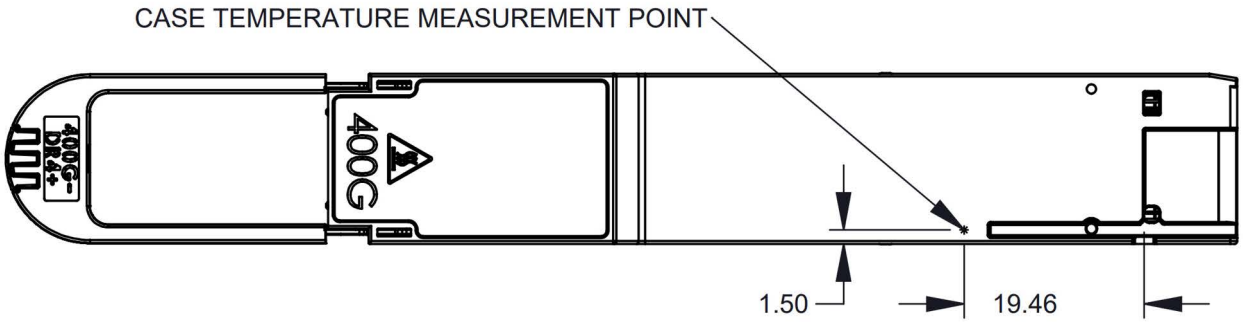
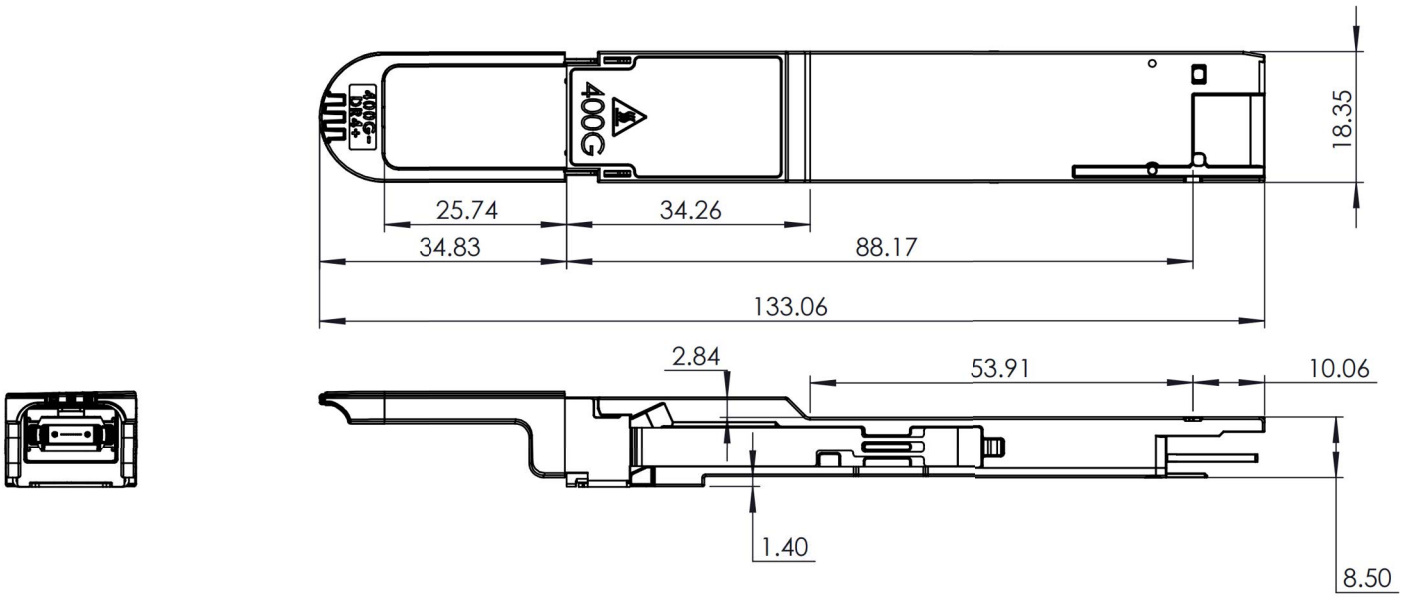


Figure 7: Case Temperature Measurement Point (All Dimensions Are in mm)



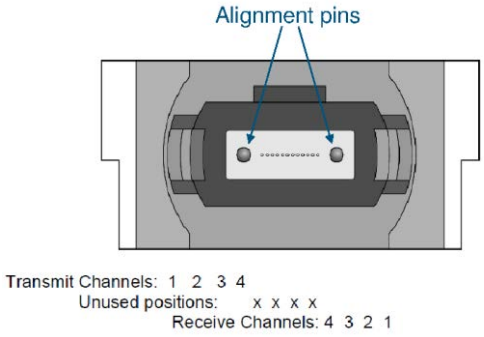
Package Outline

Figure 8: Mechanical Package Outline (All Dimensions Are in mm)



The optical interface port is a male MPO connector as specified in IEC61754-7. Use aligned key MTP/MPO patch cords to ensure alignment of the signals between the modules. The aligned key patch cord is defined in TIA-568.

Figure 9: Module Optical Interface (Looking into the Optical Port)



Control Interface and Memory Map

The control interface combines dedicated signal lines for ModSelL, LPMode, ResetL, ModPrsL, and IntL with two-wire serial (TWS), interface clock (SCL), and data (SDA) signals to provide users rich functionality over an efficient and easily used interface. The TWS interface is implemented as a target device and is compatible with industry-standard TWS protocol. It is scaled for 3.3V LVTTL. Outputs are high-Z in the high state to support busing of these signals. Signal and timing characteristics are further defined in I/O Timing for Control and Status Functions, Low-Speed Pin Electrical Specifications, and Management Interface Timing Parameters. For more details, refer to the *QSFP-DD MSA and CMIS* (Common Management Interface Specification).

ModSelL

The ModSelL is an input signal that is pulled up to V_{CC} in the QSFP-DD module. When held low by the host, the module responds to TWS communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single two-wire interface bus. When the ModSelL is *High*, the module does not respond to or acknowledge any two-wire interface communication from the host. The ModSelL signal input node is biased to the *High* state in the module. To avoid conflicts, the host system should not attempt two-wire interface communications within the ModSelL deassert time after any QSFP-DD modules are deselected. Similarly, the host must wait for at least the period of the ModSelL assert time before communicating with the newly selected module. The assertion and deasserting periods of the different modules may overlap as long as the preceding timing requirements are met.

ResetL

The ResetL signal is pulled up to V_{CC} in the QSFP-DD module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

LPMode

Low power mode. LPMode is pulled up to V_{CC} in the QSFP-DD module. The pin is a hardware control and used, in combination with soft LowPwr bit (lower page 00h byte 26 bit 6) and soft ForceLowPwr bit (lower page 00h byte 26 bit 4), to put modules into the low power mode. In low power mode, the power consumption is limited to Power Class 1 (1.5W maximum). By using the LPMode pin and the soft LowPwr bit, the host controls how much power a module can consume. Refer to the low power state truth table below.

Table 3: Low Power State Truth Table

ForceLowPwr pg 00h byte 26 bit 4	LowPwr pg 00h byte 26 bit 6	LPMode Hardware Signal	Low Power
1	—	—	1
0	1	Asserted	1
0	1	Deasserted	0
0	0	—	0

ModPrsL

ModPrsL is pulled up to V_{CC}_Host on the host board and grounded in the module. The ModPrsL is asserted *Low* when the transceiver is inserted into the host connector.

IntL

IntL is an output signal. The IntL signal is an open collector output and should be pulled to V_{CC} Host on the host board. When the IntL signal is asserted Low, it indicates a change in module state, a possible module operational fault, or a status critical to the host system. The host identifies the source of the interrupt using the two-wire serial interface. The IntL signal is deasserted *High* after all set interrupt flags are read (refer to the QSFP-DD MSA and CMIS specifications).

The user can read the present value of the various diagnostic monitors. Case module temperature, supply voltage, laser bias current for each optical lane, transmitter output power (Pave) for each optical lane, and receiver input power (Pave) for each optical lane are reported by default. All monitor items are 2-byte fields and, to maintain coherency, the host must access these with single 2-byte read sequences. For each monitored item, alarm and warning thresholds are established. If an item moves past a threshold, a flag is set, and, provided the item is not

masked, IntL is asserted. A mask bit that can be set to prevent assertion of IntL for the individual item exists for every LOS, LOL, Tx fault, and monitor flag. Entries in the mask fields are volatile.

Soft Status and Control

Several soft status signals and controls are available in the AFCT-91DRDSZ transceiver memory and accessible through the TWS interface. Some soft status signals include Receiver LOS, Transmitter LOS, and diagnostic monitor alarms and warnings. Some soft controls include module Force Low Power (ForceLowPwr), module Low Power (LowPwr), module Software Reset, Transmitter Disable (Tx_Dis), Receiver Output Disable (Rx_Dis), and masking of status signal in triggering IntL. Transmitter Squelch Disable (Tx_SqDis) and Receiver Squelch Disable (Rx_SqDis) are not available. Most soft status signals and controls are per-channel basis, but some are global. All soft control entries are volatile.

Transmitter LOS

The Transmitter LOS status signal is on page 11h address 136 bits 0 to 7 for lanes 1 to 8, respectively. Transmitter LOS is based on TP1a electrical input differential voltage and the factory-set LOS thresholds. This status register is latched, and it is cleared on read.

Receiver LOS

The Receiver LOS status signal is on page 11h address 147 bits 0 to 7 for lanes 1 to 8, respectively. Receiver LOS is based on TP3 optical input average power (Pavg), and the factory sets LOS thresholds. This status register is latched, and it is cleared on read. The Receiver LOS optional fast mode is not implemented.

Transmitter CDR LOL

The Transmitter CDR Loss of Lock status signal is on page 11h address 137 bits 0 to 7 for lanes 1 to 8, respectively. The loss of lock flag asserts if an enabled transceiver transmitter-side CDR or gearbox is not locked to the host electrical input data signal. This status register is latched, and it is cleared on read.

Receiver CDR LOL

The Receiver CDR Loss of Lock status signal is on page 11h address 148 bits 0 to 7 for lanes 1 to 8, respectively. The loss of lock flag asserts if an enabled transceiver, receiver-side electrical CDR, or gearbox is not locked to the recovered optical input data signal. This status register is latched, and it is cleared on read.

Transmitter Fault - Not Implemented

The Transmitter Fault status signal is on page 11h address 135 bits 0 to 7 for lanes 1 to 8, respectively. The Transmitter Fault is not implemented. The transceiver Transmitter Fault condition is detected if the laser output power is too high; that is, approaching eye safety levels. When fault is triggered, the corresponding transmitter channel optical output is disabled. Module reset or toggling of soft transmitter disable (page 10h, address 130) can restore the transmitter channel function unless a fault condition persists. This status register is latched, and it is cleared on read.

Module Force Low Power

The soft module ForceLowPwr control is on lower page 00h address 26 bit 4. When set to 1, the module is put into the low power mode with power consumption limited to Power Class 1 (1.5W maximum).

Module Low Power

The soft module low power control is on lower page 00h address 26 bit 6. With soft ForceLowPwr in the deasserted state (= 0), the module is put into the low power mode when the soft LowPwr bit is asserted (= 1) along with the assertion of the hardware LPMode pin (pulled up to V_{CC}).

Module Software Reset

The module Software Reset control is on lower page 00h address 26 bit 3. When set to 1, while the ResetL hardware signal is high (pulled to V_{CC}), it is equivalent to asserting the ResetL hardware signal (= 0), which prompts the module to reinitialize.

Transmitter Disable

The Transmitter Disable control is on page 10h address 130 bits 0 to 7 for lanes 1 to 8, respectively. Because every pair of 50G electrical lanes is multiplexed into one 100G optical lane, issuing a Transmitter Disable for any one lane in the electrical pair turns off the corresponding 100G Tx optical source. The transmitter disable optional fast mode is not implemented.

Receiver Disable

The Receiver Disable control is on page 10h address 138 bits 0 to 7 for lanes 1 to 8, respectively. If the receiver output is disabled, the electrical output differential voltage swing is less than 50 mVpp.

Transmitter Squelch Disable - Not Implemented

The Transmitter Squelch Disable control is on page 10h address 131 bits 0 to 7 for lanes 1 to 8, respectively. The Transmitter Squelch Disable is not implemented. The transceivers have transmitter output squelch function enabled as default. If any transmitter output is in the squelched state, the laser optical modulation output power will be turned off according to EEPROM page 00L byte 26 bit 5.

Receiver Squelch Disable - Not Implemented

The Receiver Squelch Disable control is on page 10h address 139 bits 0 to 7 for lanes 1 to 8, respectively. The Receiver Squelch Disable is not implemented. The transceivers have receiver output squelch function enabled as default. If the receiver output is in the squelched state, the electrical output differential voltage swing is less than 50 mVpp.

I/O Timing for Control and Status Functions

The following characteristics are defined over the recommended operating conditions unless otherwise noted. Per the QSFP-DD Hardware specification.

Table 4: I/O Timing

Parameter	Symbol	Min.	Max.	Unit	Reference
MgmtInitDuration	Max MgmtInit Duration	—	2000	ms	Time from power on[a], hot plug, or rising edge of Reset until completion of the MgmtInit State.
ResetL Assert Time	t_reset_init	10	—	µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL	—	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol.
IntL De-assert Time	toff_IntL	—	500	µs	Time from clear on read[b] operation of associated flag until Vout:IntL = Voh. This includes deassert times for RX LOS, TX Fault, and other flag bits.
RX LOS Assert Time[c]	ton_los	—	100	ms	Time from RX LOS condition present to RX LOS bit set (value = 1b) and IntL asserted.
TX Fault Assert Time (TX Fault Not Implemented)	ton_Txfault	—	200	ms	Time from TX Fault state to TX fault bit set (value = 1b) and IntL asserted.
Flag Assert Time	ton_flag	—	200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and IntL asserted.
Mask Assert Time	ton_mask	—	100	ms	Time from mask bit set (value = 1b)[d] until associated IntL assertion is inhibited.

Table 4: I/O Timing

Parameter	Symbol	Min.	Max.	Unit	Reference
Mask Deassert Time	toff_mask	—	100	ms	Time from mask bit cleared (value = 0b)[d] until associated IntL operation resumes.
Module Select Wait Time	ModSelL Wait Time	—	—	—	ModSelL Wait Time: See EEPROM page 01U byte 143.
DataPathDeinit Max Duration DataPathInit Max Duration	DataPathDeinit_MaxDuration / DataPathInit_MaxDuration	—	—	—	DataPathDeinit_MaxDuration / DataPathInit_MaxDuration: See EEPROM page 01U byte 144.
ModulePwrDn Max Duration ModulePwrUp Max Duration	ModulePwrDn_MaxDuration / ModulePwrUp_MaxDuration	—	—	—	ModulePwrDn_MaxDuration / ModulePwrUp_MaxDuration See EEPROM page 01U byte 167.
RX Squelch[e] Assert Time	ton_Rxsq	—	15	ms	Time from loss of RX input signal until the squelched output condition is reached.
RX Squelch[e] Deassert Time	toff_Rxsq	—	15	ms	Time from resumption of RX input signal until the normal RX output condition is reached.
TX Squelch[e] Assert Time	ton_Txsq	—	400	ms	Time from loss of TX input signal until the squelched output condition is reached.
TX Squelch[e] Deassert Time	toff_Txsq	—	400	ms	Time from resumption of TX input signal until the nominal TX output condition is reached.
TX Disable Assert Time[c]	ton_txdis	—	100	ms	Time from TX Disable bit set (value = 1b)[f] until the optical output falls below 10% of nominal.
TX Disable Deassert Time[c]	toff_txdis	—	400	ms	Time from TX Disable bit cleared (value = 0b)[f] until the optical output rises above 90% of nominal.
RX Output Disable Assert Time	ton_rxdis	—	100	ms	Time from RX Output Disable bit set (value = 1b)[f] until the RX output falls below 10% of nominal.
RX Output Disable Deassert Time	toff_rxdis	—	100	ms	Time from RX Output Disable bit cleared (value = 0b)[f] until RX output rises above 90% of nominal

a. Power-on is defined as the instant when supply voltage reach and remain at or above the minimum level specified in Table 6 of the QSFP-DD Hardware specification.

b. Measured from the rising edge of SDA in the stop bit of the read transaction.

c. RX LOS and TX Disable assert/deassert optional fast modes are not implemented.

d. Measured from the rising edge of SDA in the stop bit of the write transaction.

e. TX/RX Squelch disable is not implemented.

f. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.

Low-Speed Pin Electrical Specifications

Parameter	Symbol	Min.	Max.	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max) = 3.0 mA
	VOH	V_{CC} – 0.5	V_{CC} + 0.3	V	—
SCL and SDA	VIL	–0.3	V_{CC} × 0.3	V	—
	VIH	V_{CC} × 0.7	V_{CC} + 0.5	V	—
LPMode, ResetL and ModSelL	VIL	–0.3	0.8	V	—
	VIH	2	V_{CC} + 0.3	V	—
	|Iin|	—	360	uA	0V < Vin < V_{CC}
IntL	VOL	0	0.4	V	IOL = 2.0 mA
	VOH	V_{CC} – 0.5	V_{CC} + 0.3	V	10 kΩ pull-up to host V_{CC}
ModPrsL	VOL	0	0.4	V	IOL = 2.0 mA
	VOH	—	—	—	ModPrsL implemented as a short-circuit to GND on the module
TWS Interface Clock Rate	—	—	400	kHz	—

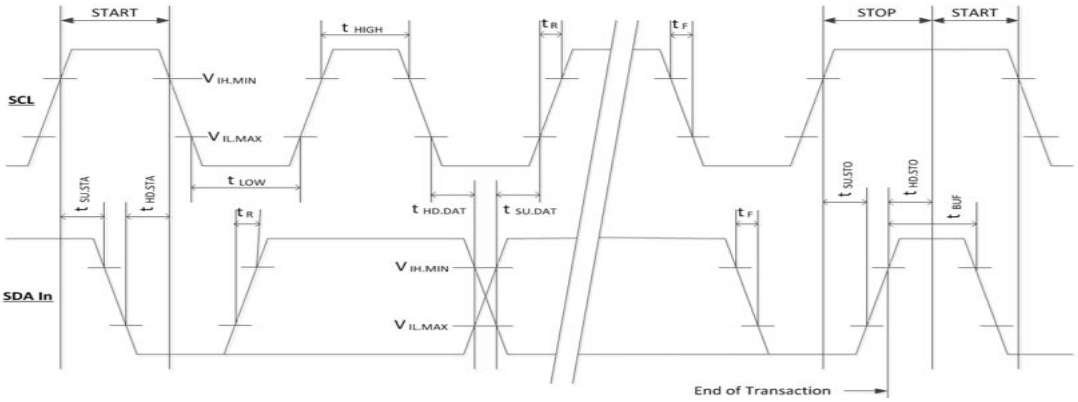
Management Interface Timing Parameters

The following characteristics are defined over the recommended operating conditions unless otherwise noted. Per QSFP-DD Hardware specification. Fast Mode Plus (1 MHz) is not available for the AFCT-91DRDSZ.

Parameter	Symbol	Fast Mode (400 kHz)		Unit	Condition
		Min.	Max.		
Clock Frequency	fSCL	0	400	kHz	—
Clock Pulse Width Low	tLOW	1.3	—	µs	—
Clock Pulse Width High	tHIGH	0.6	—	µs	—
Time Bus Free Before New Transmission Can Start	tBUF	20	—	µs	Between STOP and START and between ACK and ReStart.
START Hold Time	tHD.STA	0.6	—	µs	The delay required between SDA becoming low and SCL starting to go low in a START.
START Setup Time	tSU.STA	0.6	—	µs	The delay required between SCL becoming high and SDA starting to go low in a START.
Data In Hold Time	tHD.DAT	0	—	µs	—
Data In Setup Time	tSU.DAT	0.1	—	µs	—
Input Rise Time	tR	—	300	ns	From (VIL,MAX = 0.3 × V_{CC}) to (VIH,MIN = 0.7*V_{CC})
Input Fall Time	tF	—	300	ns	From (VIH,MAX = 0.7 × V_{CC}) to (VIL,MIN = 0.3 × V_{CC})
STOP Setup Time	tSU.STO	0.6	—	µs	—
STOP Hold Time	tHD.STO	0.6	—	µs	—
Aborted Sequence - Bus Release	Deselect_Abort	2	—	ms	Delay from a host deasserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA.
ModSelL Setup Time[a]	tSU.ModSelL	2	—	ms	ModSelL Setup Time is the setup time on the select line before the start of a host-initiated serial bus sequence.
ModSelL Hold Time[a]	tHD.ModSelL	2	—	ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of the module select status.
Serial Interface Clock Holdoff Clock Stretching	T_clock_hold	—	500	µs	Maximum time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation.
Complete Single or Sequential Write to Non-Volatile Registers	tWR	—	80	ms	Complete write of up to 8 bytes.
Endurance (Write Cycles)	—	50K	—	cycles	Module case temperature = 70°C.

a. When the host has determined that nodule is QSFP-DD, the management registers can be read to determine alternate supported ModSelL setup and hold times.

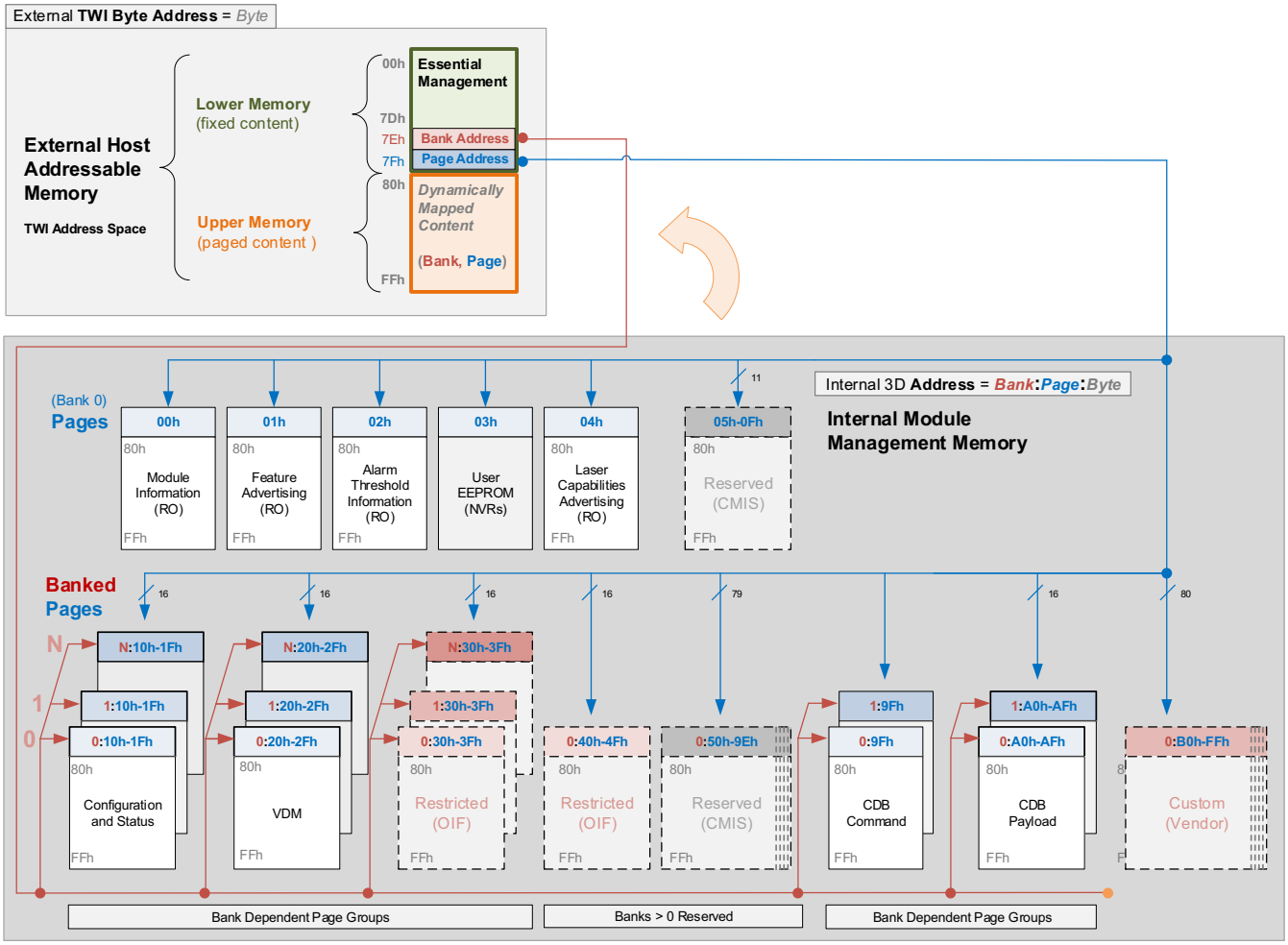
Figure 10: QSFP-DD Management Interface Timing Diagram



Memory Map

The memory is structured as a single address, multiple page approach. The 7-bit device address on the two-wire interface is 1010000b. The structure of the memory is shown in the following figure. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, for example, Interrupt Flags and Monitors. Less time critical entries, for example, serial ID information and threshold settings, are available with the Page Select function. For a more detailed description of the QSFP-DD memory map, refer to the *QSFP-DD MSA and CMIS* (Common Management Interface Specification).

Figure 11: QSFP-DD CMIS Module Memory Map (Conceptual View per CMIS 5.0)



Transmitter Input Equalization, Staged Control Sets, Tx Controls

Staged Set 0 Page 10h Bytes 156 to 159 and Staged Set 1 Page 10h Bytes 191 to 194

The module transmitter input equalization is adaptive, with no manual setting capability. From Table 6-6 of the *Common Management Interface Specification for 8X/16X Pluggable Transceivers*.

Code Value	Bit Pattern	Transmitter Input Equalization Codes	
		Input Equalization	Unit
13 to 15	—	Custom	dB
12	1100	12	dB
11	1011	11	dB
10	1010	10	dB
9	1001	9	dB
8	1000	8	dB
7	0111	7	dB
6	0110	6	dB
5	0101	5	dB
4	0100	4	dB
3	0011	3	dB
2	0010	2	dB
1	0001	1	dB
0	0000	No Equalization	—

Receiver Output Equalization, Staged Control Sets, Rx Controls

Staged Set 0 Page 10h Bytes 162 to 169 and Staged Set 1 Page 10h Bytes 197 to 204

From Table 6-7 of the C*ommon Management Interface Specification for 8X/16X Pluggable Transceivers*.

Code Value	Bit Pattern	Receiver Output Equalization Codes		
		Post-Cursor Equalization	Pre-Cursor Equalization	Unit
11 to 15	1011 to 111	Custom	Custom	dB
8 to 10	1000 to 1010	Reserved	Reserved	dB
7	0111	7	3.5	dB
6	0110	6	3.0	dB
5	0101	5	2.5	dB
4	0100	4	2.0	dB
3	0011	3	1.5	dB
2	0010	2	1.0	dB
1	0001	1	0.5	dB
0	0000	No Equalization	No Equalization	—

Receiver Output Amplitude, Staged Control Sets, Rx Controls

Staged Set 0 Page 10h Bytes 170 to 173 and Staged Set 1 Page 10h Bytes 205 to 208

From Table 6-8 of the *Common Management Interface Specification for 8X/16X Pluggable Transceivers*.

Code Value	Bit Pattern	Receiver Output Amplitude, No Output Equalization	
		Nominal	Unit
15	1111	Custom	mV (peak-to-peak)
4 to 14	0100 to 1110	Reserved	mV (peak-to-peak)
3	0011	600 to 1200	mV (peak-to-peak)
2	0010	400 to 800	mV (peak-to-peak)
1	0001	300 to 600	mV (peak-to-peak)
0	0000	100 to 400	mV (peak-to-peak)