AFCT-91DRDDZ

QSFP-DD Pluggable, Fiber-Optics Module
400GBASE-DR4, 500m SMF Ethernet Applications
8x50Gbps Electrical, 4x100Gbps Optical
MPO Connector

Preliminary Data Sheet

September 4, 2019

Description

The Avago AFCT-91DRDDZ is an Eight-Channel electrical, Four-Channel optical, Pluggable, Single Mode, Fiber-Optic QSFP-DD transceiver for 400 Gigabit Ethernet Applications. This high performance transceiver module is intended for short-range SMF data communication and interconnect applications. It converts eight host electrical data lanes in each direction at 50Gbps into four optical lanes at 100Gbps giving an aggregated bandwidth of 400Gbps, using four lasers in a parallel SMF DR4 configuration. It allows communication up to 500m over a 4+4 MPO connectored Single Mode optical fiber cable. The pull tab facilitates insertion and extraction of these transceivers in high density configurations. Each electrical lane operates at 26.5626 GBd / 53.125 Gbps (PAM4 encoded) and conforms to the IEEE 400GAUI-8 interface with host KP FEC.

These modules are designed to operate over single mode fiber systems using 1310nm lasers. The electrical interface uses a 76 contact QSFP-DD edge type connector. The optical interface uses a conventional 4+4 MPO SMF connector. This module incorporates FIT Optical Interconnect Technology proven integrated circuit and EML laser technology to provide reliable long life, high performance, and consistent service.

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Part Number Ordering Options

400 Gigabit Ethernet Transceiver	AFCT-91DRDDZ

Host Compliance Board	AFCT-91HCB
Module Compliance Board	AFCT-91MCB

*Includes GUI and User Guide
**Includes GUI, User Guide, I2C controller and Power Supply Cable

Features

- Compliant to IEEE 400GbE electrical specification 802.3bs (Annex 120E 400GAUI-8) with Host FEC
- Compliant to IEEE 400GBASE-DR4 optical specification 802.3bs Clause 124
- 400G Link Distances up to 500m SMF
- QSFP-DD MSA Specification Compliant
- Class 1 Eye Safety
- Pull Tab: Ease of Transceiver Insertion and Extraction
- 0ºC to 70ºC case temperature operating range
- Proven High Reliability Technology: Cooled EML transmitter and PIN detector
- Hot Pluggable QSFP-DD Transceiver for Ease of Installation and Servicing
- Two Wire Serial (TWS) interface with Digital Monitoring and Maskable Interrupts for Expanded Functionality

Applications

- 400 Gigabit Ethernet interconnects
- Datacom/Telecom switch & router connections
- Data aggregation and backplane applications
- Proprietary protocol and density applications

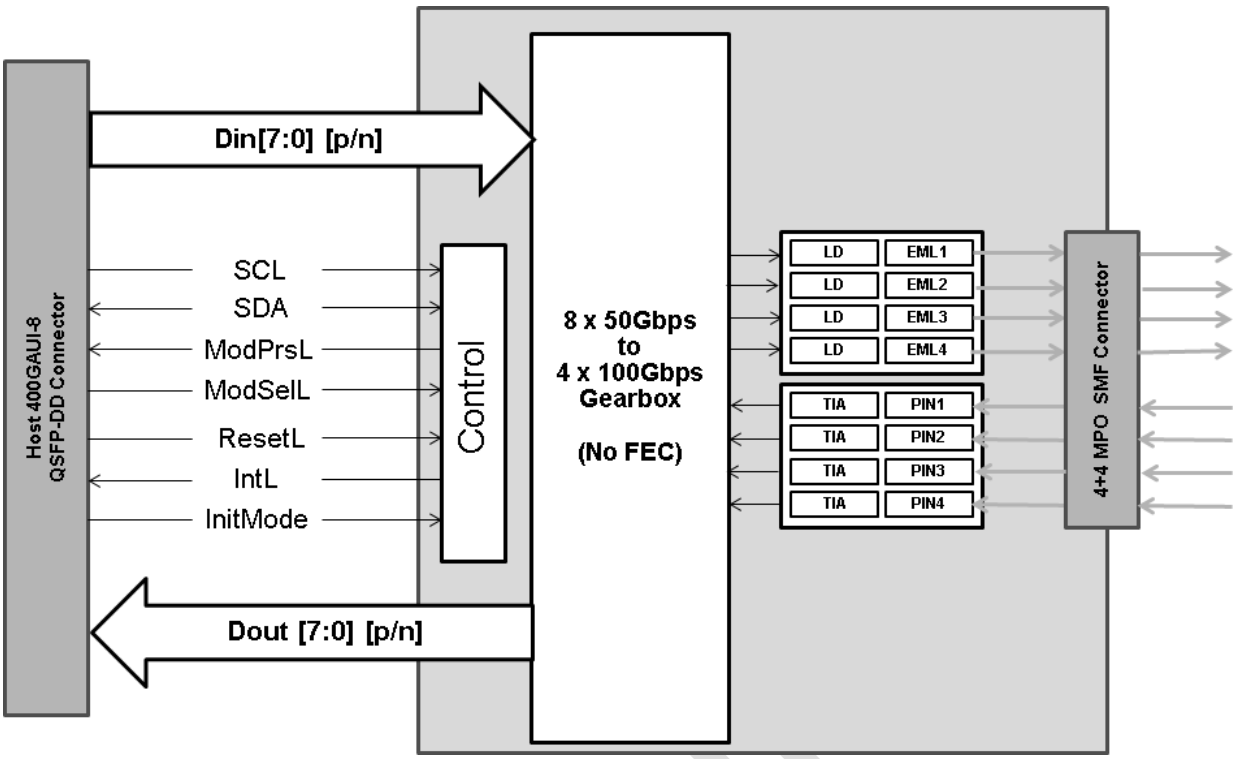


Figure 1: Transceiver Block Diagram

Transmitter

The optical transmitter portion of the transceiver (see Figure 1) incorporates an 8x50Gbps 400GAUI-8 Annex 120E compliant electrical input with Equalization (EQ) block, integrated electrical multiplexer, laser driver, diagnostic monitors, control and bias for the quad EML single mode laser source. The transmitter is designed for EN 60825 and CDRH Class 1 eye safety compliance. The Tx Input Buffer provides 400GAUI-8 compliant differential inputs presenting a nominal differential input impedance of 100 Ohms. AC coupling capacitors are located inside the QSFP-DD module and are not required on the host board**.** For module control and interrogation, the control interface (LVTTL compatible) incorporates a Two Wire Serial (TWS) interface of clock and data signals.

Receiver

The optical receiver portion of the transceiver (see Figure 1) incorporates quad PIN photodiodes, trans-impedance amplifiers (TIA), integrated de-multiplexer and 8x50G 400GAUI-8 Annex 120E compliant electrical output blocks.

The Rx Output Buffer provides 400GAUI-8 compliant differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 Ohms to AC ground and 100 Ohms differentially that should be differentially terminated with 100 Ohms. AC coupling capacitors are located inside the QSFP-DD module and are not required on the host board.

The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through TWS interface. To reduce the need for polling, a hardware interrupt signal INTL is provided to inform hosts of an assertion of LOS or Tx_FAULT.

High Speed Electrical Signal Interface

Figure 2 shows the interface between an ASIC/SerDes and the QSFP-DD module. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to module 400GAUI-8 specifications per IEEE 802.3 Annex 120E.

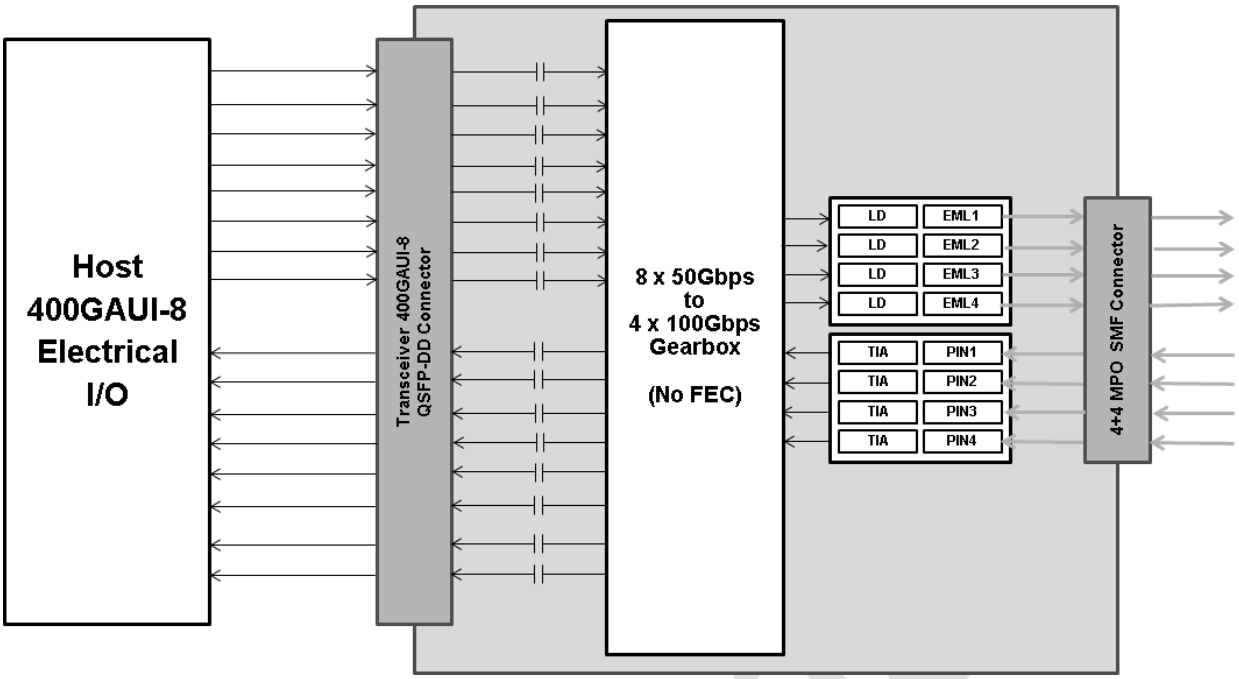


Figure 2: Application Reference Diagram

Control Signal Interface

The module has the following low speed signals for control and status: ModSelL, InitMode, ResetL, ModPrsL, IntL. In addition, there is an industry standard two wire serial interface scaled for 3.3 volt LVTTL. It is implemented as a slave device. Signal and timing characteristics are further defined in the Control Characteristics and Control Interface & Memory Map sections.

The registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Regulatory & Compliance Issues

Various standard and regulations apply to the modules. These include eye-safety, EMC, ESD and RoHS. See the Regulatory Section for details regarding these and component recognition. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

Package Outline

The module is designed to meet the package outline defined in the QSFP-DD MSA specification. See the package outline for details.

Handling and Cleaning

The transceiver module can be damaged by exposure to current surges and over voltage events. Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Wave soldering, reflow soldering and/or aqueous wash process with the modules on board are not recommended. Normal handling precautions for electrostatic discharge sensitive devices should be observed.

Each module is supplied with an inserted port plug for protection of the optical ports. This plug should always be in place whenever a fiber cable is not inserted.

The optical connector includes recessed elements that are exposed whenever a cable or port plug is not inserted. Prior to insertion of a fiber optic cable, it is recommended that the cable end be cleaned to avoid contamination from the cable plug. The port plug ensures the optics remains clean and no additional cleaning should be needed. In the event of contamination, standard MPO port cleaning methods may be used. Dry nitrogen or clean dry air at less than 20 psi can be used to dislodge the contamination. Liquids are not advised.

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Max	Units	Reference
Storage Temperature	Ts	-40	85	°C	
3.3 V Power Supply Voltage	Vcc	-0.5	3.6	V	
Data Input Voltage – Single Ended		-0.5	Vcc+0.5	V	
Data Input Voltage – Differential	$\lvert V_{DIp} - V_{DIn} \rvert$		0.8	V	[1]
Control Input Voltage	Vi	-0.5	Vcc+0.5, 3.6	V	
Control Output Current	Io	-20	20	mA	
Relative Humidity	RH	5	95	%	

Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Case Temperature	Tc	0		70	°C	[2]
3.3 V Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Electrical Signal Rate per Channel (PAM encoded)			26.5625		GBd	[3]
Optical Signal Rate per Channel (PAM encoded)			53.125		GBd	[4]
Power Supply Noise				50	mVpp	[5]
Receiver Differential Data Output Load			100		Ohm	
Fiber Length (9um SMF)	2			2000	m	[6]

* Control signals, LVTTL (3.3 V) compatible

[1] This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600 mV peak to peak differential

[2] The position of case temperature measurement is shown in Figure 7. Continuous operation at the maximum Recommended Operating Case Temperature should be avoided in order not to degrade reliability.

[3] 400GAUI-8 operation with Host generated FEC. The AFCT-91DRDDZ must receive pre-coded FEC signals from the host ASIC.

[4] 400G DR4 operation with Host generated FEC. The AFCT-91DRDDZ must receive pre-coded FEC signals from the host ASIC.

[5] Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 9 for recommended power supply filter.

[6] 9µm SMF (minimum). The maximum link distance is based on an allocation of 1dB of attenuation and 3 dB total connection and splice loss. The loss of a single connection shall not exceed 0.5 dB.

General Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Symbols	Min	Typ	Max	Units	Reference
Transceiver Power Consumption			12	14	W	Power Class 7
Transceiver Power Supply Current, Total			3636	4470	mA	
Transceiver Power Supply Current, VccTx + VccTx1				TBD	mA	
Transceiver Power Supply Current VccRx + VccRx1				TBD	mA	
Transceiver Power Supply Current Vcc1 + Vcc2				TBD	mA	
AC coupling capacitors (Internal)			0.1		uF	

* For control signal timing including ModSelL, InitMode, ResetL, ModPrsL, IntL, SCL and SDA see Control Interface Section.

High Speed Electrical Input Characteristics

From 400GAUI-8, 802.3 Annex 120E

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Signaling Rate, Per Lane (PAM4 encoded)	TP1		26.5625		GBd	+/- 100 ppm
Differential pk-pk Input Voltage Tolerance	TP1a	900			mV	
Differential Input Return Loss. min	TP1		Eq 83E-5		dB	802.3bm
Differential to common mode input return loss (min)	TP1		Eq 83E-6		dB	802.3bm
Differential Termination Mismatch	TP1			10	%	
Module stressed input test	TP1a		120E.3.4.1			802.3bs
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode output voltage	TP1	-0.35		2.85	V	[1]

Parameter	Value	Units	Notes/Conditions
Module stressed input test			[2]
Eye width	0.22	UI	
Applied pk-pk sinusoidal jitter	Table 120E-6		802.3bs
Eye height	32	mV	

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Electrical Input LOS Assert Threshold, Differential Peak-to-Peak Voltage Swing	ΔVdi pp los	10			mVpp	
LOS Hysteresis		0.5		4	dB	[3]

[1] DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

[2] Module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1

[3] LOS Hysteresis is defined as 20*Log(LOS De-assert Level / LOS Assert Level).

Module Input Electrical Characteristics

Reference Points

Test Point	Description
TP0	Host ASIC transmitter output at ASIC package pin on a DUT board
TP1	Input to module compliance board through mated module compliance board and module connector. Used to test module input
TP1A	Host ASIC transmitter output across the Host Board and Host Edge Card connector at the output of the host compliance board
TP2	Optical transmitter output as measured at the end of a 2-5m patch cord mated to the optical module
TP3	Optical test point as measured at the end of an optical fiber cable; closest test point to the presumed optical receiver input.
TP4	Module output through mated module and host edge card connector through module compliance board
TP4A	Input to host compliance board through mated host compliance board and host edge card connector. Used to test host input
TP5	Input to host ASIC

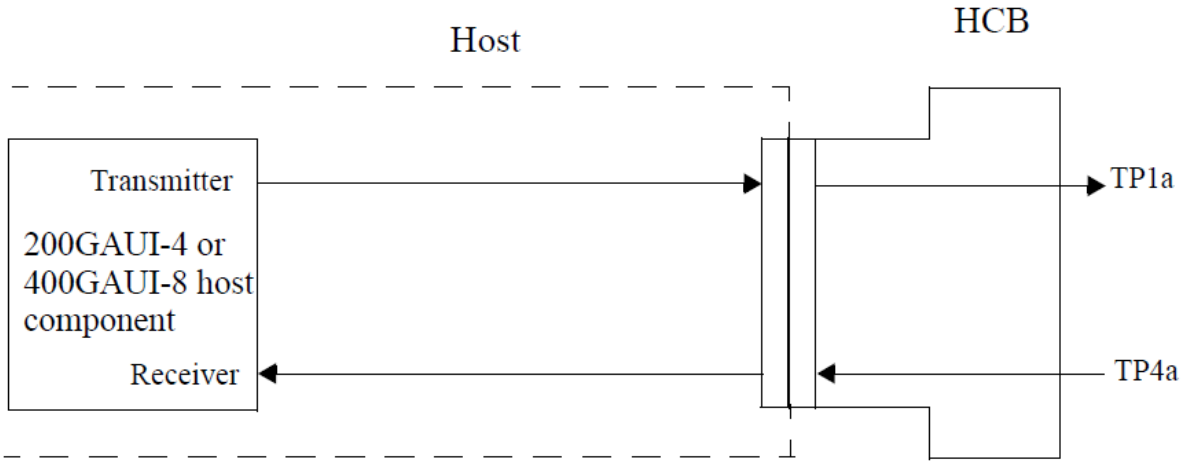


Figure 120E–5—Host 200GAUI-4 or 400GAUI-8 C2M compliance points

Figure 3: IEEE 802.3 400GAUI-8 compliance points TP1a, TP4a

The reference receiver is used to measure eye width and eye height. The reference receiver includes a selectable continuous time linear equalizer (CTLE) which is described by Equation (802.3bs 120E–2) with coefficients (802.3bs Table 120E–2).

$$H(f) \quad \frac{\qquad}{(j \qquad)(j \qquad)} \quad \frac{\qquad}{\qquad}$$

Where

H(f)	is the CTLE transfer function, f is the frequency in GHz
G	is the CTLE gain
P_1, P_2	are the CTLE poles in Grad/s
Z_1	is the CTLE zero in Grad/s
P_{LF}	is the low frequency CTLE pole in Grad/s
Z_{LF}	is the low frequency CTLE zero in Grad/2
j	is the square root of -1
f	is the frequency in GHz

Reference CTLE coefficients (Table 120E-2 IEEE 802.3)

26.5625GBd						
Peaking (dB)	**G**	**$P_1/2\pi$ (GHz)**	**$P_2/2\pi$ (GHz)**	**$Z_1/2\pi$ (GHz)**	**$P_{LF}/2\pi$ (GHz)**	**$Z_{LF}/2\pi$ (GHz)**
1	0.891251	26.5625	14.1	9.463748	1.2	1.2
1.5	0.841395	26.5625	14.1	9.248465	1.2	1.15
2	0.794328	26.5625	14.1	9.069645	1.2	1.1
2.5	0.749894	26.5625	14.1	8.640319	1.2	1.075
3	0.707946	26.5625	14.1	8.255665	1.2	1.05
3.5	0.668344	26.5625	14.1	7.906766	1.2	1.025
4	0.630957	26.5625	14.1	7.58765	1.2	1
4.5	0.595662	26.5625	14.1	7.076858	1.2	1
5	0.562341	26.5625	14.1	6.614781	1.2	1
5.5	0.530884	26.5625	14.1	6.193091	1.2	1
6	0.501187	26.5625	14.1	5.805801	1.2	1
6.5	0.473151	26.5625	14.1	5.448395	1.2	1
7	0.446684	26.5625	14.1	5.117337	1.2	1
7.5	0.421697	26.5625	14.1	4.809777	1.]2	1
8	0.398107	26.5625	14.1	4.523367	1.2	1
8.5	0.375837	26.5625	14.1	4.256129	1.2	1
9	0.354813	26.5625	14.1	4.006377	1.2	1

High Speed Electrical Output Characteristics

From 400GAUI-8, 802.3 Annex 120E

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Signaling Rate, Per Lane PAM4 Encoded	TP4		26.5625		GBd	+/- 100 ppm
AC common-mode output voltage (max, RMS)	TP4			17.5	mV, rms	
Differential Output Voltage	TP4			900	mV	
Near-end ESMW (Eye symmetry mask width), Differential	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end ESMW (Eye symmetry mask width), Differential	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end pre-cursor ratio	TP4			2.5	%	
Differential Output Return Loss, min	TP4		Eq 83E-2		dB	802.3bm
Common to differential mode conversion return loss (min)	TP4		Eq 83E-3		dB	802.3bm
Differential termination mismatch	TP4			10	%	
Transition Time (20% to 80%)	TP4	9.5			ps	
DC common mode voltage	TP4	-0.35		2.85	V	[1]

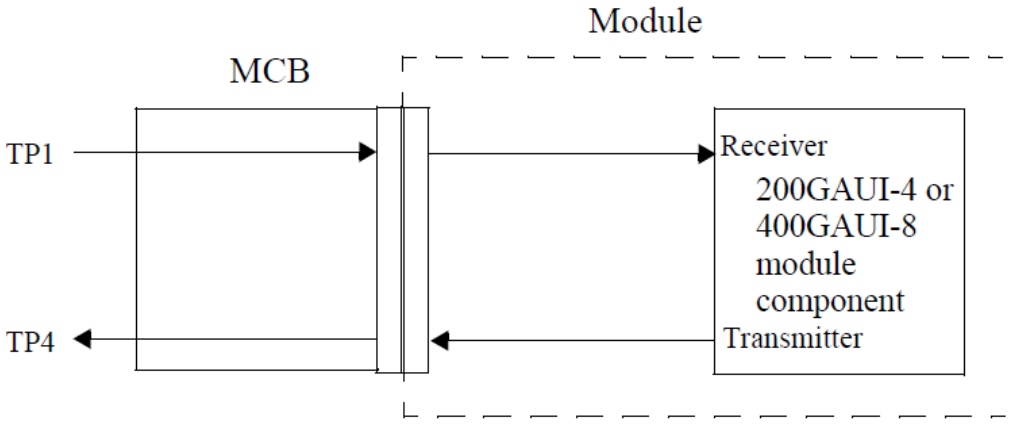


Figure 120E–6—Module 200GAUI-4 or 400GAUI-8 C2M compliance points

Figure 4: IEEE 802.3 400GAUI-8 compliance points TP1, TP4

[1] Capacitively coupled module output is compatible with DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

High Speed Optical Transmitter Characteristics

From 400GBASE-DR4, 802.3 Clause 124 (Revision 3.4)

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Signaling Rate, Per Lane PAM4 Encoded			53.125			+/- 100ppm
Center wavelength	TP2	1304.5	1310	1317.5	nm	
Side Mode Suppression Ration (SMSR)	TP2	30			dB	
Average launch power, each lane	TP2	-2.9		+4.0	dBm	Note 1
Outer Optical Modulation Amplitude (OMA) each lane	TP2	-0.8		+4.2	dBm	Note 2
Launched Power in OMA – TDECQ, each lane	TP2	-2.2			dBm	
Transmitter & Dispersion Eye Closure PAM4 TDECQ, each lane	TP2			3.4	dB	
TDECQ - $10*\log_{10}(C_{eq})$, each lane	TP2			3.4	dB	Note 3
Extinction ratio, each lane	TP2	3.5			dB	
$RIN_{21.4}OMA$	TP2			-136	dB/Hz	
Optical Return Loss Tolerance	TP2			21.4	dB	
Transmitter Reflectance	TP2			-26	dB	Note 4
Average launch power of OFF transmitter, each lane	TP2			-15	dBm	

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4dB, the OMA_{outer}(min) must exceed these values.
3. Ceq is a coefficient defined in IEEE 802.3-2018 clause 121.8.5.8 which accounts for reference equalizer noise enhancement.
4. Transmitter reflectance is defined looking into the transmitter.

High Speed Optical Receiver Characteristics

From 400GBASE-DR4, 802.3 Clause 124 (Revision 3.4)

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Signaling Rate, Per Lane PAM4 Encoded			53.125			+/- 100ppm
Center wavelength	TP3	1304.5	1310	1317.5	nm	
Damage Threshold	TP3	+5.0			dBm	Note 1
Receiver Average Power, each lane	TP3	-5.9		+4.0	dBm	Note 2
Receiver Optical Modulation Amplitude (OMA_{outer}), each lane	TP3	-4.4		+4.2	dBm	Note 3
Receiver Reflectance	TP3			-26	dB	
Receiver Stressed Sensitivity OMA_{outer}, each lane	TP3			-1.9	dBm	Note 4
Conditions of stressed receiver sensitivity	TP3					Note 5
Stressed Eye Closure (SECQ), each lane	TP3		3.4		dB	
SECQ – $10\log_{10}(C_{eq})$, lane under test	TP3			3.4	dB	Note 6
OMA_{outer} of each aggressor lane	TP3		4.2		dBm	

Parameter	Test Point*	Min	Typ	Max	Units	Notes/Conditions
LOS Assert - AVG	TP3	-15			dBm	
LOS De-Assert - OMA	TP3			TBD	dBm	
LOS Hysteresis	TP3	0.5			dB	

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
2. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Receiver sensitivity (OMA_{outer}), each lane is informative and is defined for a transmitter with SECQ of 0.9dB.
4. Measured with conformance test signal at TP3 (802.3 Clause 124, Section 124.8.9) for BER specified in 124.1.1.
5. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
6. C_{eq} is a coefficient defined in IEEE 802.3-2018 clause 121.8.5.8 which accounts for reference equalizer noise enhancement.

Regulatory Compliance

The AFCT-91DRDDZ complies with all applicable laws and regulations as detailed in the Regulatory Compliance Table. Certification level is dependent on the overall configuration of the host equipment. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

The AFCT-91DRDDZ is compatible with ESD levels found in typical manufacturing and operating environments. as described in the Regulatory Compliance Table. In the normal handling and operation of optical transceivers, ESD is of concern in two circumstances.

The first case is during handling of the transceiver prior to insertion into a QSFP-DD compliant cage. To protect the device, it is important to use normal ESD handling precautions. These include use of grounded wrist straps, workbenches and floor wherever a transceiver is handled.

The second case to consider is static discharges to the exterior of the host equipment chassis after installation. If the optical interface is exposed to the exterior of the host equipment cabinet, the transceiver may be subject to system level ESD requirements.

Electromagnetic Interference (EMI)

Equipment incorporating multi-gigabit transceivers is typically subject to regulation by the FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. The AFCT-91DRDDZ compliance to these standards is detailed in the Regulatory Compliance Table. The metal housing and shielded design of the AFCT-91DRDDZ minimizes the EMI challenge facing the equipment designer.

Flammability

The AFCT-91DRDDZ optical transceiver is made of metal and high strength, heat resistant, chemical resistant and UL94V-0 flame retardant plastic.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	EN61000-4-2, Criterion B	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing TÜV Rheinland Product Safety / BAUART GEPRÜFT / TYPE APPROVED	Complies with 21 CFR Subchapter J per Paragraphs 1040.10 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019 (IEC) EN 62368-1:2014 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number: 9521220-234 TUV File: R 72191051 CB File: US-TUVR-011594-A1
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E484615
RoHS Compliance		Less than 1000 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls (PPB) and polybrominated biphenyl ethers (PBDE).

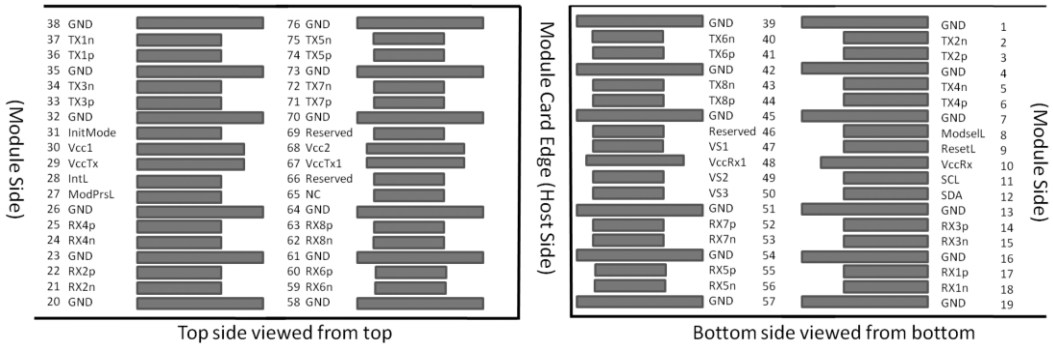


Figure 5: QSFP-DD module pin layout

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	3
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	3
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	3
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select, When held low by the host, the module responds to 2-wire serial communication commands.	3B	
9	LVTTL-I	ResetL	Module Reset, The ResetL signal is pulled up to Vcc in the QSFP-DD module.	3B	
10		Vcc Rx	+3.3V Power supply receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock, Requires pull-up resistor to 3.3V on the host board.	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data, Requires pull-up resistor to 3.3V on the host board.	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	3
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	3
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	3
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	3
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	3
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	3
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	3
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	3
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present, Requires pull-up resistor to 3.3V on the host board. Module Present is pulled low in the module.	3B	
28	LVTTL-O	IntL	Interrupt, the IntL signal is an open collector output and must be pulled to host supply voltage (3.3V) on the host board.	3B	
29		Vcc Tx	+3.3V Power Supply	2B	2
30		Vcc1	+3.3V Power Supply	2B	2
31	LVTTL-I	InitMode	Low Power Mode. InitMode is pulled up to Vcc in the module.	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	3
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	3
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	3
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	3
38		GND	Ground	1B	1

Pin	Logic	Symbol	Description	Plug Sequence	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	3
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	3
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	3
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	3
45		GND	Ground	1A	1
46		NC	No Connect	3A	
47		NC	No Connect	3A	
48		Vcc Rx1	+3.3V Power supply receiver	2A	2
49		NC	No Connect	3A	
50		NC	No Connect	3A	
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	3
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	3
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	3
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	3
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	3
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	3
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	3
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	3
64		GND	Ground	1A	1
65		NC	No Connect	3A	
66		NC	No Connect	3A	
67		Vcc Tx1	+3.3V Power Supply	2A	2
68		Vcc2	+3.3V Power Supply	2A	2
69		NC	No Connect	3A	
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	3
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	3
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	3
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	3
76		GND	Ground	1A	1

Note 1: GND is the symbol for signal supply (power) common for the QSFP-DD module. All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

Note 3: For all Tx and Rx High-Speed differential inputs/outputs, there are 0.1uF AC coupling capacitors are located inside the QSFP-DD module and are not required on the host board.

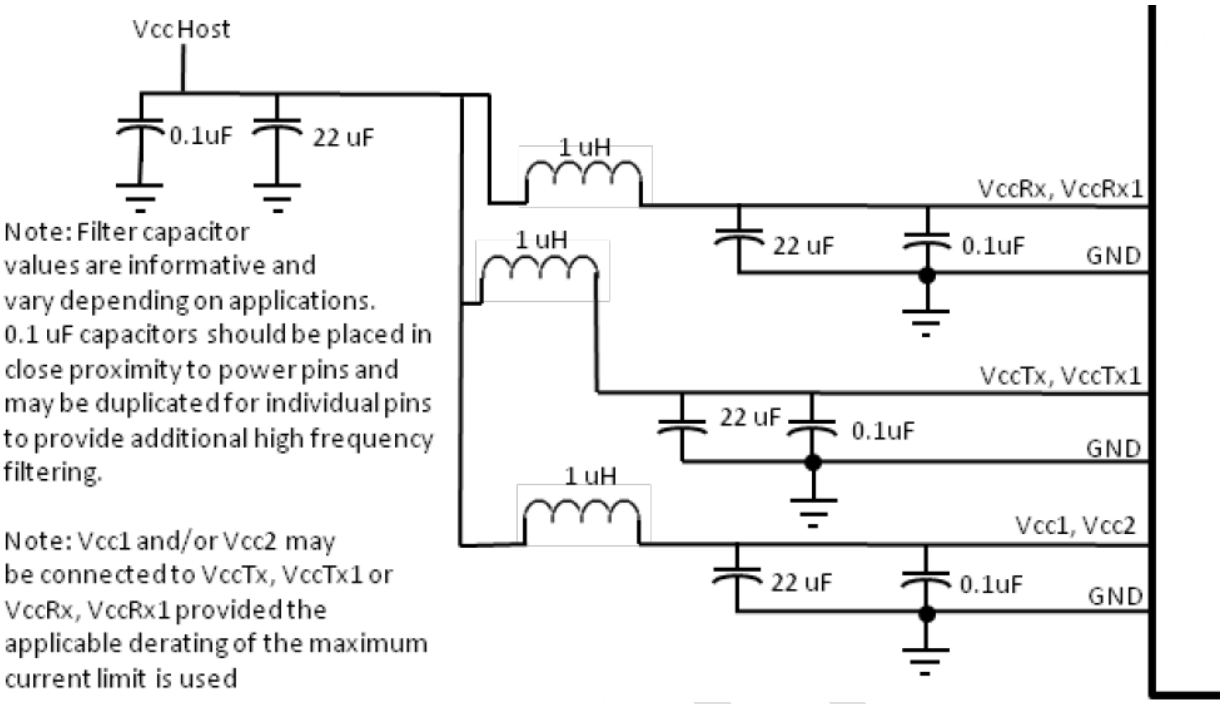


Figure 6: Recommended Power Supply Filter

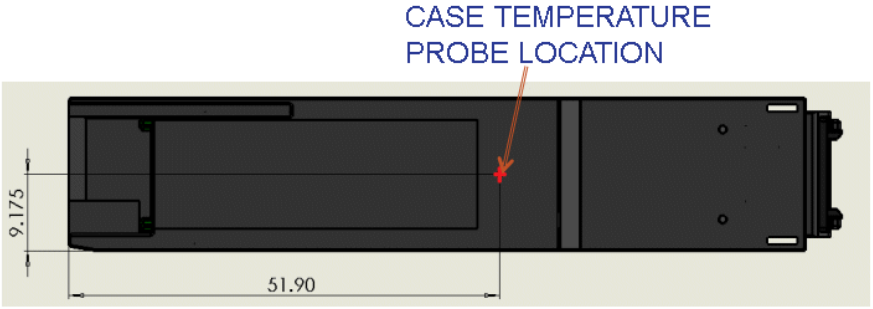


Figure 7: Case Temperature Measurement Point

Package Outline

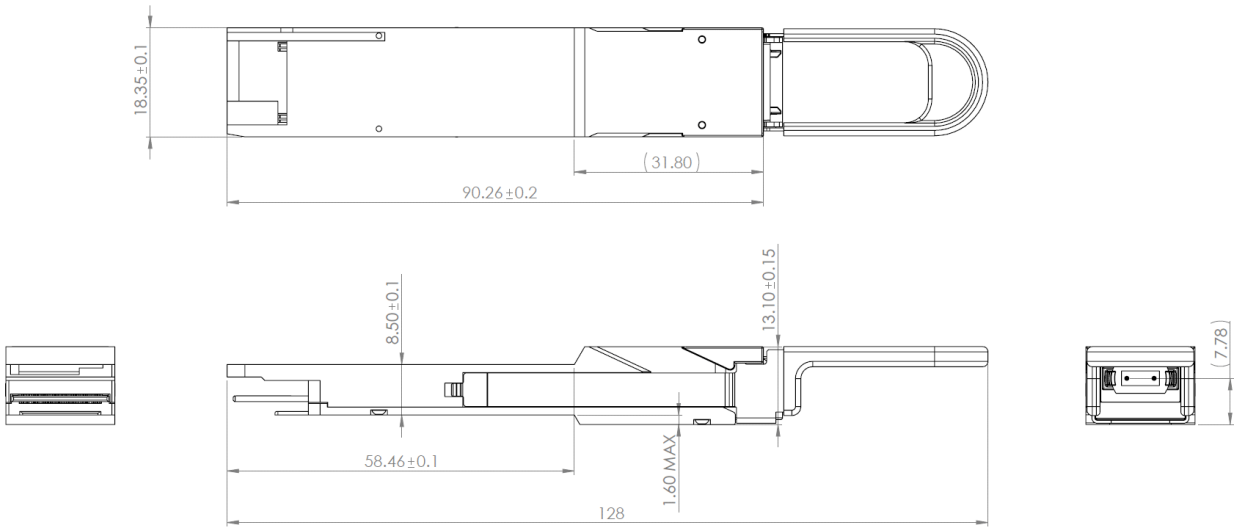
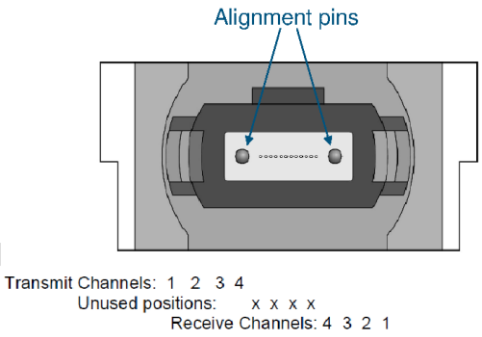


Figure 8: Mechanical Package Outline (All dimensions in mm)



The optical interface port is a male MPO connector as specified in IEC61754-7. Aligned key MTP/MPO patch cords should be used to ensure alignment of the signals between the modules. The aligned key patch cord is define in TIA-568.

Figure 9: Module Optical Interface (looking into the optical port)

Control Interface & Memory Map

The control interface combines dedicated signal lines for ModSelL, InitMode, ResetL, ModPrsL, IntL with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface. The TWS interface is implemented as a slave device and compatible with industry standard two-wire serial protocol. It is scaled for 3.3 volt LVTTL. Outputs are high-Z in the high state to support busing of these signals. Signal and timing characteristics are further defined in the Control I/O Characteristics section. For more details, see the QSFP-DD MSA and CMIS (Common Management Interface Specification).

ModSelL

The ModSelL is an input signal. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node is biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL

The ResetL signal is pulled up to Vcc in the QSFP-DD module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

InitMode

Low power mode. InitMode is pulled up to Vcc in the QSFP-DD module. The pin is a hardware control used to put modules into a low power mode when high. By using the InitMode pin and a combination of software control bits, the host controls how much power a module can dissipate.

ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL will be asserted "Low" when the transceiver is inserted into the host connector.

IntL

IntL is an output signal. When "Low", indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is an open collector output and must be pulled to host supply voltage on the host board.

The INTL pin is de-asserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see the QSFP-DD CMIS specification).

The user can read the present value of the various diagnostic monitors. Case module temperature, supply voltage, laser bias current for each channel and receiver input power (Pave) for each channel are reported. All monitor items are two-byte fields and to maintain coherency, the host must access these with single two-byte read sequences. For each monitored item, alarm and warning thresholds are established. If an item moves past a threshold, a flag is set, and, provided the item is not masked, IntL is asserted. A mask bit that can be set to prevent assertion of IntL for the individual item exists for every LOS, Tx fault and monitor flag. Entries in the mask fields are volatile.

Soft Status and Control
A number of soft status signals and controls are available in the AFCT-91DRDDZ transceiver memory and accessible through the TWS interface. Some soft status signals include receiver LOS, transmitter LOS, and diagnostic monitor alarms and warnings. Some soft controls include transmitter disable (Tx_Dis), receiver output disable (Rx_Dis), transmitter squelch disable (Tx_SqDis), receiver squelch disable (Rx_SqDis), and masking of status signal in triggering IntL. Most soft status signals and controls are per channel basis, but some are global. All soft control entries are volatile.

Transmitter LOS
The transmitter LOS status signal is on page 00h address 4 bits 0-7 for channels 1-8 respectively. Transmitter LOS is based on TP1 electrical input differential voltage and factory set LOS thresholds. This status register is latched and it is cleared on read.

Receiver LOS
The receiver LOS status signal is on page 00h address 3 bits 0-7 for channels 1-8 respectively. Receiver LOS is based on TP3 optical input modulation amplitude (OMA) and factory set LOS thresholds. This status register is latched and it is cleared on read.

Transmitter LOL
The transmitter loss of lock status signal is on page 00h address 6 bits 0-7 for channels 1-8 respectively. The loss of lock flag will assert if an enabled transceiver transmitter side CDR or gearbox is not locked to the host electrical input data signal. This status register is latched and it is cleared on read.

Receiver LOL
The receiver loss of lock status signal is on page 00h address 5 bits 0-7 for channels 1-8 respectively. The loss of lock flag will assert if an enabled transceiver receiver side electrical CDR or gearbox is not locked to the recovered optical input data signal. This status register is latched and it is cleared on read.

Transmitter Fault
The transmitter fault status signal is on page 00h address 7 bits 0-7 for channels 1-8 respectively. The transceiver transmitter fault condition will flag if the laser output power is too high – i.e. approaching eye safety levels. When fault is triggered, the corresponding transmitter channel optical output will be disabled. Module reset or toggling of soft transmitter disable (page 00h, address 84) can restore the transmitter channel function unless a fault condition persists. This status register is latched and it is cleared on read.

Transmitter Disable
The transmitter disable control is on page 00h address 84 bits 0-7 for channels 1-8 respectively. When each transceiver transmitter lane is disabled the optical power shall be less than -30 dBm. Because the eight 50G electrical lanes are multiplexed into four 100G optical lanes, logically paired for a composite 400G link, issuing a Tx Disable for any one lane in address 84 bits 0-7 will turn off all 100G Tx optical sources.

Receiver Disable
The receiver disable control is on page 00h address 90 bits 0-7 for channels 1-8 respectively. If the receiver output is disabled, the electrical output differential voltage swing shall be less than 50 mVpp.

Transmitter Squelch Disable
The transmitter squelch disable control is on page 00h address 85 bits 0-7 for channels 1-8 respectively. AFCT-91DRDDZ transceivers have transmitter output squelch function enabled as default. If any transmitter output is in the squelched state, the laser optical output power will be turned off.

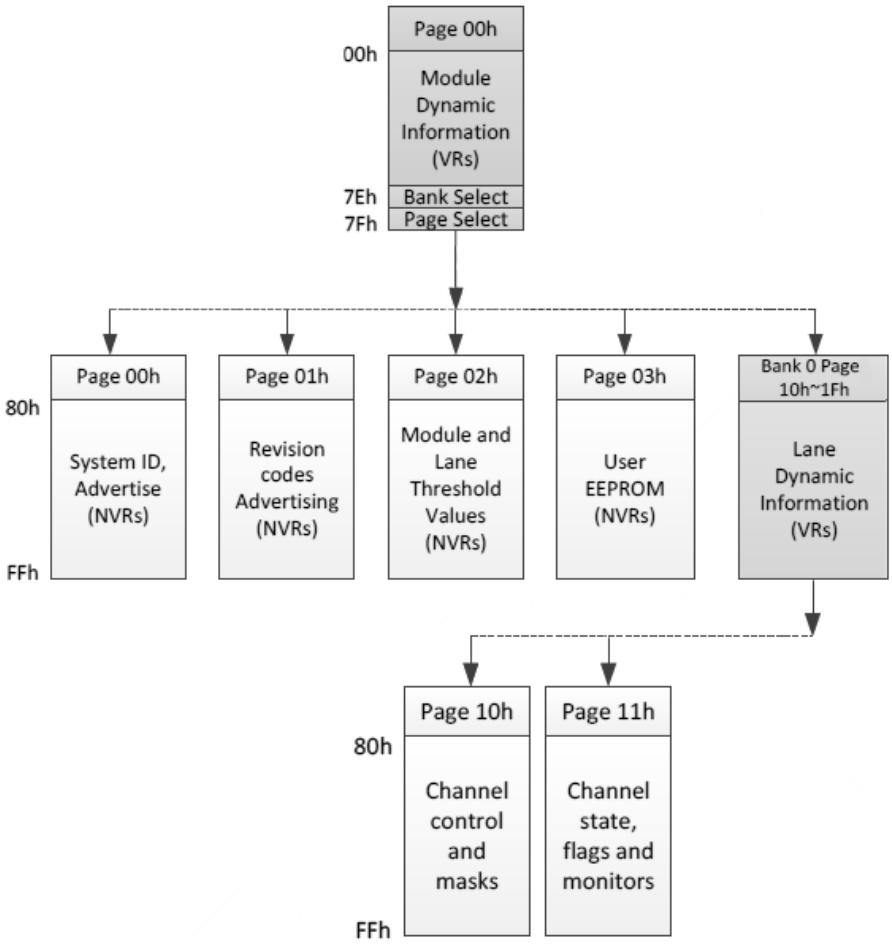
Receiver Squelch Disable
The receiver squelch disable control is on page 00h address 91 bits 0-7 for channels 1-8 respectively. AFCT-91DRDDZ transceivers have receiver output squelch function enabled as default. If the receiver output is in the squelched state, the electrical output differential voltage swing shall be less than 50 mVpp.

Low Speed Pin Electrical Specifications

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V	|Iin|<=125 uA for 0V<Vin,Vcc
	VIH	2	Vcc+0.3	V	
ModPrsL and IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	
Two Wire Serial (TWS) Interface Clock Rate			400	kHz	

Memory Map

The memory is structured as a single address, multiple page approach. The 7 bit device address on the two wire interface is 1010000b. The structure of the memory is shown below. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. For a more detailed description of the QSFP-DD memory map see the QSFP-DD MSA and CMIS (Common Management Interface Specification).



Simplified QSFP-DD CMIS Module Memory Map Architecture

Transmitter Input Equalization, Staged Control Sets, Tx Controls, Set 0 Page 10h Bytes 156-159

From Table 10 of *Common Management Interface Specification for 8X/16X Pluggable Transceivers*

Code Value	Code	Transmitter Input Equalization Codes	
		Input Equalization	Units
13-15		Custom	dB
12	1100	12	dB
11	1011	11	dB
10	1010	10	dB
9	1001	9	dB
8	1000	8	dB
7	0111	7	dB
6	0110	6	dB
5	0101	5	dB
4	0100	4	dB
3	0011	3	dB
2	0010	2	dB
1	0001	1	dB
0	0000	No Equalization	

Receiver Output Equalization, Staged Control Sets, Rx Controls, Set 0 Page 10h Bytes 162-169

From Table 11 of *Common Management Interface Specification for 8X/16X Pluggable Transceivers*

Code Value	Code	Receiver Output Equalization Codes		
		Post-Cursor Equalization	Pre-Cursor Equalization	Units
11-15	1011-111	Custom	Custom	dB
8-10	1000-1010	Reserved	Reserved	dB
7	0111	7	3.5	dB
6	0110	6	3.0	dB
5	0101	5	2.5	dB
4	0100	4	2.0	dB
3	0011	3	1.5	dB
2	0010	2	1.0	dB
1	0001	1	0.5	dB
0	0000	No Equalization	No Equalization	

Receiver Output Amplitude, Staged Control Sets, Rx Controls, Set 0 Page 10h Bytes 170-173

From Table 12 of *Common Management Interface Specification for 8X/16X Pluggable Transceivers*

Code Value	Code	Receiver Output Amplitude No Output Equalization	
		Nominal	Units
15	1111	Custom	mV (p-p)
4-14	0100-1110	Reserved	mV (p-p)
3	0011	600 - 1200	mV (p-p)
2	0010	400 – 800	mV (p-p)
1	0001	300 – 600	mV (p-p)
0	0000	100 – 400	mV (p-p)

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