AFBR-S50-LP

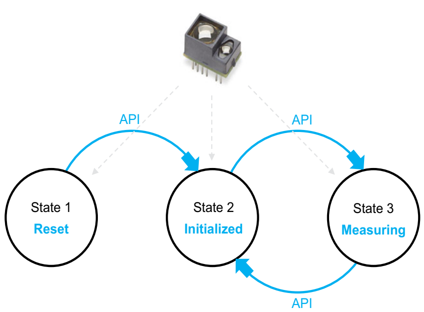
Low-Power and Battery Applications

Overview

Mobile or other locally independent sensing systems are battery powered by definition and therefore require minimum power consumption. Because the AFBR-S50 time-of-flight (ToF) sensor family does not have a native sleep mode, this application note describes a special implementation in hardware and software to minimize current consumption over time. The following figure displays the sensor states with their typical current consumption.

Figure 1: Default Current States

State	Typical Current Consumption
1	1.5 mA
2	20 mA
3	33 mA

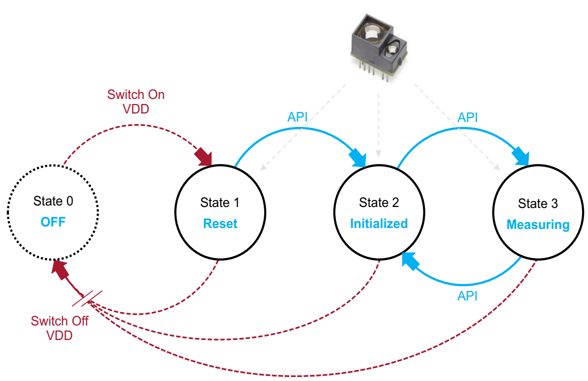


In a standard use case, the AFBR-S50 API allows switching between states 2 and 3, which results in an average current consumption of about 26.5 mA considering a 50% duty cycle. Alternating between these two states can be carried out either by manually triggering single measurements or by invoking periodic start and stop measurements.

To further optimize the sequence and significantly reduce the current consumption, Broadcom suggests completely switching off VDD/VDDL (+5V power supply) during idle times and switching it on again when a distance measurement is required. The consequence of alternating between states 0 and 3 with a low duty cycle, as shown in the following figure, can yield current consumption in the µA order of magnitude.

Figure 2: Optimized State Sequence for Low-Power Consumption

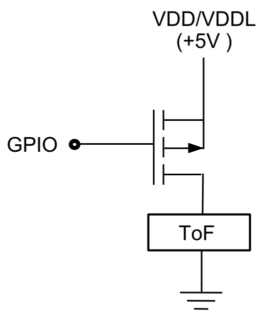
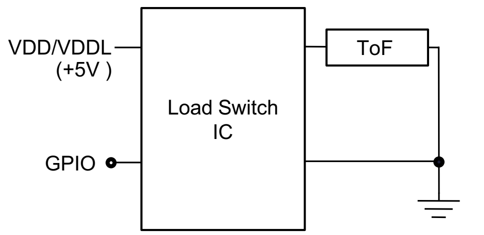
State	Typical Current Consumption
0	0 mA
1	1.5 mA
2	20 mA
3	33 mA



Hardware

In general, power or load switching can be realized by utilizing a switching device together with a GPIO pin from the microcontroller both connected to the ToF sensor. The most common options are depicted in the following figure.

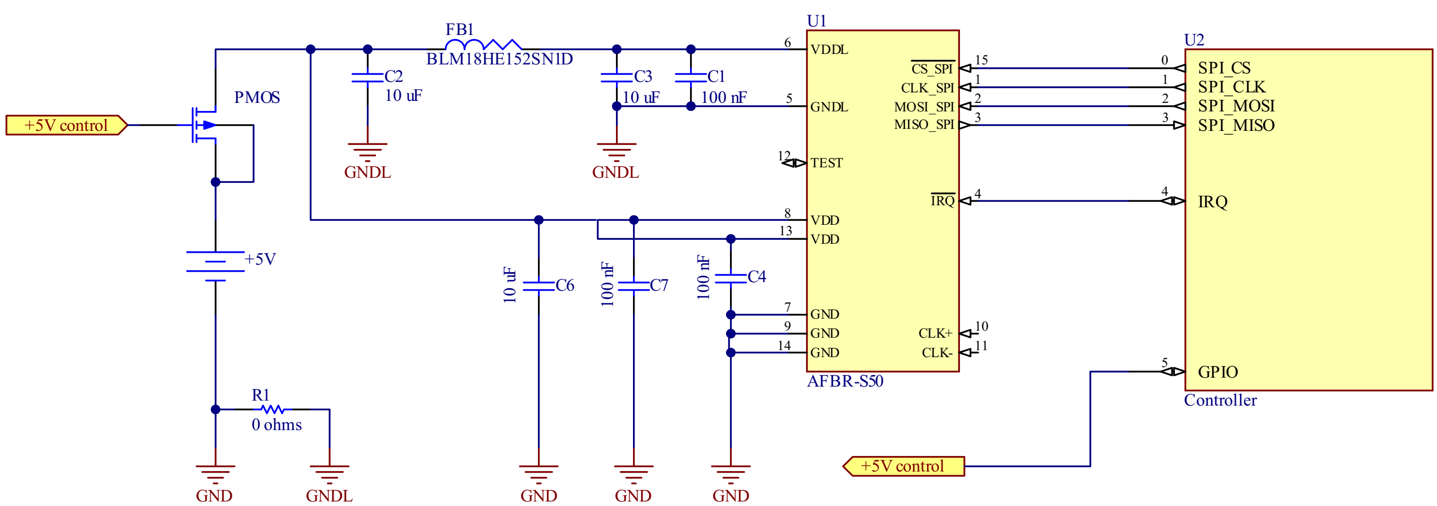
Figure 3: Load Switching Options

PMOS Switch	Load Switch IC
	
Pros: Low cost, small footprint Cons: No slew rate and inrush current control	Pros: Slew rate and inrush current control Cons: Higher cost, larger footprint

NOTE: See How do I know which power switch is the best for my application? for further information on load-switching options.

The following figure shows an example schematic with a PMOS switch with its gate controlled by a GPIO of the microcontroller. Usually VDD and VDDL are shorted to a common supply branch that is connected to the drain. Eventually, the PMOS source is, for instance, connected to a battery as a power source.

Figure 4: Example Circuitry Utilizing a PMOS Switch



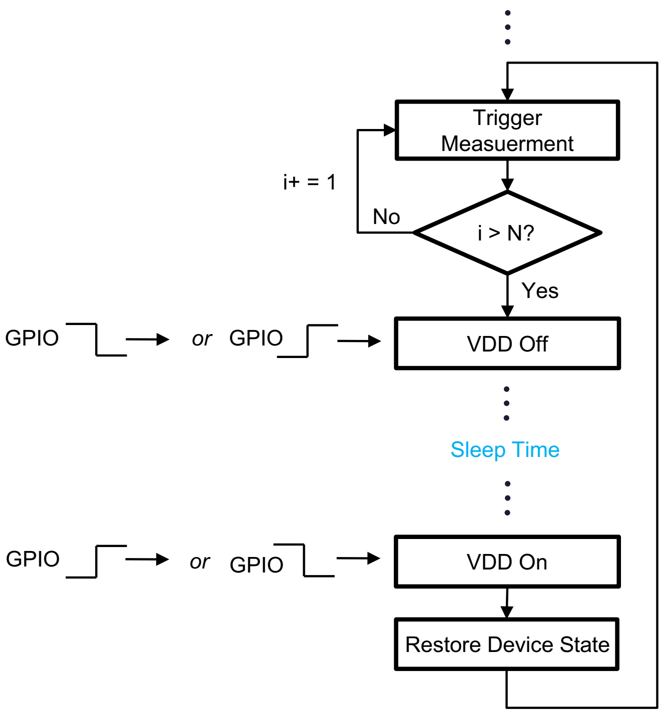
NOTE: See Are there any suggestions when using a PMOS transistor? for additional tips on the hardware implementation of a PMOS.

Software

This section explains the basic implementation sequence in software. Before starting, make sure that you have cloned or downloaded the latest software from the Broadcom AFBR-S50 GitHub repository under https://github.com/Broadcom/AFBR-S50-API.

The following figure shows the basic sequence of power switching and measurement cycles.

Figure 5: Measurement Sequence for the Lowest Power Consumption



The sequence depicts a complete power cycle, including a certain number *N* of measurements, followed by a power cycle and a register state restore to quickly start again after wake-up. A full example based on an STM HAL implementation can be retrieved from our GitHub repository.

Apart from the settings for the final current calculation given in the next section, the following points must be considered when implementing the code:

1. A switch of the power rail can be accomplished by a GPIO transition from high to low or low to high depending on your actual circuitry and GPIO configuration. For instance, a MOSFET in enhancement mode is by default a closed switch, whereas a depletion type MOSFET is open.
2. By configuring the GPIO at the MOSFET gate as open-drain, the logic can be inverted by default.
3. After *VDD On* is asserted, a delay of at least 1 ms is needed to boot the ToF ASIC. Additional time might be needed if the VDD switch-on inrush current is regulated by a load switch to avoid unnecessary wake-up iterations. For more information, see What can I do if error -114 appears before the first measurement?
4. To avoid additional current consumption, make sure that any post-processing, such as print commands, is invoked after the sensor is set to sleep.

Example

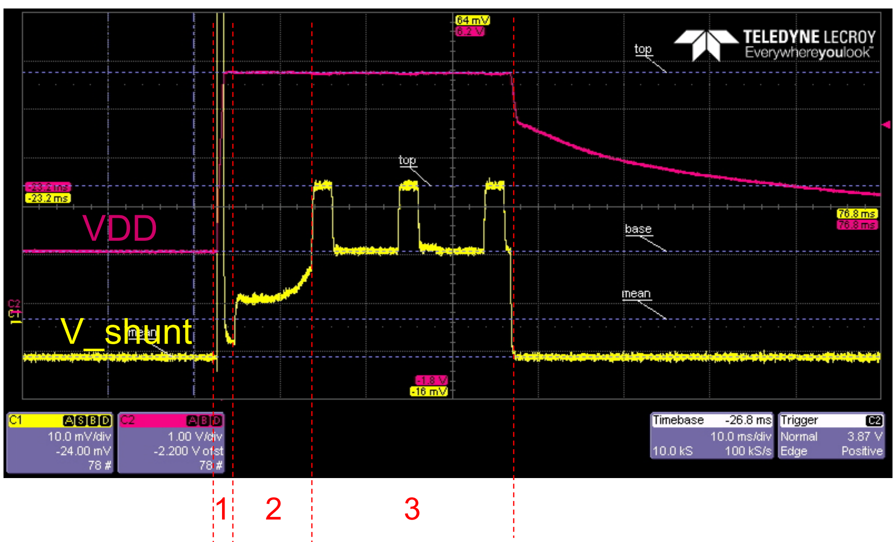
To better understand the current saving, this section presents a typical example with timing and current calculations. The following figure displays an oscilloscope acquisition of a wake-up utilizing the PMOS switch NDS0610 from Onsemi. While the pink waveform indicates the assertion of VDD, the yellow waveform shows the dropped voltage over a shunt resistor in the GND path, which directly translates into the sensors current consumption.

Timing

As can be seen, the current curve can be subdivided into three sections:

1. Inrush current: Caused by loading the capacitors and the slew rate of VDD.
2. Sensor configuration current: PLL lock + charge-pump ramp.
3. Measurement current: The following figure shows, as an example, 3 x trigger measurements @ 100 Hz with DFM off.

Figure 6: AFBR-S50 Wake-up Sequence Followed by 3 x Triggered Measurements



Timing:

1 – Typical 1-5 ms

2 – Typical 10-15 ms

3 – Frame time for x-measurements (depends on needed integration)

NOTE: (1) Inrush current can differ in terms of amplitude and duration. Additionally ~1 ms is used for the internal power-on-reset circuitry in the reset state. The sensor configuration phase (2) depends on the last used gain setting before going to sleep. The measurement phase (3) consists of the active integration time (high pulse peak @ typ. 33 mA) and the residual frame time (typ. 20 mA). Integration time varies depending on target reflectivity and distance.

Calculation

Assuming that there is a wake-up cycle every 10 seconds with 3 x measurements @ 100 Hz, the following calculation returns the average current consumption I_{av} of one cycle:

$$I_{av} = ((I_{inrush} \times t_{inrush}) + (I_{reset} \times t_{reset}) + (I_{config} \times t_{config}) + (I_{meas} \times (n \times t_{meas}))) / t_{sleep}$$

$$= ((300\text{ mA} \times 0.002\text{s}) + (1\text{ mA} \times 0.001\text{s}) + (20\text{ mA} \times 0.01\text{s}) + (33\text{ mA} \times (3 \times 0.01\text{s}))) / 10\text{s}$$

$$= \sim 180\ \mu\text{A}$$

With a total *on-time* of:

$t_{awake} = t_{inrush} + t_{reset} + t_{config} + t_{meas}$ = 35 ms (duty cycle of 0.35%)

NOTE: The real consumption might be even lower, because the maximum integration and maximum gain (ramp-up time) are used to simplify the calculation.

FAQs

How do I know which power switch is the best for my application?

CMOS component suppliers usually provide basic documentation with comparisons of the characteristics. An example can be found in the *Integrated Load Switches Versus Discrete MOSFETs* application report. In principle, the cheapest solution is the discrete PMOS (or NMOS), which also has the smallest footprint. On the other hand, a load switch IC has a clear advantage in terms of signal conformity.

Are there any suggestions when using a PMOS transistor?

It is suggested to use a logic level MOSFET transistor (in data sheets mostly referred to as *suited for low-voltage applications* or similar). Because most microcontrollers use +3.3V (or lower) and the AFBR-S50 sensor needs +5V, the PMOS switch circuitry shown in Figure 3 might need to be upgraded with a pull-up (for example, 20 kΩ) resistor from gate to source. When doing so, make sure that your GPIO is configured for open drain mode operation and is 5V tolerant. You can even save this pull-up if your PMOS already has a *Gate threshold voltage* minimum of –1.7V (3.3V to 5V).

What can I do if error -114 appears before the first measurement?

See the *AFBR-S50 API Reference Manual*.A possible root cause for this error is the waiting time before calling the function *Argus_RestoreDeviceState* being too small. By default, the example uses 1 ms for POR circuitry; however, this might not be enough for all configurations. For instance, load-switching ICs with inrush and slew rate control mostly use an RC combination in the input stage, which might require an increased waiting time after the wake-up. Best practice is to check the sensor current waveform with an oscilloscope by using a low-resistive shunt resistor and a differential probe and checking the pulse width of the inrush current.

What are the standard methods to achieve the lowest current consumption?

- **Minimize the number of triggered measurements.**

  As can be seen in the preceding example, the frame time contributes the most to the calculation. If the environmental conditions have completely changed from sleep to wake-up, the dynamic configuration adaptation (DCA) algorithm must adapt the integration parameters, which requires more frames. With dual frequency mode (DFM) on, the DCA may need up to five frames; without DFM, it may need up to three frames. Distance values might not be reliable if the wake-up interval uses fewer measurements.

- **Increase the power saving ratio.**

  By default, the PSR is 20% for all AFBR-S50 variants. This means that especially for close-range applications (<2m), the digital integration will use most of the residual frame time at the cost of power consumption. To reduce current consumption, carefully increase the PSR value by trading off current consumption and required digital integration for better precision.

For more information and technical support, contact support.tof@broadcom.com.