BROADCOM®

Data Sheet

AFBR-89CTHZ

QSFP28 Pluggable, Parallel Fiber-Optic Module Short Reach with 50m FEC-less Capability 100 GbE Applications 850-nm SR4, MMF, MPO Connector

Description

The Broadcom® AFBR-89CTHZ is a four-channel, pluggable, multimode, fiber-optic QSFP28 transceiver for 100 Gigabit Ethernet (GbE) applications. The transceiver is a high-performance module for short-range multilane data communication and interconnect applications. It integrates four data lanes in each direction with each lane operating at 25.78125 Gb/s, giving an aggregated bandwidth of 103.125 Gb/s. It allows optical interoperability up to 100m (with IEEE 802.3 Clause 91 KR-FEC) or 50m (FEC-less with 1E-12 bit error rate) over an 8-fiber (or 12-fiber) MPO optical multimode OM4 cable. The push-pull tab facilitates the insertion and extraction of these transceivers in a high-density environment. Each electrical lane operates at 25.78125 Gb/s and conforms to the 100 GbE CAUI4 interface.

Per channel transmitter and receiver retimers, configured for 4x25.78125G operation can be bypassed to enable alternative data rate transmission.

These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850 nm. The electrical interface uses a 38 contact QSFP28 edge type connector. The optical interface uses a conventional 8-fiber (or 12-fiber) MPO connector. This module incorporates a Broadcom proven integrated circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

Features

- Compliant to 100 GbE electrical and optical specifications IEEE 802.3 (Annex 83E CAUI-4 with Clause 91 RS-FEC, Clause 95 100GBASE-SR4)
- 100GbE Link Distances 100m OM4, 70m OM3 with KR-FEC and 50m OM4, 30m OM3 without FEC (1E–12 BER)
- QSFP28 MSA specification compliant, including new functions per SFF-8636 Rev 2.9
- Class 1 eye safety
- Push-pull tab: ease of transceiver insertion and extraction
- Operates at 25.78125 Gb/s per channel with 64b/66b coded data
- 0 to +70°C case temperature operating range
- Proven high reliability 850-nm technology: Broadcom VCSEL transmitter and Broadcom PIN detector
- Hot pluggable QSFP28 transceiver for ease of installation and servicing
- Two-wire serial (TWS) interface with digital monitoring and maskable interrupts for expanded functionality

Applications

- 100 GbE interconnects
- Datacom/telecom switch and router connections
- Data aggregation and backplane applications
- Proprietary protocol and density applications

Part Number Ordering Options

100 Gigabit Ethernet	AFBR-89CTHZ
Evaluation Board[a]	AFBR-89EVB
Evaluation Kit[b]	AFBR-89EVK

a. Includes GUI and user guide.

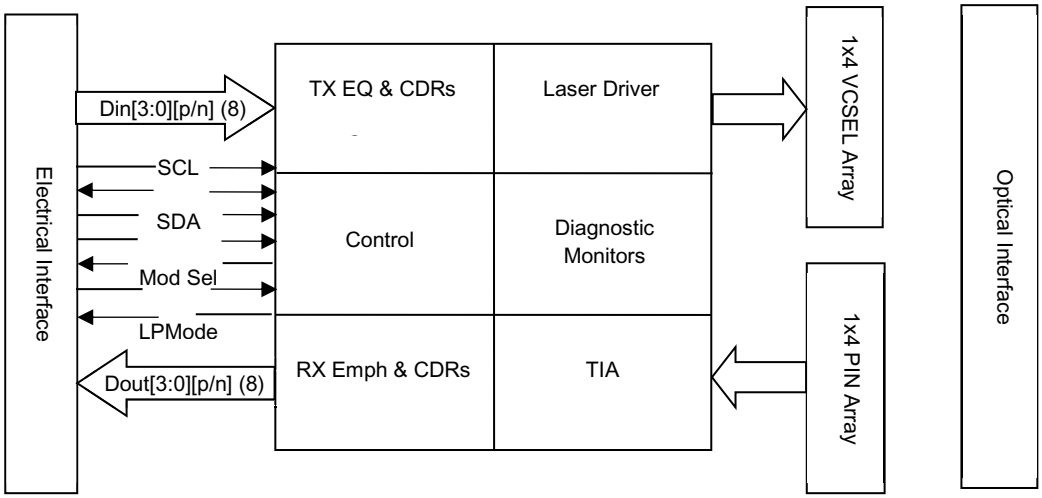
b. Includes GUI, user guide, I^2C controller and power supply cable.

Module and Label

QSFP28 Relevant Specifications per SFF-8024 (rev3.3)

Steering Document	Low Speed, Connector, and Electrical Requirements	Common Management Specification/ Memory Map	Form Factor/ Module Mechanical	Cage/Connector Solution	
SFF-8665	SFF-8679	SFF-8636	SFF-8661	SFF-8662 and SFF-8663	Style A
				SFF-8672 and SFF-8683	Style B

Figure 1: Transceiver Block Diagram



Transmitter

The optical transmitter portion of the transceiver (see Figure 1) incorporates a 4-channel vertical cavity surface emitting laser (VCSEL) array, a 4-channel equalization (EQ) block with integrated CDR and laser driver, diagnostic monitors, and control and bias blocks. The transmitter is designed for IEC-60825 and CDRH eye safety compliance; Class 1 out of the module. The TX input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100Ω. AC coupling capacitors are located inside the QSFP28 module and are not required on the host board. For module control and interrogation, the control interface (LVTTL compatible) incorporates a two-wire serial (TWS) interface of clock and data signals. Diagnostic monitors for VCSEL bias, temperature, and power supply voltage are implemented, and results are available through the TWS interface.

Alarm and warning thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of input signal (LOS) and transmitter fault conditions. All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset by reading the appropriate flag register. The optical output will squelch for loss of input signal unless squelch is disabled. Fault detection or channel deactivation through the TWS interface will disable the channel. Status, alarm/warning and fault information are available through the TWS interface. To reduce the need for polling, the hardware interrupt signal is provided to inform hosts of an assertion of alarm, warning, LOS, and/or TX fault.

Receiver

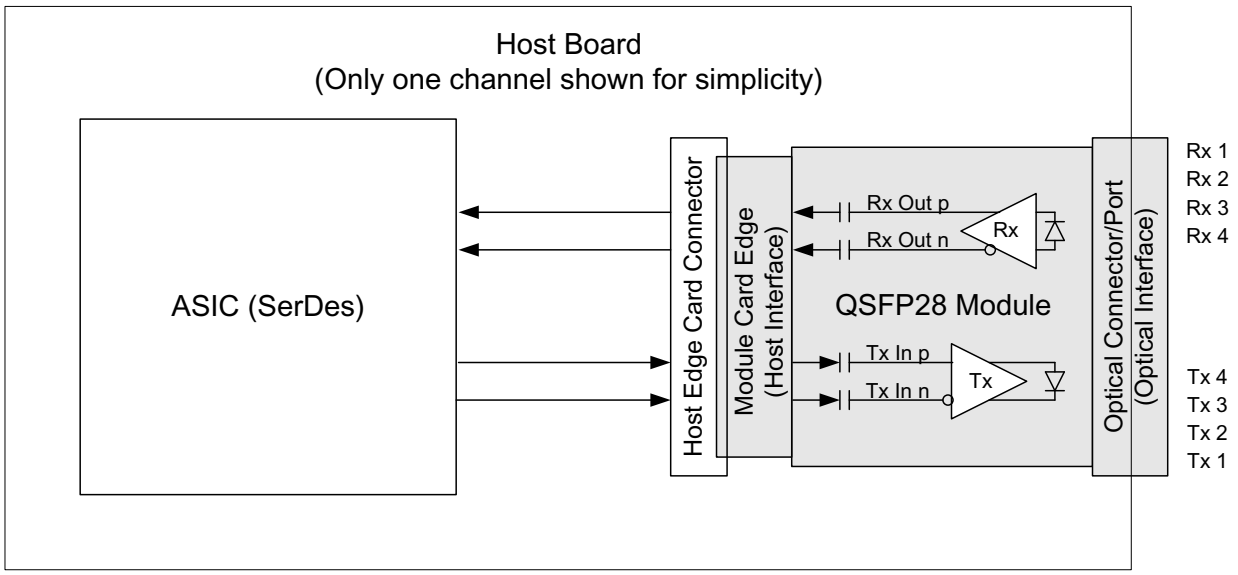
The optical receiver portion of the transceiver (see Figure 1) incorporates a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4-channel line driver with integral CDR, diagnostic monitors, and control and bias blocks. The RX output buffer provides CML compatible differential outputs for the high-speed electrical interface that should be differentially terminated with 100Ω. AC coupling capacitors are located inside the QSFP28 module and are not required on the host board. Diagnostic monitors for optical input power are implemented, and results are available through the TWS interface.

Alarm and warning thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of optical input signal (LOS). All flags are latched and will remain set even if the condition initiating the flag clears and operation resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register. The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel deactivation through TWS interface. Status and alarm/warning information are available via the TWS interface. To reduce the need for polling, the hardware interrupt signal is provided to inform hosts of an assertion of alarm, warning and/or LOS.

High-Speed Electrical Signal Interface

Figure 2 shows the interface between an ASIC/SerDes and the QSFP28 module. For simplicity, only one channel is shown. The high-speed signal lines are AC-coupled 100Ω differential lines. The AC coupling is inside the QSFP28 module and is not required on the host board. The 100Ω differential terminations are inside the QSFP28 module for the transmitter lines and at the host ASIC/SerDes for the receiver lines.

Figure 2: Application Reference Diagram



Control Signal Interface

The module has the following low-speed signals for control and status: ModSelL, LPMode, ResetL, ModPrsL, IntL. In addition, there is an industry-standard two-wire serial interface scaled for 3.3V LVTTL. It is implemented as a slave device. Signal and timing characteristics are further defined in Control Interface and Memory Map.

The registers of the serial interface memory are defined in Control Interface and Memory Map.

Digital Diagnostic Monitoring

This information provides opportunity for predictive failure identification, compliance prediction, fault isolation, and component monitoring.

- Predictive Failure Identification – This diagnostic information allows the host system to identify potential link problems. Once identified, a *failover* technique can be used to isolate and replace suspect devices before system uptime is impacted.
- Compliance Prediction – These real-time diagnostic parameters can be monitored to alert the system when operating limits are exceeded and compliance cannot be ensured. As an example, the real-time average receiver optical power can be used to assess the compliance of the cable plant and remote transmitter.
- Fault Isolation – This diagnostic information can allow the host to pinpoint the location of a link problem and accelerate system servicing and minimize downtime.
- Component Monitoring – As part of host system qualification and verification, this real-time transceiver diagnostic information can be combined with system-level monitoring to ensure the performance and operating environment are meeting application requirements.

Digital diagnostic monitoring for the following attributes is implemented:

- Transceiver module temperature – Represents the module case temperature (Page 00h, Addresses 22-23).
- Transceiver module power supply – Reports the module +3.3V supply voltage (Page 00h, Addresses 26-27).
- Transmitter output power – Reports the average output optical power for each transmitter channel (Page 00h, Addresses 50-51 for ch.1, Addresses 52-53 for ch.2, Addresses 54-55 for ch.3, Addresses 56-57 for ch.4).
- Transmitter laser bias current – Reports the DC laser bias current for each transmitter channel (Page 00h Addresses 42-43 for ch.1, Addresses 44-45 for ch.2, Addresses 46-47 for ch.3, Addresses 48-49 for ch.4).
- Receiver input power – Reports the average input optical power for each receiver channel (Page 00h Addresses 34-35 for ch.1, Addresses 36-37 for ch.2, Addresses 38-39 for ch.3, Addresses 40-41 for ch.4).

All diagnostic monitor attributes are two-byte fields. To maintain coherency, the host must access these with single two-byte read sequences.

For each monitored attribute, alarm and warning thresholds are established. Flags are set and interrupts generated when the attributes are outside the thresholds. All flags are latched and will remain set even if the condition initiating the flag clears. A mask bit that can be set to prevent assertion of interrupt for each individual attribute exists for every monitor flag. Entries in the mask fields are volatile.

Package Outline

The module is designed to meet the package outline defined in the QSFP28 SFF-8661 specification. See QSFP28 Package Outline for details.

Handling and Cleaning

The transceiver module can be damaged by exposure to current surges and overvoltage events. Care should be taken to restrict exposure to the conditions defined in Absolute Maximum Ratings. Wave soldering, reflow soldering and/or aqueous wash process with the modules on board are not recommended. Normal handling precautions for electrostatic discharge sensitive devices should be observed.

Each module is supplied with an inserted port plug for protection of the optical ports. This plug should always be in place whenever a fiber cable is not inserted.

The optical connector includes recessed elements that are exposed whenever a cable or port plug is not inserted. Prior to insertion of a fiber optic cable, it is recommended that the cable end be cleaned to avoid contamination from the cable plug. The port plug ensures the optics remains clean and no additional cleaning should be needed. In the event of contamination, dry nitrogen or clean dry air at less than 20 psi can be used to dislodge the contamination. The optical port features (for example, guide pins) preclude use of a solid instrument. Liquids are also not advised.

Absolute Maximum Ratings

Stress in excess of any of the individual absolute maximum ratings can cause immediate catastrophic damage to the module even if all other parameters are within recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the absolute maximum ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min.	Max.	Units	Reference
Storage Temperature	Ts	–40	85	°C	
3.3V Power Supply Voltage	Vcc	–0.5	3.6	V	
Data Input Voltage – Single Ended		–0.5	Vcc + 0.5	V	
Data Input Voltage – Differential	$\lvert V_{DIp} - V_{DIn} \rvert$	—	0.8	V	a
Control Input Voltage	Vi	–0.3	Vcc + 0.5, 3.6	V	
Control Output Current	Io	–20	20	mA	
Relative Humidity	RH	5	95	%	

a. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. Per SFF-8679, the damage threshold of the module input must be at least 1600 mV peak-to-peak differential.

Recommended Operating Conditions

Recommended operating conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the recommended operating conditions. Reliability is not implied and damage to the module can occur for such operation over an extended period of time.

Parameter	Symbol	Min.	Typ.	Max.	Units	Reference
Case Temperature	Tc	0	—	70	°C	a
3.3 V Power Supply Voltage	Vcc	3.1	3.3	3.465	V	
Signal Rate per Channel, 100 GbE		—	25.78125	—	GBd	b
Power Supply Noise		—	—	66	mVpp	c
Receiver Differential Data Output Load		—	100	—	Ω	
Fiber Length (OM3) – 5E–5 BER		0.5	—	70	m	d
Fiber Length (OM4) – 5E–5 BER		0.5	—	100	m	e
Fiber Length (OM3) – 1E–12 BER		0.5	—	30	m	f
Fiber Length (OM4) – 1E–12 BER		0.5	—	50	m	g

a. The position of case temperature measurement is shown in Figure 8. Continuous operation at the maximum recommended operating case temperature should be avoided in order not to degrade reliability.

b. 256b/257b coding. This translates to a nominal unit interval of 38.787879 ps.

c. Power supply noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 9 for recommended power supply filter.

d. OM3 fiber effective modal bandwidth is 2000 MHz·km 50-µm MMF (minimum). The RS-FEC correction function cannot be bypassed for any operating distance. The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. The loss of a single connection must not exceed 0.75 dB.

e. OM4 fiber effective modal bandwidth is 4700 MHz·km 50-µm MMF (minimum). The RS-FEC correction function cannot be bypassed for any operating distance. The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. The loss of a single connection must not exceed 0.75 dB.

f. OM3 fiber effective modal bandwidth is 2000 MHz·km 50-µm MMF (minimum). The link can be without FEC and the BER is 1E–12. The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. The loss of a single connection must not exceed 0.75 dB.

g. OM4 fiber effective modal bandwidth is 4700 MHz·km 50-µm MMF (minimum). The link can be without FEC and the BER is 1E–12. The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. The loss of a single connection must not exceed 0.75 dB.

General Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. For control signal timing including ModSelL, LPMode, ResetL, ModPrsL, IntL, SCL, and SDA, see I/O Timing for Control and Status Functions.

Parameter	Symbols	Min.	Typ.	Max.	Units	Reference
Transceiver Power Consumption		—	2.0	2.5	W	a
Transceiver Power Supply Current		—	606	—	mA	
AC Coupling Capacitors (Internal)		—	0.1	—	µF	

a. Power Class 3.

High-Speed Electrical Module Input Characteristics

From CAUI-4, IEEE 802.3 Clause 83E, Table 83E-7. The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/Conditions
Signaling Rate, per Lane	TP1	—	25.78125	—	GBd	±100 ppm
Differential pk-pk Input Voltage Tolerance	TP1a	900	—	—	mV	
Differential Input Return Loss (min)	TP1	—	Eq 83E-5	—	dB	IEEE 802.3
Differential to Common Mode Input Return Loss (min)	TP1	—	Eq 83E-6	—	dB	IEEE 802.3
Differential Termination Mismatch	TP1	—	—	10	%	
Module Stressed Input Test	TP1a	—	83E.3.4.1	—		IEEE 802.3, below
Single-ended Voltage Tolerance Range	TP1a	–0.4	—	3.3	V	
DC Common-mode Output Voltage	TP1	–0.350	—	2.85	V	a
Module Stressed Input Test						b
Eye Width		0.46			UI	
Applied pk-pk Sinusoidal Jitter		Table IEEE 802.3 88-13				
Eye Height		95			mV	
Electrical Input LOS Assert Threshold, Differential Peak-to-Peak Voltage Swing	ΔVdi pp los	10	—	—	mVpp	
LOS Hysteresis		0.5	—	4	dB	c

a. DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.

b. Module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1.

c. LOS hysteresis is defined as 20 × Log (LOS deassert level/LOS assert level).

Reference Points

Test Point	Description
TP0	Host ASIC transmitter output at ASIC package pin on a DUT board.
TP1	Input to module compliance board through mated module compliance board and module connector. Used to test module input.
TP1A	Host ASIC transmitter output across the host board and host edge card connector at the output of the host compliance board.
TP2	Optical transmitter output as measured at the end of a 2m to 5m patch cord mated to the optical module.
TP3	Optical test point as measured at the end of an optical fiber cable; closest test point to the presumed optical receiver input.
TP4	Module output through mated module and host edge card connector through module compliance board.
TP4A	Input to host compliance board through mated host compliance board and host edge card connector. Used to test host input.
TP5	Input to host ASIC.

Figure 3: IEEE 802.3 CAUI-4 Compliance Points TP1a, TP4a

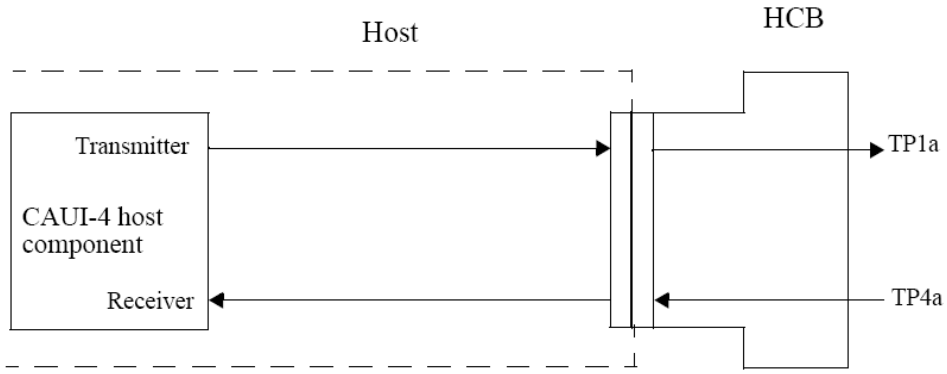


Figure 83E–4—Host CAUI-4 compliance points

NOTE: A reference receiver is used to measure host eye width and eye height at TP1a. The reference receiver includes a selectable continuous time linear equalizer (CTLE) which is described by Equation (83E–4, below) with coefficients given in Table 83E–2.

$$H(f) = \frac{GP_1P_2}{Z_1}$$

Where:

- H(f) is the CTLE transfer function, f is the frequency in GHz.
- G is the CTLE gain.
- P_1, P_2 are the CTLE poles in Grad/s.
- Z_1 is the CTLE zero in Grad/s.

Figure 4: Table 83E-2 – Reference CTLE Coefficients

Table 83E–2—Reference CTLE coefficients

Peaking (dB)	G	$\frac{P_1}{2\pi}$	$\frac{P_2}{2\pi}$	$\frac{Z_1}{2\pi}$
1	0.89125	18.6	14.1	8.364
2	0.79433	18.6	14.1	7.099
3	0.70795	15.6	14.1	5.676
4	0.63096	15.6	14.1	4.9601
5	0.56234	15.6	14.1	4.358
6	0.50119	15.6	14.1	3.844
7	0.44668	15.6	14.1	3.399
8	0.39811	15.6	14.1	3.012
9	0.35481	15.6	14.1	2.672

High-Speed Electrical Module Output Characteristics

From CAUI-4, IEEE 802.3 Clause 83E, Table 83E-3. The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/Conditions
Signaling Rate, Per Lane	TP4	—	25.78125	—	GBd	±100 ppm
AC Common-mode Output Voltage (max, RMS)	TP4	—	—	17.5	mV, rms	
Differential Output Voltage	TP4	—	—	900	mV	
Eye Width	TP4	0.57	—	—	UI	
Eye Height, Differential	TP4	228	—	—	mV	
Vertical Eye Closure	TP4	—	—	5.5	dB	
Differential Output Return Loss (min)	TP4	—	Eq 83E-2	—	dB	IEEE 802.3
Common to Differential Mode Conversion Return Loss (min)	TP4	—	Eq 83E-3	—	dB	IEEE 802.3
Differential Termination Mismatch	TP4	—	—	10	%	
Transition Time (20% to 80%)	TP4	12	—	—	ps	
DC Common-mode Voltage	TP4	–0.35	—	2.85	V	

Figure 5: IEEE 802.3 CAUI-4 Compliance Points TP1, TP4

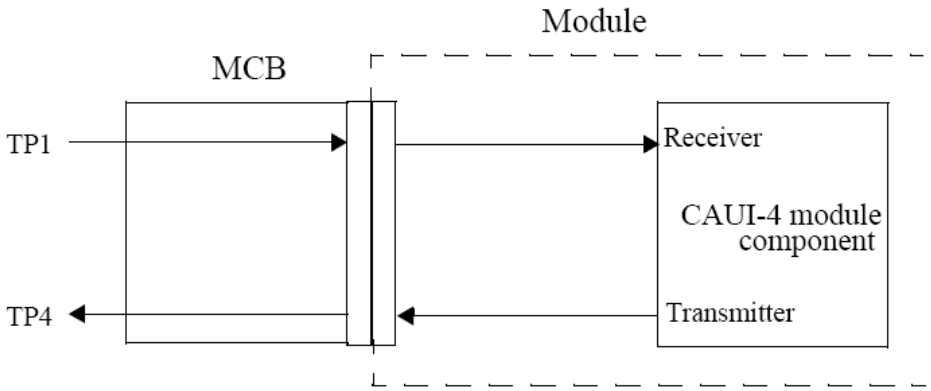


Figure 83E–5—Module CAUI-4 compliance points

High-Speed Optical Transmitter Characteristics

From 100GBASE-SR4, IEEE 802.3 Clause 95, Table 95-6. The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

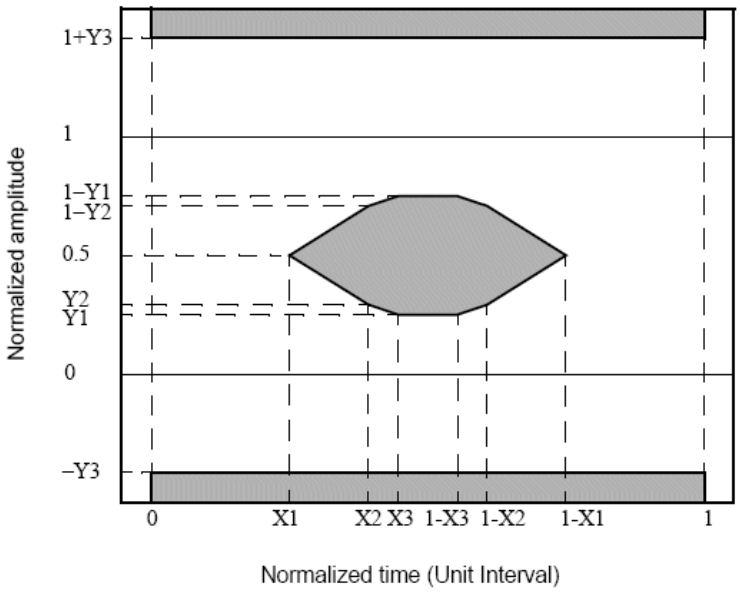
Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/Conditions
Signaling Rate, Per Lane		—	25.78125	—		±100 ppm
Center Wavelength Range	TP2	840	—	860	nm	
RMS Spectral Width	TP2	—	—	0.60	nm	a
Average Launch Power, Each Lane	TP2	–8.4	—	+2.4	dBm	
Optical Modulation Amplitude (OMA) Each Lane	TP2	–6.4[b]	—	+3.0	dBm	
Launch Power in OMA Minus TDEC, Each Lane	TP2	–7.3	—	—	dBm	
Transmitter and Dispersion Eye Closure (TDEC), Each Lane	TP2	—	—	4.3	dB	
Average Launch Power Of Off Transmitter, Each Lane	TP2	—	—	–30	dBm	
Extinction Ratio	TP2	2	—	—	dB	
Optical Return Loss Tolerance	TP2	—	—	12	dB	
Encircled Flux[c]	TP2	≥86% at 19 µm ≤30% at 4.5 µm				Type A1a.2 50-µm Fiber per IEC 61280-1-4
Transmitter Eye Mask Definition: {X1, X2, X3, Y1, Y2, Y3}	TP2	Specification Values {0.3, 0.38, 0.45, 0.35, 0.41, 0.5}				Hit Ratio 1.5 x 10^{-3} hits per sample

a. RMS spectral width is the standard deviation of the spectrum.

b. Even if the TDEC < 0.9 dB, the OMA (min) must exceed this value.

c. If measured into Type A1a.2 50 µm fiber in accordance with IEC 61280-1-4.

Figure 6: Transmitter Eye Mask Definitions



High-Speed Optical Receiver Characteristics

From 100GBASE-SR4, IEEE 802.3 Clause 95, Table 95-7. The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/Conditions
Signaling Rate, per Lane		—	25.78125	—		±100ppm
Center Wavelength Range, Each Lane	TP3	840	—	860	nm	
Damage Threshold	TP3	+3.4	—		dBm	a
Average Receive Power, Each Lane	TP3	–10.3	—	+2.4	dBm	b
Receive Power (OMA), Each Lane	TP3	—	—	+3.0	dBm	
Receiver Reflectance	TP3	—	—	–12	dB	
Stressed Receiver Sensitivity OMA, Each Lane	TP3	—	—	–5.2	dBm	c
Conditions of Stressed Receiver Sensitivity Test		—	—	—		d
Stressed Eye Closure (SEC), Lane Under Test		—	4.3	—	dB	
Stressed Eye J2 Jitter, Lane Under Test		—	0.39	—	UI	
Stressed Eye J4 Jitter, Lane Under Test		—	0.53	—	UI	
OMA of Each Aggressor Lane		—	3	—	dBm	
Stressed Receiver Eye Mask Definition: X1, X2, X3, Y1, Y2, Y3		Specification Values {0.28, 0.50, 0.50, 0.33, 0.33, 0.40}				Hit Ratio 5 x 10^{-5} hits per sample
LOS Assert (OMA)	TP3	–30	—	—	dBm	
LOS Deassert (OMA)	TP3	—	—	–9.1	dBm	
LOS Hysteresis	TP3	0.5	—	—	dB	

a. The receiver must be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

b. Average receive power, each lane (min), is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

c. Measured with conformance test signal at TP3 (refer to IEEE 802.3 Section 95.8.8) for BER specified in IEEE 802.3 Section 95.1.1.

d. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Regulatory Compliance

The AFBR-89CTHZ complies with all applicable laws and regulations as detailed in Regulatory Compliance Table. Certification level is dependent on the overall configuration of the host equipment. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

The AFBR-89CTHZ is compatible with ESD levels found in typical manufacturing and operating environments. as described in Regulatory Compliance Table. In the normal handling and operation of optical transceivers, ESD is of concern in two circumstances.

The first case is during handling of the transceiver prior to insertion into a QSFP compliant cage. To protect the device, it is important to use normal ESD handling precautions. These include use of grounded wrist straps, workbenches, and floor wherever a transceiver is handled.

The second case to consider is static discharges to the exterior of the host equipment chassis after installation. If the optical interface is exposed to the exterior of the host equipment cabinet, the transceiver might be subject to system-level ESD requirements.

Electromagnetic Interference (EMI)

Equipment incorporating multigigabit transceivers is typically subject to regulation by the FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe, and VCCI in Japan. The AFBR-89CTHZ compliance to these standards is detailed in Regulatory Compliance Table. The metal housing and shielded design of the AFBR-89CTHZ minimizes the EMI challenge facing the equipment designer.

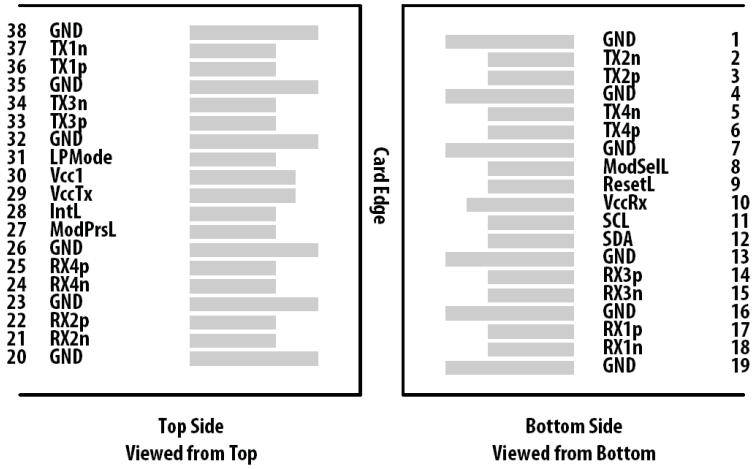
Flammability

The AFBR-89CTHZ optical transceiver is made of metal and high strength, heat resistant, chemical resistant and UL94V-0 flame retardant plastic.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JS-001-2017)	All contacts must withstand 1000V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	EN61000-4-2, Criterion B	When installed in a properly grounded housing and chassis, the units are subjected to 15 kV air discharges during operation and 8 kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing	Class 1 Laser Product Complies with 21 CFR 1040.10 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019 (IEC) EN 62368-1: 2014+A11 (IEC) EN 60825-1: 2014 (IEC) EN 60825-2: 2004+A1+A2	CDRH Accession Number: 9720151-196 TUV File: R 72201311 CB File: US-TUVR-012148
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E484615
RoHS Compliance		Less than 1000 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls (PPB) and polybrominated biphenyl ethers (PBDE).

Figure 7: QSFP28 Transceiver Pin Layout



QSFP28 Transceiver Pin Layout

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground.	1	a
2	CML-I	TX2n	Transmitter Inverted Data Input.	3	b
3	CML-I	TX2p	Transmitter Noninverted Data Input.	3	b
4		GND	Ground.	1	a
5	CML-I	TX4n	Transmitter Inverted Data Input.	3	b
6	CML-I	TX4p	Transmitter Noninverted Data Input.	3	b
7		GND	Ground.	1	a
8	LVTTL-I	ModSelL	Module Select. When held low by the host, the module responds to 2-wire serial communication commands.	3	
9	LVTTL-I	ResetL	Module Reset. The ResetL signal is pulled up to Vcc in the QSFP28 module.	3	
10		VccRx	+3.3V Power Supply Receiver.	2	c
11	LVCMOS-I/O	SCL	2-wire Serial Interface Clock. Requires pull-up resistor to 3.3V on the host board.	3	
12	LVCMOS-I/O	SDA	2-wire Serial Interface Data. Requires pull-up resistor to 3.3V on the host board.	3	
13		GND	Ground.	1	a
14	CML-O	RX3p	Receiver Noninverted Data Output.	3	b
15	CML-O	RX3n	Receiver Inverted Data Output.	3	b
16		GND	Ground.	1	a
17	CML-O	RX1p	Receiver Noninverted Data Output.	3	b
18	CML-O	RX1n	Receiver Inverted Data Output.	3	b
19		GND	Ground.	1	a
20		GND	Ground.	1	a
21	CML-O	RX2n	Receiver Inverted Data Output.	3	b
22	CML-O	RX2p	Receiver Noninverted Data Output.	3	b
23		GND	Ground.	1	a
24	CML-O	RX4n	Receiver Inverted Data Output.	3	b
25	CML-O	RX4p	Receiver Noninverted Data Output.	3	b
26		GND	Ground.	1	a
27	LVTTL-O	ModPrsL	Module Present. Requires pull-up resistor to 3.3V on the host board. Module Present is pulled low in the module.	3	
28	LVTTL-O	IntL	Interrupt. The IntL signal is an open collector output and must be pulled to host supply voltage (3.3V) on the host board.	3	
29		VccTx	+3.3V Power Supply.	2	c
30		Vcc1	+3.3V Power Supply.	2	c
31	LVTTL-I	LPMode	Low Power Mode. LPMode is pulled up to Vcc in the module.	3	
32		GND	Ground.	1	a
33	CML-I	TX3p	Transmitter Noninverted Data Input.	3	b

Pin	Logic	Symbol	Description	Plug Sequence	Notes
34	CML-I	TX3n	Transmitter Inverted Data Input.	3	b
35		GND	Ground.	1	a
36	CML-I	TX1p	Transmitter Noninverted Data Input.	3	b
37	CML-I	TX1n	Transmitter Inverted Data Input.	3	b
38		GND	Ground.	1	a

a. GND is the symbol for signal supply (power) common for the QSFP28 module. All are common within the QSFP28 module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

b. For all TX and RX high-speed differential inputs/outputs, there are 0.1-µF AC coupling capacitors that are located inside the QSFP28 module and are not required on the host board.

c. VccRx, Vcc1, and VccTx are the receiver and transmitter power supplies and must be applied concurrently.

Figure 8: Case Temperature Measurement Point

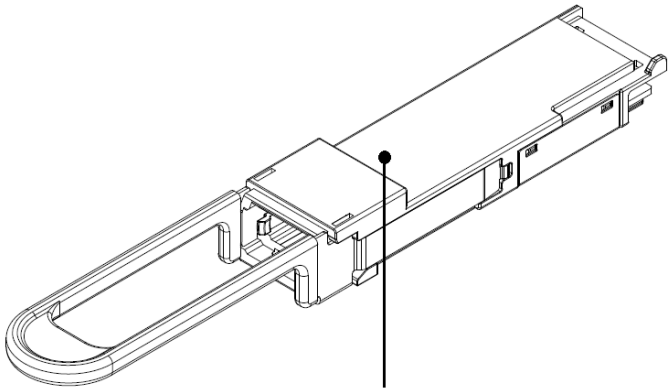


Figure 9: Recommended Power Supply Filter

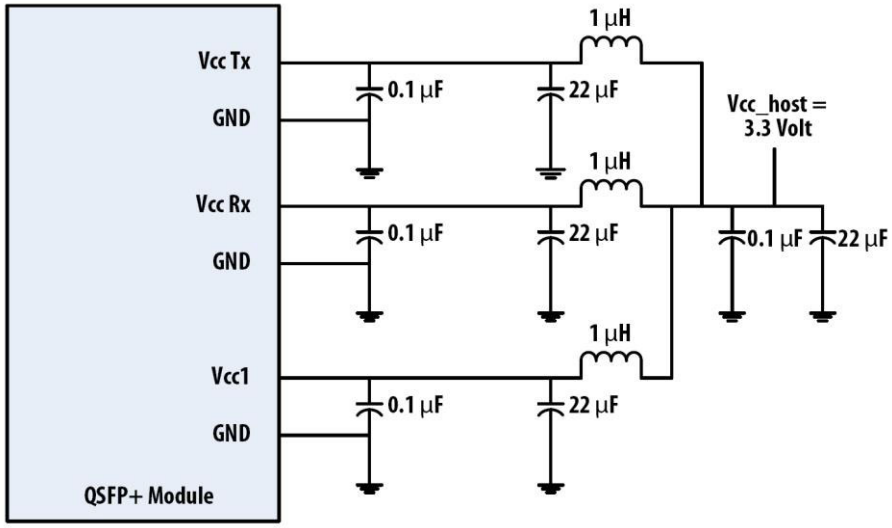


Figure 10: Transmitter Data Input Equivalent Circuit

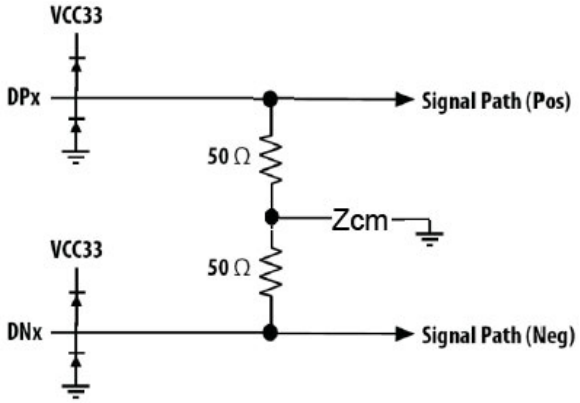


Figure 11: Receiver Data Output Equivalent Circuit

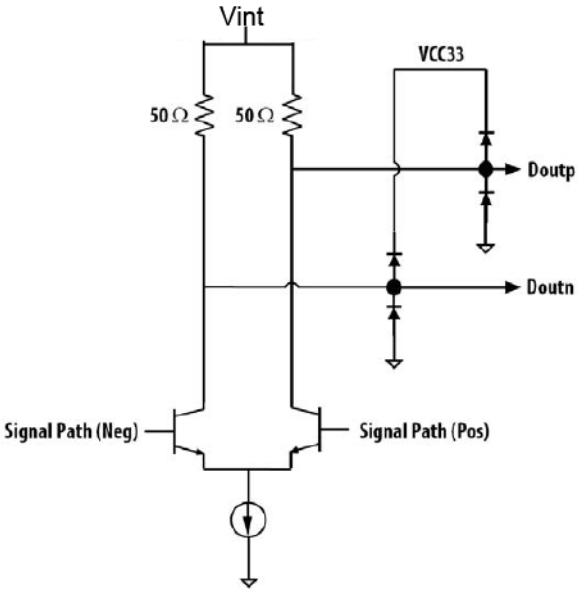
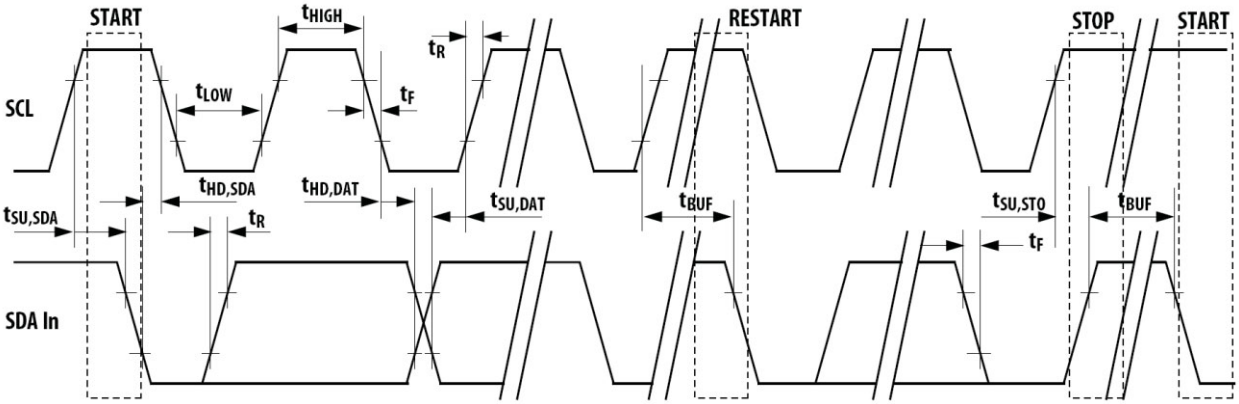
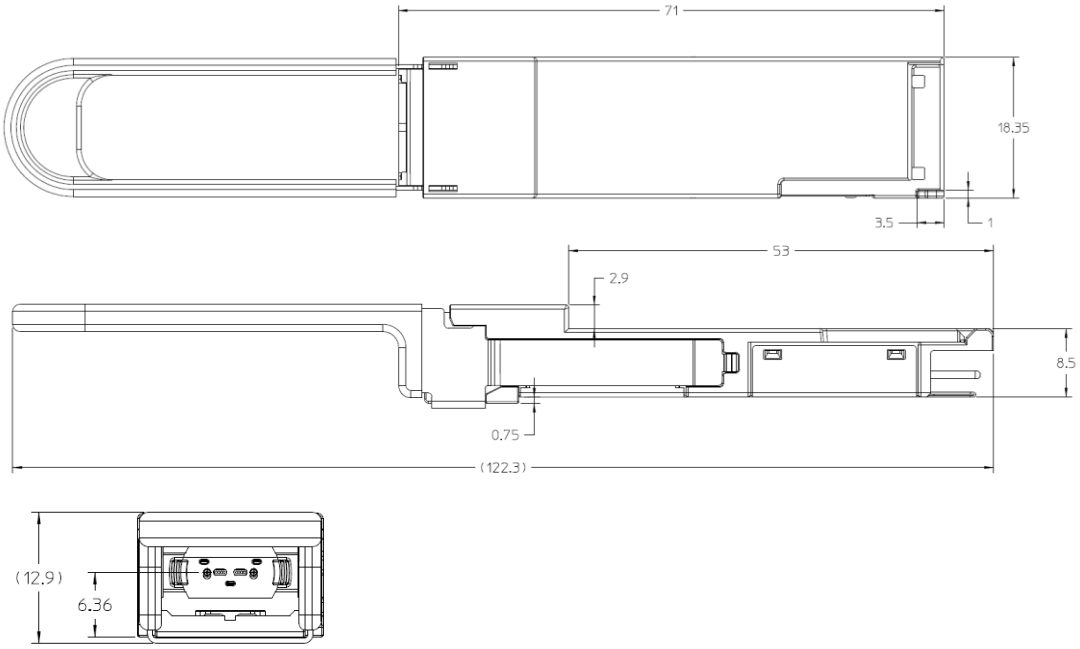


Figure 12: TWS Interface Bus Timing



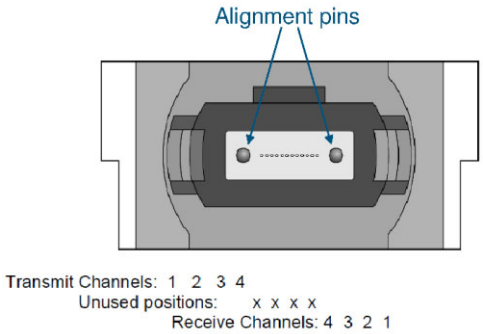
QSFP28 Package Outline

Figure 13: Mechanical Package Outline (All dimensions in mm)



Per SFF-8679, the pull-tab is color coded as Beige for 850-nm optical devices.

Figure 14: Module Optical Interface (Looking into the Optical Port)



The optical interface port is a male MPO connector as specified in IEC 61754-7.
Aligned key MTP/MPO patch cords should be used to ensure alignment of the signals between the modules.
The aligned key patch cord is defined in TIA-568.

Control Interface and Memory Map

The control interface combines dedicated signal lines for ModSelL, LP Mode, ResetL, ModPrsL, IntL with two-wire serial (TWS), interface clock (SCL), and data (SDA) signals to provide users rich functionality over an efficient and easily used interface. The TWS interface is implemented as a slave device and compatible with industry-standard two-wire serial protocol. It is scaled for 3.3V LVTTL. Outputs are high-Z in the high state to support busing of these signals. Signal and timing characteristics are further defined in I/O Timing for Control and Status Functions and Low-Speed Pin Electrical Specifications. For more details, refer to QSFP28 SFF-8436.

ModSelL

The ModSelL is an input signal. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interface bus. When the ModSelL is High, the module will not respond to or acknowledge any 2-wire interface communication from the host. The ModSelL signal input node is biased to the High state in the module. In order to avoid conflicts, the host system must not attempt 2-wire interface communications within the ModSelL deassert time after any QSFP28 modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and deasserting periods of different modules can overlap as long as the timing requirements in QSFP Management Interface Timing Parameters are met.

ResetL

The ResetL signal is pulled up to Vcc in the QSFP28 module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init), the host must disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power-up (including hot insertion), the module will post this completion of reset interrupt without requiring a reset.

LPMode

Low power mode (LPMode) is pulled up to Vcc in the QSFP28 module. The pin is a hardware control used to put modules into a low power mode when high. In low power mode, the module power consumption is limited to Power Level 1 (1.5W max). By using the LPMode pin and a combination of the Power_override, Power_set, and High_Power_Class Enable software control bits (Address A0h, byte 93 bits 0,1,2), the host controls how much power a module can dissipate.

ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted Low when inserted and deasserted High when the module is physically absent from the host connector.

IntL

IntL is an output signal. When Low, this signal indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is an open collector output and must be pulled to host supply voltage on the host board.

The INTL pin is deasserted High after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of 0 and the flag field is read (refer to SFF-8636).

The present value of the various diagnostic monitors can also be read using the 2-wire serial interface. Case module temperature, supply voltage, laser bias current for each channel, and receiver input power (Pave) for each channel are reported. All monitor items are two-byte fields, and to maintain coherency, the host must access these with single two-byte read sequences. For each monitored item, alarm and warning thresholds are established. If an item moves past a threshold, a flag is set, and provided the item is not masked, IntL is asserted. A mask bit that can be set to prevent assertion of IntL for the individual item exists for every LOS, TX fault, and monitor flag. Entries in the mask fields are volatile.

Soft Status and Control

A number of soft status signals and controls are available in the AFBR-89CTHZ transceiver memory and are accessible through the TWS interface. Some soft status signals include receiver LOS, transmitter LOS, and diagnostic monitor alarms and warnings. Some soft controls include transmitter disable (Tx_Dis), receiver output disable (Rx_Dis), transmitter squelch disable (Tx_SqDis), receiver squelch disable (Rx_SqDis), and masking of status signal in triggering IntL. All soft status signals and controls are per-channel basis. All soft control entries are volatile.

Transmitter LOS

The transmitter LOS status signal is on Page 00h, Address 3, bits 4–7 for channels 1–4, respectively. Transmitter LOS is based on input differential voltage. This status register is latched, and it is cleared on read.

Receiver LOS

The receiver LOS status signal is on Page 00h, Address 3, bits 0-3 for channels 1-4 respectively. Receiver LOS is based on input optical modulation amplitude (OMA). This status register is latched, and it is cleared on read.

Transmitter LOL

The transmitter loss of lock status signal is on Page 00h, Address 5, bits 4–7 for channels 1–4, respectively. The loss of lock flag will assert if an enabled TX-side CDR is not locked to the input data signal. This status register is latched, and it is cleared on read.

Receiver LOL

The receiver loss of lock status signal is on Page 00h, Address 5, bits 0–3 for channels 1–4, respectively. The loss of lock flag will assert if an enabled RX-side CDR is not locked to the input data signal. This status register is latched, and it is cleared on read.

Transmitter Fault

The transmitter fault status signal is on Page 00h, Address 4, bits 0–3 for channels 1–4, respectively. The transmitter fault condition will flag if the laser output power is too high, that is, approaching eye safety levels. When fault is triggered, the corresponding transmitter channel output will be disabled. Module reset or toggling of soft transmitter disable (Address 86 decimal) can restore the transmitter channel function unless fault condition persists. This status register is latched, and it is cleared on read.

Transmitter Disable

The transmitter disable control is on Page 00h, Address 86, bits 0–3 for channels 1–4, respectively. When the TX is disabled, the transmitter power must be less than –30 dBm.

Receiver Output Disable

The receiver output disable control is on Page 03h, Address 241, bits 4–7 for channels 1–4, respectively. If the receiver output is disabled, the output differential voltage swing must be less than 50 mVpp.

Transmitter Squelch Disable

The transmitter squelch disable control is on Page 03h, Address 240, bits 0–3 for channels 1–4, respectively. AFBR-89CTHZ transceivers have the transmitter output squelch function enabled as default. If the transmitter output is in the Squelched state, the laser output power will be turned off.

Receiver Squelch Disable

The receiver squelch disable control is on Page 03h, Address 240, bits 4–7 for channels 1–4, respectively. AFBR-89CTHZ transceivers have the receiver output squelch function enabled as default. If the receiver output is in the Squelched state, the output differential voltage swing must be less than 50 mVpp.

Module Start-Up Behavior

Default Host Conditions

The host system should ensure the following default conditions are present at an empty QSFP28 connector. This ensures the transceiver will see a known state for power-up and initialization.

- IntL (pin 28) – Pulled high by host via resistor.
- ModPrsL (pin 27) – Pulled high by host via resistor.
- ResetL (pin 9) – Tristate on host (or pulled high by GPIO).
- LPMode (pin 31) – Tristate on host (or pulled high by GPIO).
- ModSelL (pin 8) – Tristate on host (or pulled high by GPIO).

Module Insertion (Hot Plug) or Power On (Cold Start)

Upon insertion of a QSFP28 transceiver (or upon power-up of a preinstalled transceiver), the QSFP28 will immediately result in the following conditions at the connector.

- ModPrsL (pin 27) – Pulled low internally by QSFP28 (internally grounded).
- ResetL (pin 9) – Pulled high internally by QSFP28 (default to normal operation enabled).
- LPMode (pin 31) – Pulled high internally by QSFP28 (default to low power mode enabled).

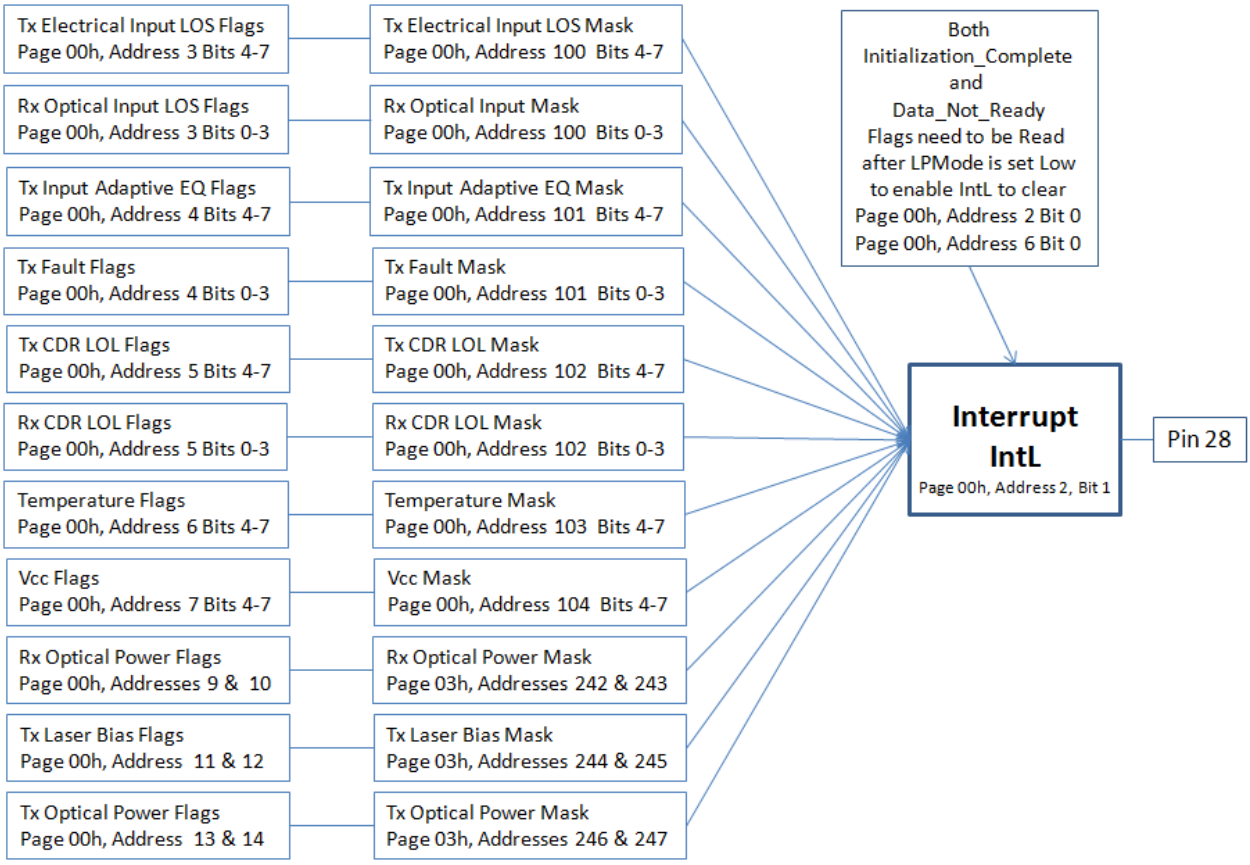
Host Reads Transceiver Vitals and Enables Operation

When QSFP28 powers up and initializes, the host should use the following to enable normal operation. AFBR-89CTHZ requires more than 1.5W to operate, requiring LPMode management to enable.

NOTE: While in low power mode (LPMode pin 31 high), AFBR-89CTHZ Data_Not_Ready Flag is asserted (TWS Page 00h, Address 2, bit 0 = 1) and Initialization Complete Flag is not asserted (TWS Page 00h, Address 6, bit 0 = 0).

- ModSelL (pin 8) is pulled low by host GPIO to enable QSFP28 two-wire serial (TWS) communication.
- IntL (pin 28) will be pulled low by the QSFP28 after initialization (alarming).
- Host reads TWS Page 00h 128-255. Check Power Class requirements and confirm compatibility.
- Host clears LPMode; pull pin 31 low with GPIO, or use TWS Page 00h, Address 93, bits 0-1.
- Host reads TWS Page 00h, Address 2, bit 0 (Data_Not_Ready Flag).
- Host reads TWS Page 00h, Address 6, bit 0 (Initialization Complete Flag).
- IntL (pin 28) is allowed high by QSFP28 after LPMode released and Flag Bits read.
- Diagnostics can now be polled. Conrol/Status registers are now active.
- If IntL (pin 28) alarms again (i.e., pulled low by QSFP28), flags and masks are now active.

Figure 15: Flags, Masks, and Interrupt Condition



I/O Timing for Control and Status Functions

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Per SFF-8679 Rev 1.8.

Parameter	Symbol	Min	Max	Unit	Reference
Initialization Time	t_init	—	2000	ms	Time from power-on, hot plug or rising edge of reset until the module is fully functional. This time does not apply to non power level 0 modules in the Low Power state.
Reset Init Assert Time	t_reset_init	—	10	µs	A reset is generated by a low level longer than the minimum reset pulse time present on ResetL.
Serial Bus Hardware Ready Time	t_serial	—	2000	ms	Time from power-on until module responds to data transmission over the 2-wire serial bus.
Monitor Data Ready Time	t_data	—	2000	ms	Time from power-on to data not ready, bit 0 of byte 2, deasserted and IntL asserted.
Reset Assert Time	t_reset	—	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional.
LPMode Assert Time	ton_LPMode	—	100	ms	Time from assertion of LPMode until the module power consumption enters power level 1.
LPMode Deassert Time	toff_LPMode	—	300	ms	Time from deassertion of LPMode until module is fully functional.
Interrupt Assert Time	ton_IntL	—	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol.
Interrupt Deassert Time	Toff_IntL	—	500	µs	Time from clear-on-read operation of associated flag until Vout:IntL = Voh. This includes deassert times for RX LOS, TX Fault, and other flag bits.
RX LOS Assert Time	ton_los	—	100	ms	Time from RX LOS state to RX LOS bit set and IntL asserted.
TX Fault Assert Time	ton_Txfault	—	200	ms	Time from TX Fault state to TX Fault bit set and IntL asserted.
Flag Assert Time	ton_Flag	—	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted.
Mask Assert Time	ton_Mask	—	100	ms	Time from mask bit set until associated IntL assertion is inhibited.
Mask Deassert Time	toff_Mask	—	100	ms	Time from mask bit cleared until associated IntL operation resumes.
Power_override or Power_set Assert Time	ton_Pdown	—	100	ms	Time from P_Down bit set (value = 1b) until module power consumption reaches power level 1.
Power_override or Power_set Deassert Time	toff_Pdown	—	300	ms	Time from P_Down bit cleared (value = 0b) until module is fully functional.
RX Squelch Assert Time	ton_Rxsq	—	15	ms	Time from loss of RX input signal until the squelched output condition is reached.
RX Squelch Deassert Time	toff_Rxsq	—	15	ms	Time from resumption of RX input signals until normal RX output condition is reached
TX Squelch Assert Time	ton_Txsq	—	400	ms	Time from loss of TX input signal until the squelched output condition is reached.
TX Squelch Deassert Time	toff_Txsq	—	400	ms	Time from resumption of TX input signals until nominal TX output condition is reached.
TX Disable Assert Time	ton_txdis	—	100	ms	Time from TX Disable bit set until optical output falls below 10% of nominal.

Parameter	Symbol	Min	Max	Unit	Reference
TX Disable Deassert Time	toff_txdis	—	400	ms	Time from TX Disable bit cleared until optical output rises above 90% of nominal.
RX Output Disable Assert Time	ton_rxdis	—	100	ms	Time from RX Output Disable bit set until RX output falls below 10% of nominal.
RX Output Disable Deassert Time	toff_rxdis	—	100	ms	Time from RX Output Disable bit cleared until RX output rises above 90% of nominal.
Squelch Disable Assert Time	ton_sqdis	—	100	ms	This applies to RX and TX Squelch and is the time from bit set until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	—	100	ms	This applies to RX and TX Squelch and is the time from bit cleared until squelch functionality enabled.

QSFP Management Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit	Condition
ModSelL Setup Time[a]	Host_select_setup	2	—	ms	Setup time on the select lines before start of a host-initiated serial bus sequence.
ModSelL Hold Time[a]	Host_select_hold	10	—	µs	Delay from completion of a serial bus sequence to ModSelL rising edge.
Aborted Sequence – Bus Release	Deselect_Abort	—	2	ms	Delay from a host setting ModSelL to high (at any point in a bus sequence) to the QSFP module releasing SCL and SDA.

a. ModeSelL Setup and Hold times are requirements of the host system.

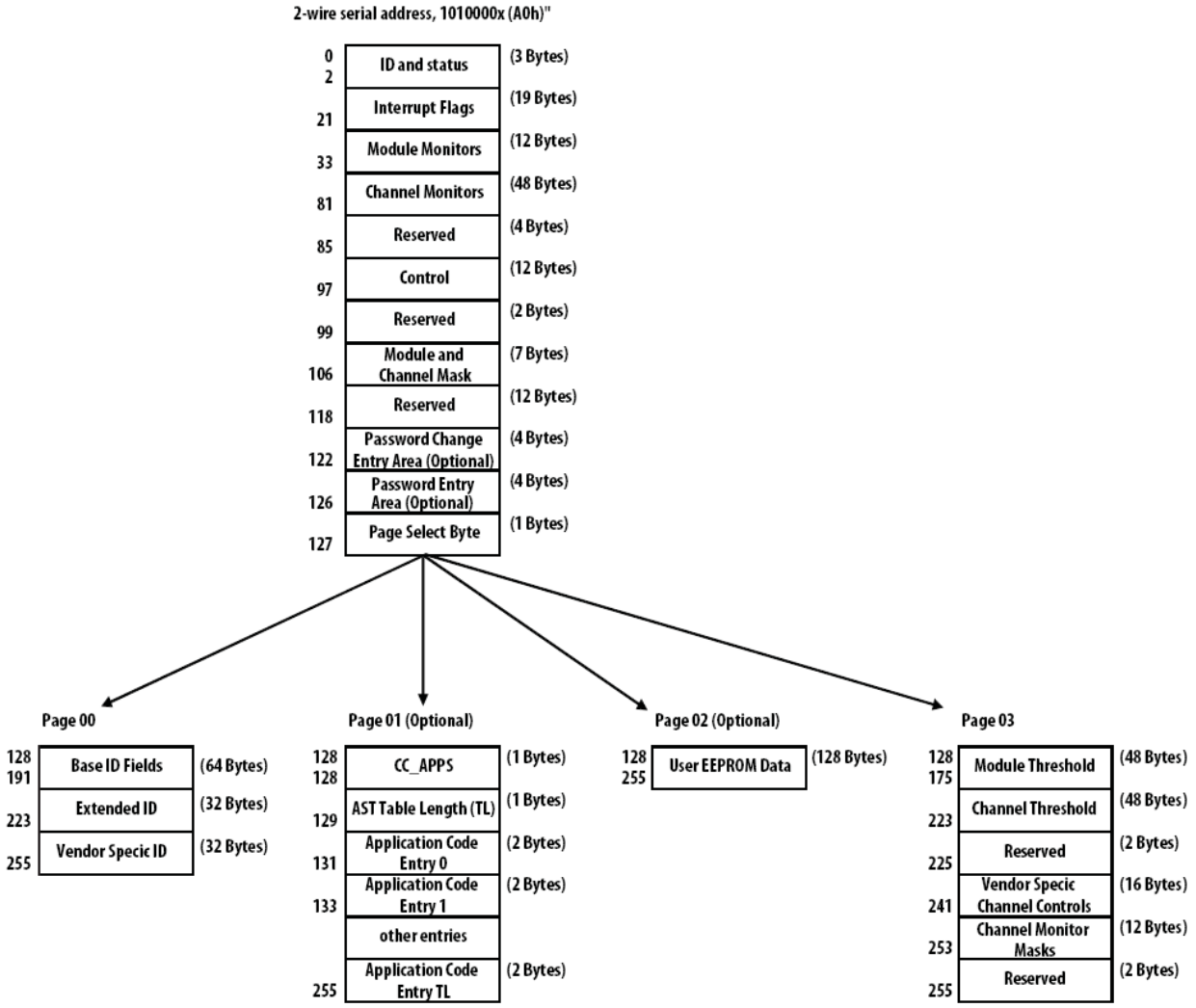
Low-Speed Pin Electrical Specifications

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max) = 3.0mA
	VOH	Vcc – 0.5	Vcc + 0.3	V	
SCL and SDA	VIL	–0.3	Vcc × 0.3	V	
	VIH	Vcc × 0.7	Vcc + 0.5	V	
LPMode, ResetL and ModSelL	VIL	–0.3	0.8	V	|Iin| ≤ 125 µA for 0V < Vin,Vcc
	VIH	2	Vcc + 0.3	V	
ModPrsL and IntL	VOL	0	0.4	V	IOL = 2.0 mA
	VOH	Vcc – 0.5	Vcc + 0.3	V	
Two-Wire Serial (TWS) Interface Clock Rate			400	kHz	

Memory Map

The memory is structured as a single address, multiple page approach. The 7-bit device address on the two-wire interface is 1010000b. The structure of the memory is shown in Figure 16. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g., Interrupt Flags and Monitors. Less time critical entries, for example, serial ID information and threshold settings, are available with the Page Select function. For a more detailed description of the QSFP28 memory map, refer to the QSFP28 SFF-8636 Specification.

Figure 16: Memory Map Diagram



Transmitter Input Equalization Control

Upper Memory Page 03h, Bytes 234-235 (EAh-EBh). From Table 6-34 of SFF-8636.

Code	Transmitter Input Equalization		Note
	Nominal	Unit	
11xx	Reserved, Equalization equal to 1010 setting	dB	
1011	Reserved, Equalization equal to 1010 setting	dB	
1010	10	dB	
1001	9	dB	
1000	8	dB	
0111	7	dB	
0110	6	dB	
0101	5	dB	
0100	4	dB	
0011	3	dB	Manual/Static default setting
0010	2	dB	
0001	1	dB	
0000	0	No Equalization	

Receiver Output Emphasis Control

Upper Memory Page 03h, Bytes 236-237 (ECh-EDh). From Table 6-35 of SFF-8636.

Code	Receiver Output Emphasis		Note
	Nominal	Unit	
1xxx	Reserved, Emphasis equal to 0111 setting	dB	
0111	7	dB	
0110	6	dB	
0101	5	dB	
0100	4	dB	
0011	3	dB	
0010	2	dB	
0001	1	dB	Default setting
0000	0	No Emphasis	

Receiver Output Amplitude Control

Upper Memory Page 03h, Bytes 238-239 (EEh-EFh). From Table 6-33 of SFF-8636.

Code	Receiver Output Amplitude No Output Equalization		Note
	Nominal	Unit	
1xxx-0100	Reserved. Amplitude stays at Max; equal to 0011 level	mV(P-P)	
0011	600 to 1200	mV(P-P)	Default setting
0010	400 to 800	mV(P-P)	
0001	300 to 600	mV(P-P)	
0000	100 to 400	mV(P-P)