

## AELT-8000 Series

### Line Driver IC with High-Voltage Quad Differential Output



#### Description

The Broadcom® AELT-8000 Series is an industrial-power line driver featuring four identical short-circuit-proof differential line drivers, capable of handling up to 36V of driver supply with a joint enable function and operating at a maximum frequency of up to 5 MHz.

The AELT-8000 is equipped with a thermal shutdown feature that provides over-temperature protection during overload conditions. Its high data rate, combined with wide operating voltage and temperature range, makes it an ideal, versatile, and robust line driver suitable for typical industrial line driver applications.

The small-outline SOIC and TSSOP packages offer excellent thermal power dissipation, making them suitable for use in space-limited applications.

#### Key Features

- Operating frequency: up to 5 MHz
- Driver supply range: 4.5V to 36V
- Pin compatible to 26xx31, xx7272
- Short-circuit-proof tri-state outputs
- Low propagation delay: 80 ns (typical)
- High impedance CMOS-compatible and TTL-compatible buffered inputs with hysteresis
- Operating temperature range: -40°C to 125°C
- Over-temperature protection circuit
- Under-voltage monitoring

#### Applications

- Line driver for 5V to 36V control systems
- Rotary and linear encoder interfacing
- Industrial controls
- Sensor systems

**NOTE:** This product is not specifically designed or manufactured for use in any specific device. Customers are solely responsible for determining the suitability of this product for its intended application and are liable for all loss, damage, expense, or liability in connection with such use.

## Pin Assignment

Figure 1: SOIC-16

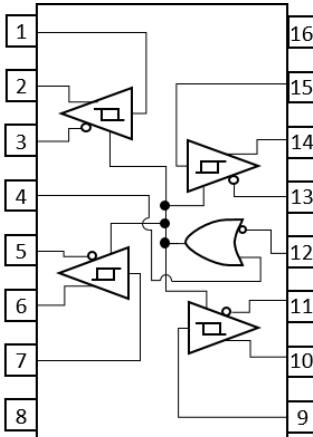


Figure 2: TSSOP-16

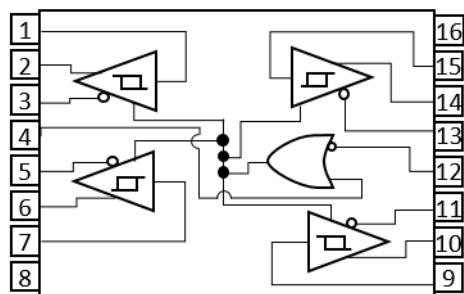
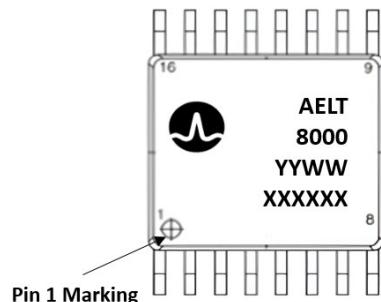
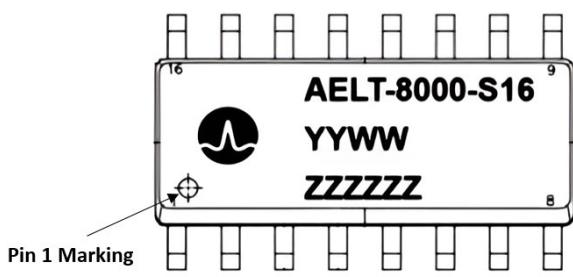


Figure 3: Device Marking Information



AELT-8000-S16 = Product Part Number

YYWW = Package Assembly Date

ZZZZZZ = Assembly Lot Number

AELT-8000 = Product Part Number

YYWW = Package Assembly Date

XXXXXX = Assembly Lot Number

Table 1: Pin Configurations

Number	Name	Type	Description
1	A <sub>IN</sub>	I	Input A
2	A+	O	Driver Output A
3	A-	O	Inverted Driver Output A
4	ENH	I	Enable Active HIGH
5	B-	O	Inverted Driver Output B
6	B+	O	Driver Output B
7	B <sub>IN</sub>	I	Input B
8	GND	S	Ground

Number	Name	Type	Description
9	C <sub>IN</sub>	I	Input C
10	C+	O	Driver Output C
11	C-	O	Inverted Driver Output C
12	ENL	I	Enable Active LOW
13	D-	O	Inverted Driver Output D
14	D+	O	Driver Output D
15	D <sub>IN</sub>	I	Input D
16	VDD	S	Supply Voltage

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Supply Voltage	VDD	0	40	V	
Voltage at Inputs	x <sub>IN</sub> ()	0	VDD	V	x is one of the input channels: A, B, C, or D
Voltage at Input Enable	V <sub>IN</sub> ()	0	VDD	V	
Voltage at Output	V ()	0	VDD	V	
ESD Susceptibility at All Pins	V <sub>d</sub> ()	-2	2	kV	HBM, JS-001-2014
Junction Temperature	T <sub>j</sub>	-40	150	°C	
Storage Temperature	T <sub>S</sub>	-40	150	°C	
Thermal Resistance	R <sub>JA</sub>	25	45	°C/W	No load, junction-to-ambient
Moisture Sensitive Level	MSL	—	1	—	

**CAUTION!** Subjecting the product to stresses beyond those listed in this section may cause permanent damage to the devices. These are stress ratings only and do not imply that the devices will function beyond these ratings. Exposure to the extremes of these conditions for extended periods may affect product reliability.

## Thermal Information

Parameter	Symbol	Typ.	Unit	Notes
Thermal Resistance SOIC TSSOP	R <sub>JA</sub>	103 129	°C/W	No load, junction-to-ambient
Thermal Resistance SOIC TSSOP	R <sub>JC</sub>	36 61	°C/W	No load, junction-to-case

## Electrical Characteristics

Typical operating conditions: VDD = 5V, TA = 25°C, unless otherwise specified.

- Operation Mode:**
- 1) Standard: ENL = Low, ENH = High
  - 2) Tri-state: ENL = High, ENH = Low

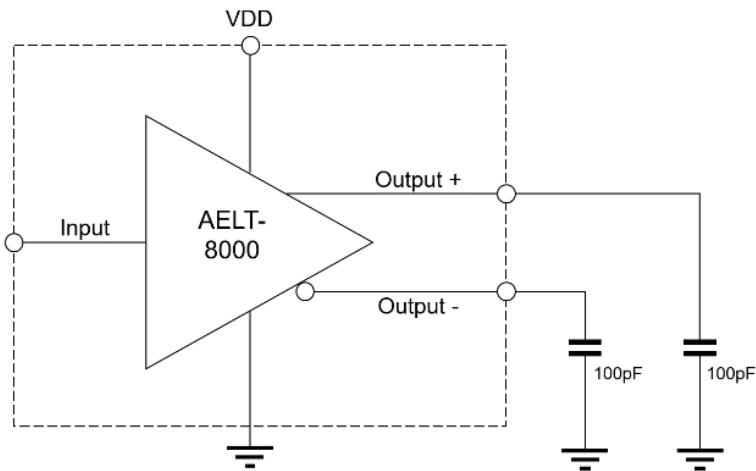
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Supply Parameters</b>						
Operating Frequency	f <sub>OPERATE</sub>	—	—	—	5	MHz
Permissible Supply Voltage	VDD	—	4.5	5	36	V
Operating Ambient Temperature	T <sub>A</sub>	—	-40	—	125	°C
Supply Current in VDD	ICC	VDD = 5V, No load/toggle standard	—	8	15	mA
		VDD = 36V, No load/toggle standard	—	16	30	mA
Tri-state Current Consumption in VDD	ICC (TRI)	VDD = 5V, No load/toggle Tri-state	—	3	—	mA
		VDD = 36V, No load/toggle Tri-state	—	10	—	mA
Clamp Voltage lo at ENH, ENL	Vclamp Δ lo	IΔ = -1 mA	-1.4	-0.6	-0.3	V
Clamp Voltage hi at ENH, xIN <sup>a</sup> , ENL	Vclamp Δ hi	IΔ = 1 mA	VDD + 0.3	VDD + 0.7	VDD + 1.5	V
Clamp Voltage lo at xOUT <sup>b</sup>	Vclamp Δ lo	VDD = 0V, IΔ = -10 mA	-1.2	-0.75	-0.3	V
Clamp Voltage hi at xOUT	Vclamp Δ hi	VDD = 0V, IΔ = 10 mA	VDD + 0.8	VDD + 1.5	VDD + 2.2	V
<b>Driver Input</b>						
Driver Threshold Voltage Low	V <sub>TH-</sub>	—	0.8	1.2	—	V
Driver Threshold Voltage High	V <sub>TH+</sub>	—	—	1.7	2.4	V
Driver Input Hysteresis	V <sub>ΔHYS</sub>	—	0.2	0.5	—	V
Driver Input Leakage Current	I <sub>IL</sub>	xIN = 0V / VDD	—	0	5	μA
Enable Input Threshold Voltage Low	V <sub>TH-EN</sub>	—	0.8	1.2	—	V
Enable Input Threshold Voltage High	V <sub>TH+EN</sub>	—	—	1.7	2.4	V
Enable Input Hysteresis	V <sub>ΔHYS_EN</sub>	—	0.2	0.5	—	V
Input Current at ENL	I <sub>IL</sub> – ENL	ENL = 0V	-60	-40	—	μA
<b>Driver Output</b>						
Low Side Short-Circuit Current	I <sub>SC</sub> (LS)	VDD = 5V, xOUT = VDD	—	185	300	mA
High Side Short-Circuit Current	I <sub>SC</sub> (HS)	VDD = 5V, xOUT = 0V	—	185	300	mA
Low Side Driving Capability	I <sub>DRV</sub> (LS)	VDD = 5V, VΔ = 3V	80	165	300	mA
High Side Driving Capability	I <sub>DRV</sub> (HS)	VDD = 5V, VΔ = VDD – 3V	-300	-135	-60	mA
Low Side Switch Output Resistance	R <sub>OUT</sub> (LS)	I <sub>LOAD</sub> = 40 mA	—	13	30	Ω
High Side Switch Output Resistance	R <sub>OUT</sub> (HS)	I <sub>LOAD</sub> = -40 mA	—	22	—	Ω
Output Leakage Current	I <sub>Leak</sub>	Tri-state	—	0	10	μA

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Driver Output Timing</b>						
Propagation Delay from 50% Point of Rising Edge of Input Pulse to Zero Crossing of Differential Outputs with a C Load of 100 pF	$t_{PLH}$	VDD = 5V, $C_{load}$ = 100 pF	—	65	130	ns
		VDD = 12V, $C_{load}$ = 100 pF	—	70	140	ns
		VDD = 36V, $C_{load}$ = 100 pF	—	75	165	ns
Propagation Delay from 50% Point of Falling Edge of Input Pulse to Zero Crossing of Differential Outputs with a C Load of 100 pF	$t_{PHL}$	VDD = 5V, $C_{load}$ = 100 pF	—	70	140	ns
		VDD = 12V, $C_{load}$ = 100 pF	—	75	150	ns
		VDD = 36V, $C_{load}$ = 100 pF	—	80	175	ns
Delay Skew ( $t_{PLH} - t_{PHL}$ )	$t_{DELAY}$ Δ	VDD = 4.5V ~ 36V	—	7	—	ns
Output Rise Time with a C Load of 100 pF	$t_{RISE}$	VDD = 5V, $C_{load}$ = 100 pF	—	35	100	ns
		VDD = 12V, $C_{load}$ = 100 pF	—	45	110	ns
		VDD = 36V, $C_{load}$ = 100 pF	—	65	180	ns
Output Fall Time with a C Load of 100 pF	$t_{FALL}$	VDD = 5V, $C_{load}$ = 100 pF	—	25	80	ns
		VDD = 12V, $C_{load}$ = 100 pF	—	30	85	ns
		VDD = 36V, $C_{load}$ = 100 pF	—	35	95	ns
<b>Undervoltage Detection</b>						
Undervoltage Threshold Low	$V_{TRIG}$	—	3.2	3.8	—	V
Undervoltage Threshold High	$V_{REC}$	—	—	3.9	4.4	V
Undervoltage Hysteresis	$V_{HYS}$	—	30	100	—	mV
Undervoltage Lockout Delay	$t_{SHUT}$ Δ	—	—	7	—	μs
<b>Over-Temperature Detection</b>						
Shutdown Temperature Threshold <sup>c</sup>	$T_{OFF}$	Standard	135	165	185	°C
Temperature Hysteresis	$T_{\Delta OFF}$	Standard	—	25	—	°C

a.  $xIN$  = Any input ( $A_{IN}$ ,  $B_{IN}$ ,  $C_{IN}$ , or  $D_{IN}$ )b.  $xOUT$  = Any output ( $A+$ ,  $A-$ ,  $B+$ ,  $B-$ ,  $C+$ ,  $C-$ ,  $D+$ , or  $D-$ )c. AELT-8000 will trigger thermal shutdown when  $T_j > 165^\circ\text{C}$ , under stress conditions.

## Test Circuit Diagram

Figure 4: Example of a Test Circuit Diagram with AELT-8000 Series, Implementing 100-pF Load at Each Output



## Functional Output Modes

Table 2: Output Modes for the AELT-8000 Series

Input	Enables		Output +	Output -
	ENH	ENL		
High	High	X	High	Low
Low	High	X	Low	High
High	X	Low	High	Low
Low	X	Low	Low	High
X	Low	High	Z	Z

**NOTE:**

- X = Either / Irrelevant
- Z = High Impedance

## Timing Diagrams

The following are examples of the timing characteristics of AELT-8000 input and output waveforms.

Figure 5: Propagation Delay Time

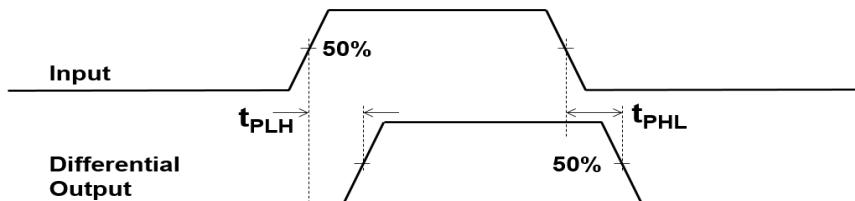
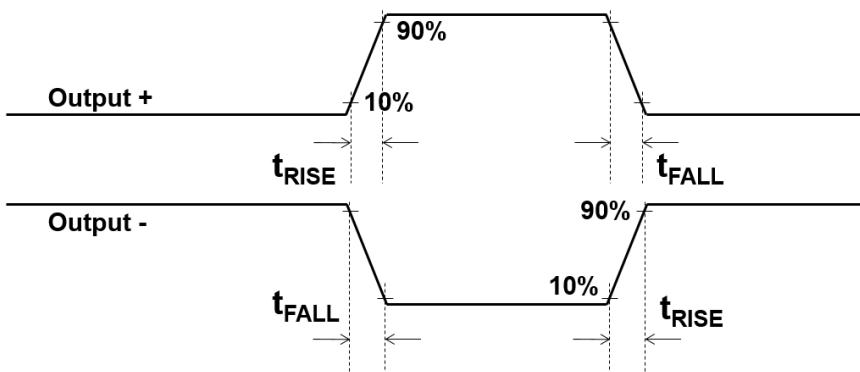


Figure 6: Rise Time and Fall Time of Differential Output Waveforms



## Differential Output Diagrams

Figure 7: Example of Typical Line-End Signal with  $C_{load} = 100 \text{ pF}$ ,  $VDD = 5\text{V}$ ,  $f_{OPERATE} = 5 \text{ MHz}$

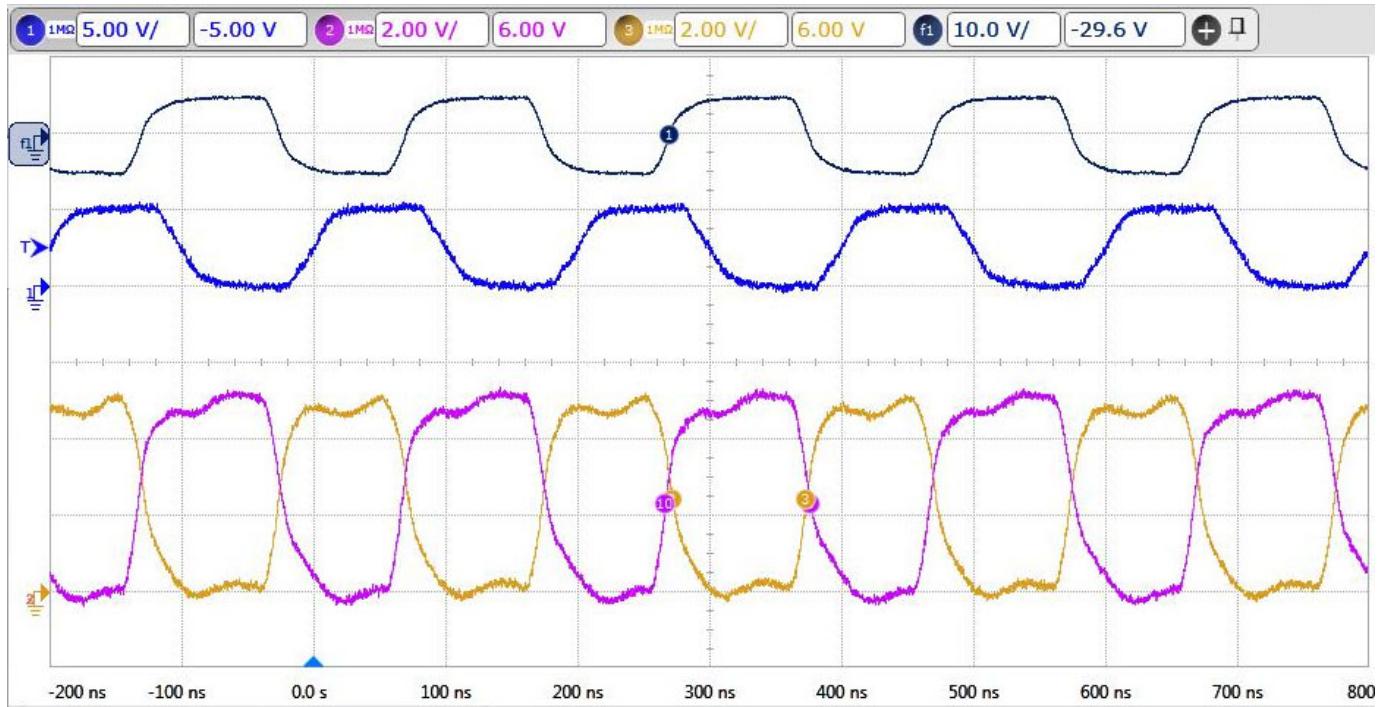
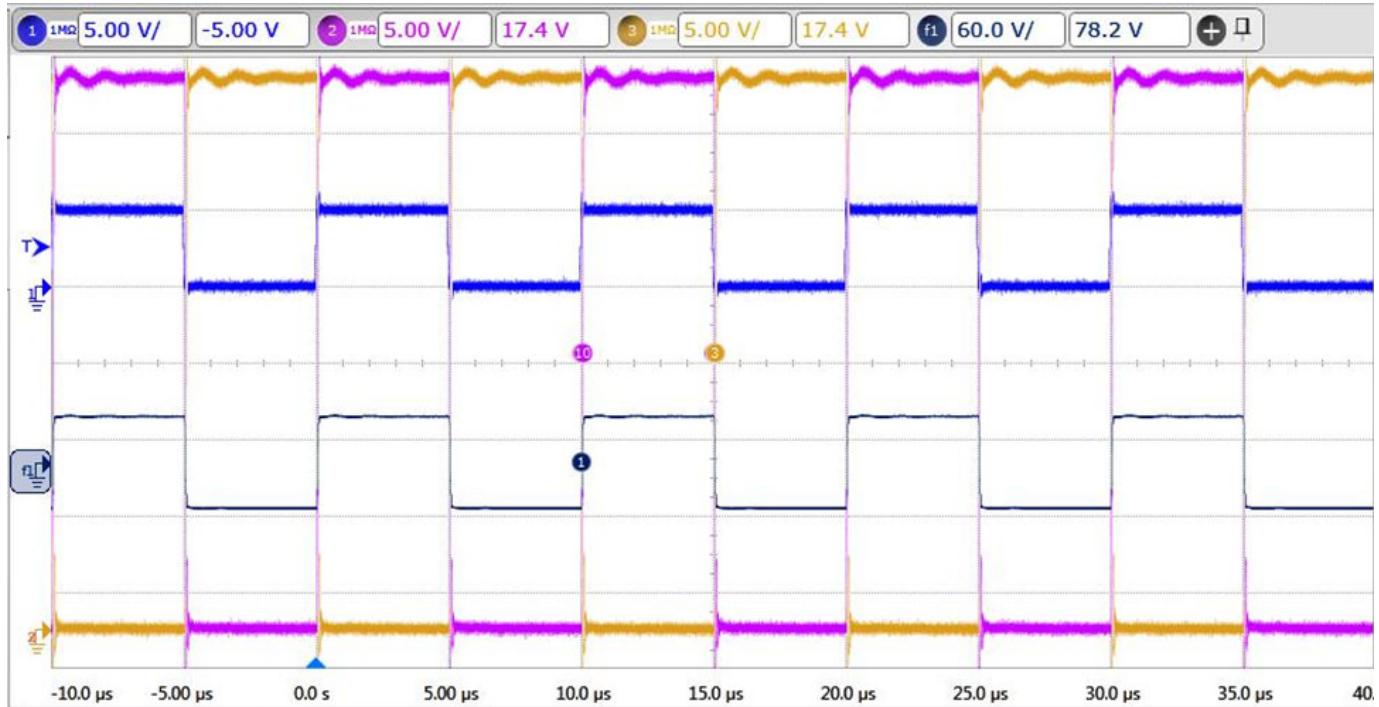


Figure 8: Example of Typical Line-End Signal with  $C_{load} = 100 \text{ pF}$ ,  $VDD = 36\text{V}$ ,  $f_{OPERATE} = 100 \text{ kHz}$

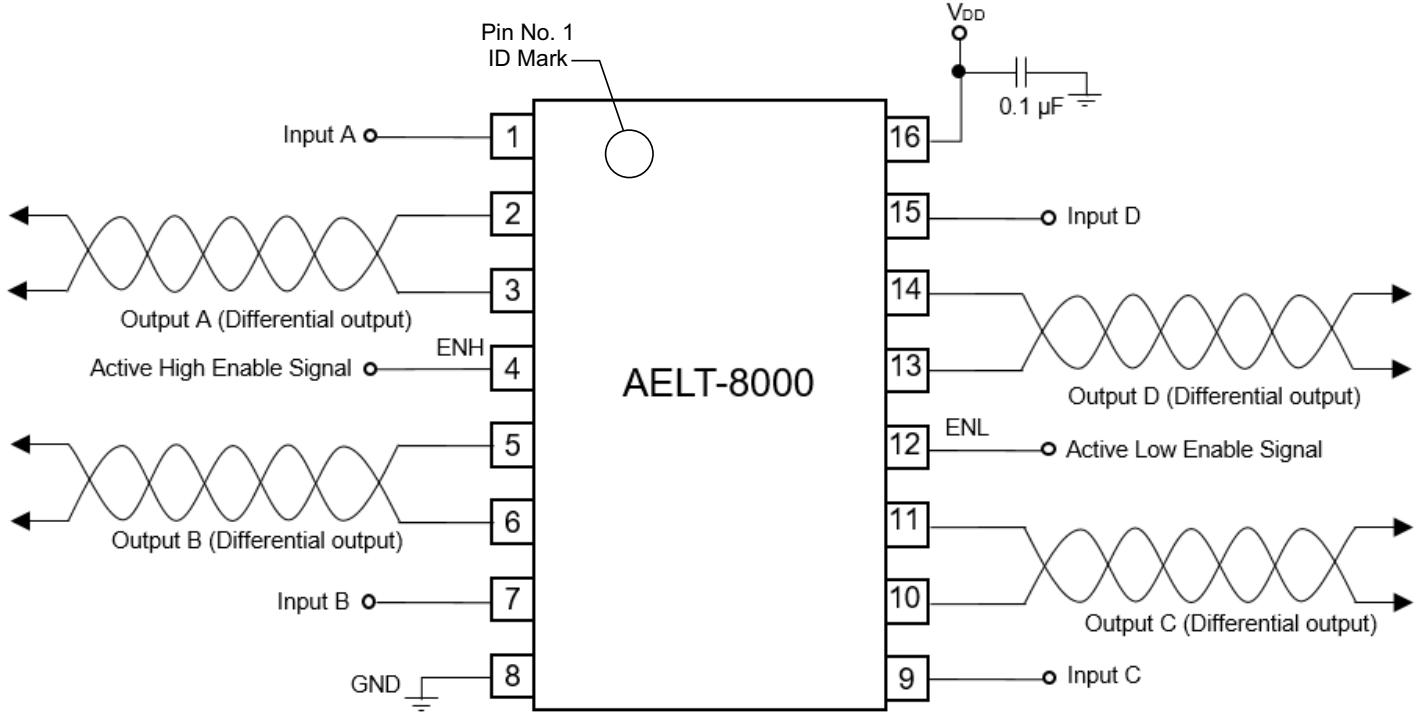


**NOTE:** Black line (Differential): Output+ – Output- (MATH); blue line: Input; purple line: Output+; yellow line: Output-

## Application Example

**Figure 9** shows an example of the differential output configuration with all channels used. This configuration includes the recommended use of a 0.1- $\mu$ F coupling capacitor at the VDD line.

**Figure 9: Example of Differential Line Driver Application**

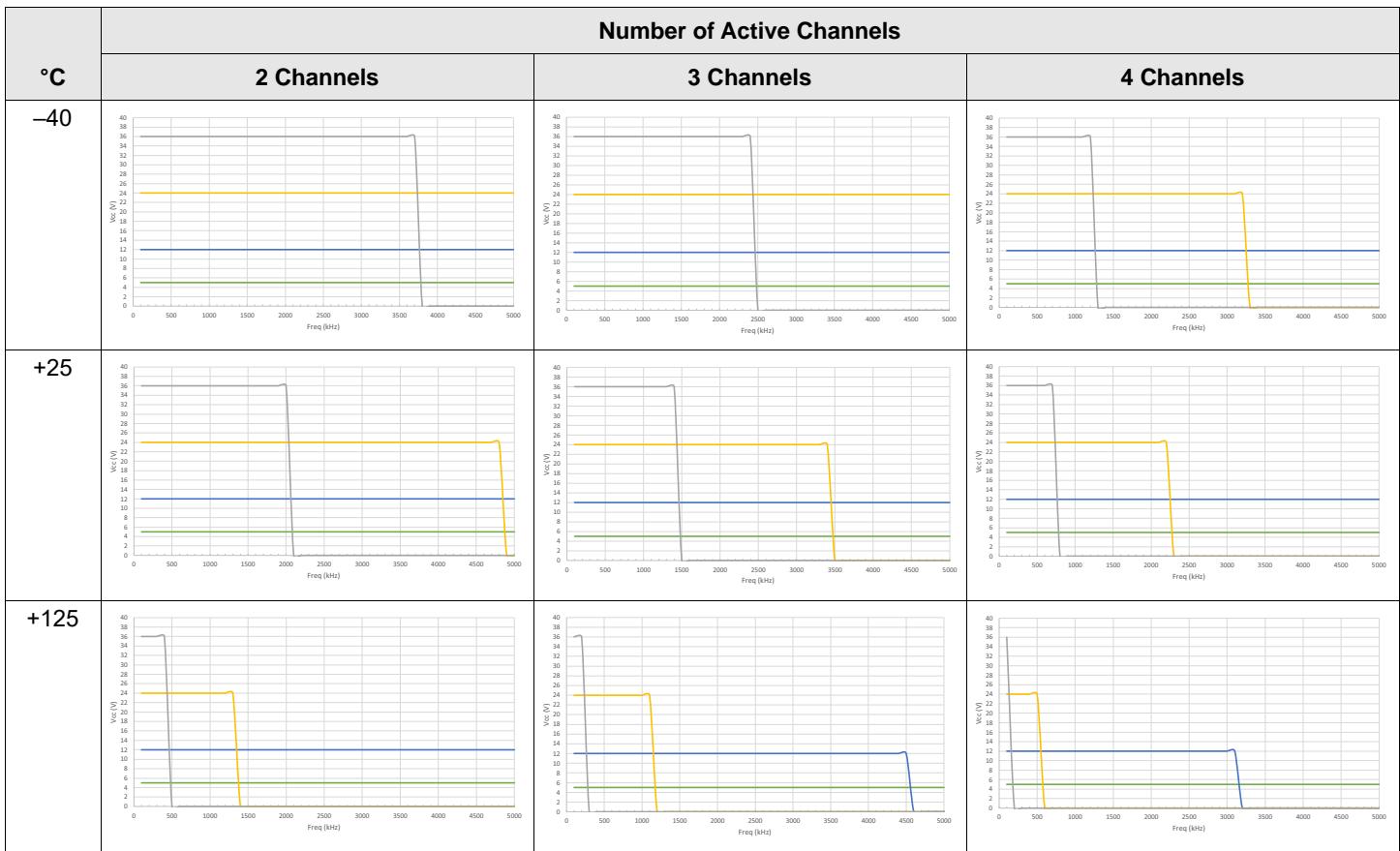


## Thermal Shutdown Characteristics for SOIC and TSSOP Packages

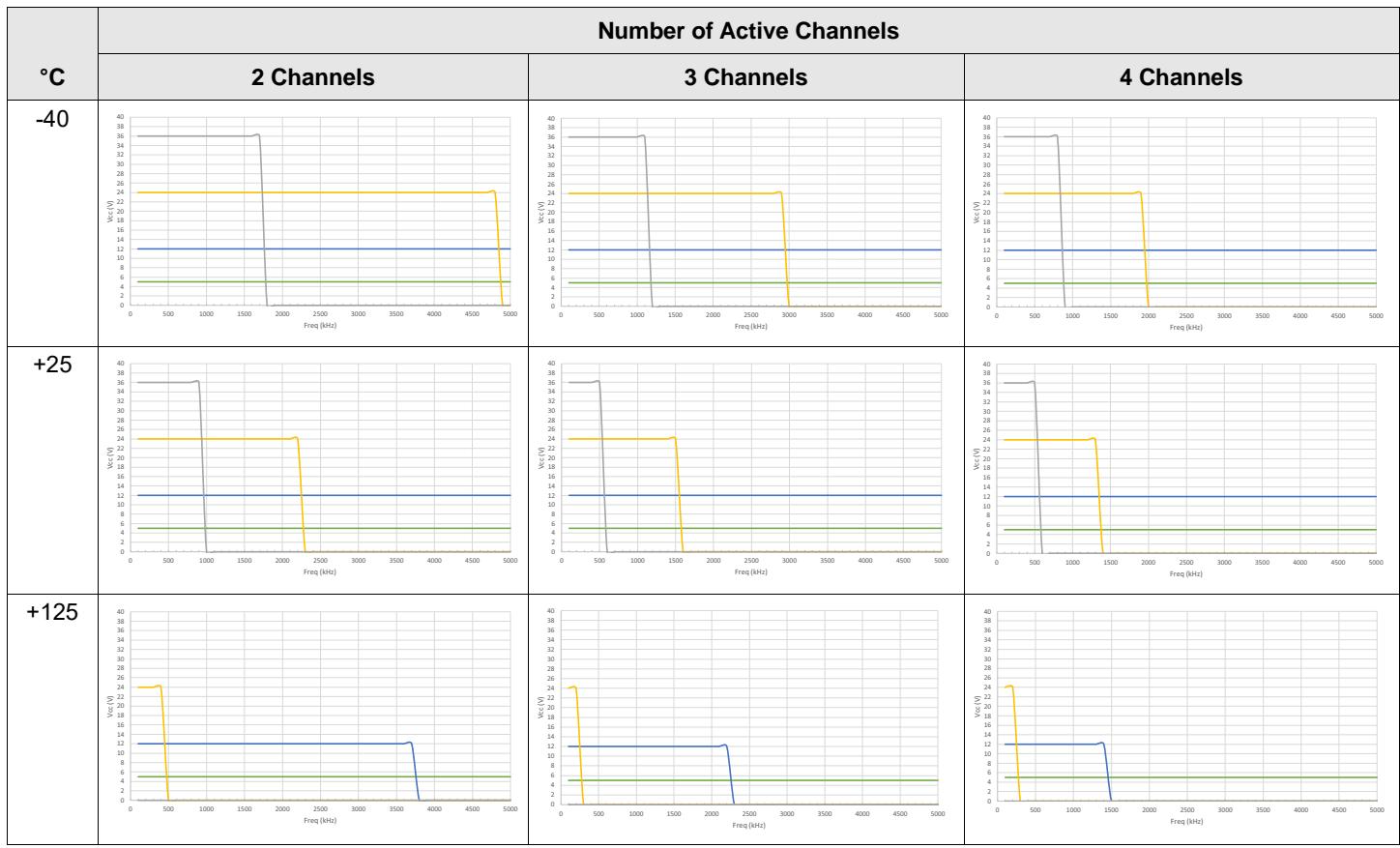
Thermal shutdown is influenced by the operating frequency, the number of active channels, and the ambient temperature. The SOIC package offers better thermal resistance compared to the TSSOP package. At high temperatures (for example, 125°C), it is recommended to use the SOIC package at 12V in order for the IC to function below a 3-MHz operating frequency. Meanwhile, it is recommended to use the TSSOP package at 12V for the an operating frequency below 1400 KHz.

**NOTE:** Condition: Each channel is loaded with 100 pF across an operating temperature range from -40°C to 125°C.

**Table 3: Graph Overview of the Thermal Shutdown State Across Voltage and Temperature (SOIC)**



— SOIC-5V   — SOIC-12V   — SOIC-24V   — SOIC-36V

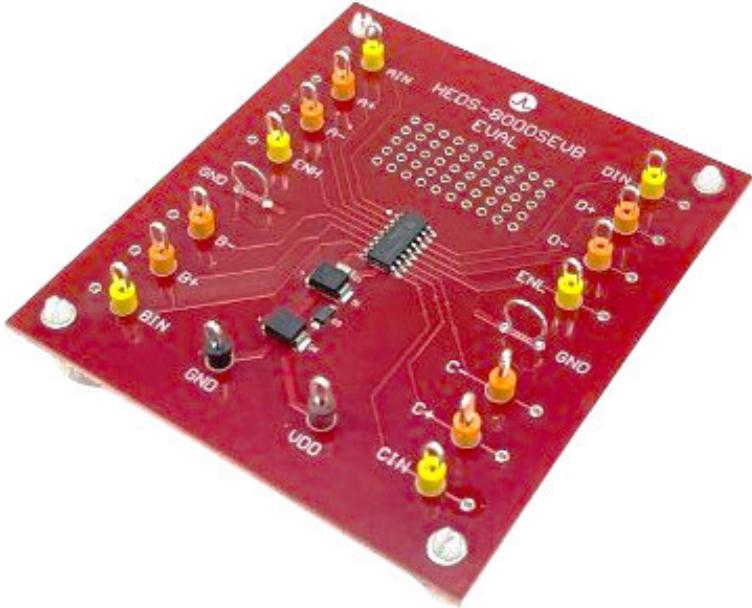
**Table 4: Graph Overview of the Thermal Shutdown State across Voltage and Temperature (TSSOP)**

— TSSOP-5V   — TSSOP-12V   — TSSOP-24V   — TSSOP-36V

## Evaluation Board

The evaluation board is designed to help users evaluate the performance and features of the AELT-8000 Line Driver IC. There are two types of evaluation boards: HEDS-8000SEVB (for SOIC-16) and HEDS-8000TEVB (for TSSOP-16). Each test point is connected to the IC's pins, and each evaluation board is prepopulated with a capacitor (which functions as a decoupling capacitor) and diodes (for reverse voltage protection and voltage clamping).

**Figure 10: AELT-8000 Evaluation Board with Components Prepopulated**



**Figure 11: AELT-8000 Evaluation Board Dimensions**

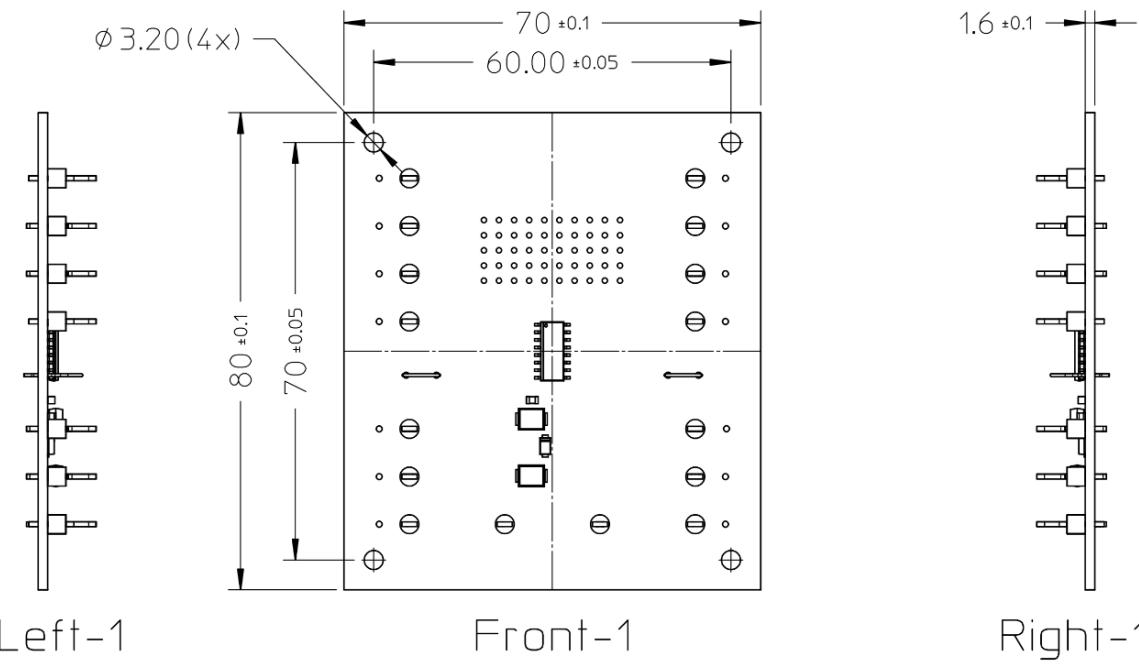
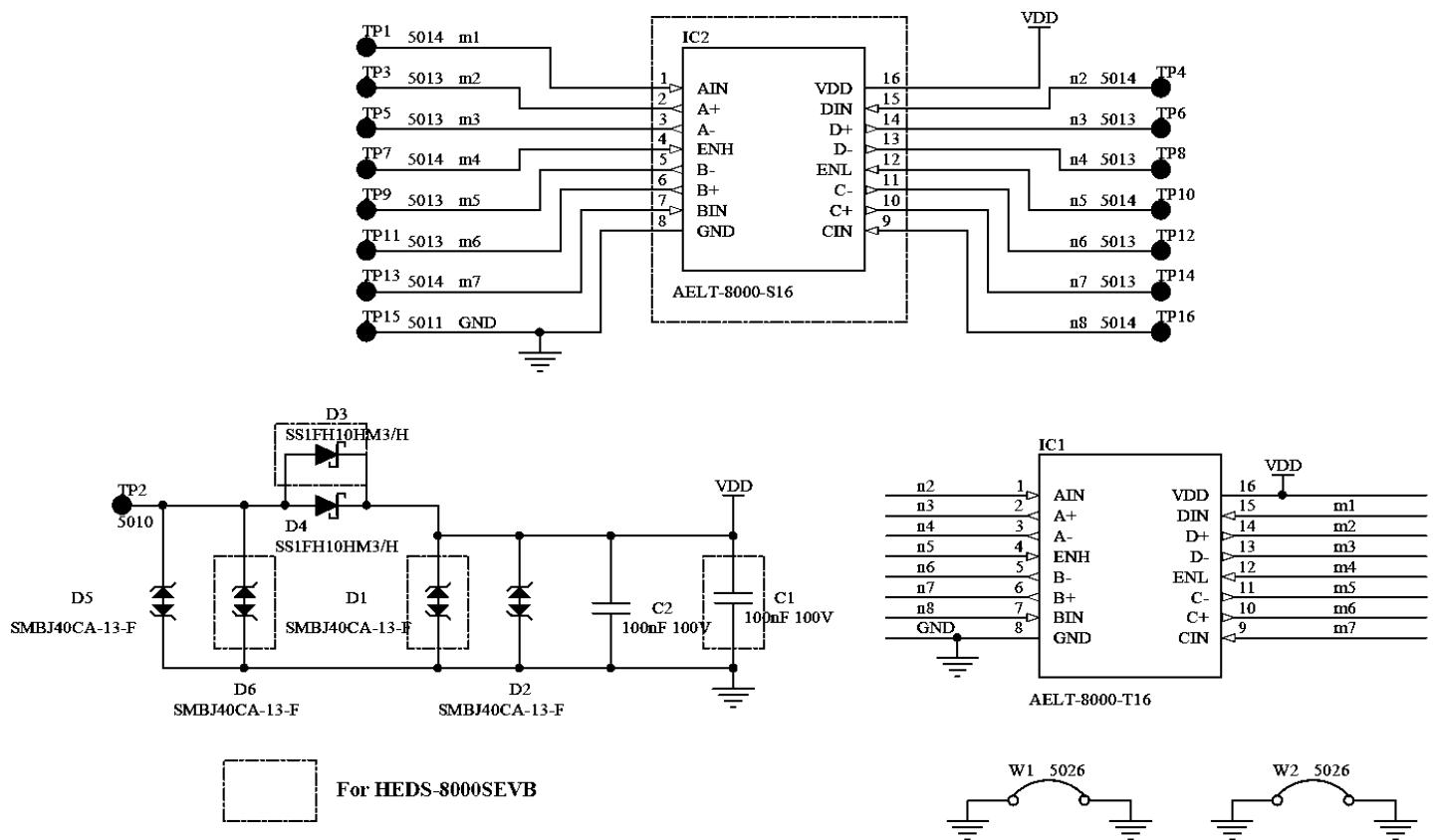


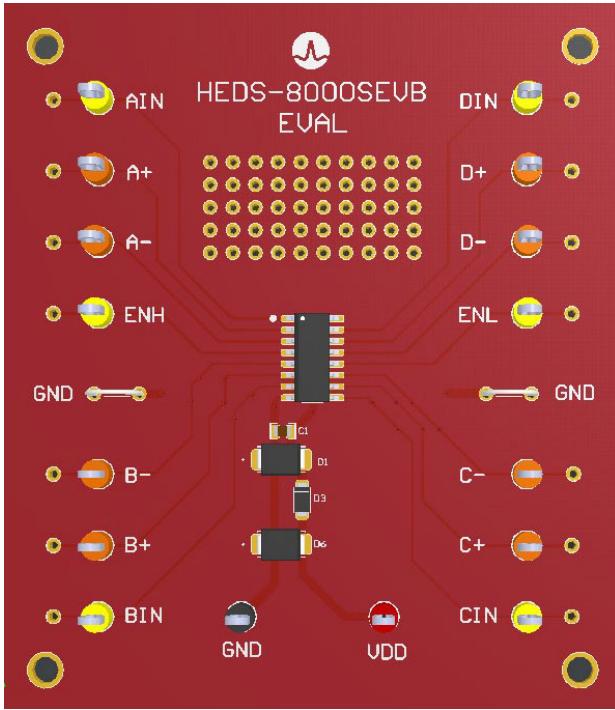
Figure 12: Evaluation Board Schematic



## HEDS-8000SEVB

This evaluation board is mounted with the AELT-8000-S16 (SOIC-16) IC component.

**Figure 13: HEDS-8000SEVB Evaluation Board**



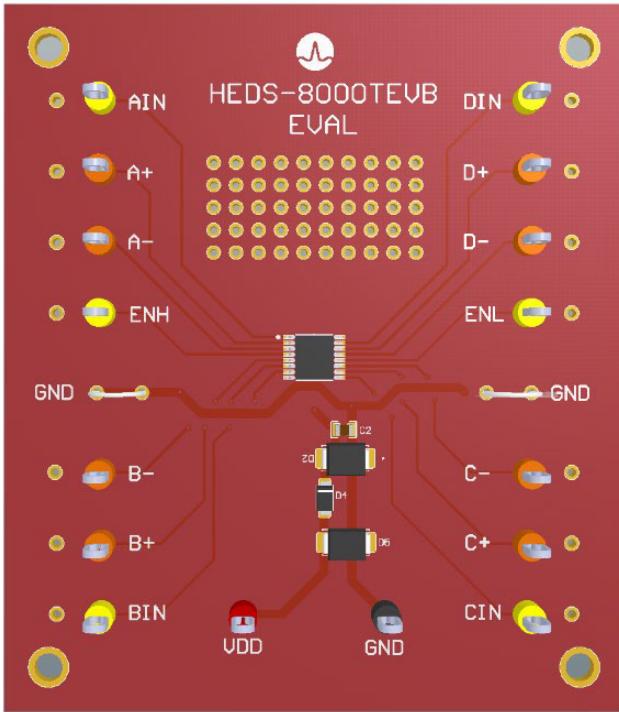
**Table 5: HEDS-8000SEVB List of Components**

Description	Designator	MPN	Quantity
Broadcom High Voltage Quad Differential Line Driver (SOIC-16)	IC2	AELT-8000-S16	1
Multilayer Ceramic Capacitors MLCC - SMD/SMT 50V .1uF X7R 0805 10% AEC-Q200	C1	KAM21BR71H104KM	1
ESD Protection Diodes / TVS Diodes 600W 40.0V	D1, D6	SMBJ40CA-13-F	2
Schottky Diodes & Rectifiers If 1A Vrrm 100V AEC-Q101 Qualified	D3	SS1FH10HM3/H	1
Keystone Test Plugs & Test Jacks YELLOW TEST POINT	TP1, TP4, TP7, TP10, TP13, TP16	5014	6
Keystone Test Plugs & Test Jacks RED TEST POINT	TP2	5010	1
Keystone Test Plugs & Test Jacks ORANGE TEST POINT	TP3, TP5, TP6, TP8, TP9, TP11, TP12, TP14	5013	8
Keystone Test Plugs & Test Jacks BLACK TEST POINT	TP15	5011	1
Keystone Test Plugs & Test Jacks THRU-HOLE MOUNT UNINSUL TEST POINT	W1, W2	5026	2
Standoffs & Spacers CB Spt, Mini, Natural, 5/16 in Spc	SO1, SO2, SO3, SO4	MSPM-5-01	4

## HEDS-8000TEVB

This evaluation board is mounted with the AELT-8000-T16 (TSSOP-16) IC component.

**Figure 14: HEDS-8000TEVB Evaluation Board**



**Table 6: HEDS-8000TEVB List of Components**

Description	Designator	MPN	Quantity
Broadcom High Voltage Quad Differential Line Driver (TSSOP-16)	IC1	AELT-8000-T16	1
Multilayer Ceramic Capacitors MLCC - SMD/SMT 50V .1uF X7R 0805 10% AEC-Q200	C2	KAM21BR71H104KM	1
ESD Protection Diodes / TVS Diodes 600W 40.0V	D2, D5	SMBJ40CA-13-F	2
Schottky Diodes & Rectifiers If 1A Vrrm 100V AEC-Q101 Qualified	D4	SS1FH10HM3/H	1
Keystone Test Plugs & Test Jacks YELLOW TEST POINT	TP1, TP4, TP7, TP10, TP13, TP16	5014	6
Keystone Test Plugs & Test Jacks RED TEST POINT	TP2	5010	1
Keystone Test Plugs & Test Jacks ORANGE TEST POINT	TP3, TP5, TP6, TP8, TP9, TP11, TP12, TP14	5013	8
Keystone Test Plugs & Test Jacks BLACK TEST POINT	TP15	5011	1
Keystone Test Plugs & Test Jacks THRU-HOLE MOUNT UNINSUL TEST POINT	W1, W2	5026	2
Standoffs & Spacers CB Spt, Mini, Natural, 5/16 in Spc	SO1, SO2, SO3, SO4	MSPM-5-01	4

## Moisture Sensitivity Level

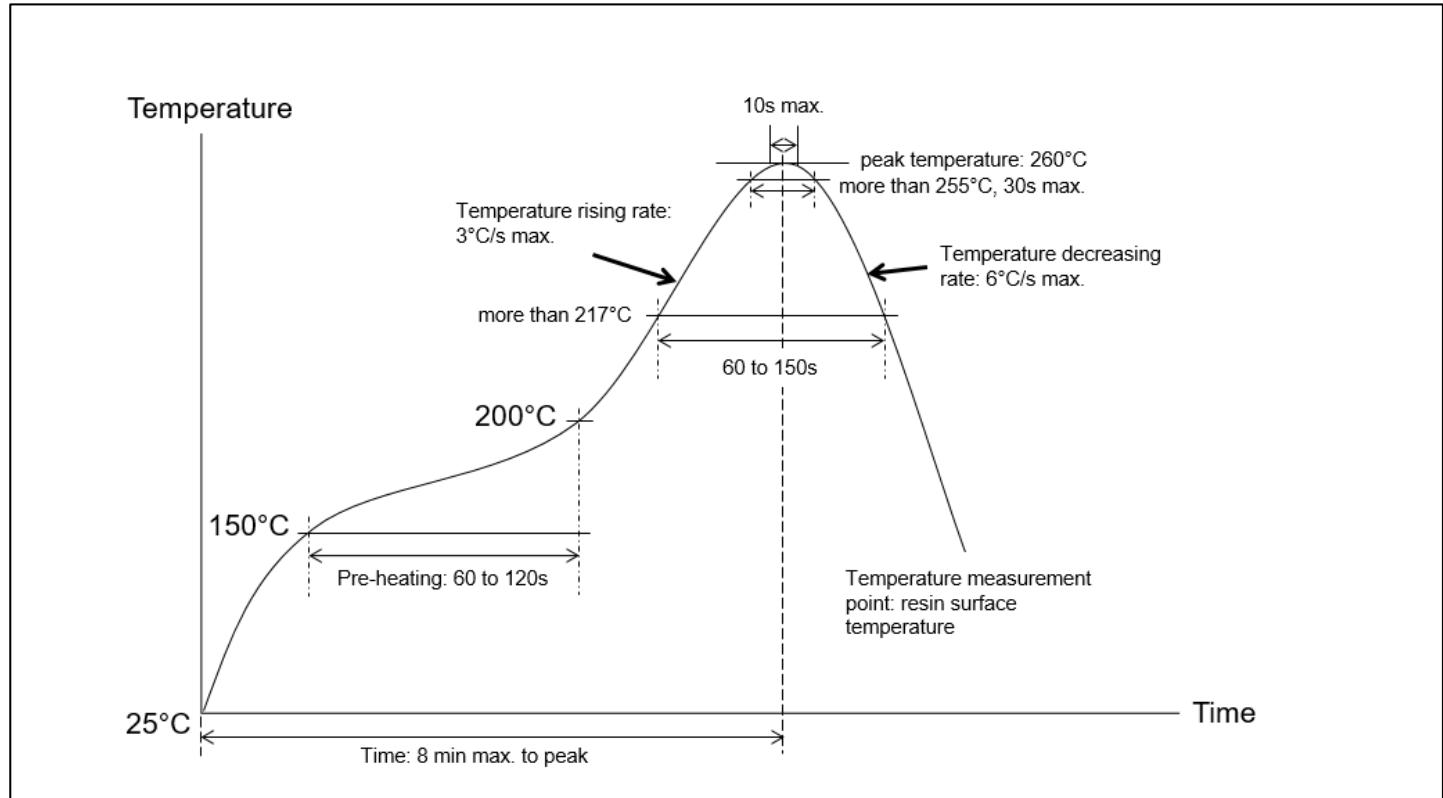
The AELT-8000 is specified to MSL 1.

### CAUTION!

- Keep the components in the original packaging to protect them from contaminants.
- Store the components in a temperature-controlled and humidity-controlled environment.

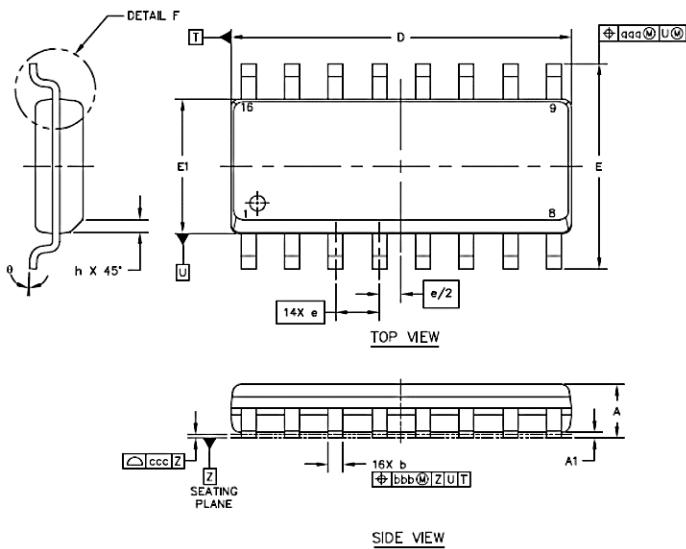
## Recommended Lead-Free Reflow Soldering Temperature Profile

Figure 15: Typical Lead-Free Reflow Soldering Profile



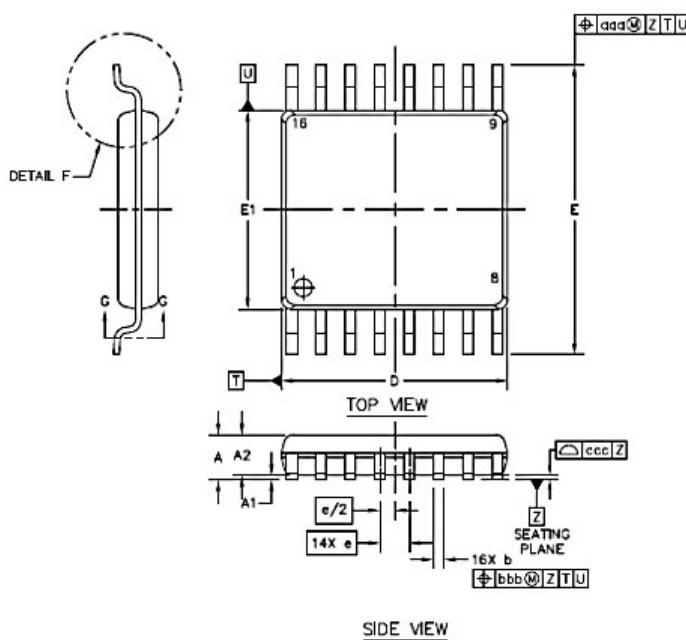
## Package Outline and Dimensions

Figure 16: AELT-8000-S16, 16-Pin SOIC Dimensions (mm)



Parameter	Symbol	Min.	Nom.	Max.
Total Thickness	A	1.35	—	1.75
Standoff	A1	0.10	—	0.25
Lead Width	b	0.35	—	0.49
L/F Thickness	c	0.19	—	0.25
Body Size	D	9.80	—	10.00
	E1	3.80	—	4.00
	E	5.80	—	6.20
Lead Pitch	e	1.27 BSC		
	L	0.40	—	1.25
	h	0.25	—	0.50
	$\theta$	0°	—	7°
Lead Edge Offset	aaa	0.25		
Lead Offset	bbb	0.25		
Coplanarity	ccc	0.10		

Figure 17: AELT-8000-T16, 16-Pin TSSOP Dimensions (mm)



Parameter	Symbol	Min.	Nom.	Max.
Total Thickness	A	—	—	1.10
Standoff	A1	0.05	—	0.15
Mold Thickness	A2	0.85	0.90	0.95
Lead Width (Plating)	b	0.19	—	0.30
Lead Width	b1	0.19	0.22	0.25
L/F Thickness (Plating)	c	0.09	—	0.20
L/F Thickness	c1	0.09	—	0.16
Body Size	X	D	4.90	5
	Y	E1	4.30	4.40
		E	6.20	6.40
Lead Pitch	e	0.65 BSC		
	L	0.45	0.6	0.75
Footprint	L1	1 REF		
	$\theta 1$	0°	—	8°
	$\theta 2$	14° (typical)		
	$\theta 3$	14° (typical)		
	R1	0.09	—	—
	R2	0.09	—	—
	S	0.20	—	—
Lead Edge Offset	aaa	0.20		
Lead Offset	bbb	0.10		
Coplanarity	ccc	0.10		
Mold Flatness	ddd	0.05		

## Recommended Land Pattern for PCB Layout

Figure 18: Recommended Land Pattern for SOIC Package (in mm)

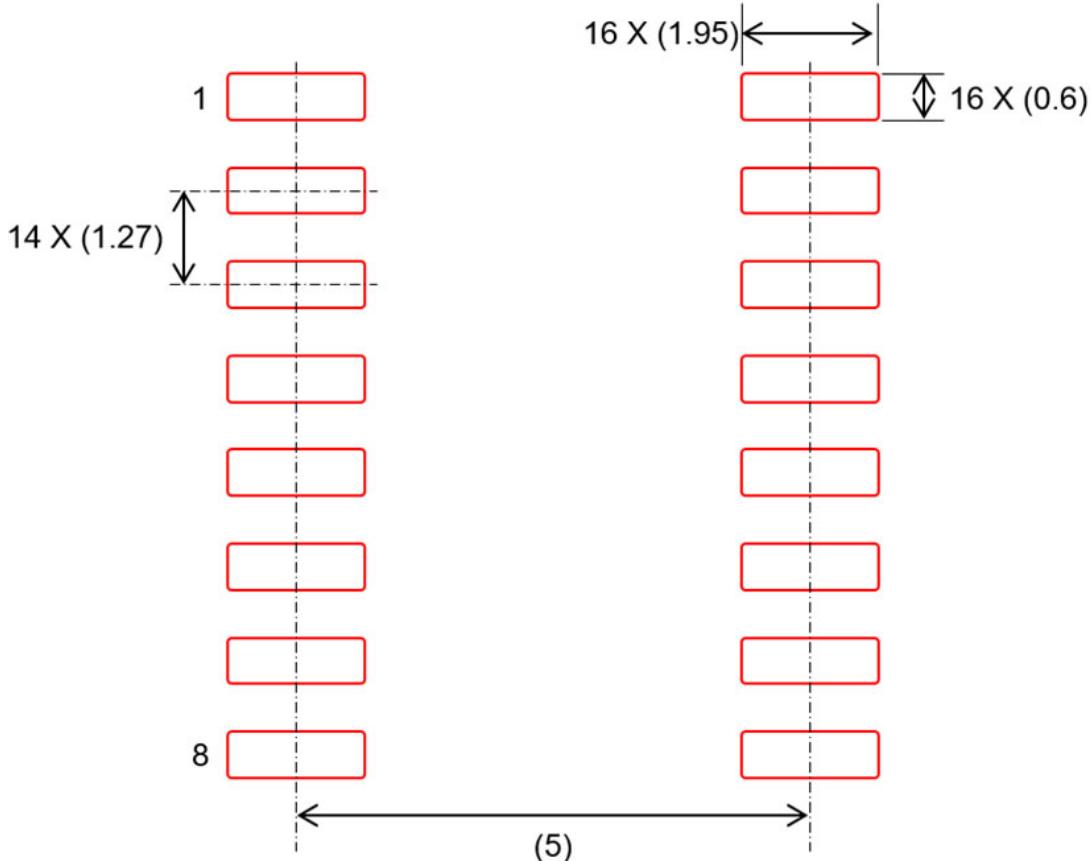
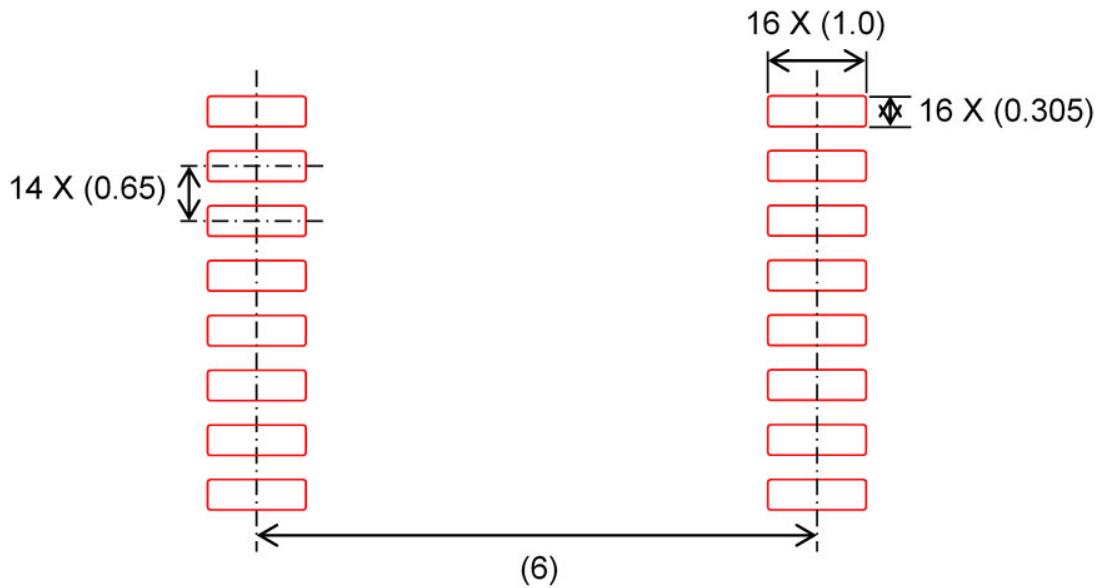
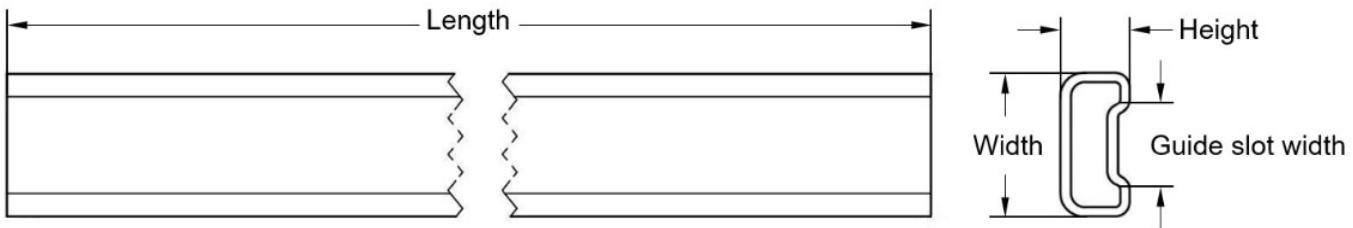


Figure 19: Recommended Land Pattern for TSSOP Package (in mm)



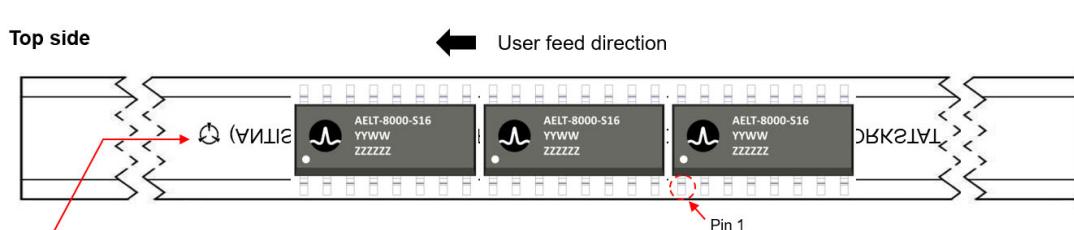
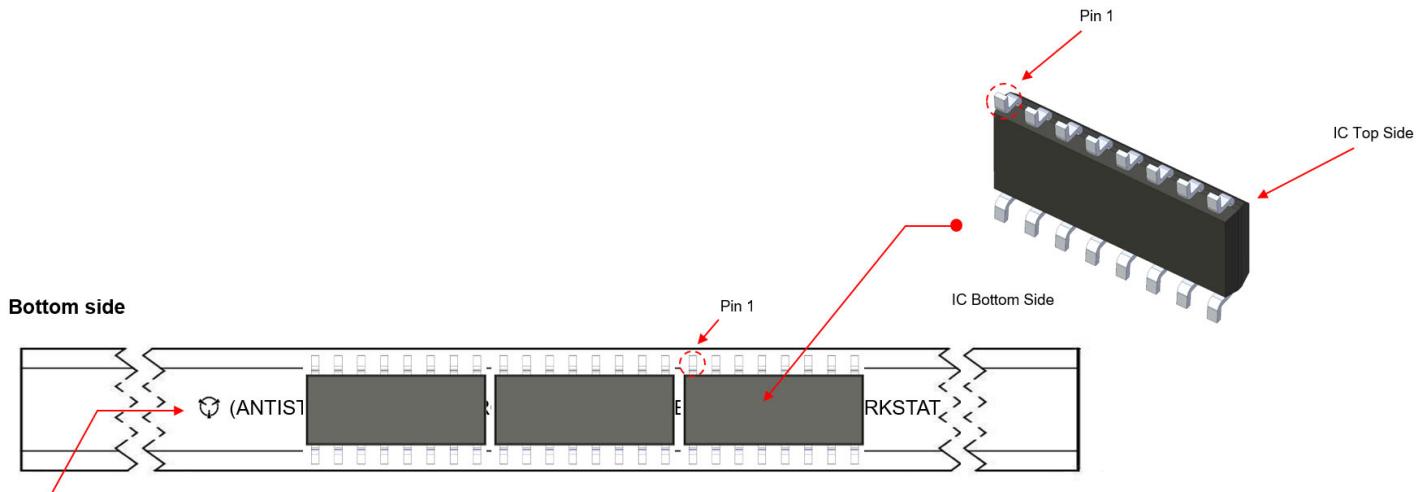
## Tube Information



Package Type	Length (mm)	Width (mm)	Height (mm)	Guide Slot Width (mm)
SOIC	508	7.68	3.81	4.32
TSSOP	508	7.80	3.15	4.06

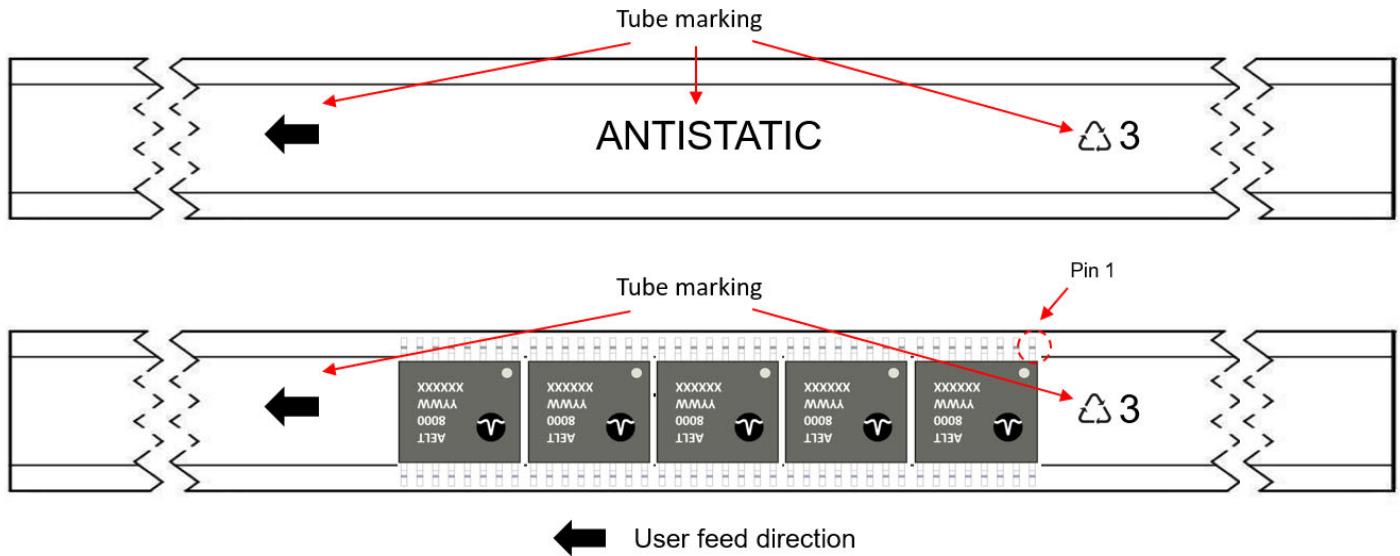
**NOTE:** All dimensions are nominal.

### SOIC Package Tube



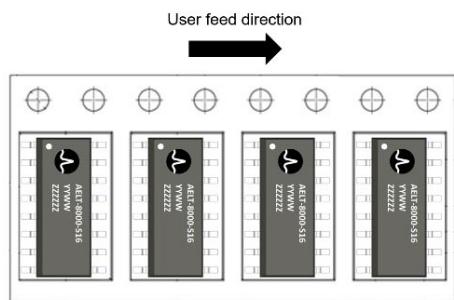
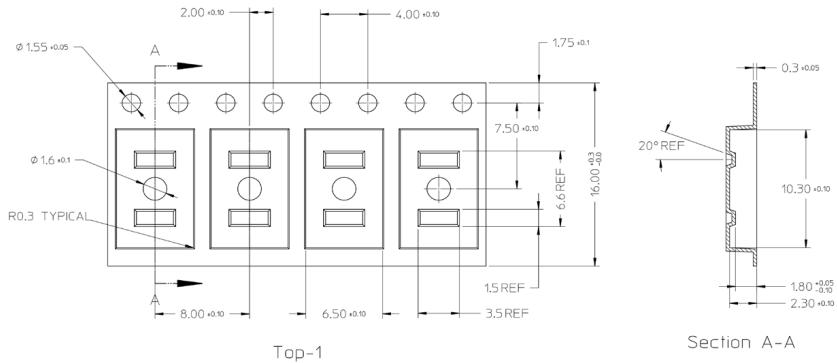
Tube marking upside down: (ANTISTAT) OPEN AT APPROVED FIELD FORCE PROTECTIVE WORKSTATION XXXX XXXXXXXXXX

## TSSOP Package Tube

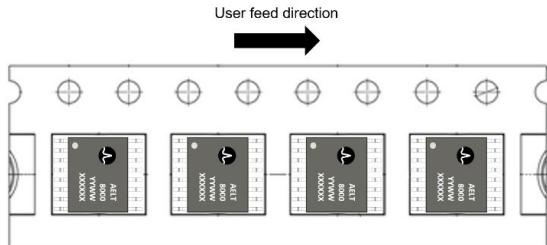
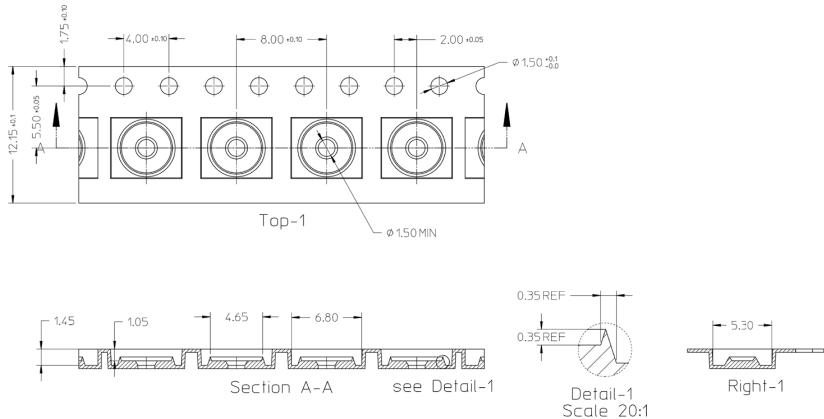


## Tape and Reel Information

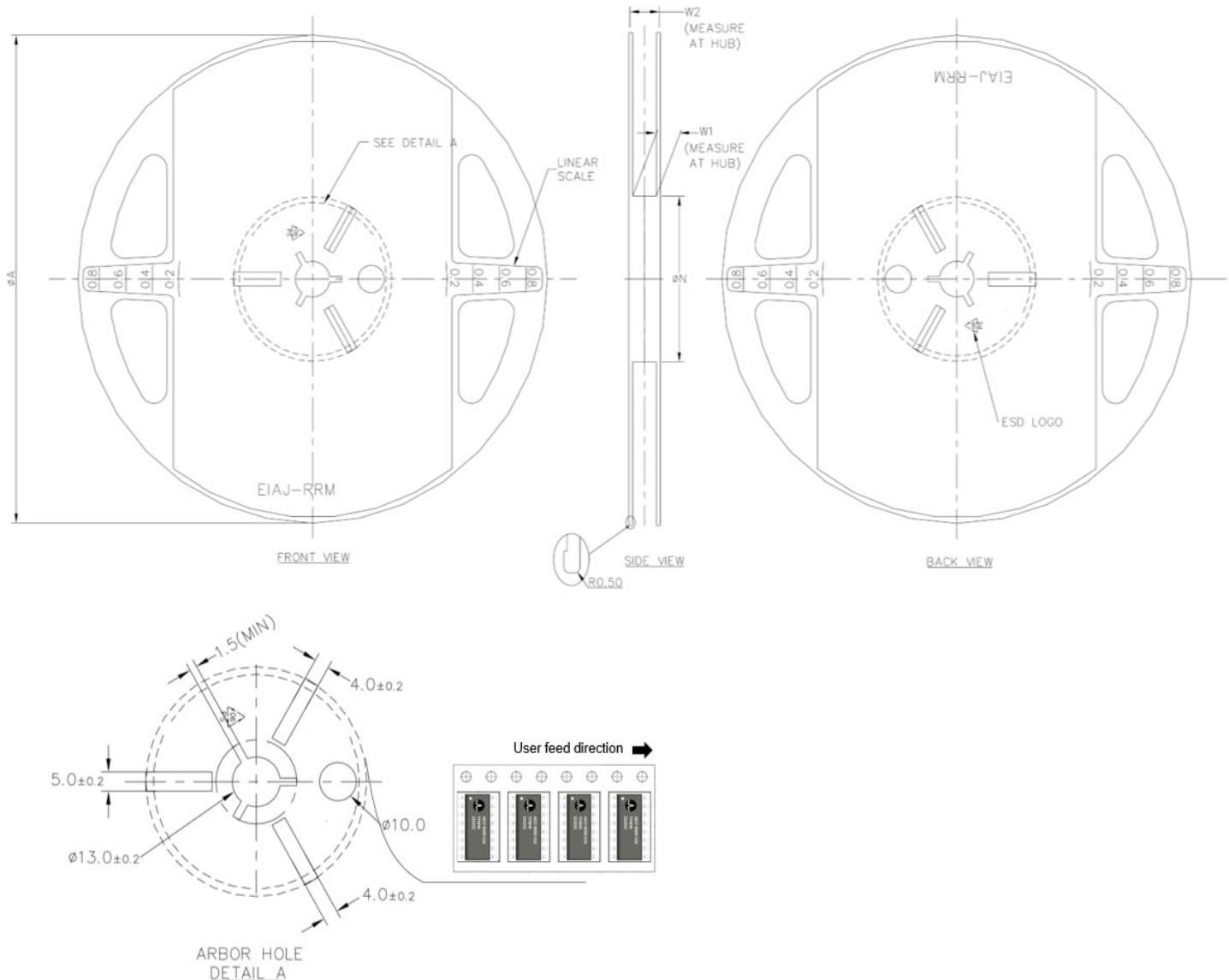
### SOIC Package Tape



### TSSOP Package Tape



## SOIC and TSSOP Reel



Customer Specifications							
Device	Package	Qty	Tape Width	ØA ±2.0	ØN ±2.0	W1 +2.0 -0.0	W2 ±1.0
AELT-8000-T102	TSSOP	100	12MM	180.0	60.0	12.4	15.4
AELT-8000-T100	TSSOP	1000	12MM	180.0	60.0	12.4	15.4
AELT-8000-S102	SOIC	100	16MM	180.0	60.0	16.4	19.4
AELT-8000-S100	SOIC	1000	16MM	330.0	60.0	16.4	19.4

## Product Ordering Information

**Table 7: Ordering Information**

Ordering Part No.	Product Description	Package Size	Delivery Form
AELT-8000-S16	High Voltage Quad Differential Line Driver	SOIC-16, 4 mm x 10 mm	Tube, 48 pieces
AELT-8000-S100	High Voltage Quad Differential Line Driver	SOIC-16, 4 mm x 10 mm	Tape and Reel, 1000 pieces
AELT-8000-S102	High Voltage Quad Differential Line Driver	SOIC-16, 4 mm x 10 mm	Tape and Reel, 100 pieces
AELT-8000-T16	High Voltage Quad Differential Line Driver	TSSOP-16, 4.4 mm x 5 mm	Tube, 96 pieces
AELT-8000-T100	High Voltage Quad Differential Line Driver	TSSOP-16, 4.4 mm x 5 mm	Tape and Reel, 1000 pieces
AELT-8000-T102	High Voltage Quad Differential Line Driver	TSSOP-16, 4.4 mm x 5 mm	Tape and Reel, 100 pieces
HEDS-8000SEVB	AELT-8000 (SOIC-16) Evaluation Board	—	1 piece of SOIC evaluation board
HEDS-8000TEVB	AELT-8000 (TSSOP-16) Evaluation Board	—	1 piece of TSSOP evaluation board

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