Application Note

AEAT-9988M

Magnetic Encoder IC: High-Resolution 23-Bit Absolute Incremental Encoder

Description

The Broadcom® AEAT-9988M is an angular magnetic rotary sensor that provides accurate angular measurement over a full 360 degrees of rotation. It is a versatile solution capable of supporting a broad range of applications with its robust architecture to measure and deliver both absolute and incremental signals.

This sophisticated system uses integrated Hall sensor elements with complex analog and digital signal processing within a single device.

A dual-track magnet generates the necessary magnetic fields by rotating perpendicularly. A wide range of selection is available on the magnet ring sizes, up to a 60-mm outer diameter.

The absolute angle measurement provides an instant indication of the magnet's angular position with a selectable and reprogrammable resolution from 16 bits to 23 bits. Once the resolution is selected, the absolute position data is represented in digital form and can be accessed via standard communication protocols such as SSI, SPI, BiSS-C, or RS-485.

The AEAT-9988M also has a built-in multi-turn counter with battery backup power-off mode operation. The multi-turn resolution is programmable from 10 bits to 16 bits.

Users can choose to receive the absolute angle position in PWM-encoded output signals. The incremental positions are transmitted on ABI and UVW signals with a wide user-configurable resolution from 1 CPR to 65,536 CPR of ABI signals and pole pairs from 1 to 64 pole pairs (2 to 128 poles) for UVW commutation signals.

Operation Mode

The AEAT-9988M features two operational modes: normal operation mode and configuration mode.

Normal Operation Mode

Normal mode is the normal operating mode of the chip. The absolute output (16-bit to 23-bit absolute position data) is available through the serial protocol pin (Port A).

Configuration Mode

The AEAT-9988M has a built-in memory for multiple-time programming (MTP).

Programming of the AEAT-9988M can be performed with the HEDS-9988PRGEVB programming kit or any tester or programmer device using the guidelines provided.

Absolute and Incremental Programming

The absolute resolution can be set to 16, 17, 18, 19, 20, 21, 22, or 23 bits. For incremental selection, ABI or UVW can be selected by following the instructions in the following sections. The PWM output is available as well.

The shadow registers are programmable using the SPI, BiSS-C, and RS-485 protocols. Writing specific commands to specific addresses of the internal registers programs shadow register values to memory. The memory can be programmed multiple times.

Memory Map

The AEAT-9988M uses nonvolatile EEPROM as shown in the tables that follow. The memory is separated into 12 pages with 8 bits per address.

Nonvolatile Register (EEPROM)

MTP shadow registers are volatile registers that are loaded with corresponding MTP values after power-on.

All bits are in LOCK mode by default after power-on. To enter UNLOCK mode, write 0xAB to address 0x00.

In UNLOCK mode, you may write to any registers. Values written will remain until power-off.

The UNLOCK state is maintained until the power supply is turned off or any value (except 0xAB) is written to address 0x00.

MTP Shadow Registers

MTP shadow registers are volatile (upon power-up, the value are reloaded from EEPROM) and are not automatically written to EEPROM.

To write MTP shadow registers values to EEPROM (nonvolatile) memory, see EEPROM Programming.

The MTP shadow registers will be from address 0x00 to address 0x7E.

Customer Configuration Registers

The following registers are available for users to store information and configure the encoder as required.

Table 1: Customer Configuration Registers – Page 7

Addr (Hex)	Bit							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	track_cnt[7:0]							
0x01	DIR	MT_Select[2:0]			N/A	ST_Select[2:0]		
0x02	Temp Max Limit Offset[7:0]							
0x03	Temp Offset[7:0]							
0x04	Temperature Limit[7:0]							
0x05	Temperature Output[7:0]							
0x06	ST_ZR[23:16]							
0x07	ST_ZR[15:8]							
0x08	ST_ZR[7:0]							
0x09	index_mult[7:0]							
0x0A	N/A	I_Polarity	Iwidth_Select[1:0]		Iphase_Select[1:0]		abi_ini	ABI_CPR[16]
0x0B	ABI_CPR[15:8]							
0x0C	ABI_CPR[7:0]							
0x0D	uvw_ini	UVW_Select[6:0]						
0x0E	pwm_ini	N/A			pwm_mode	pwm_select[3:0]		
0x0F	SE_Slew_SEL[1:0]		N/A		LD_Slew_SEL[1:0]		LD_Drive_SEL[1:0]	
0x10	GPIO0_cfg[7:0]							
0x11	GPIO1_cfg[7:0]							
0x12	GPIO2_cfg[7:0]							
0x13	gpio_abi_stat	eep_srst	eep_size [2:0]			eep_psize[2:0]		
0x14	SP Magnetic High Threshold[6:0]							N/A
0x15	SP Magnetic Low Threshold[6:0]							N/A
0x16	MP Magnetic High Threshold[6:0]							N/A
0x17	MP Magnetic Low Threshold[6:0]							N/A
0x18	digital filter[7:0]							
0x19	cal filter[7:0]							
0x1A	hys2_on	arc_en	acc2.1_en	acc2.2_en	sleep[3:0]			
0x1B	RS485 encoder ID[7:0]							
0x1C	RS485 Setting1[4:0]					RS485_Enc_Addr[2:0]		
0x1D	RS485 Setting2[7:0]							
0x1E	ssi2_ring	ssi3_config	ssi_temp	ssi_alm	ssi_crc	ssi2_to_flex	alm_sel	N/A
0x1F	spi4_cfg	N/A	spi4_crc_init[1:0]		N/A			
0x20	Alarm Enable[31:0]							
0x21								
0x22								
0x23								

Table 1: Customer Configuration Registers – Page 7 (Continued)

Addr (Hex)	Bit 7	6	5	4	3	2	1	0
0x24	Alarm Latch Enable[31:0]							
0x25								
0x26								
0x27								
0x28	Warning Mask[31:0]							
0x29								
0x2A								
0x2B								
0x2C	Error Mask[31:0]							
0x2D								
0x2E								
0x2F								
0x30	sync_offset							
0x31	N/A	Pole_length[2:0]			h1_sign	sync_dir	dpc2_dir	N/A
0x32	N/A				hysterisis_setting[3:0]			
0x35	zero_latency	N/A				fixed_delay[10:8]		
0x36	fixed_delay[7:0]							
0x7F	Page Selection							
0x44	BiSS Map 0x41 [7:0]							
0x45	BiSS Map 0x42 to 0x43 [15:0]							
0x46								
0x47	BiSS Map 0x44 to 0x47 [31:0]							
0x48								
0x49								
0x4A								
0x4B	BiSS Map 0x4B [7:0]							
0x4C	BiSS Map 0x4C [7:0]							
0x4D	BiSS Map 0x4D [7:0]							
.....	.....							
0x67	BiSS Map 0x67 [7:0]							
0x76	BiSS Map 0x78 to 0x7D [47:0]							
.....								
0x7B								
0x7C	BiSS Map 0x7E [15:8]							
0x7D	BiSS Map 0x7F [7:0]							

Table 2: Customer Configuration Registers – Page 7 Descriptions

Address	Bit(s)	Registers	Description
0x00	[7:0]	track_cnt	Magnet multi-pole pair count. 0: 1 pole pair 1: 2 pole pair : 7: 8 pole pair (default) : 127: 128 pole pair
0x01	[7]	DIR	Counting direction selection. 0: Counter clockwise 1: Clockwise (default)
	[6:4]	MT_Select	Multi-turn output resolution. 0: OFF 1: 10-bit : 7: 16-bit (default)
	[2:0]	ST_Select	Absolute output resolution selection. 0: 16-bit 1: 17-bit : 7: 23-bit (default)
0x02	[7:0]	Temp Max Limit Offset	See Temperature Sensor for further explanation. Default value: Temperature max. limit offset: 0 (decimal) = 0°C Temperature offset: 0 (decimal) = 0°C Temperature limit: 125 (decimal) = 125°C
0x03	[7:0]	Temperature Offset	
0x04	[7:0]	Temperature Limit	
0x05	[7:0]	Temperature Output	
0x06	[7:0]	ST_ZR	Single-turn zero rest value via register: ■ ST_ZR[23:16]: MSB bit 23 to bit 16 of absolute single turn ■ ST_ZR[15:8]: Bit 15 to bit 8 of absolute single turn ■ ST_ZR[7:0]: LSB bit 7 to bit 0 of absolute single turn
0x07	[7:0]		
0x08	[7:0]		
0x09	[7:0]	index_mult	Index multiplier for number of index pulse per revolution. 0: 1 index pulse per revolution (default) 1: 2 index pulse per revolution 2: 3 index pulse per revolution : 255: 256 index pulse per revolution

Table 2: Customer Configuration Registers – Page 7 Descriptions (Continued)

Address	Bit(s)	Registers	Description
0x0A	[6]	I_Polarity	ABI index polarity. 0: Index pulse is 1 (default) 1: Index pulse is 0
	[5:4]	Iwidth_Select	Index width selection. 00: 90 e° (default) 01: 180 e° 10: 270 e° 11: 360 e°
	[3:2]	Iphase_Select	Index location within incremental period selection. 00: A low B low (default) 01: A low B high 10: A high B high 11: A high B low
	[1]	abi_ini	ABI output off state. 0: Low (default) 1: High **NOTE:** Enable when ABI_CPR is 0.
0x0A	[0]	ABI_CPR	ABI count per revolution (CPR) setting. Incremental resolution selection (0 = Off; On range: 1 to 65536 or 2^{16} CPR) 0-0000-0000-0000-0000'b: 0 CPR (Off) 0-0000-0000-0000-0001'b: 1 CPR : 0-0000-0100-0000-0000'b: 1024 CPR : 0-0001-0000-0000-0000'b: 4096 CPR (default) : 1-0000-0000-0000-0000'b: 65536 or 2^{16} CPR > 1-0000-0000-0000-0000'b: 65536 or 2^{16} CPR
0x0B	[7:0]		
0x0C	[7:0]		
0x0D	[7]	uvw_ini	UVW output off state. 0: Low (default) 1: High
	[6:0]	UVW_Select	UVW number of pole pair setting. 0x00: 0 pole pair 0x01: 1 pole pair 0x02: 2 pole pair 0x03: 3 pole pair (default) : 0x40: 64 pole pair > 0x7F: 64 pole pair

Table 2: Customer Configuration Registers – Page 7 Descriptions (Continued)

Address	Bit(s)	Registers	Description
0x0E	[7]	pwm_ini	PWM output off state. 0: Low (default) 1: High
	[3]	pwm_mode	PWM output mode. 0: Fixed clock 1: Fixed period (default)
	[2:0]	pwm_select	PWM resolution. 000: 10 bits 001: 11 bits 010: 12 bits (default) 011: 13 bits 100: 14 bits > 100: 14 bits
0x0F	[7:6]	SE_Slew_SEL	Single-ended slew rate. 00: Very slow (default) 01: Slow 10: Fast 11: Very fast
	[3:2]	LD_Slew_SEL	Line driver slew rate. 00: Very slow (default) 01: Slow 10: Fast 11: Very fast
	[1:0]	LD_Drive_SEL	Differential line driver drivability control. 00: 25% (default) 01: 50% 10: 75% 11: 100%
0x10	[7:0]	GPIO0_cfg	See Programmable GPIO for further explanation. GPIO0 = 1 / ST ZR Cal (default) GPIO1 = 0 / N/A (default) GPIO2 = 0 / N/A (default)
0x11	[7:0]	GPIO1_cfg	
0x12	[7:0]	GPIO2_cfg	

Table 2: Customer Configuration Registers – Page 7 Descriptions (Continued)

Address	Bit(s)	Registers	Description
0x13	[7]	gpio_abi_stat	Programmable GPIO – ABI output function. When using GPIO to perform calibration. 0: Calibration status not reflect on ABI output (default) 1: Calibration status reflect on ABI output
	[6]	eep_srst	External EEPROM – soft reset. 0: Disable automatic soft reset on external EEPROM soft reset during power-up (default) 1: Enable automatic soft reset on external EEPROM soft reset during power-up
	[5:3]	eep_size	External EEPROM – memory size. 000: 1 kB (default) 001: 2 kB 010: 4 kB 011: 8 kB 100: 16 kB 101: 32 kB 110: 64 kB 111: 128 kB
	[2:0]	eep_psize	External EEPROM – page size. 000: 1 kB (default) 001: 2 kB 010: 4 kB 011: 8 kB 100: 16 kB 101: 32 kB 110: 64 kB 111: 128 kB
0x14	[7:1]	SP Magnetic High Threshold	Single-pole magnetic high threshold (15.625 mV per step). 0: 0 mV 1: 15.625 mV : 64: 1000 mV 104: 1625 mV (default) : 127: 1984 mV
0x15	[7:1]	SP Magnetic Low Threshold	Single-pole magnetic low threshold (15.625 mV per step). 0: 0 mV 1: 15.625 mV 32: 500 mV (default) : 64: 1000 mV : 127: 1984 mV

Table 2: Customer Configuration Registers – Page 7 Descriptions (Continued)

Address	Bit(s)	Registers	Description
0x16	[7:1]	MP Magnetic High Threshold	Multi-pole magnetic high threshold (15.625 mV per step). 0: 0 mV 1: 15.625 mV : 64: 1000 mV 104: 1625 mV (default) : 127: 1984 mV
0x17	[7:1]	MP Magnetic Low Threshold	Multi-pole magnetic low threshold (15.625 mV per step). 0: 0 mV 1: 15.625 mV 32: 500 mV (default) : 64: 1000 mV : 127: 1984 mV
0x18	[7:0]	digital filter	Filter/averaging setting (20.48 µs per step). 0x00: 1x, 56 µs 0x01: 1x, 56 µs 0x02: 2x, 76 µs : 0x30: 48x, 1019 µs (default) : 0x7F: 127x, 2636 µs >0x7F: Invalid
0x19	[7:0]	cal filter	Filter/averaging setting during auto-calibration (20.48 µs per step). 0x00: 1x, 56 µs (default) 0x01: 1x, 56 µs 0x02: 2x, 76 µs : 0x30: 48x, 1019 µs : 0x7F: 127x, 2636 µs >0x7F: invalid

Table 2: Customer Configuration Registers – Page 7 Descriptions (Continued)

Address	Bit(s)	Registers	Description
0x1A	[7]	hys2_on	Absolute hysteresis setting. 0: Disable absolute hysteresis (default) 1: Enable absolute hysteresis
	[6]	arc_en	Accuracy correction enable – single-pole + multi-pole. 0: Disable 1: Enable (default)
	[5]	acc2.1_en	Accuracy correction enable – single-pole (before combining with multi-pole). 0: Disable 1: Enable (default)
	[4]	acc2.2_en	Accuracy correction enable – multi-pole (before combining with single-pole). 0: Disable 1: Enable (default)
	[3:0]	sleep	Wake-up time selection. 0000: OFF (default) 0001: 1 second : 1010: 10 seconds 1011: 20 seconds : 1111: 60 seconds
0x1B	[7:0]	RS485 encoder ID	Encoder ID for RS-485. Default is 0x17.
0x1C	[7:3]	RS485 Setting 1	Reserved setting. Default is 00000.
	[2:0]	RS485_Enc_Addr	RS-485 encoder address. Default is 0x2.
0x1D	[7:0]	RS485 Setting 2	Reserved setting. Default is 0x38.

Table 2: Customer Configuration Registers – Page 7 Descriptions (Continued)

Address	Bit(s)	Registers	Description
0x1E	[7]	ssi2_ring	SSI2 mode selection. 0: No ring (default) 1: Ring
	[6]	ssi3_config	SSI3 mode selection. 0: Idle low (default) 1: Hi-Z
	[5]	ssi_temp	SSI temperature output enable. 0: Exclude from SSI output (default) 1: Include to SSI output
	[4]	ssi_alm	SSI alarm format/size. 0: 2 bits [nERR+nWRN] (default) 1: 8 bits (See Table 14, Alarm 8-Bit Selection (Used by nALRM for SSI))
	[3]	ssi_crc	SSI check type selection. 0: Parity (default) 1: CRC 6 bits
	[2]	ssi2_to_flex	SSI2 flexible time-out (monoflop time). 0: Default (typical 16.5 µs) 1: 1.5x SCK
	[1]	alm_sel	SSI 8-bit alarm format. 0: Single-turn only 1: Multi-turn + single-turn (default) **NOTE:** Applicable when SSI alarm format is 8 bits.
0x1F	[7]	spi4_cfg	SPI4 format/mode configuration. 0: 16b-Parity 1: 8b-OpCode (default)
	[5:4]	spi4_crc_init	SPI4-8 bit/SSI CRC init. 00: 000000 (default) 01: 010101 10: 101010 11: 111111 **NOTE:** Applicable for SPI4 8-bit and SSI mode only.
0x20 0x21 0x22 0x23	[31:0]	Alarm Enable	See the Alarm section. 0: Enable 1: Disable
0x24 0x25 0x26 0x27	[31:0]	Alarm Latch Enable	See the Alarm section. 0: Enable 1: Disable
0x28 0x29 0x2A 0x2B	[31:0]	Warning Mask	See the Alarm section. 0: Unmask 1: Mask

Table 2: Customer Configuration Registers – Page 7 Descriptions (Continued)

Address	Bit(s)	Registers	Description
0x2C	[31:0]	Error Mask	See the Alarm section. 0: Unmask 1: Mask
0x2D			
0x2E			
0x2F			
0x30	[7:0]	sync_offset	Single-pole-multi-pole offset synchronization.
0x31	[6:4]	Pole_length	Pole length selection. 001: 1.90 mm 010: 2.60 mm 100: 3.34 mm (default)
	[3]	h1_sign	First harmonic sign multi-pole from single-pole. 0: Positive sign (default) 1: Negative sign
	[2]	sync_dir	Direction of synchronization. 0: Clockwise (default) 1: Counterclockwise
	[1]	dpc2_dir	Direction of dynamic phase correction of multi-pole. 0: Clockwise (default) 1: Counterclockwise
0x32	[3:0]	hysteresis_setting	Incremental hysteresis setting. 0x0: 0.0000 degree 0x1: 0.0001 degree 0x2: 0.0002 degree 0x3: 0.0003 degree 0x4: 0.0007 degree 0x5: 0.0014 degree 0x6: 0.0027 degree 0x7: 0.0055 degree 0x8: 0.0110 degree 0x9: 0.0220 degree (default) 0xA: 0.0439 degree 0xB: 0.0879 degree 0xC: 0.1758 degree 0xD: 0.3516 degree 0xE: 0.7031 degree 0xF: 1.4063 degree
0x35	[7]	zero_latency	Zero latency/prediction enable. 0: Disable zero latency 1: Enable zero latency (default)
	[2:0]	fixed_delay	Static latency delay to be compensated.
0x36	[7:0]		fixed_delay (ns) = N × 80 ns, where N = 0 to 2047 Default, N = 450 or 36 µs
0x7F	[7:0]	Page Selection	Memory page selection. See the EEPROM Page section.
0x44	[7:0]	BiSS Map 0x41	BiSS EDS-Bank (BiSS Map 0x41)
0x45	[15:0]	BiSS Map 0x42 to 0x43	BiSS Profile ID (BiSS Map 0x42 to 0x43)
0x46			

Table 2: Customer Configuration Registers – Page 7 Descriptions (Continued)

Address	Bit(s)	Registers	Description
0x47	[31:0]	BiSS Map 0x44 to 0x47	BiSS Serial Number (BiSS Map 0x44 to 0x47)
0x48			
0x49			
0x4A			
0x4B	[7:0]	BiSS Map 0x4B	BiSS Map 0x4B
0x4C	[7:0]	BiSS Map 0x4C	BiSS Map 0x4C
0x4D	[7:0]	BiSS Map 0x4D	BiSS Map 0x4D
…..	…..	…..	…..
0x67	[7:0]	BiSS Map 0x67	BiSS Map 0x67
0x76	[47:0]	BiSS Map 0x78 to 0x7D	BiSS Device ID (BiSS Map 0x78 to 0x7D)
…..			
0x7B			
0x7C	[15:8]	BiSS Map 0x7E	BiSS Manufacturer ID (BiSS Map 0x7E)
0x7D	[7:0]	BiSS Map 0x7F	BiSS Manufacturer ID (BiSS Map 0x7F)

Table 3: Customer Configuration Registers – Page 9

Address	Bit							
[hex]	7	6	5	4	3	2	1	0
00	Unlock Memory							
01	Program Memory							
02	N/A				ZR Clear	Alarm Clear	ZR Calibrate	MT Clear
04	N/A					Auto-All Clear	N/A	Auto-All Calibrate
0E	N/A					GPO2_EXT	GPO1_EXT	GPO0_EXT
21	Chip Ready	EEPROM Err	CRC Err	N/A				
24	Alarm[31:24]							
25	Alarm[23:16]							
26	Alarm[15:8]							
27	Alarm[7:0]							
28	N/A	PCode Status	N/A	N/A	ZR Status [1:0]		Auto-All Status [1:0]	
2B	Chip ID [7:0]							
2C	temp_data [7:0]							
70	Passcode[55:0]							
71								
72								
73								
74								
75								
76								
77	Pcode OTP							
7F	Page Selection							

Table 4: Customer Configuration Registers – Page 9 Descriptions

Address	Bit(s)	Registers	Description
0x00	[7:0]	Unlock Memory	Unlock memory (level 1) by writing 0xAB.
0x01	[7:0]	Program Memory	Program memory by writing 0xC0.
0x02	[3]	ZR Clear	Single-turn zero reset (offset value) clear. 0: Release 1: Initiate
	[2]	Alarm Clear	Clear all alarm status. 0: Release 1: Initiate
	[1]	ZR Calibrate	Single-turn zero reset calibration. See the Zero Reset Calibration section.
	[0]	MT Clear	Multi-turn counter clear. 0: Release 1: Initiate
0x04	[2]	Auto-All Clear	Auto-all clear for signal conditioning and linearization offset (reset all values to zero). 0: Release 1: Initiate
	[0]	Auto-All Calibrate	Auto-all calibration for calibrate signal conditioning and linearization offset. 0: Release 1: Initiate
0x0E	[2]	GPO2_EXT	State control for GPIO2 (when GPIO2 set as GPO_EXT). 0: Low 1: High
	[1]	GPO1_EXT	State control for GPIO1 (when GPIO1 set as GPO_EXT). 0: Low 1: High
	[1]	GPO0_EXT	State control for GPIO0 (when GPIO0 set as GPO_EXT). 0: Low 1: High
0x21	[7]	Chip Ready	Status of chip (ready when is 1).
	[6]	EEPROM Err	EEPROM error status.
	[5]	CRC Err	CRC error for EEPROM.
0x24	[31:0]	Alarm [31:0]	Alarm status. See the Alarm section.
0x25			
0x26			
0x27			
0x28	[6]	Pcode Status	EERPOM user passcode status.
	[3:2]	ZR Status [1:0]	Zero reset status. 1: Done 0: Error
	[1:0]	Auto-All Status [1:0]	Auto-all status. 1: Done 0: Error
0x2B	[7:0]	Chip ID	ID of the chip.

Table 4: Customer Configuration Registers – Page 9 Descriptions (Continued)

Address	Bit(s)	Registers	Description
0x70	[55:0]	Passcode	User passcode. See the EEPROM Passcode (Level 2 Memory Access) section.
0x71			
0x72			
0x73			
0x74			
0x75			
0x76			
0x77	[7:0]	Pcode OTP	EEPROM user passcode one-time programming. See the EEPROM Passcode (Level 2 Memory Access) section.
0x7F	[7:0]	Page Selection	Memory page selection. See the EEPROM Page section.

EEPROM Passcode (Level 2 Memory Access)

Perform the following steps to set a memory passcode:

1. Write the value 0x09 to address 0x7F to access the Customer Configuration Registers – Page 9.
2. Write the value 0xAB to address 0x00 to unlock Level 1 memory access.
3. Write the desired passcode 7 x 8 bits to the memory address from 0x70 to 0x76.
4. Write 0xBA to address 0x77 to set the passcode.

NOTE: The factory default passcode is 0x00-0x00-0x00-0x00-0x00-0x00-0x00.

EEPROM Unlock

Perform the following steps to unlock the memory:

1. Write the value 0x09 to address 0x7F to access the Customer Configuration Registers – Page 9.
2. Write the value 0xAB to address 0x00 to unlock Level 1 memory access.
3. Write the correct user passcode 7 x 8 bits to the memory address from 0x70 to 0x76 to unlock Level 2 memory access.
4. Read address 0x28 bit-6, Pcode Status, in Customer Configuration Registers – Page 9.
5. Read and write memory are now accessible.

EEPROM Page

Perform the following steps to load the EEPROM page:

1. Perform the steps in EEPROM Unlock to unlock the EEPROM.
2. Write one of the following values to address 0x7F to load the desired EEPROM page:
   – 0x07 to load the Customer Configuration Registers – Page 7.
   – 0x09 to load the Customer Configuration Registers – Page 9.

NOTE: Upon power-up, the memory is automatically loaded with the Customer Configuration Registers – Page 9.

EEPROM Programming

Perform the following steps to program the memory to EEPROM:

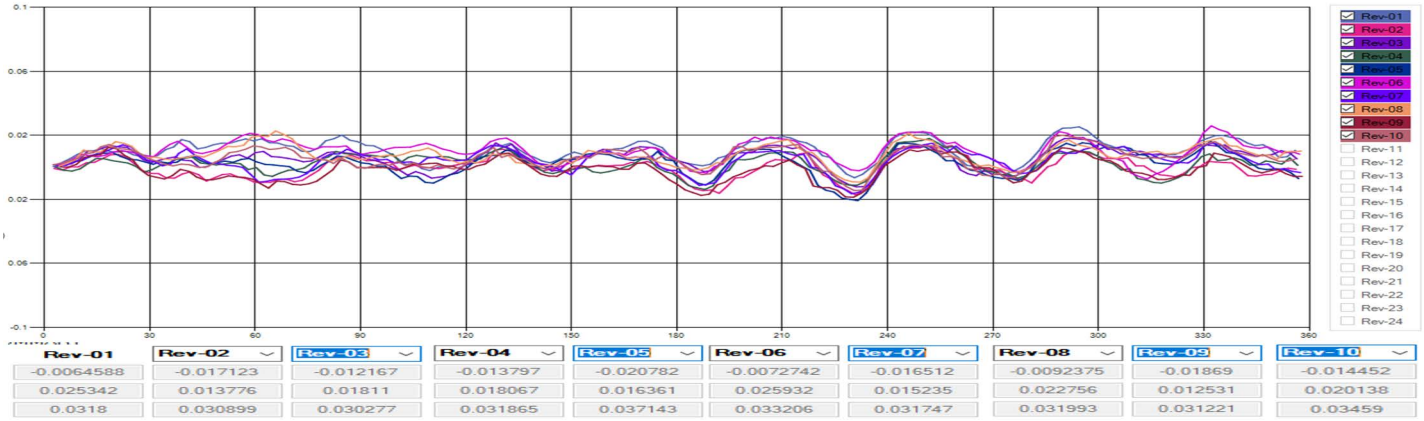
1. Write the desired values to the current memory registers.
2. Verify the written values by reading back all registers.
3. Write the value 0x09 to address 0x7F to access the Customer Configuration Registers – Page 9.
4. Write the value 0xC0 to address 0x01 to program the current memory registers to EEPROM.

NOTE: EEPROM programming is necessary to retain changes made to the EEPROM.

Encoder Calibration

Accuracy Angle Calibration

To achieve a high degree of angle accuracy, the AEAT-9988M comes with a built-in correction algorithm. This algorithm corrects the errors upon installation of the encoder to the motor. The following figure shows the corrected accuracy after multiple rotations.



NOTE:

- The magnet is set up with 8-pole pair with 3.34-mm pole length.
- The motor jitter during calibration will impact the accuracy.

The calibration procedures are as follows.

Customer Configuration Register

1. Mount the encoder onto the motor system, ensuring the magnet is properly attached.
2. Rotate the magnet at a constant speed ranging from 100 RPM to 2000 RPM; a higher speed is recommended.
3. Once the speed stabilizes, write 0x01 to address 0x04 (Page 9) to initiate the calibration sequence.
4. Read the calibration status on bit [1:0], address 0x28 (Page 9).
   – 10: Calibration passed.
   – 11: Calibration failed.
5. Write 0x00 to address 0x04 (Page 9) to exit the calibration sequence.
6. The calibration value is automatically stored in memory; no further programming is required.
   – To erase the calibration value, write 0x04 to address 0x04 (Page 9).
   – To return the operation mode, write 0x00 to address 0x04 (Page 9).

Zero Reset Calibration

The AEAT-9988M allows users to configure a zero reset position. The following is the calibration procedure.

Customer Command Register

1. Stop the encoder at the desired location on the motor system.
2. Once it is stationary, write 0x02 to address 0x02 (Page 9) to reset the absolute single-turn position.
3. Read the calibration status on bit [3:2], address 0x28 (Page 9).
   – 10: Calibration passed.
   – 11: Calibration failed.
4. Write 0x00 to address 0x02 (Page 9) to exit the calibration sequence.
5. The offset value is automatically stored in memory; no further programming is required.
   – To erase the calibration value, write 0x08 to address 0x02 (Page 9).
   – To return to operation mode, write 0x00 to address 0x02 (Page 9).

Temperature Sensor

Reading the temperature value via register.

Table 5: Temperature Sensor Data

Temperature	TEMP[7:0]
–64°C	1100 0000
–40°C	1100 1110
–20°C	1110 1100
–1°C	1111 1111
0°C	0000 0000
1°C	0000 0001
10°C	0000 1010
25°C	0001 1001
50°C	0011 0010
85°C	0101 0101
127°C	0111 1111

NOTE:

- The minimum supported range for temperature output is –64°C.
- Negative temperature values are limited to the range of –1°C to –64°C.
- The maximum positive temperature value is 191°C.
- An alternative method to read the temperature is by accessing the memory register at Page 7, address 0x05 (see Table 6).

For configuring temperature values and alarms, see Table 6. The default temperature upper limit is set to 0x7D, corresponding to 125°C. This value is based on the ambient temperature measured by the AEAT-9988M encoder ASIC.

Table 6: Temperature Alarm Limit Setting and Temperature Output Address

Page	Address [hex]	Bit								Initialize Value
		7	6	5	4	3	2	1	0	
7	02	Temp Max Limit Offset[7:0]								8'h00
	03	Temp Offset[7:0]								8'h00
	04	Temperature Limit[7:0]								8'h7D
	05	Temperature Output[7:0]								N/A

Table 7 provides an example based on the initial setting of 0x04 (Temperature Limit) to trigger a temperature alarm at 125°C. The temperature offset can be either positive or negative.

Table 7: Temperature Sensor Offset Setting Example

Case	Temperature Sensor Offset	0x02	0x03	0x04	0x05	Alarm Trigger
	Offset Value (Decimal)	Temperature Max. Limit Offset (Hex)	Temperature Offset (Hex)	Temperature Limit (Hex)	Temp Output (Dec)	
1	0	0	0	7D	124	N
					125	Y
					126	Y
2	10	0A	0A	7D	124	N
					125	Y
					126	Y
3	–1	0	FF	7D+01	124	N
					125	Y
					126	Y
4	–10	0	F6	7D+0A	124	N
					125	Y
					126	Y

NOTE:

- Case 1: No offset applied.
- Case 2: If the Temperature Offset (0x03) is a positive value, then the Temperature Max. Limit Offset (address 0x02) is set to the same value.
- Case 3: If the Temperature Offset (0x03) is a negative value, its absolute value must be added to the default Temperature Limit (0x05).
- Case 4: Example of another negative offset value scenario.

Intelligent Temperature Compensation

During initial power-up at varying temperatures, it is common for the accuracy error to degrade during the first revolution; but the accuracy will gradually improve to the specified level after a few revolutions. This effect arises because the encoder initially loads static offset and gain values based on calibration conditions (typically performed at room temperature), which may not align with the current temperature conditions each time the encoder is powered up.

The encoder features a new dynamic compensation algorithm that uses a built-in temperature sensor to detect the current temperature and apply corresponding compensation values. During real-time operation (as the motor rotates and the temperature fluctuates), the encoder continuously monitors and adjusts the static offset and gain to account for temperature variations. These adjustments are stored in memory for use during future power cycles.

NOTE: It is recommended to perform a temperature sweep on the encoder during assembly to establish the initial intelligent compensation values.

Programmable GPIO

Table 8 is a list of available programmable GPIO functions.

GPIO location pads: GPIO0 pad 26, GPIO1 pad 25, and GPIO2 pad 24.

Table 8: AEAT-9988M Programmable GPIO Functions

No.	Name	Type	Description	Cfg[7:0]	Calibration Mode
1	No Function	GPI	Idle GPIO function	0x00	—
2	ST-ZR_Cal	GPI	ST zero reset calibration	0x01	Yes
3	EXT_GPO	GPO	External digital output (control H/L by command)	0x02	—
4	AutoAll_Cal	GPI	Auto-all calibration	0x03	Yes
5	AutoAll_Clear	GPI	Auto-all clear	0x04	Yes
6	ST-ZR_Clear	GPI	ST zero reset clear	0x05	Yes
7	AccCorr_Ctrl	GPI	Accuracy correction control (enable/disable)	0x06	—
8	AbsHys_Ctrl	GPI	Absolute hysteresis control (enable/disable)	0x07	—
9	Cal_Result	GPO	ZR or auto-all calibration result (successful without error)	0x08	—
10	AlarmLatch_Ctrl	GPI	Alarm latch (enable/disable)	0x09	—
11	Alarm_ClearAll	GPI	Clear all alarm	0x0A	—
12	Alarm_MHI	GPO	Magnet high alarm trigger	0x0B	—
13	Alarm_MLO	GPO	Magnet low alarm trigger	0x0C	—
14	Alarm_MHI_MLO	GPO	Magnet high or low alarm trigger	0x0D	—
15	Alarm_OV	GPO	Over voltage alarm trigger	0x0E	—
16	Alarm_UV	GPO	Under voltage alarm trigger	0x0F	—
17	Alarm_OV_UV	GPO	Over or under voltage alarm trigger	0x10	—
18	Alarm_MEM	GPO	Memory alarm trigger	0x11	—
19	Alarm_TRACK	GPO	Track alarm trigger	0x12	—
20	Alarm_TEMP	GPO	Temp alarm trigger	0x13	—
21	Alarm_BE	GPO	BBMT battery error trigger	0x14	—
22	Alarm_BA	GPO	BBMT battery alarm trigger	0x15	—
23	Pulse_SinglePole	GPO	Pulse transition of pole pair in single-pole magnet	0x16	—
24	Pulse_MultiPole	GPO	Pulse each transition of pole pair in multi-pole magnet	0x17	—
25	DIR_Ctrl	GPI	Direction setting (CW/CCW)	0x18	—
26	Dir_CW	GPO	Indication direction of rotation (CW active high)	0x19	—
27	Dir_CCW	GPO	Indication direction of rotation (CCW active high)	0x1A	—
28	MT_Clr	GPI	MT zero reset	0x1B	Yes
29	Pos_Cal	GPI	MT = clear and ST = calibration	0x1C	Yes
30	EXT_EEPROM	GPIO	GPIO as I2C bridge[a]	0x1D	—
31	Alarm_MT-OVS	GPO	MT over speed alarm trigger	0x1E	—
32	Alarm_MT-Track	GPO	MT track alarm trigger	0x1F	—
33	Alarm_MT-XC	GPO	MT counter compare miss match alarm trigger	0x20	—
34	Alarm_MT-CFG	GPO	MT battery backup configuration alarm trigger	0x21	—
35	Alarm_MT-OVF	GPO	MT overflow alarm trigger	0x22	—
36	Pos_Clr	GPI	MT = clear and ST = clear	0x23	Yes
37	Port B En	GPI	Port B (Incremental) ON/OFF	0x24	—
38	Avg En	GPI	Averaging enable/disable	0x25	—

a. GPIO as I2C bridge: GPIO0 = Not available; GPIO1 = I2C as SCL (serial clock); GPIO2 = I2C as SDA (serial data).

GPIO as Calibration Mode

The AEAT-9988 enables users to perform the Auto-Calibration function through various communication protocols via software. Additionally, it allows the same calibration to be performed via hardware using GPIO pads. This section explains how to execute hardware-based, pad-initiated calibration.

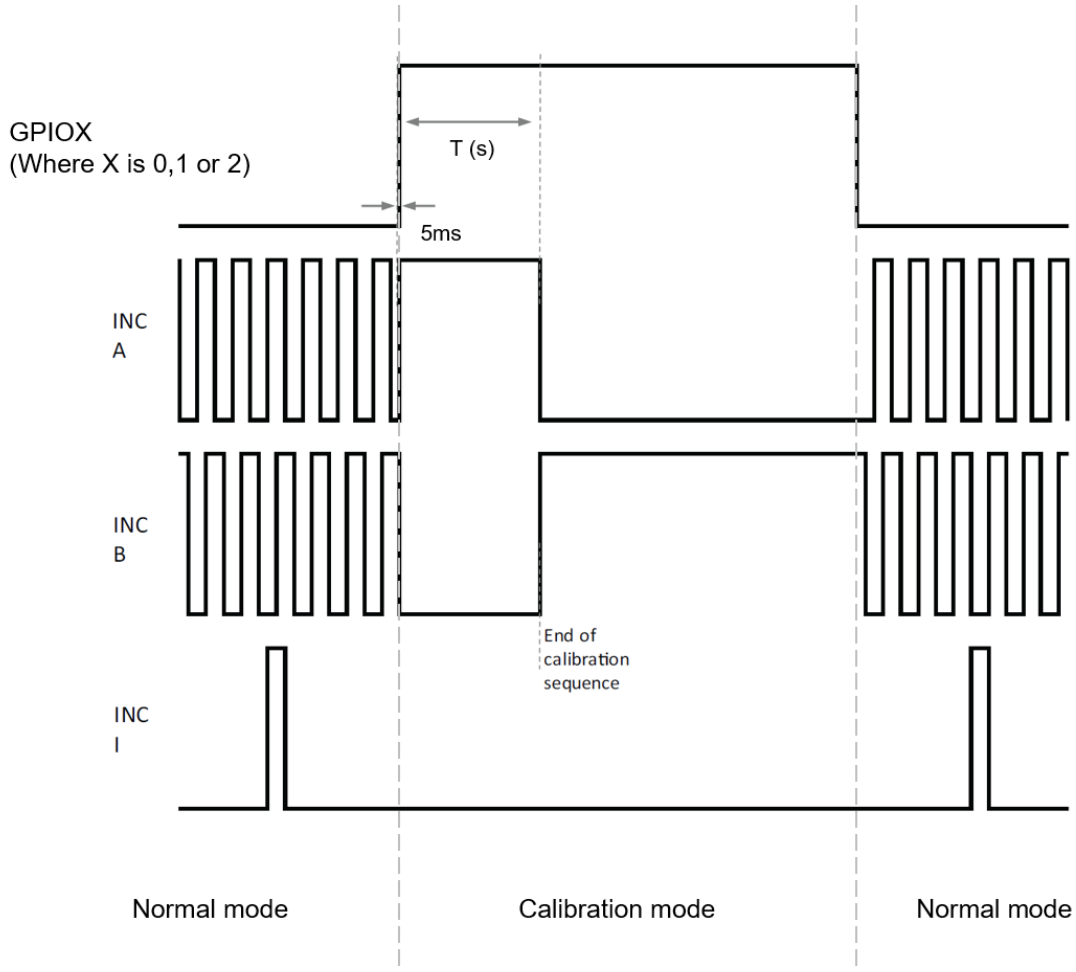
As outlined in the Table 8, some functions, such as Auto-All Calibration and ST Zero Reset Calibration, are specifically designed for calibration.

The ABI signals can indicate the calibration status. To enable this feature, see Table 2, Customer Configuration Registers – Page 7 Descriptions, address 0x13, bit 7. If this function is enabled, the user must monitor the ABI pad to determine whether the pad-initiated calibration is successful:

- If A/B/I = From High/Low/Low to Low/High/Low, calibration is successful.
- If A/B/I = From High/Low/Low to Low/High/High, calibration is not successful.

Figure 1 illustrates the pattern of signal necessary to trigger a pad-initiated calibration.

Figure 1: GPIO as Calibration Mode



* Where T is depending on the calibration functions.

Magnet Design and IC Placement

This section explains the guidelines for the recommended magnet design and specifications for the AEAT-9988M. The configuration features a single-pole ring magnet on the outer track and a multi-pole ring magnet on the inner track.

Inner Ring (Multi-Pole Magnet)

Figure 2: Inner Ring (Multi-Pole Magnet)

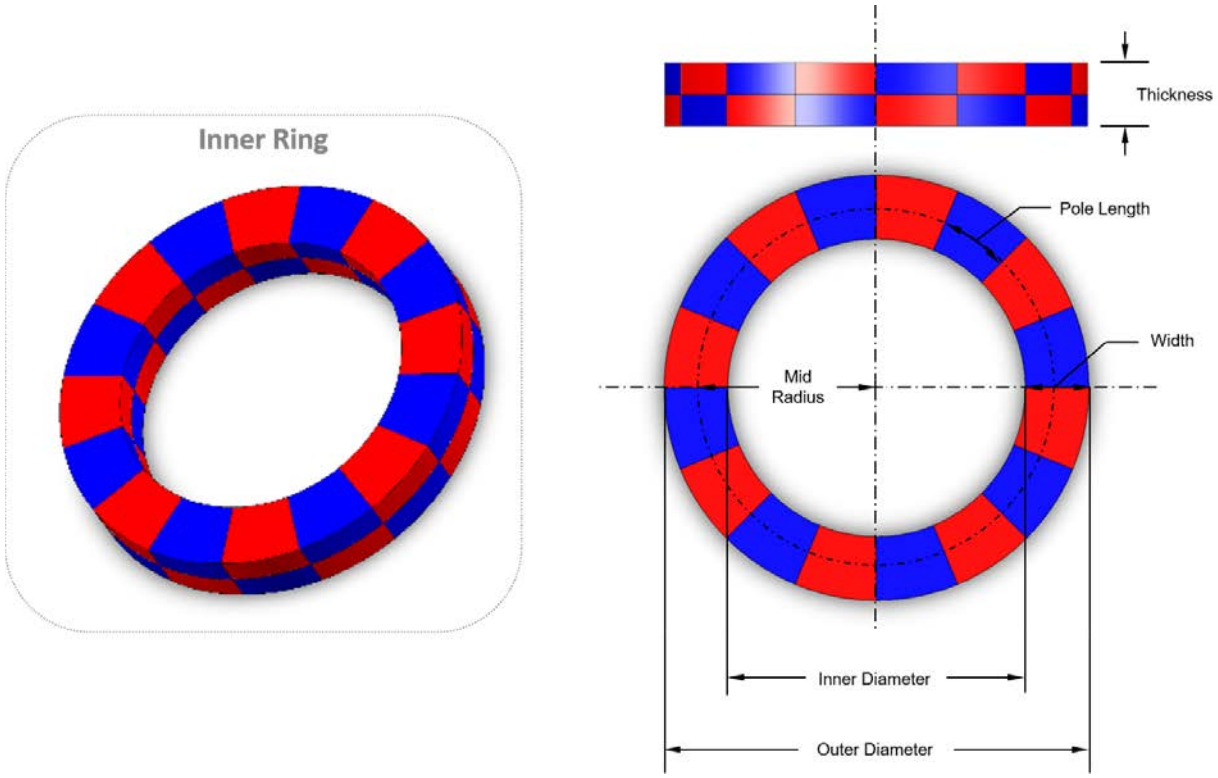


Table 9: Inner Ring (Multi-Pole Magnet) Specifications

Properties	Details
Number of Pole Pair	1, 2, 3, 4…., 63, 64
Magnetization	Axial
Magnet Width (Outer Diameter – Inner Diameter)	3.00 mm
Magnet Thickness	3.00 mm
Pole Length	~3.34, 2.60, 1.90 (mm)

$$\text{Mid Radius} = \frac{(\text{Number of Pole Pair} \times 2) \times \text{Pole Length}}{2\pi}$$

$$\text{Outer Diameter} = \left(\text{Mid Radius} + \left(\frac{\text{Magnet Width}}{2}\right)\right) \times 2$$

$$\text{Inner Diameter} = \left(\text{Mid Radius} - \left(\frac{\text{Magnet Width}}{2}\right)\right) \times 2$$

Outer Ring (Single-Pole Magnet)

Figure 3: Outer Ring (Single-Pole Magnet)

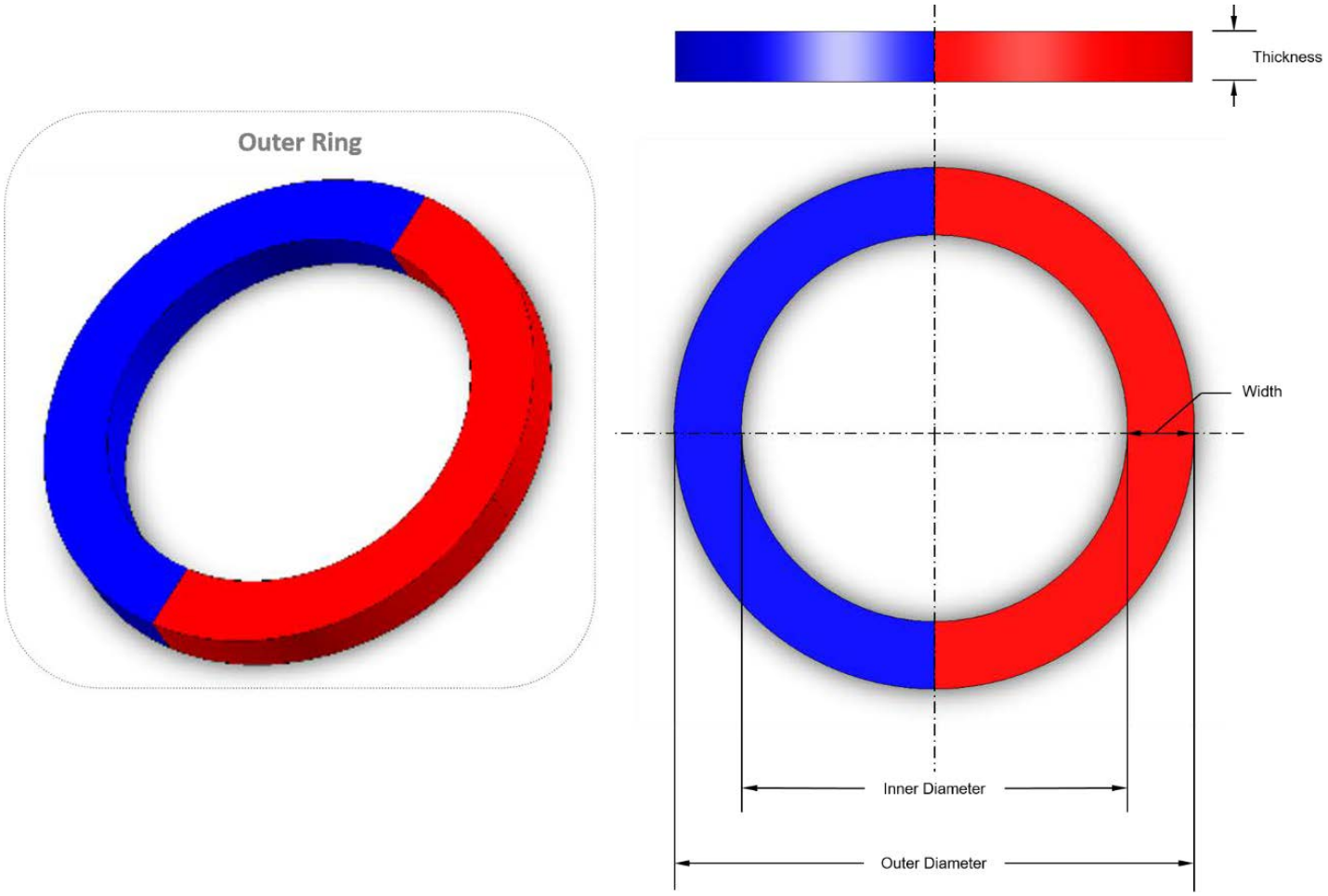


Table 10: Outer Ring (Single-Pole Magnet) Specifications

Properties	Details
Number of Pole Pair	1
Magnetization	Diametrical/Axial
Magnet Width (Outer Diameter – Inner Diameter)	4.00 mm
Magnet Thickness	3.00 mm
Pole Length	N/A

$$\text{Outer Diameter} = \left(\left(\frac{\text{Inner Ring Outer Diameter}}{2}\right) + \text{Ring Air Gap} + \text{Magnet Width}\right) \times 2$$

$$\text{Inner Diameter} = \left(\left(\frac{\text{Inner Ring Outer Diameter}}{2}\right) + \text{Ring Air Gap}\right) \times 2$$

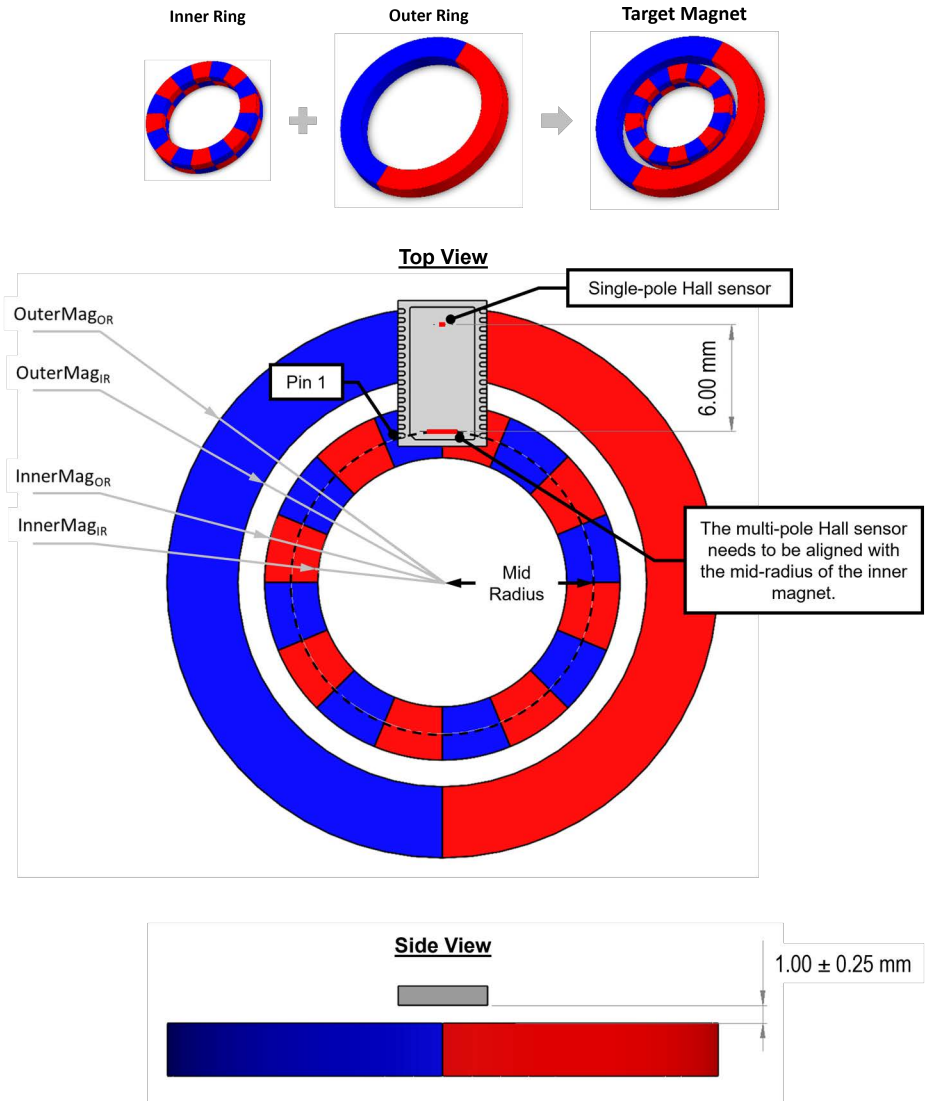
Ring Air Gap

The ring-to-ring spacing ($OuterMag_{IR}$ – $InnerMag_{OR}$) is a minimum of 1.0 mm.

Magnet and IC Package Placement

Figure 4 shows the magnet and IC package placement. The multi-pole Hall sensor must be aligned with the mid-radius of the inner magnet.

Figure 4: Magnet and IC Package Placement



NOTE:

- $OuterMag_{OR}$: Outer radius of outer ring magnet.
- $OuterMag_{IR}$: Inner radius of outer ring magnet.
- $InnerMag_{OR}$: Outer radius of inner ring magnet.
- $InnerMag_{IR}$: Inner radius of inner ring magnet.

Battery Backup Multi-Turn Operation

The AEAT-9988M series has an integrated function to track multi-turn revolutions by employing battery backup technology.

Table 11: Operating Considerations with Battery Mode

Parameters	Conditions	Min.	Typ.	Max.	Units
Electrically Permissible Speed	In battery mode (VDDA = 0V)	—	—	3000	rpm
External Battery Supply Voltage	V_{CC} > 4.5V	—	3.6	4.5	V
	V_{CC} > 4.75V	—	3.6	4.75	V
Battery Mode Current Consumption	T_{amb} = 25°C	—	85	—	µA

NOTE:

- Normal mode: Encoder operates on encoder main power supply.
- Battery mode: Encoder operates in OFF State, while multi-turn data is tracked by battery circuitry.

External Battery

Figure 5: Recommended External Battery

Table 12: Recommended External Battery Specifications

Parameters	Specifications
Product Name	Toshiba ER6V/3.6V ER6VP
Manufacturer Part Number	ER6VP
Brand	Toshiba Ultra Lithium
Nominal Voltage	3.6V
Nominal Capacity	2000 mAh
Operating Temperature Range	–55°C ~ +85°C
Size	AA

CAUTION!

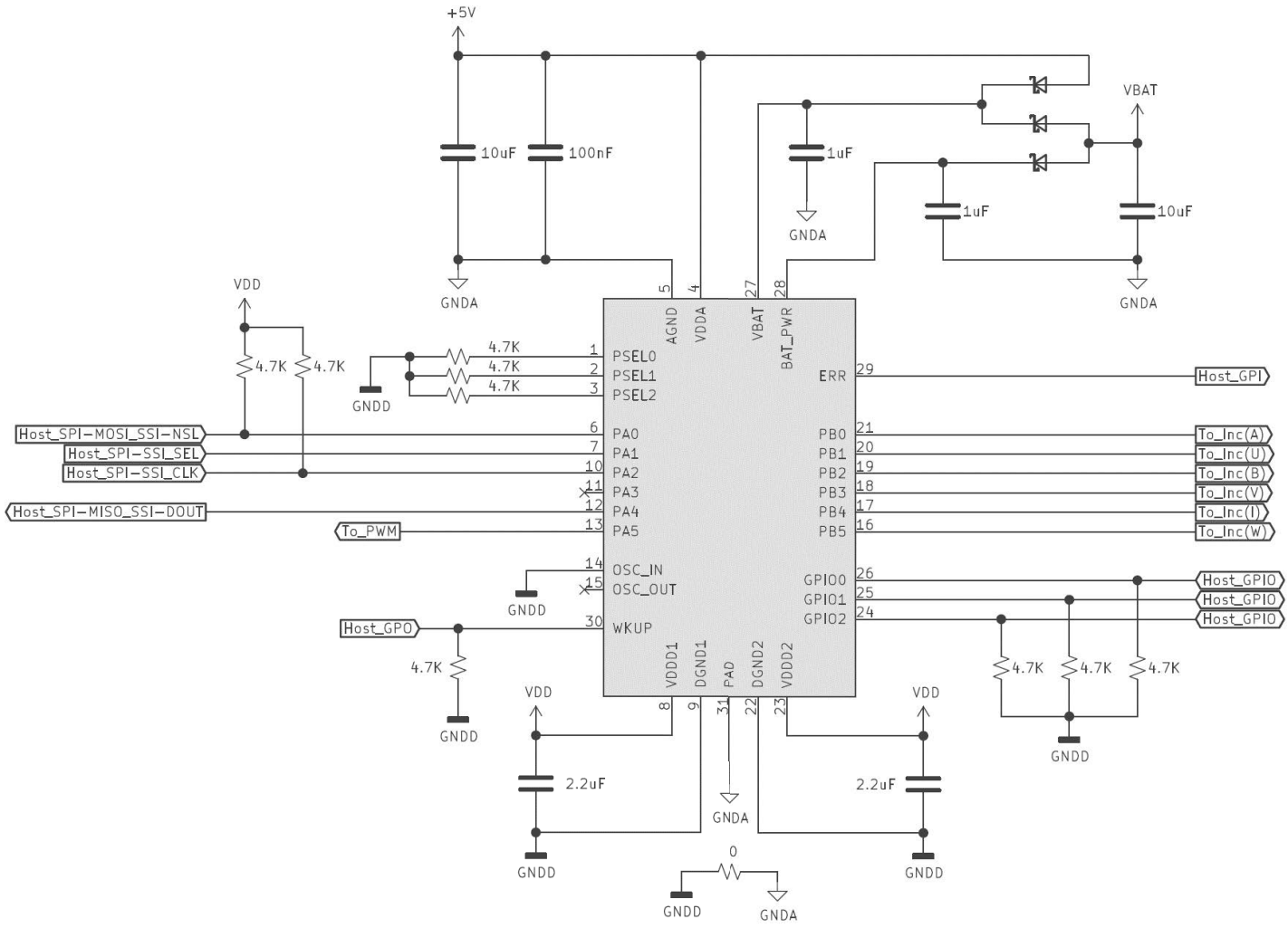
- The multi-turn data position is maintained with battery power during battery mode. The battery replacement process will cause data loss, therefore the multi-turn counter must be reset after every battery change.
- The battery life calculation depends on user application conditions.

Recommended Operation Circuit

Absolute and Incremental (PSEL = 000’b)

Absolute: SPI3 and SSI, Single Ended

Incremental: ABI and UVW, Single Ended



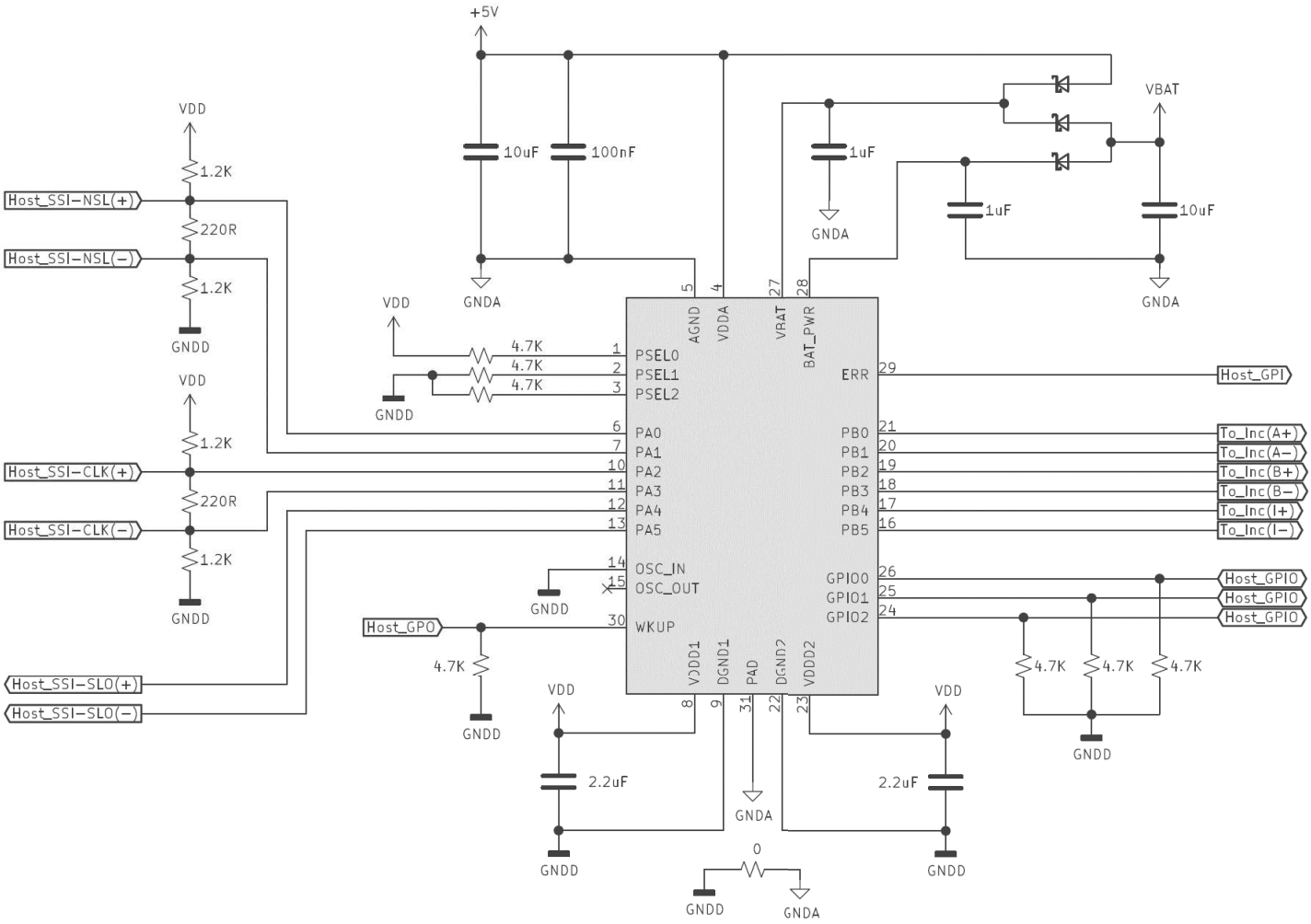
NOTE: Recommended components:

- Diode: Manufacturer: OnSemi, Part Number: RB520S30T1G

Absolute and Incremental (PSEL = 001’b)

Absolute: SSI3 Differential with Line Driver

Incremental: ABI Differential with Line Driver



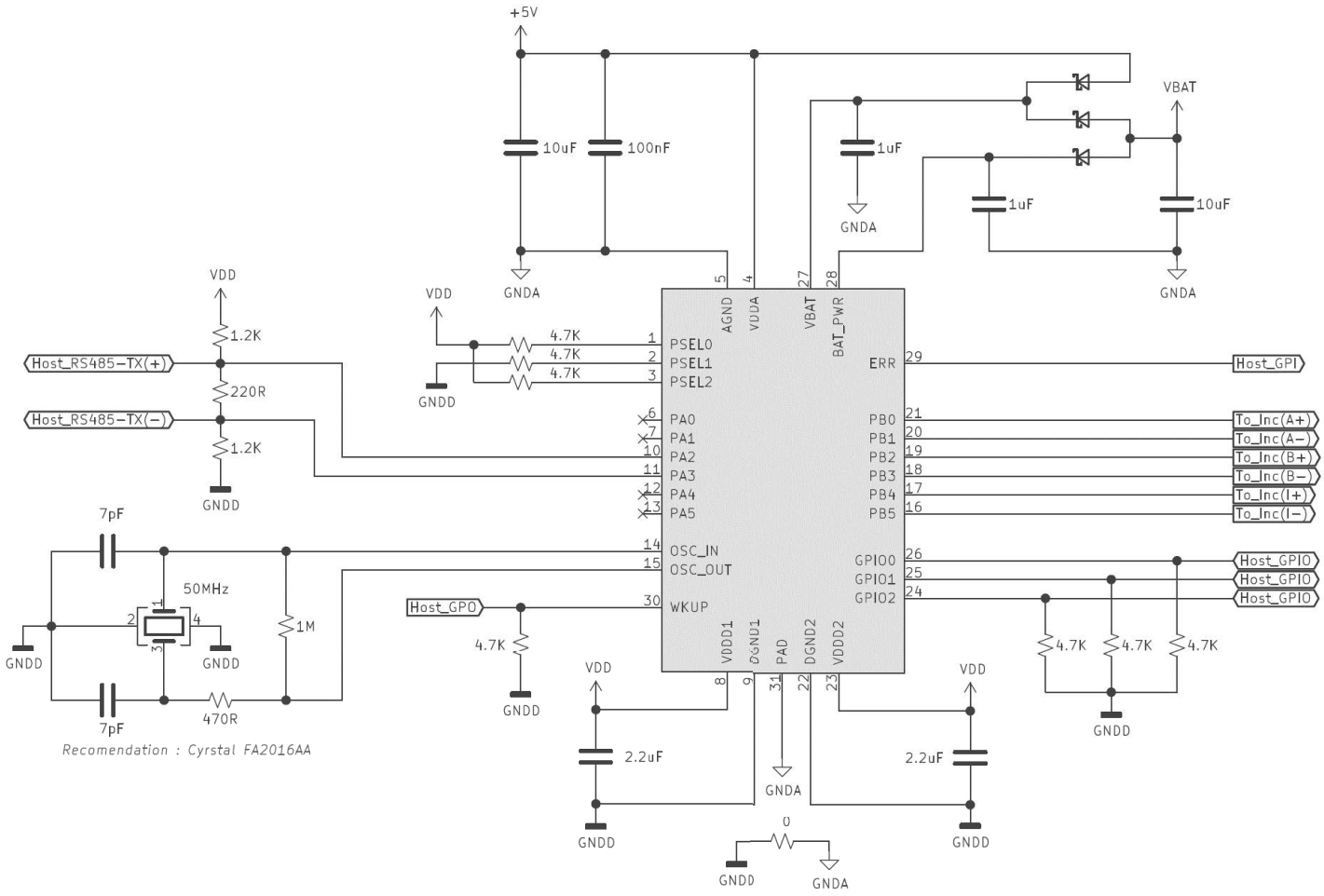
NOTE: Recommended components:

- Diode: Manufacturer: OnSemi, Part Number: RB520S30T1G

Absolute and Incremental (PSEL = 101’b)

Absolute: RS-485 Differential with Line Driver

Incremental: ABI Differential with Line Driver



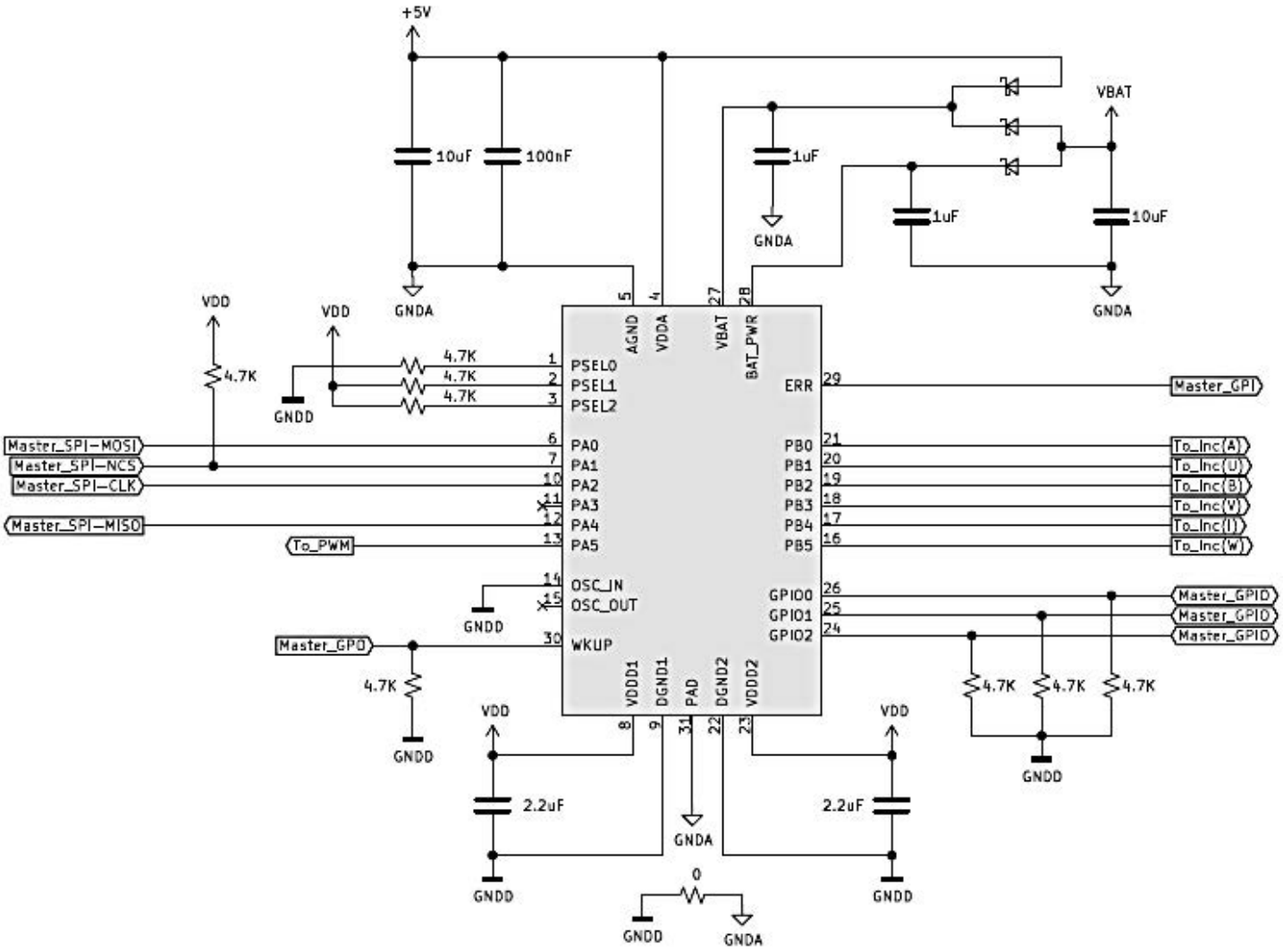
NOTE: Recommended components:

- Diode: Manufacturer: OnSemi, Part Number: RB520S30T1G
- Crystal Clock: Manufacturer: Epson, Part Number: FA2016AA 50.000000MHz

Absolute and Incremental (PSEL = 110'b)

Absolute: SPI4 Single Ended

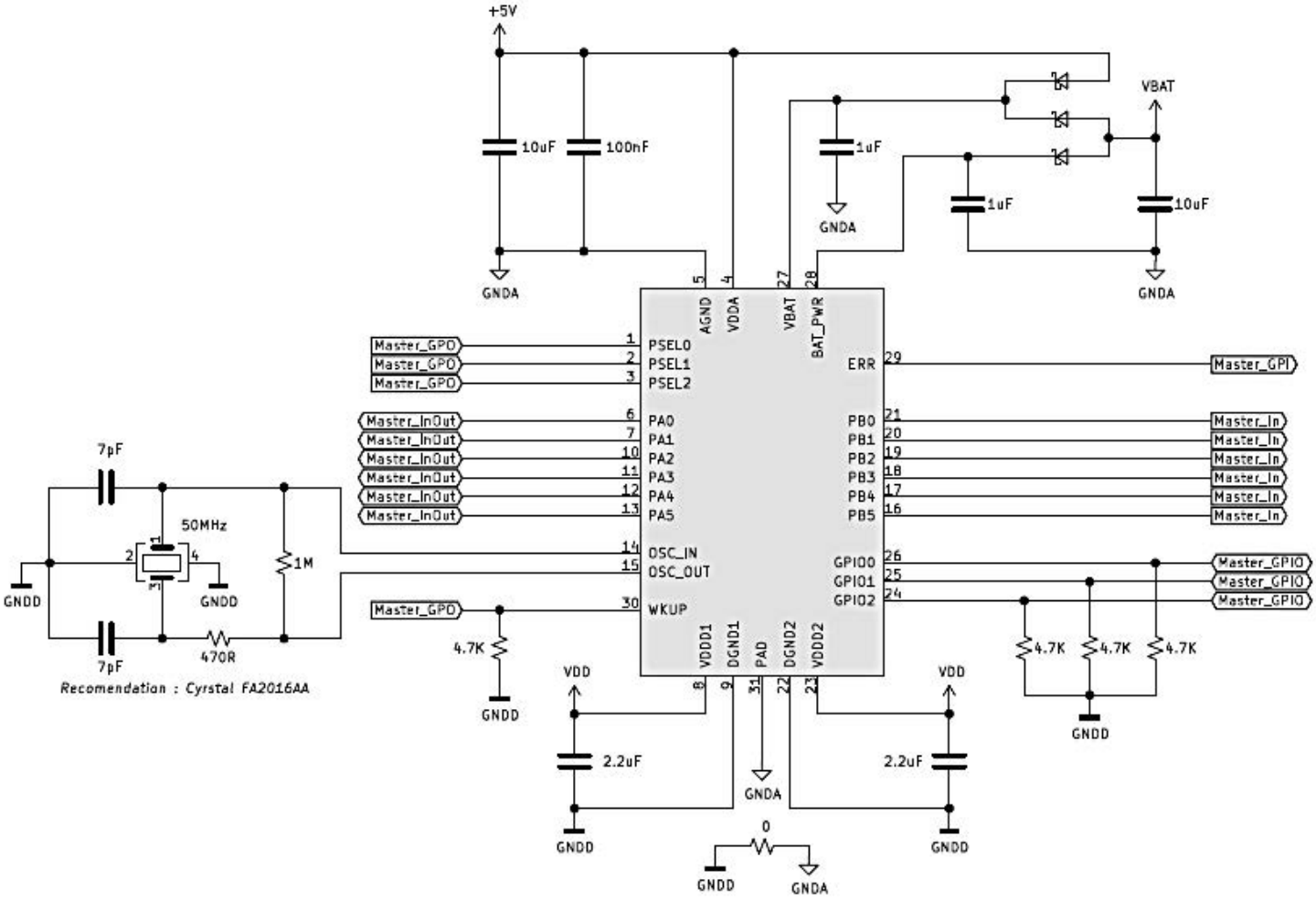
Incremental: UVW and ABI Differential with Line Driver



NOTE: Recommended components:

- Diode: Manufacturer: OnSemi, Part Number: RB520S30T1G

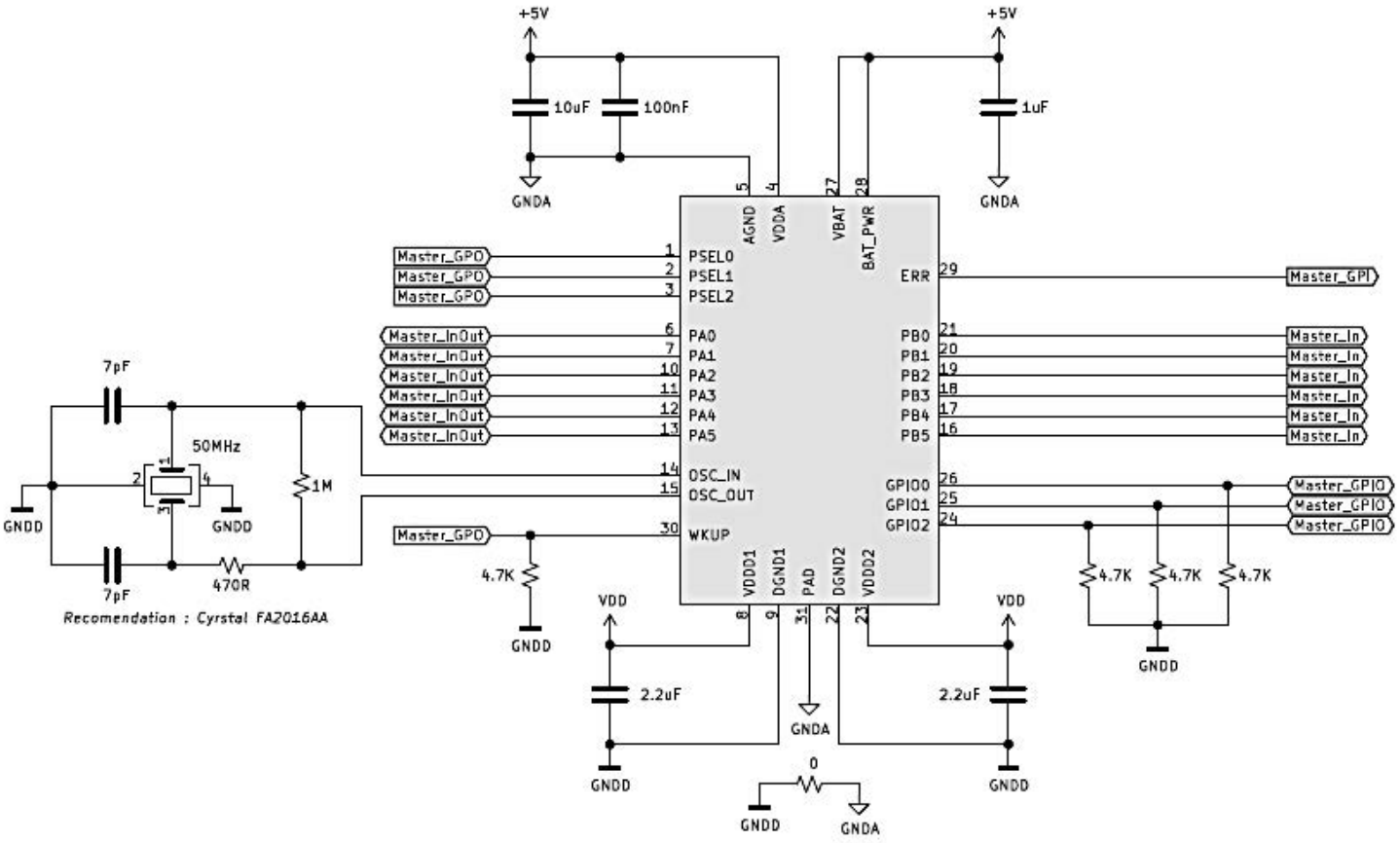
Generic with BBMT (Battery Backup Multi-Turn)



NOTE: Recommended components:

- Diode: Manufacturer: OnSemi, Part Number: RB520S30T1G
- Crystal Clock: Manufacturer: Epson, Part Number: FA2016AA 50.000000MHz

Generic without BBMT (Battery Backup Multi-Turn)



NOTE: Recommended components:

- Diode: Manufacturer: OnSemi, Part Number: RB520S30T1G
- Crystal Clock: Manufacturer: Epson, Part Number: FA2016AA 50.000000MHz

Communication Protocol

Serial Interface Format

The AEAT-9988M serial interface hosts up to 10 different communication interfaces for position output and memory access. The protocol is configurable with the PSEL pin (2 to 0). The output pin can be configured to high impedance mode for multi-client connection or bus connection.

The AEAT-9988M has two communications ports, Port A and Port B:

- Port A communication supports both Single Ended (SE) and Differential with Line Driver (LD) modes, ensuring compatibility across various systems. This versatility extends to its SPI capabilities accommodating SPI3 and SPI4 (16-bit parity and 8-bit Operation Command [OC]) functionalities. Additionally, it facilitates SSI via SSI3 and SSI2. Beyond these standard interfaces, Port-Com in Port A configuration integrates seamlessly with other protocols including BiSS-C, RS-485, PWM, and UVW.
- Port B configuration is for incremental configuration. When operating in Single Ended mode, it is able to support simultaneous ABI and UVW output. Transitioning to Differential with Line Driver mode, Port B ensures ABI output in a differential format.

All protocol selections can be switched during operation.

Table 13: MATS Table

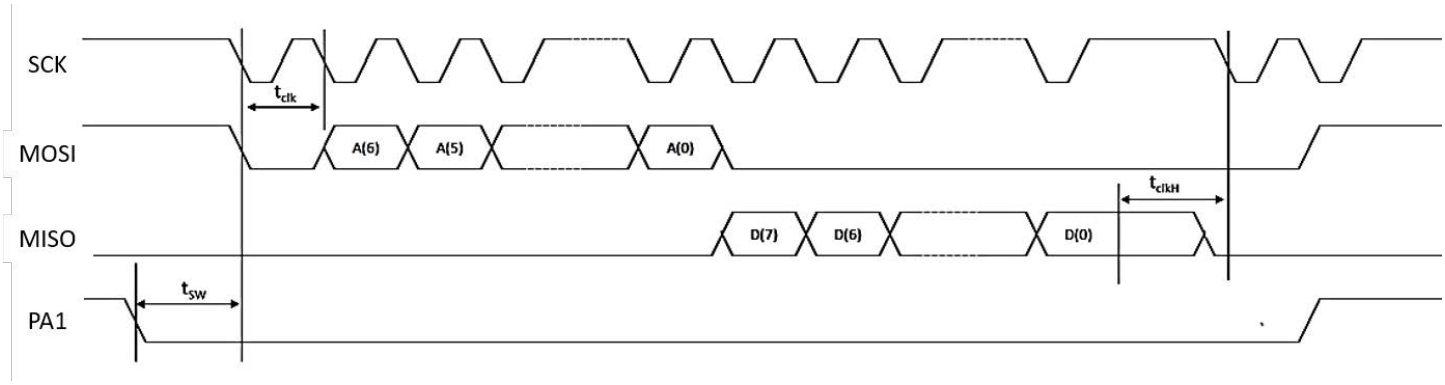
Port Configurator									
PSEL2	0	0	0	0	0	1	1	1	1
PSEL1	0	0	0	1	1	0	0	1	1
PSEL0	0	0	1	0	1	0	1	0	1
Port Assignment									
	SPI3	**SSI**	**SSI**	**BiSS-C**	**BiSS-C**	**RS-485**	**RS-485**	**SPI4**	**UVW/PWM**
	SE	**SE**	**LD**	**SE**	**LD**	**SE**	**LD**	**SE**	**LD**
PA0	MOSI	NSL	NSL+	SLI	SLI+	RX		MOSI	U+
PA1	0	1	NSL–		SLI–			NCS	U–
PA2	SCK	SCK	SCL+	MA	MA+	TX	D+	SCK	V+
PA3			SCL–		MA–		D–		V–
PA4	MISO	SOUT	SLO+	SLO	SLO+	CTS		MISO	W+
PA5	PWM	PWM	SLO–		SLO–	PWM		PWM	W–
PB0	A	A	A+	A	A+	A	A+	A	A+
PB1	U	U	A–	U	A–	U	A–	U	A–
PB2	B	B	B+	B	B+	B	B+	B	B+
PB3	V	V	B–	V	B–	V	B–	V	B–
PB4	I	I	I+	I	I+	I	I+	I	I+
PB5	W	W	I–	W	I–	W	I–	W	I–

NOTE:

- To activate the SPI3 SE protocol, assert 0 on the PA1.
- To activate the SSI SE protocol, assert 1 on the PA1.
- The protocol switch wait time is 2 ms.

Serial Peripheral Interface (SPI3)

Figure 6: SPI3 Timing Diagram



Symbol	Description	Min.	Typ.	Max.	Unit
t_{SW}	Time between PA1 falling edge and CLK rising edge	1	—	—	µs
t_{clk}	Serial clock period	1	—	—	µs
t_{clkH}	CLK high time after end of last clock period	300	—	—	ns

NOTE: Read back the data to confirm it has been written successfully.

Figure 7: SPI3 Read

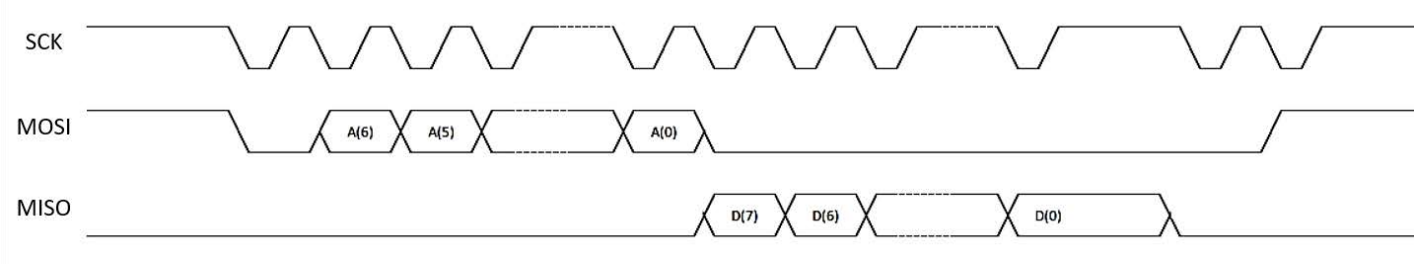
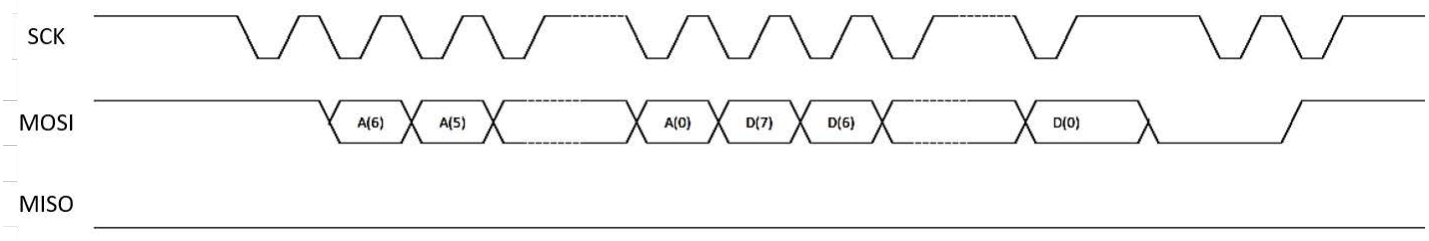
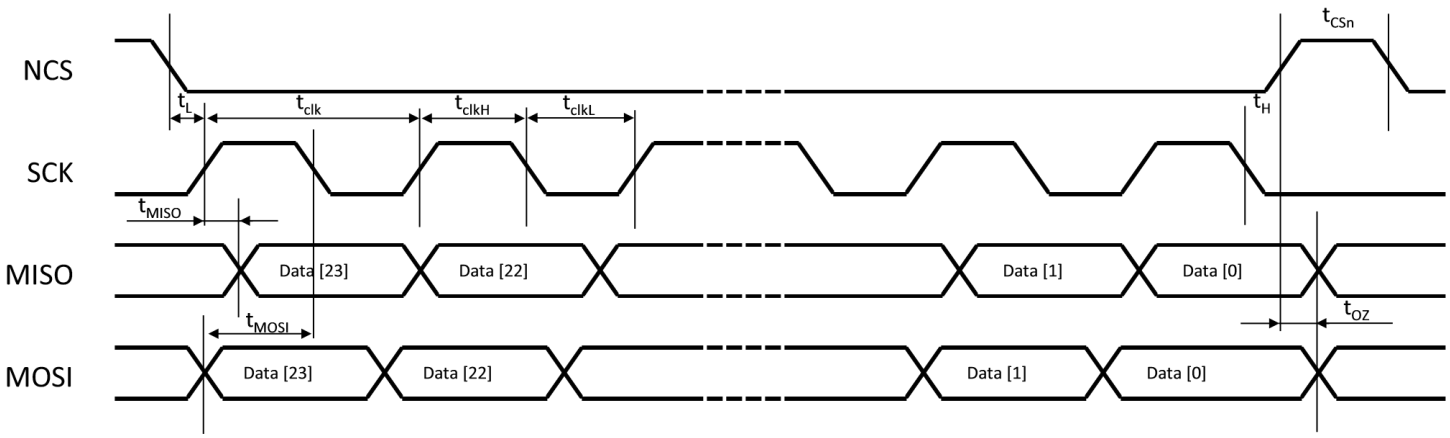


Figure 8: SPI3 Write



Serial Peripheral Interface (SPI4)

Figure 9: SPI4 Timing Diagram



Symbol	Description	Min.	Typ.	Max.	Unit
t_L	Time between the SCn falling edge and the CLK rising edge	350	—	—	ns
t_{clk}	Serial clock period	50	—	—	ns
t_{clkL}	Low period of the serial clock	25	—	—	ns
t_{clkH}	High period of the serial clock	25	—	—	ns
t_H	Time between the last falling edge of CLK and the rising edge of CSn	$t_{clk}/2$	—	—	ns
t_{CSn}	High time of CS between two transmission	350	—	—	ns
t_{MOSI}	Data input valid to clock edge	20	—	—	ns
t_{MISO}	CLK edge to data output valid	—	—	51	ns
t_{OZ}	Time between CSn rising edge and MISO HiZ	—	—	10	ns

NOTE: Read back the data to confirm it has been written successfully.

SPI4 Command and Data Frame

Figure 10: SPI4 Read Sequence

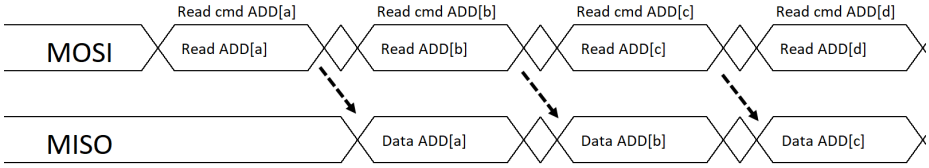
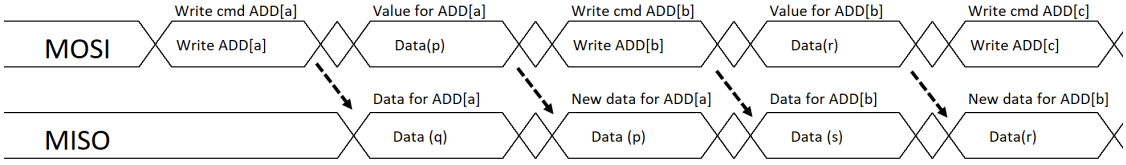
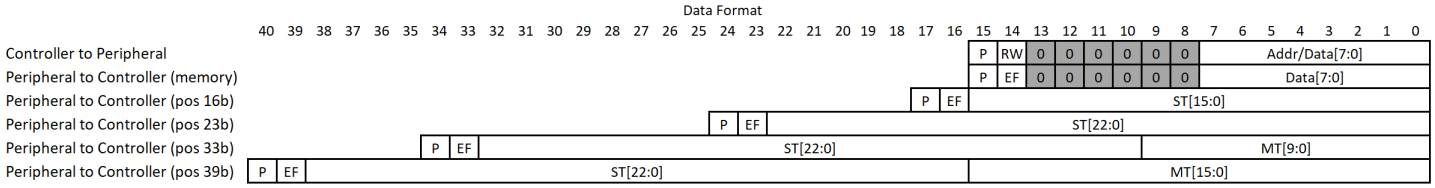


Figure 11: SPI4 Write Sequence



SPI4 16-Bit (Parity)

To configure the chip to the SPI4 16-bit selection, set spi4_cfg = 0 in the register setting (Customer Configuration Registers – Page 7, address 0x1F, bit 7).

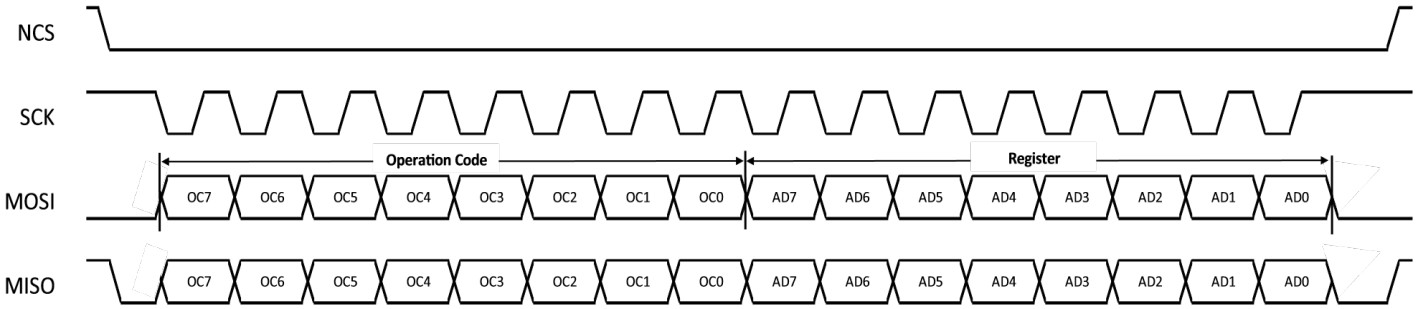


NOTE:

- P: Parity
- EF: Error Flag
- RW: Read = 1, Write = 0

SPI4 8-Bit

By default, the chip is configured to the SPI4 8-bit selection, set spi4_cfg = 1 in the register setting (Customer Configuration Registers – Page 7, address 0x1F, bit 7).

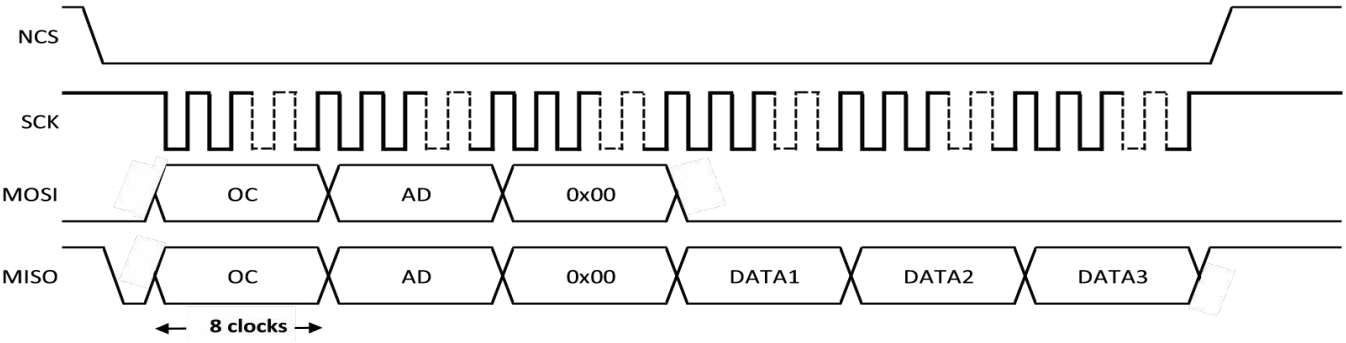


NOTE:

- When NCS is low, the communication line is activated and the data is sampled on the rising edge of SCK.
- The MISO state turns to high impedance mode (hi-Z) when NCS is high. The transmission works over a specific operation command (OC).

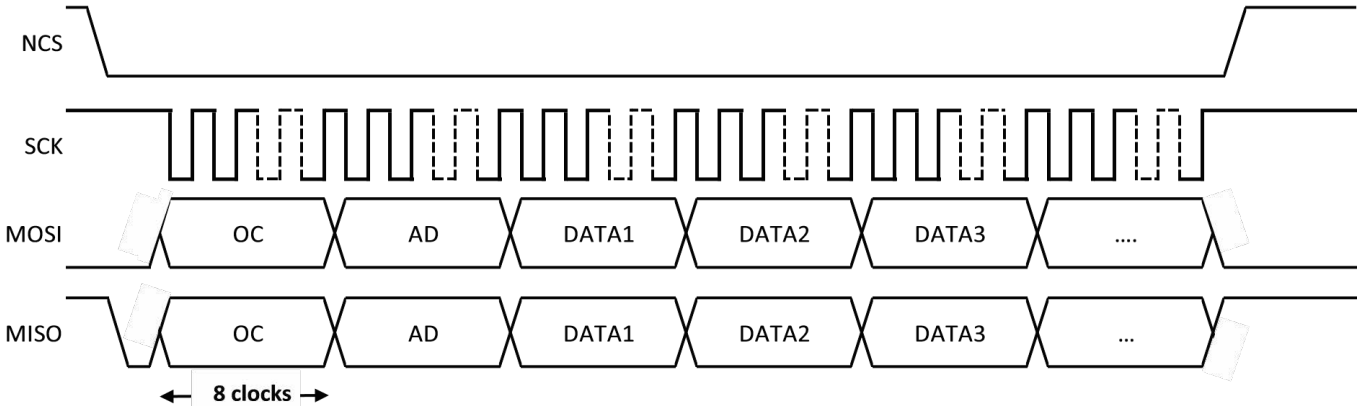
Register Read (OC = 0x81’h)

This operation is used to read data from the internal register of the chip. It can be performed consecutively starting from any register address. The data continues to be transmitted as long the clock (SCK) is sent and the chip select (NCS) remains active.



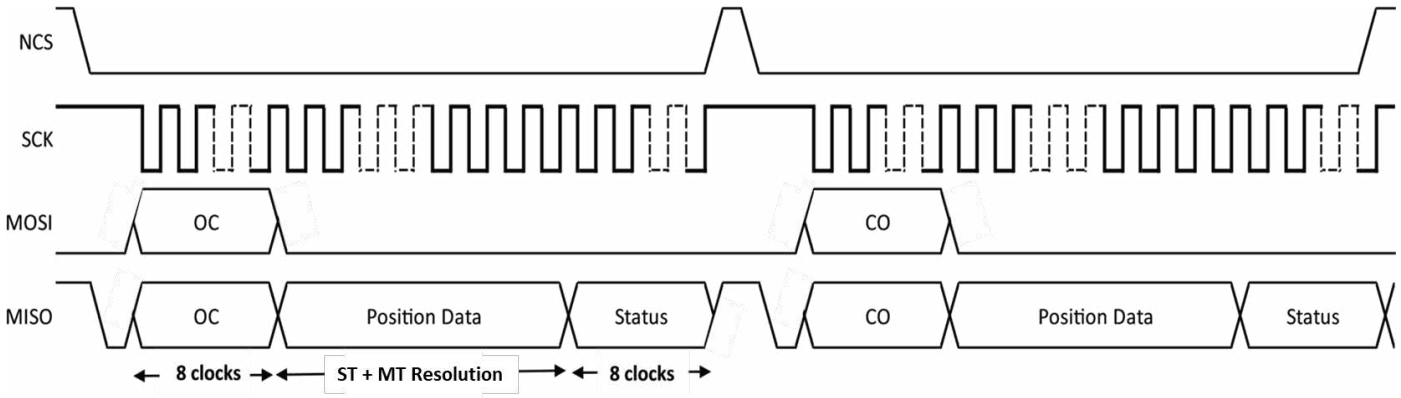
Register Write (OC = 0xCF'h)

This operation is used to write data into the internal register of the chip. It can be performed consecutively starting from any register address. The subsequent data byte is written into the next register address (AD+1), while the NCS signal stays active. Complete written data is transmitted back via MISO.



Position Read (OC = 0xA6'h)

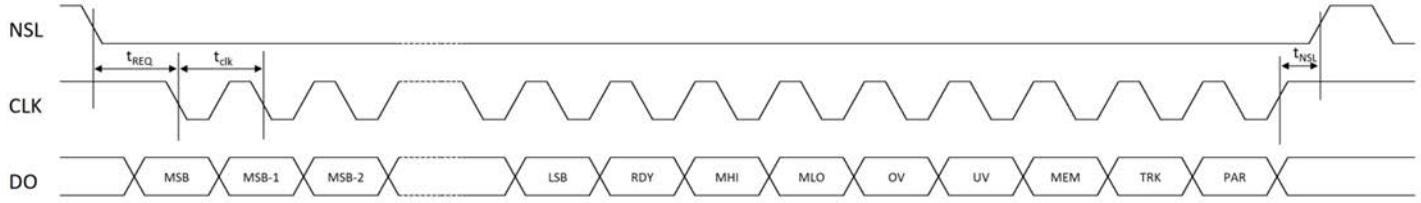
Read the absolute position by sending the operation command, and the data will be transmitted on the MISO line. The position data consists of the multi-turn and single-turn position data length and status byte. The position data length follows the multi-turn and single-turn resolution setting.



Serial Synchronous Interface 3-Wire (SSI3)

It is available in two options per ssi3_config register setting.

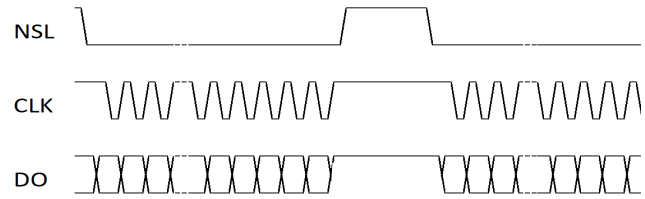
Figure 12: SSI Protocol Timing. Default: Data Output with 3-Wire SSI to 10-MHz Clock Rates



Symbol	Description	Min.	Typ.	Max.	Unit
t_{clk}	SSI_SPI_SEL switch time	100	—	—	ns
t_{REQ}	SCL high time between the NLS falling edge and the first SCL falling edge	300	—	—	ns
t_{NSLH}	NSL high time between two successive SSI reads	200	—	—	ns

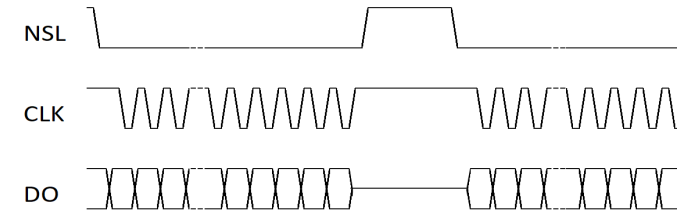
SSI-3(A)

By default, the chip is configured to the SSI-3(A) selection, ssi3_config = 0 in the register setting (Customer Configuration Registers – Page 7, address 0x1E, bit 6). The D0 pin is held at a high state once the NSL pin is high.

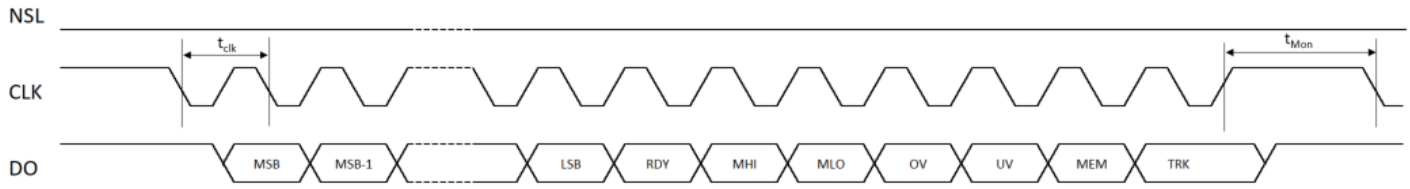


SSI-3(B)

To configure the chip to the SSI-3(B) selection, set ssi3_config = 1 in the register setting (Customer Configuration Registers – Page 7, address 0x1E, bit 6). The D0 pin is at a tristate (high-impedance) state once the NSL pin is high.



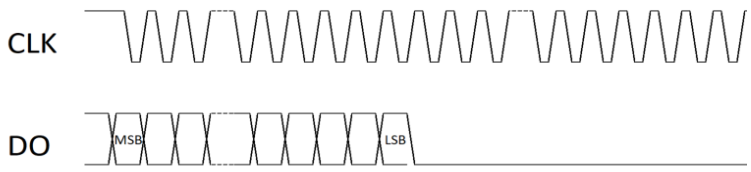
Serial Synchronous Interface 2-Wire (SSI2)



Symbol	Description	Min.	Typ.	Max.	Unit
t_{Clk}	NSL low time after the rising edge of the last clock period for an SSI read	250	—	$t_M/2$	ns
t_M	NSL high time between two successive SSI reads	—	16.5	18.0	µs

SSI-2(A)

By default, the chip is configured to the SSI-2(A) selection, ssi2_ring = 0 in the register setting (Customer Configuration Registers – Page 7, address 0x1E, bit 7). Output is a single data position and remains low after LSB until the next monoflop (t_M) expires.

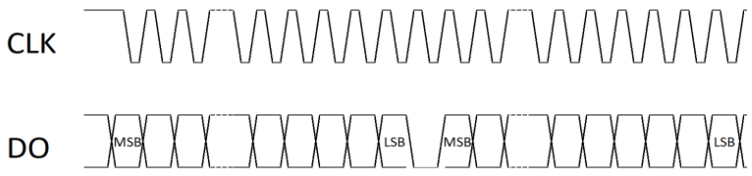


SSI-2(B)

To configure the chip to the SSI-2(B) selection, set ssi2_ring = 1 in the register setting (Customer Configuration Registers – Page 7, address 0x1E, bit 7).

The same position data can be continuously output by sending clock train, and the data is separated by a single low pulse.

Data will be refreshed when the next monoflop (t_M) expires.



SSI READ Data Format

Protocol	Type			Frame Structure				
	Temp.	Alarm	Check					
SSI	0	0	0	MT[0:16]	ST[16:23]	(nERR+nWRN)[2]	CRC[6]	
	0	0	1	MT[0:16]	ST[16:23]	(nERR+nWRN)[2]	PAR[1]	
	0	1	0	MT[0:16]	ST[16:23]	nALARM[8]	CRC[6]	
	0	1	1	MT[0:16]	ST[16:23]	nALARM[8]	PAR[1]	
	1	0	0	MT[0:16]	ST[16:23]	TEMP[8]	(nERR+nWRN)[2]	CRC[6]
	1	0	1	MT[0:16]	ST[16:23]	TEMP[8]	(nERR+nWRN)[2]	PAR[1]
	1	1	0	MT[0:16]	ST[16:23]	TEMP[8]	nALARM[8]	CRC[6]
	1	1	1	MT[0:16]	ST[16:23]	TEMP[8]	nALARM[8]	PAR[1]

Table 14: Alarm 8-Bit Selection (Used by nALRM for SSI)

ALARM Selection	Bit							
	7	6	5	4	3	2	1	0
ST Only	MHI	MLO	TRACK	TEMP	MEM	OV	UV	0
Full (MT + ST)	BA	BE	MT_Track XC	TEMP	OV UV	Track MHI MLO	MEM BB_Cfg	OVS OVF

BiSS-C Full Duplex Serial Communication Protocol

Table 15: General Specification of BiSS-C Serial Communication

Interface	Symbol	Recommended Circuit
Serial Clock	MA or SCLK	Transmitter (P/N: ISL3295E) or equivalent
Serial Data Output	SLO or DAT	Receiver (P/N: ISL3283E) or equivalent

Table 16: BiSS-C Timing Characteristics

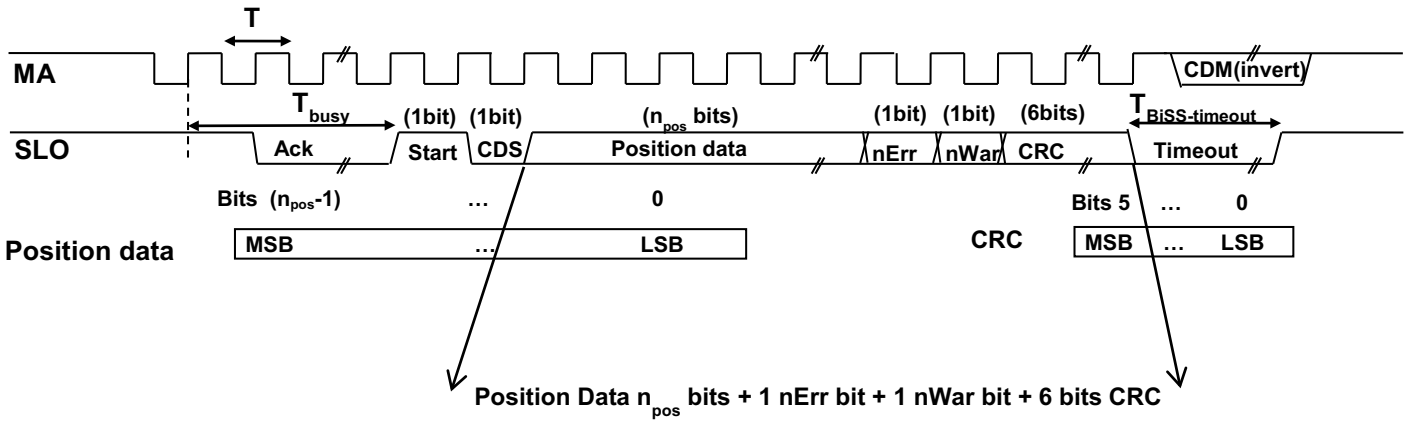
Parameter	Symbol	Condition	Min.	Typ.	Max.	Units	Notes
MA Frequency	f_{MA}	—	0.08	—	10	MHz	
MA Duty	DUT_{CLK}	—	—	50	—	%	
Busy	T_{busy}	5 MHz < f_{MA} ≤ 10 MHz	—	$3/f_{MA}$	—	µs	a
		100 kHz ≤ f_{MA} ≤ 5 MHz	—	$2/f_{MA}$	—		
Timeout	$t_{BiSS\text{-}timeout}$	—	$1.5/f_{MA}$	—	5	µs	a
Frame to Frame	—	—	—	—	1	µs	
Encoder Initialization Time	—	—	—	20	—	ms	

a. See Figure 13 for the timing description.

Table 17: BiSS-C Data Field

MT[15:0]	ST[22:0]	nError[0]	nWarning[0]	CRC[5:0]

Figure 13: BiSS-C Interface Timing Diagram



NOTE:

- CRC Polynomial = Invert of ($X^6 + X^1 + X^0$).
- nErr bit is active low. Combine all the Error Status and reflect in nErr bit.
- nWar bit is active low. Combine all the Warning Status and reflect in nWar bit.
- Position data varies depending on Single-turn and Multi-turn resolution.
- Position data is latched at the first rising edge of MA.

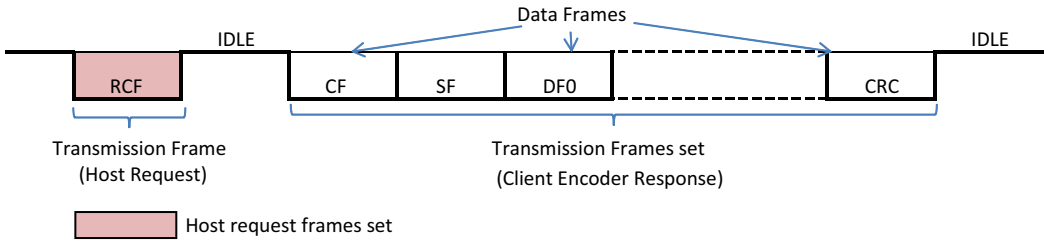
RS-485 Half-Duplex Serial Communication Protocol

Table 18: General Specification of RS-485 Serial Communication

Item	Specification	Note
Transmission Type	Differential transceiver	
Communication Type	Half duplex	Recommended transceiver: ISL8485E or equivalent
Transmission Code Type	Binary, non-zero return (NRZ) code	
Synchronization Type	Asynchronous	
Communication Baud Rate	2.5 Mb/s, 5.0 Mb/s, and 10.0 Mb/s	
Frame Length	10 bits/Frame	
Transmission Error Checking	8 bits CRC	CRC equation G(X) = X^8 + 1 X = CRC0 ~ CRC7

A one-to-one half-duplex serial communication is established between the host (for example, a servo driver) and the client encoder. The communications are in a differential transmission format. The encoder will carry out specific operations based on the command requests made by the host. An acknowledgment of the command request is necessary before the encoder executes the requested operation by checking the Start Bit, Information Data Field, and Stop Bit. If this check fails, the encoder will not acknowledge and execute the received command request.

Figure 14: General Transmission Frames Format on Half-Duplex Line



NOTE:

- **Start of the Transmission Frames Set:** Upon detecting the first logic of low state 0 on the transmission line after an idling state, and if the following 3 bits conform to the sync code, the encoder will acknowledge it as a valid request control field (RCF) and indicates the start of a transmission frame set. Otherwise, the encoder will continue to search for the next available logic of low state 0.
- **End of the Transmission Frames Set:** After the command frame is detected, if there is no start bit after the end bit of the last frame read and no subsequent frame is detected, the end of transmission frame set is concluded.
- **Idle State:** Idle state means a space between each transmission frames set and subsequent transmission frames. At idling state, the logic of output in transmission line is kept to high state 1.

RS-485 Encoder Read Out Frame Sets Format and Timing

Figure 15: Encoder Position RS-485 Data Read Out Frames Set

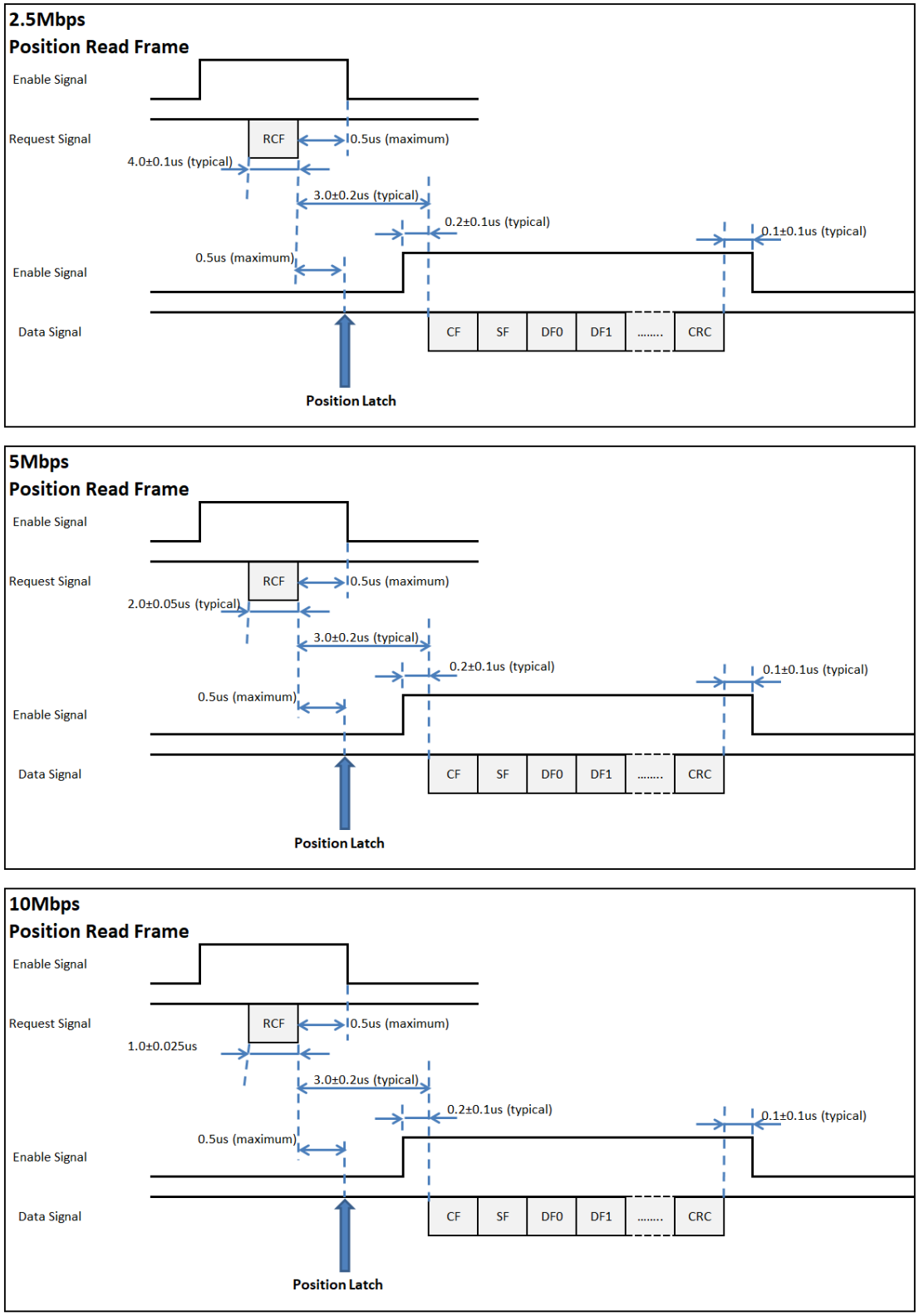
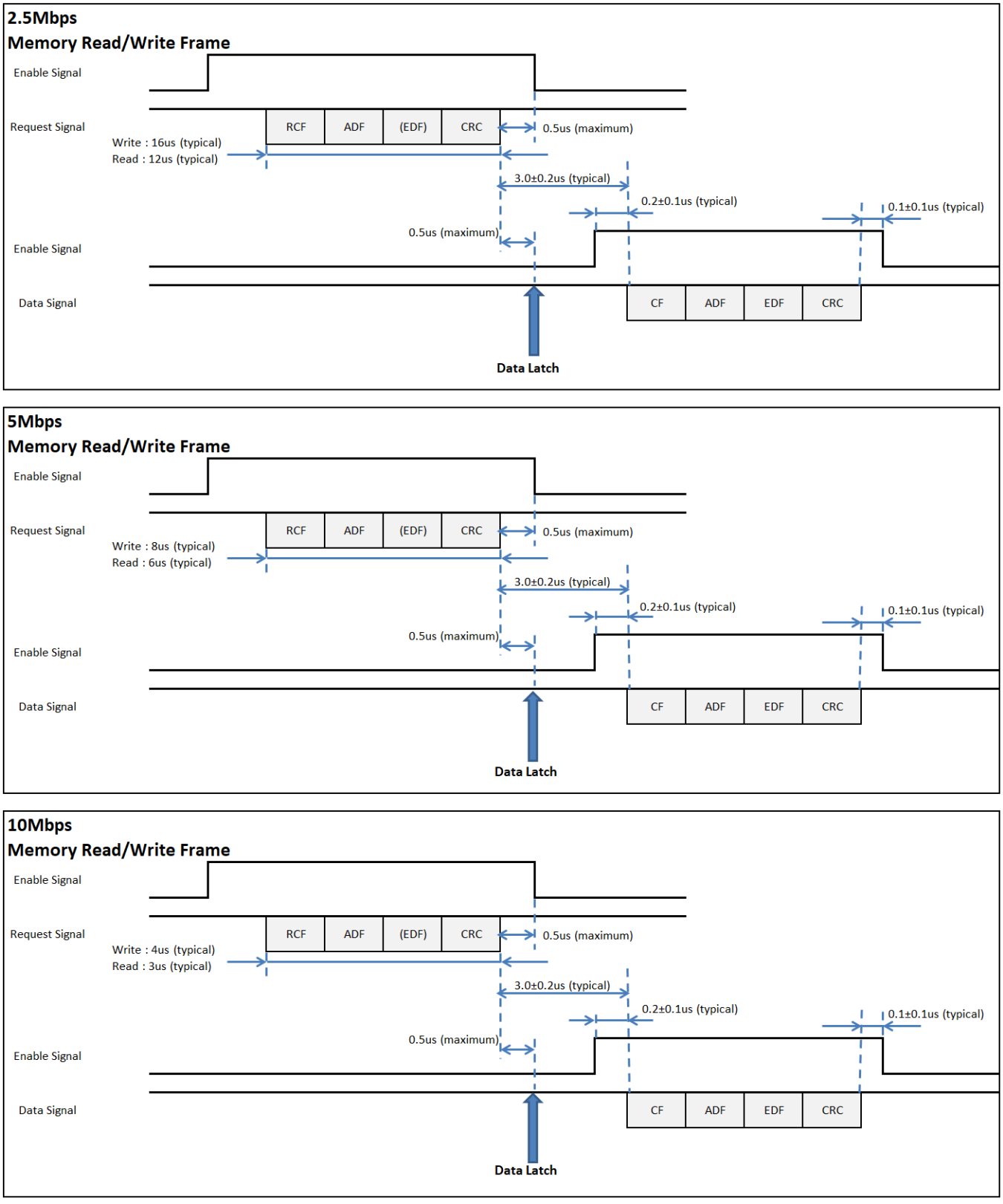


Figure 16: Encoder Memory Data Read and Write Frames Set



Encoder Position Data Read Out Frame Sets

When the host issues a RCF frame request, the encoder shall respond after 3.0 µs (typical) with an encoder data frames set with the following contents:

1. CF: Control Field; corresponds to the command frame issued by the Host.
2. SF: Status Field.
3. DF0~DF7: Encoder Data Field.
4. CRC: Cyclic Redundancy Check frame.

The encoder response data frame sets are dependent on the requested operation by the host; see Table 22.

Memory Data Read Out Frames Set

Content of transmission frames:

1. CF: Control Field; same for both host command and encoder response.
2. ADF: Address Data Field; indicates the memory location to read.
3. EDF: Memory Data Field; contains the data read from memory.
4. CRC: Cyclic Redundancy Check.

Memory Data Write Frames Set

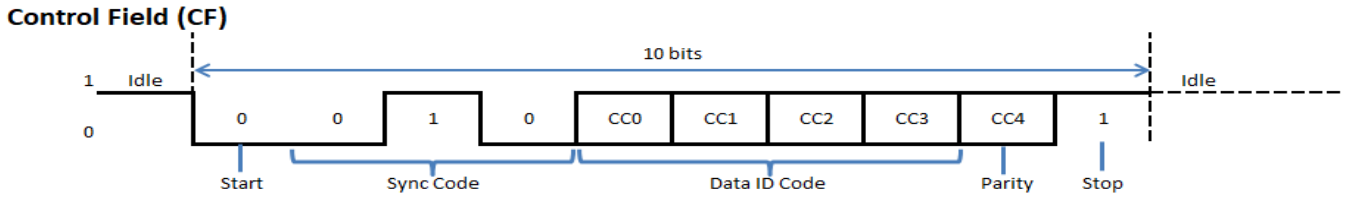
Content of transmission frames:

1. CF: Control Field; same for both host command and encoder response.
2. ADF: Address Data Field; indicates the memory location to write.
3. EDF: Memory Data Field; contains the written data to memory.
4. CRC: Cyclic Redundancy Check.

Detailed Description of Data Frames

Control Field (CF)

Figure 17: Control Field Format



The contents of the CF frame are as follows:

1. Start Bit: Indicates the start of a frame, always 0.
2. Sync Code: Indicates a valid encoder address sync code has been issued, default is 010.
3. Data ID: A combination of bits defining command instructions, see Table 19 and Table 20.
4. Parity Bit: Parity check bit for the data ID, see Table 19.
5. Stop Bit: Indicates the end of a frame, always 1.

Data ID and Client Encoder Operation Definition

Table 19: Encoder Operation Command Code Definition and Parity Bit

Encoder Operation	Data ID	Encoder Sync Code			Data ID Bits				Parity	HEX
		BIT 0	BIT 1	BIT 2	CC0	CC1	CC2	CC3	CC4	
Position or Encoder Information Read Command	0	0	1	0	0	0	0	0	0	02
	1	0	1	0	1	0	0	0	1	8A
	2	0	1	0	0	1	0	0	1	92
	3	0	1	0	1	1	0	0	0	1A
	4	0	1	0	0	0	1	0	1	A2
Memory Write Command	6	0	1	0	0	1	1	0	0	32
Alarm Clear Command	7	0	1	0	1	1	1	0	1	BA
Position Zero Reset Command	8	0	1	0	0	0	0	1	1	C2
Multi-turn and Alarm Clear Command	C	0	1	0	0	0	1	1	0	62
Memory Read Command	D	0	1	0	1	0	1	1	1	EA

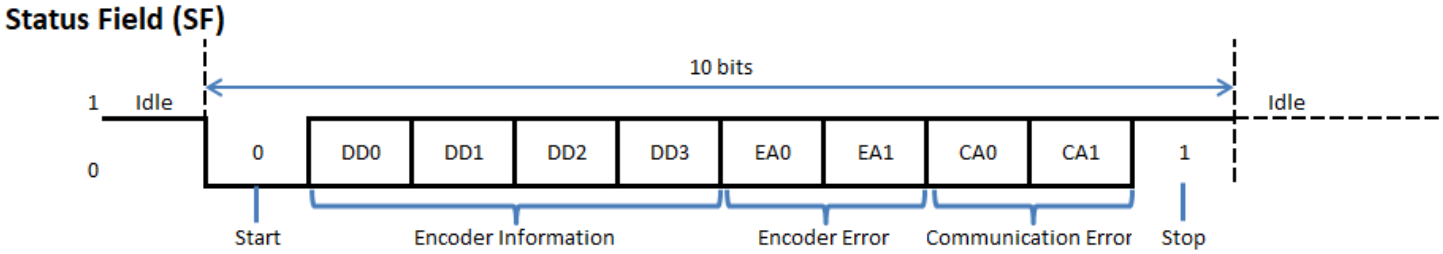
Table 20: Description of Encoder Operation

Operation	Data ID	Description of Operation
Position Read Command	0, 1, 2, 3, 4	Transmit Data ID code (Table 19) according to the List of Data field to the Encoder.
Memory Write Command	6	8 bits of data to be written into a designated memory address of the user accessible area.
Alarm Clear Command	7	Consecutive sending to perform Alarm Clear command.
Position Zero Reset Command	8	Consecutive sending to perform Position Zero Reset command
Multi-turn and Alarm Clear Command	C	Consecutive sending to perform Multi-turn and Alarm Clear command
Memory Read Command	D	8 bits of data to be read from a designated memory address of the user-accessible area.

NOTE: See Table 22 for the requirements of consecutive sending for the clear or reset commands.

Status Field (SF)

Figure 18: SF Frame Format



The contents of the SF frame are as follows:

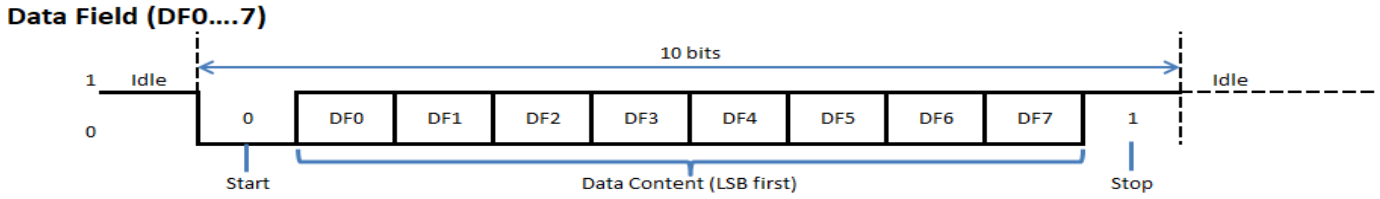
1. Start Bit: Indicates the start of a frame, always 0.
2. Encoder Information: Defined as 0000.
3. Encoder Error: Returns with state of 1 if an encoder error is detected.
4. Stop Bit: Indicates the end of a frame, always 1.

Table 21: Status Field Description of Error Flags

Logic When Error Is Detected	Error Flag	Error Description
Encoder Error Bit 1	EA0	Encoder counting error
	EA1	Multi-turn counting error
Communication Error Bit 1	CA0	Parity error detected in Host Request Frames set
	CA1	End bit error detected in Host Request Frames set

Data Field (DF_n)

Figure 19: DF_n Frame Format



The contents of the DF_n frame are as follows:

1. Start Bit: Indicates the start of frame, always 0.
2. DF0~DF7: 8 bits data set, with LSB first in the sequence.
3. End bit: Indicates the end of frame, always 1.

Description of Data Frames with Respective Data ID

Table 22: Data Frames Content with Respective Data ID for up to 24-Bit Multi-turn

Data ID	CF	SF	DF0	DF1	DF2	DF3	DF4	DF5	DF6	DF7	CRC	Remark	Frame Size
0	CF	SF	ABS0	ABS1	ABS2						Include CRC	Position Read Command	6
1	CF	SF	ABM0	ABM1	ABM2								6
2	CF	SF	ENID									Encoder Identification	4
3	CF	SF	ABS0	ABS1	ABS2	ENID	ABM0	ABM1	ABM2	ALMC		Position Read Command	11
4	CF	SF	ABS0	ABS1	ABS2	ENID	ABM0	ABM1	ABM2	TEMP			11
6	CF	ADF	EDF									Memory or Register Write Command	4
7	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to perform Alarm Clear Command	6
8	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to perform ST Zero Reset Command	6
C	CF	SF	ABS0	ABS1	ABS2							Consecutive 10x to perform MT & Alarm Clear Command	6
D	CF	ADF	EDF									Memory or Register Read Command	4

NOTE:

- **ABSn:** Single-turn counts; LSB of the single-turn counts is located in ABS0 and MSB of the counts, data is located in ABS2.
- **ABMn:** Multi-turn counts; LSB of the multi-turn counts is located in ABM0 and MSB of the counts, data is located in ABM2.
- **ENID:** Encoder single-turn bits identification in 8-bit format; for example, 23-bit output is set to 17h.
- **ALMC:** Encoder alarm data in 8-bit format.
- **TEMP:** Encoder temperature readout data in 8-bit format.

Alarm

Details of the alarm bit are available in the following register.

Byte (Alarm)	Bit(s)	Bit							
		7	6	5	4	3	2	1	0
Byte 3	[31:24]	0	0	0	OVS	MT_Track	0	0	0
Byte 2	[23:16]	0	0	XC	0	0	0	BB_cfg	OVF
Byte 1	[15:8]	0	0	0	Temp	Mem	0	ST_Track	0
Byte 0	[7:0]	OV	UV	MHI	MLO	BE	BA	0	0

Byte (Alarm)	Address Associated with Alarm				
	Status	Enable	Latch	Warning Mask	Error Mask
Byte 3	Page 9, 0x24	Page 7, 0x20	Page 7, 0x24	Page 7, 0x28	Page 7, 0x2C
Byte 2	Page 9, 0x25	Page 7, 0x21	Page 7, 0x25	Page 7, 0x29	Page 7, 0x2D
Byte 1	Page 9, 0x26	Page 7, 0x22	Page 7, 0x26	Page 7, 0x2A	Page 7, 0x2E
Byte 0	Page 9, 0x27	Page 7, 0x23	Page 7, 0x27	Page 7, 0x2B	Page 7, 0x2F

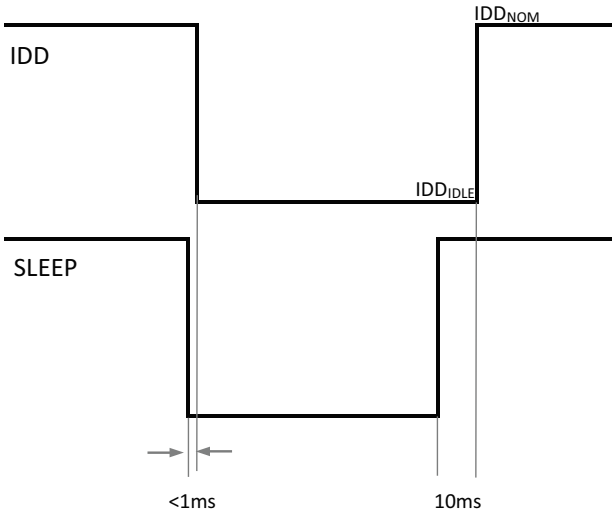
- **Multi-Turn Over Speed (OVS) Alarm:** This indicates the over-speed detection during the multi-turn counting in battery mode.
- **Multi-Turn Tracker (MT_Track) Error:** This indicates that the multi-turn position is potentially wrong due to the single-turn position count.
- **Multi-Turn Counter Comparison (XC) Alarm:** This indicates that the raw multi-turn position is not a match with the software multi-turn position count.
- **Multi-Turn Battery Backup Configuration (BB_cfg) Alarm:** This indicates that corruption of the multi-turn battery backup configuration has occurred.
- **Multi-Turn Overflow (OVF) Alarm:** This indicates overflow of the multi-turn counting.
- **Temperature (Temp) Alarm:** This indicates that the temperature has exceeded the temperature limit setting.
- **Memory (Mem) Error:** This indicates that memory corruption has occurred. When this is set high, perform a power cycle to reload the memory. The value for this alarm is represented as 1.
- **Single-Turn Tracker (ST_Track) Error:** This indicates that the angular error has exceeded 5° within 5 ms. When this is set high consistently, perform a power cycle to reinitialize the sensor. The value for this alarm is represented as 1.
- **Overvoltage (OV) Error:** This indicates that the input supply has exceeded the limit. When this is set high consistently, check the supply line. The value for this alarm is represented as 1.
- **Undervoltage (UV) Error:** This indicates that the input supply has dropped below the limit. When this is set high consistently, check the supply line. The value for this alarm is represented as 1.
- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is set high consistently, change to a weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error:** This indicates that the magnet strength detected by the chip is too weak. When this is set low consistently, change to a stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Battery-Backup Multi-Turn Battery Error (BE):** This indicates that the battery level is below 3.0V. When this is set high consistently, the battery must be replaced and the multi-turn counter will be reset. The multi-turn counter will not function during battery mode.
- **Battery-Backup Multi-Turn Battery Alarm (BA):** This indicates that the battery level is below 3.2V. Replacing the battery is recommended. The multi-turn counter is functioning during battery mode.

Power Modes

The AEAT-9988M is designed with two power modes:

- **Active Mode** where the chip operates under full functions with normal current consumption, IDD_{NOM}.
- **Sleep Mode** powers down the chip front-end and digital processing blocks, leaving only the detection block to track on user input with low current consumption, IDD_{IDLE}.
- The SLEEP pin is an active low, tied to VDDA if unused.
- The wake-up duration can be configured in Page 7, Address 0x1Ah : Sleep [3:0].

Figure 20: Sleep Mode Timing



PWM

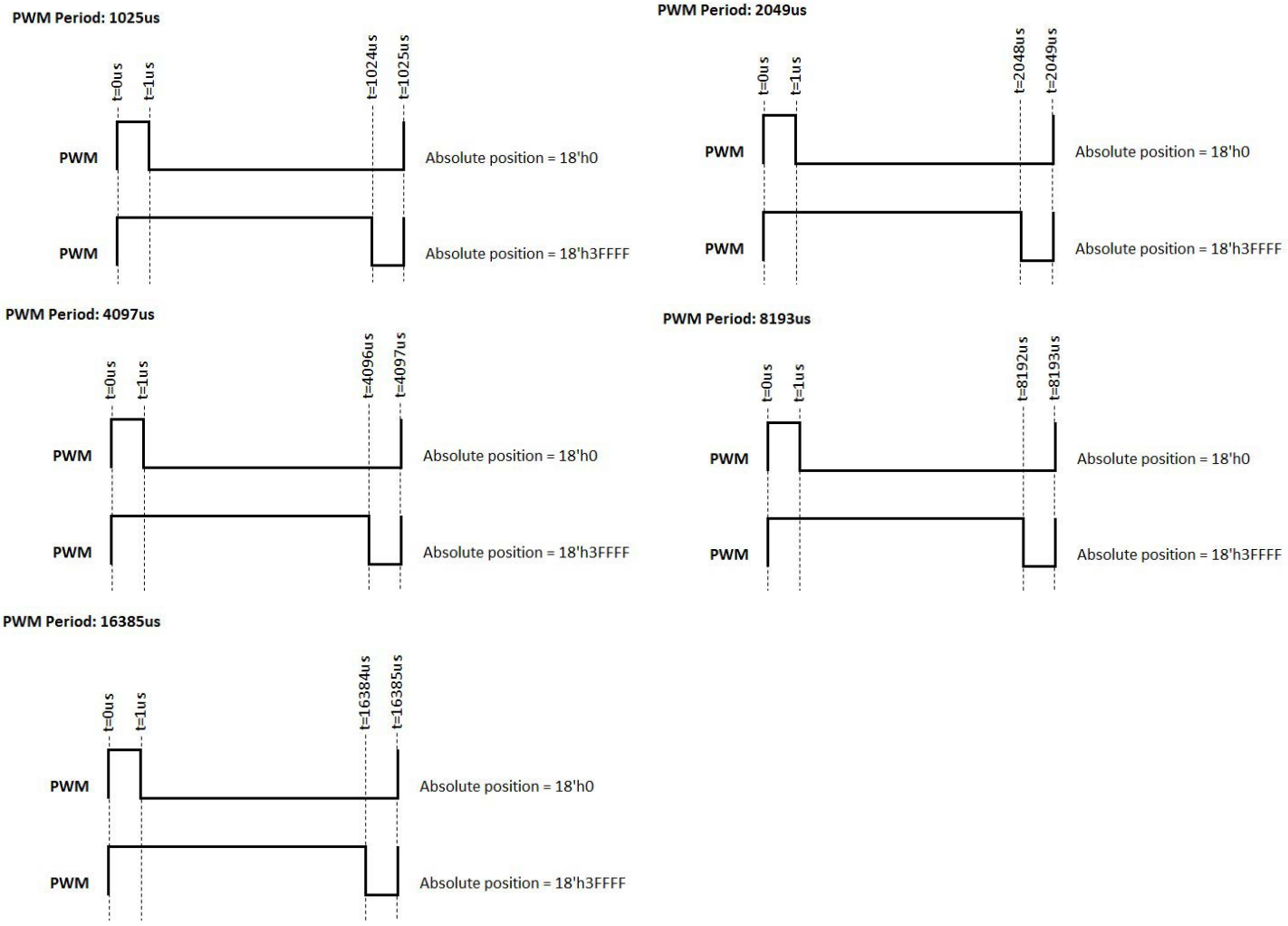
The PWM protocol uses one output pin (PA5) from the AEAT-9988M.

PWM Fixed Clock

The PWM signals are configurable to have a period of 1025, 2049, 4097, 8193, or 16385 µs. During power-up, the PWM signal is 0 before the chip is ready.

PWM Signals (Period = 1025/2049/4097/8193/16385 µs)

PWM Period: 1025, 2049, 4097, 8193, 16385 µs

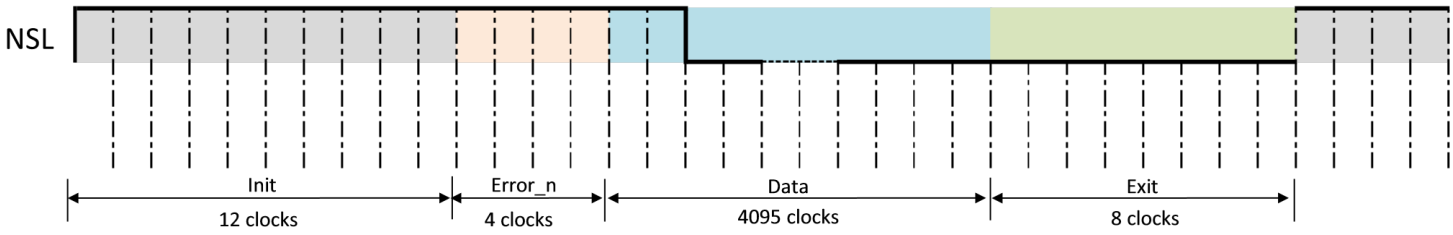


PWM Fixed Period

The PWM protocol is also available with Init, Error_n, and Exit, along with Data information.

PWM Signals (Period = 1047/2071/4119/8215/16407 µs)

PWM Period: 4119 µs



Incremental Output Format

The AEAT-9988M provides ABI and UVW signals to indicate the incremental position of the motor.

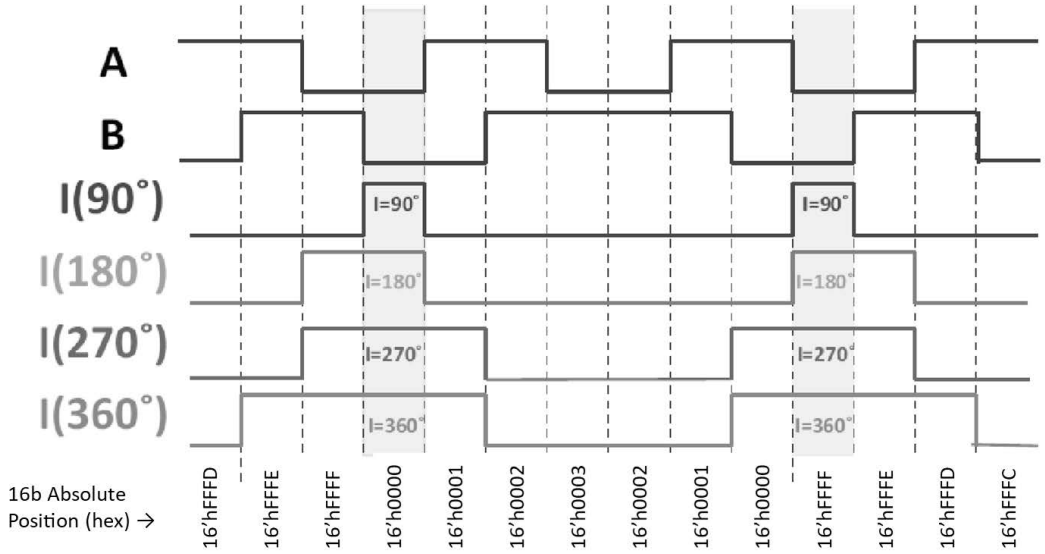
ABI

The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B and I).

The index signal marks the absolute angular position and typically occurs once per revolution. The ABI signal is configurable using the memory map registers. It supports the following configuration:

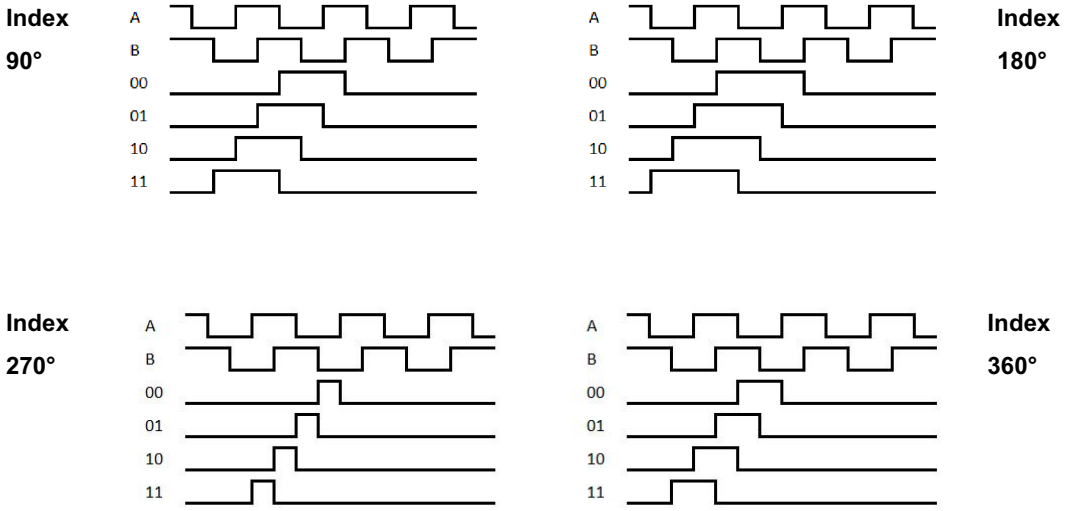
- Programmable CPR: 0 to 65,536 CPR
- Programmable I-width: 90, 180, 270 or 360 electrical degrees (edeg)
- Programmable I-state: 90, 180, 270 or 360 electrical degrees (edeg)

Figure 21: ABI Signal (4096 CPR, with Different I-Width Settings), Assuming Hysteresis is Set at 0.02 Mechanical Degrees



The index position is configurable among the incremental states.

The index signal rises high once per turn at the absolute zero position.



The number of indexes per revolution is configurable from 1 pulse up to 256 pulses.

Figure 22: 1 Index per Revolution

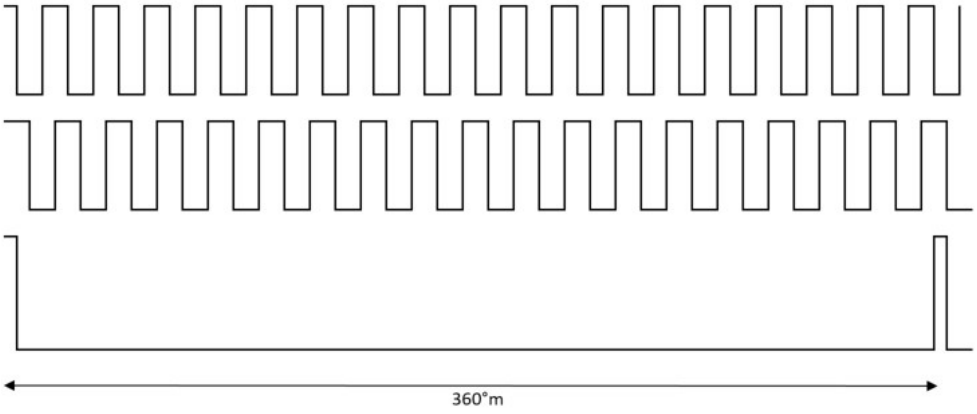
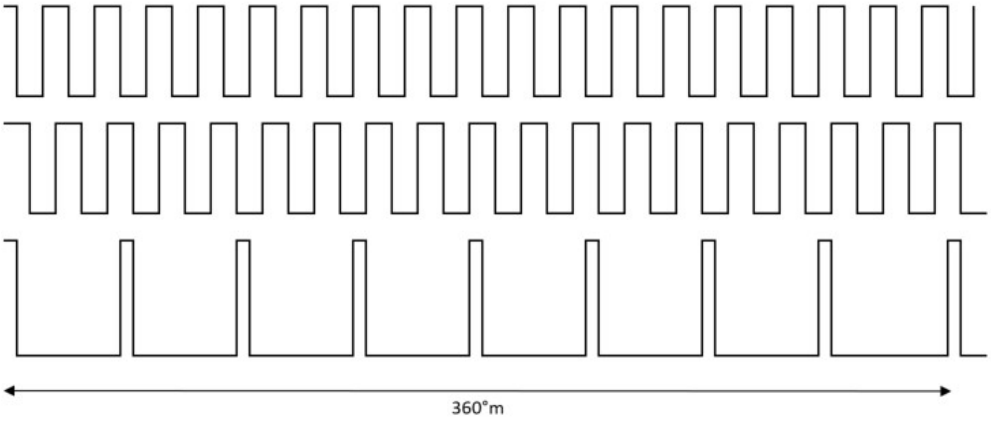


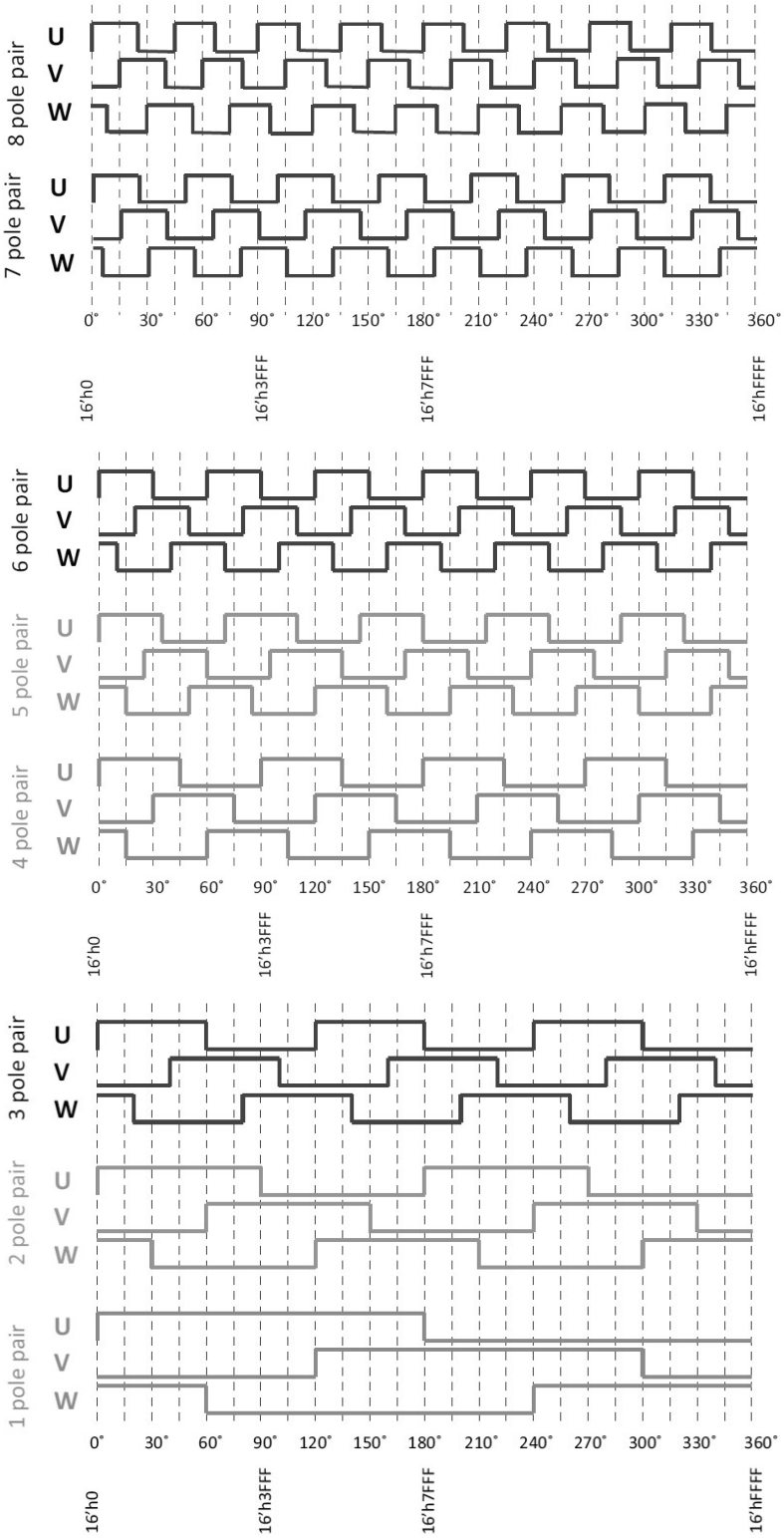
Figure 23: 8 Indexes per Revolution



UVW

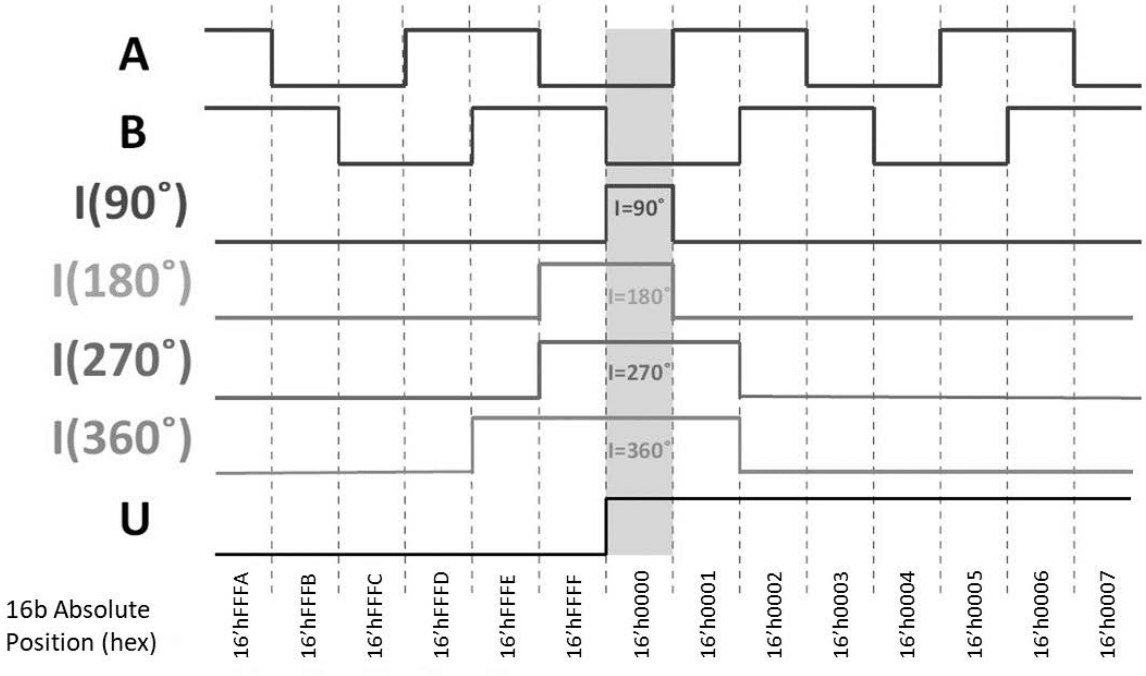
Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback.

The AEAT-9988M can configure pole pairs from 1 to 64 (equivalent to 2 to 128 poles).



NOTE: Signal U from the UVW protocol is tagged to signal I from the ABI protocol as shown in the following figure.

Figure 24: U-to-I Tagging



Recommended PCB Land Pattern (in mm)

Figure 25: Recommended PCB Land Pattern Details

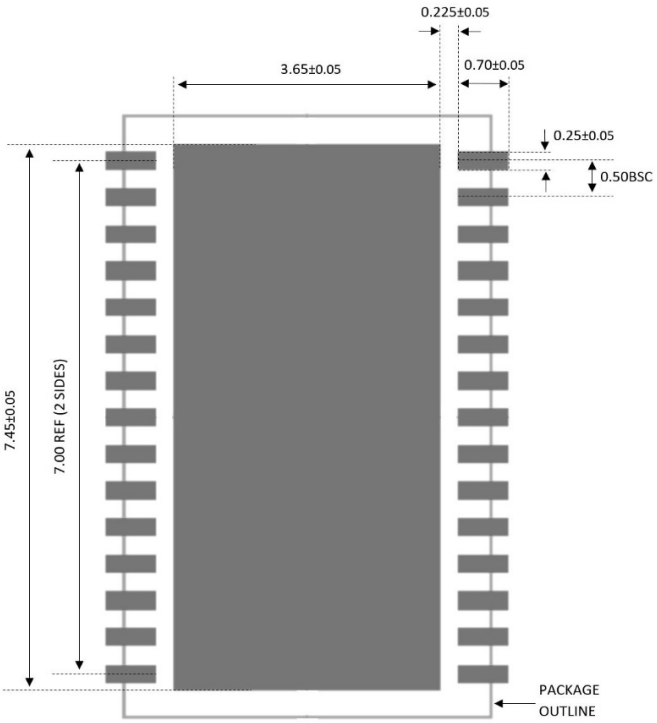
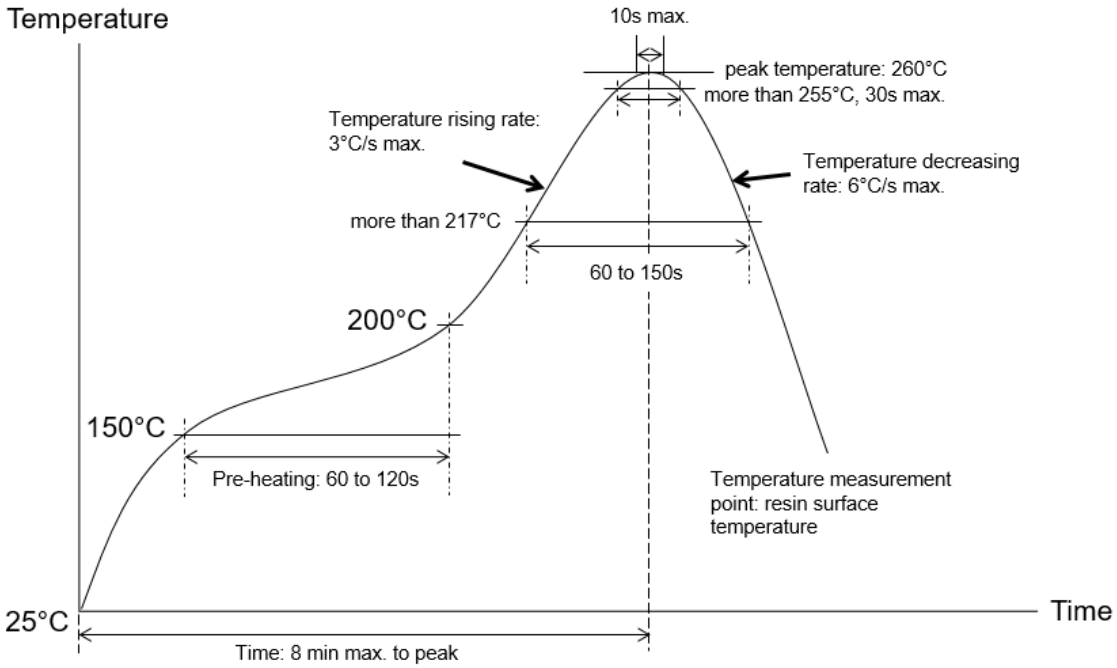


Figure 26: Recommended Lead-Free Solder Reflow Temperature Profile



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