BROADCOM®

Application Note

AEAT-9955

Magnetic Encoder IC: 10-Bit to 18-Bit Programmable Angular Magnetic Encoder with Safety

Description

The Broadcom® AEAT-9955 is a CMOS magnetic sensor structure that is suitable for contactless 360° encoding based on the Hall effect. It provides an angle output up to 18 bits of resolution and simultaneous incremental output up to 20,000 CPR. An integrated Hall structure at the core of the device uses a single 2-pole disc or ring magnet to convert the magnetic field vector in the chip plane into an AC signal whose amplitude and phase correspond to the magnitude and direction of the field.

An internal digital-signal-processing unit then processes and conditions the raw AC signal from the sensor. The output signals are available in three different forms:

- Pulse-width modulation (PWM)
- Absolute 18-bit position through the 3-wire and 2-wire Synchronous Serial Interface (SSI) and the 4-wire Serial Protocol Interface (SPI)
- Incremental output (ABI and UVW signals)

These features can be programmed by configuring the internal registers in program mode.

More information about the AEAT-9955 product specifications is available in the product data sheet.

Operation Mode

The AEAT-9955 features two types of operational modes: normal operation mode and configuration mode.

Normal Operation Mode

Normal mode is the normal operating mode of the chip. The absolute output (10-bit to 18-bit absolute position data) is available through serial protocol pins (M0, M1, M2, and M3). The following are the output signal conditions during AEAT-9955 initialization:

- PWM signals all 0s
- ABI signals all 1s
- UVW signals all 0s

The incremental positions are indicated on ABI and UVW signals with a user-configurable CPR from 0 to 20,000 of ABI signals and pole pairs from 1 to 32 (2 to 64 poles) for UVW commutation signals.

Configuration Mode

The AEAT-9955 has a built-in memory for multiple-time programming (MTP).

Programming of the AEAT-9955 can be performed with the HEDS-9955 programming kit or any tester/programmer device using the guidelines provided.

Absolute and Incremental Programming

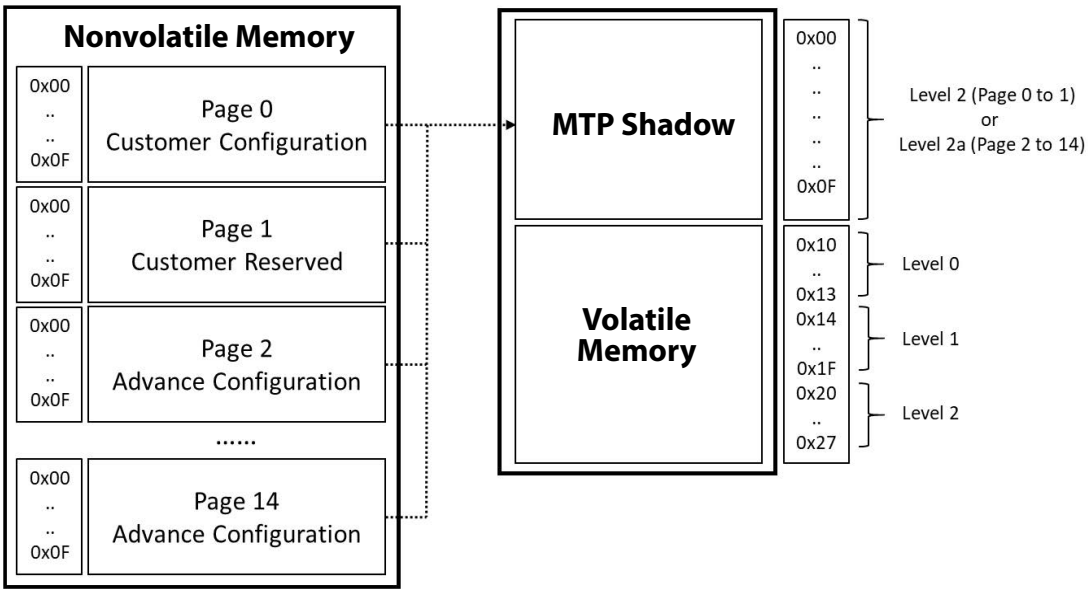
The absolute resolution can be set to 10, 11, 12, 13, 14, 15, 16, 17, or 18 bits. For incremental selection, ABI or UVW can be selected by following the instructions in the following sections. The PWM output is available as well.

The shadow registers are programmable using the SPI protocol. Writing specific commands to specific addresses of the internal registers will program values of shadow registers to memory. The memory can be programmed multiple times.

Memory Map

The AEAT-9955's memory consists of nonvolatile memory and volatile memory. The following figure illustrates the concept of nonvolatile memory, which is loaded into the MTP shadow.

Figure 1: Nonvolatile/Volatile Memory and MTP Shadow Block Diagram



MTP shadow registers are nonvolatile (upon power-up, the values are reloaded from EEPROM) and are not automatically written to EEPROM. To write MTP shadow register values to EEPROM (nonvolatile) memory, see EEPROM Programming. Additionally, EEPROM programming can be performed at a supply voltage of 3.3V or 5V. The MTP shadow registers are from address 0x00 to address 0x27. The following table lists the configurations of the volatile memory for address 0x20 to 0x2F.

Table 1: Volatile Memory

Address	Bit(s)	Name	Description
0x20 to 0x28	N/A	Factory Reserved	Factory reserved.
0x29	[7:0]	Chip Status	See Alarm.
0x2A	[7]	Memory Busy	Memory busy bit. 0: EEPROM programming completed 1: EEPROM programming in progress
	[6]	OTP Unlocked	OTP unlocked status. 0: Locked 1: Unlocked
	[3:2]	Zero Reset Status	Zero reset status. 10: Calibration pass 11: Calibration fail
	[1:0]	Auto Calibration Status	Calibration status. 10: Calibration pass 11: Calibration fail
0x2B	[7:0]	Chip ID	Chip identification.
0x2C to 0x2F	N/A	Factory Reserved	Factory reserved.

Customer Configuration Registers

The following registers are available for users to store information and configure the encoder as required.

Table 2: Customer Reserved Registers (Page 1)

Address	Bit(s)	Name	Description	Default
0x00	[7:0]	Customer Reserve 0	User programmable	8'h0
0x01	[7:0]	Customer Reserve 1	User programmable	8'h0
0x02	[7:0]	Customer Reserve 2	User programmable	8'h0
0x03	[7:0]	Customer Reserve 3	User programmable	8'h0
0x04	[7:0]	Customer Reserve 4	User programmable	8'h0
0x05	[7:0]	Customer Reserve 5	User programmable	8'h0
0x06	[7:0]	Customer Reserve 6	User programmable	8'h0
0x07	[7:0]	Customer Reserve 7	User programmable	8'h0
0x08	[7:0]	Customer Reserve 8	User programmable	8'h0
0x09	[7:0]	Customer Reserve 9	User programmable	8'h0
0x0A	[7:0]	Customer Reserve 10	User programmable	8'h0
0x0B	[7:0]	Customer Reserve 11	User programmable	8'h0
0x0C	[7:0]	Customer Reserve 12	User programmable	8'h0
0x0D	[7:0]	Customer Reserve 13	User programmable	8'h0
0x0E	[7:0]	Customer Reserve 14	User programmable	8'h0
0x0F	[7:0]	Customer Reserve 15	User programmable	8'h0

Table 3: Customer Configuration Registers (Page 0)

Address	Bit(s)	Name	Description	Default
0x00	[7]	Safety Bit	Enables the safety feature in the serial interface. 1: Enable safety. 0: Disable safety.	1
	[6]	CRC Select	Selects the CRC type when the “Safety bit” = 1. 1: 16b CRC (CCITT False) 0: 8b CRC (SAE J1850)	1
	[5:4]	CRC Initialize	CRC initialize value when the “Safety bit” = 1. 00: 16’h0000 / 8’h00 01: 16’h5555 / 8’h55 10: 16’hAAAA / 8’hAA 11: 16’hFFFF / 8’hFF	11
	[3:0]	SC Initialize	Sequence Counter initialize value when the “Safety bit” = 1. 0000: 1 : 1111: 16	0000

Table 3: Customer Configuration Registers (Page 0) (Continued)

Address	Bit(s)	Name	Description	Default
0x01	[7]	Alarm Latch	Alarm report condition. 1: Triggered alarm remains until user clears or power-cycles. 0: Triggered alarm resets once error recovered.	1
	[6]	SPI Output High-Z	Enable high impedance mode. 1: Disable high-z. 0: Enable high-z.	1
	[5]	Reserved	Reserved.	0
	[4]	Abs. Hysteresis Off	Turn Off absolute position hysteresis. 1: Turn Off absolute position hysteresis. 0: Do not turn Off absolute position hysteresis (follow the Level 2a setting).	0
	[3]	Inc. Safety Off	Turn Off incremental output (ABI/UVW) safe state. 1: Turn Off incremental output (ABI/UVW) safe state. 0: Turn On incremental output (ABI/UVW) safe state.	0
	[2]	Accuracy Cal Skip	Skip accuracy calibration during auto-calibration. 1: Turn Off accuracy calibration during auto-calibration. 0: Do not turn Off accuracy calibration during auto-calibration (follow the Level 2a setting).	0
	[1]	Auto-calibration Hardware Hold Time	Time required to enable auto-calibration on the M1 pin. 1: Auto-calibration started after holding M1 pin = 1 for 50 ms. 0: Auto-calibration started after holding M1 pin = 1 for 1 ms.	0
	[0]	Multiple Auto-calibration Hardware	Enable multiple use of auto-calibration on the M1 pin. 1: Does not automatically clear auto-calibration hardware (page 0, 0x06[7]) after auto-calibration using the M1 pin. 0: Automatically clear auto-calibration hardware (page 0, 0x06[7]) after auto-calibration using the M1 pin.	0
0x02	[7:4]	Magnetic High	Magnetic field input high limit. 0000: 0 (lowest limit) 1111: 15 (highest limit)	1011
	[3:0]	Magnetic Low	Magnetic field input low limit. 0000: 0 (lowest limit) 1111: 15 (highest limit)	0101

Table 3: Customer Configuration Registers (Page 0) (Continued)

<table>
<tr><th>Address</th><th>Bit(s)</th><th>Name</th><th>Description</th><th>Default</th></tr>
<tr><td rowspan="2">0x03</td><td>[7:4]</td><td>Filter Config1 (Level 1)</td><td>[7:4] = Position filter configuration.</td><td>0000</td></tr>
<tr><td>[3:0]</td><td>Lag Compensation Adjustment</td><td>[3:0] = Lag composition adjustment on lag compensation value.
Recommend the following configuration set for a different filter.
<table><tr><th>Filter Value</th><th>Filter Config1 [7:4]</th><th>Lag Compensation Adjustment [3:0] (Recommended)</th></tr><tr><td>Follow Filter Config2 (Level 2a)</td><td>0000</td><td>0000</td></tr><tr><td>163 µs</td><td>0001</td><td>1000</td></tr><tr><td>237 µs</td><td>0010</td><td>1000</td></tr><tr><td>491 µs</td><td>0011</td><td>1000</td></tr><tr><td>655 µs</td><td>0100</td><td>1000</td></tr><tr><td>984 µs</td><td>0101</td><td>1000</td></tr><tr><td>1.3 ms</td><td>0110</td><td>1000</td></tr><tr><td>1.6 ms</td><td>0111</td><td>0111</td></tr><tr><td>2.0 ms</td><td>1000</td><td>0111</td></tr><tr><td>2.3 ms</td><td>1001</td><td>1010</td></tr><tr><td>2.6 ms</td><td>1010</td><td>1000</td></tr><tr><td>3.3 ms</td><td>1011</td><td>1101</td></tr><tr><td>3.9 ms</td><td>1100</td><td>1110</td></tr><tr><td>4.6 ms</td><td>1101</td><td>1100</td></tr><tr><td>5.2 ms</td><td>1110</td><td>1000</td></tr><tr><td>6.6 ms</td><td>1111</td><td>1111</td></tr></table></td><td>0000</td></tr>
<tr><td>0x04</td><td>[7:0]</td><td>Reserved</td><td>Reserved</td><td>0</td></tr>
<tr><td rowspan="4">0x05</td><td>[7:5]</td><td>Multi-Index</td><td>Number of indexes per revolution.
000: 1 pulse
001: 2 pulses
010: 4 pulses
011: 8 pulses
100: 16 pulses
101: 32 pulses
110: 64 pulses
111: 128 pulses</td><td>000</td></tr>
<tr><td>[4]</td><td>Reserved</td><td>Reserved.</td><td>00000</td></tr>
<tr><td>[3:2]</td><td>Acceleration Configuration</td><td>Configuration for acceleration/deceleration response.
00: Basic
01: Moderately aggressive
10: Highly aggressive
11: Basic</td><td>00</td></tr>
<tr><td>[1:0]</td><td>Reserved</td><td>Reserved.</td><td>0</td></tr>
</table>

Table 3: Customer Configuration Registers (Page 0) (Continued)

Address	Bit(s)	Name	Description	Default
0x06	[7]	Auto-calibration Hardware	Enables auto-calibration on the M1 pin. 0: Disable calibration. 1: Enable calibration.	0
	[6:4]	Sensing Axis	Sensing axis configuration selection. 000: On-Axis 101: Off-Axis (radial) 110: Off-Axis (axial) 111: Off-Axis (side shaft)	000
	[3:0]	Vertical Hall Selection[a]	Vertical Hall selection (off-axis only). 1000: VH#1 0100: VH#2 0010: VH#3 0001: VH#4 Other 4-bit combination values are invalid.	0000
0x07	[7:6]	SPI4 Mode	SPI4 mode selection (per the MATS Table). 00: SPI4-16 (16-bit parity) 01: SPI4-24a (24-bit parallel CRC) 10: SPI4-24b (24-bit serial CRC) 11: SPI4-8 (8-bit safety)	00
	[5:0]	UVW Resolution[b]	Commutation output pole-pair selection. 000000: 0 pole pairs / OFF 000001: 1 pole pair : 011111: 31 pole pairs 100000: 32 pole pairs 100001: 32 pole pairs * Out-of-range limit to 32 pole pairs.	000011

Table 3: Customer Configuration Registers (Page 0) (Continued)

Address	Bit(s)	Name	Description	Default
0x08	[7:4]	PWM Resolution[b]	0000: PWM fixed period = 10 bits 0001: PWM fixed period = 11 bits 0010: PWM fixed period = 12 bits 0011: PWM fixed period = 13 bits 0100: PWM fixed period = 14 bits *0101-0111: Out of range, PWM fixed period = 14 bits 1000: PWM fixed clock = 10 bits 1001: PWM fixed clock = 11 bits 1010: PWM fixed clock = 12 bits 1011: PWM fixed clock = 13 bits 1100: PWM fixed clock = 14 bits *1101-1111: Out of range, PWM fixed clock = 14 bits	0000
	[3:2]	Index Width	Index width selection. 00: 90e° 01: 180e° 10: 270e° 11: 360e°	00
	[1:0]	Index State	Index location within incremental period selection. 00: A low B low 01: A low B high 10: A high B high 11: A high B low	00
0x09	[7]	PSEL[c]	Protocol mode selection with the MATS Table. 0: SSI3a / SSI2a / All SPI4 modes 1: SSI3b / SSI2b / PWM	0
	[6:0]	Incremental Resolution [14:8][d]	Incremental resolution selection.	0000100
0x0A	[7:0]	Incremental Resolution [7:0][d]	000-0000-0000-0000: 0 CPR (OFF) 000-0000-0000-0001: 1 CPR 000-0000-0000-0010: 2 CPR 000-0000-0000-0011: 3 CPR : 000-0000-1000-0000: 128 CPR : 000-0100-0000-0000: 1024 CPR : 010-0000-0000-0000: 8192 CPR : 100-1110-0010-0000: 20,000 CPR	00000000

Table 3: Customer Configuration Registers (Page 0) (Continued)

Address	Bit(s)	Name	Description	Default
0x0B	[7:5]	Hysteresis	Incremental output hysteresis selection. 000: Hysteresis OFF 001: 0.01m° 010: 0.02m° 011: 0.04m° 100: 0.08m° 101: 0.17m° 110: 0.35m° 111: 0.70m°	100
	[4]	Direction	Counting direction selection. 0: Count up in clockwise direction. 1: Count up in counter-clockwise direction.	0
	[3:0]	Single Turn Resolution	Absolute output resolution selection. 0000: 18 bits 0001: 17 bits : 1000: 10 bits * Out-of-range limit to 8-bit minimum.	0000

a. See Off-Axis Sensing Orientation.

b. UVW: Flexible 6-bit UVW resolution up to 32 pole pairs.
PWM: Only the shown setting is available; other combinations are invalid.

c. In conjunction with the MATS Table for input/output configuration.

d. Flexible 15-bit Incremental resolution up to 20,000 CPR. Combinations above 20,000 are invalid.

Table 4: Customer Single-Turn Reset (Page 0)

Address	Bit(s)	Name	Description	Default
0x0C	[7:0]	Zero Reset 2	MSB bit-17 to bit-10 of absolute single-turn.	0000-0000
0x0D	[7:0]	Zero Reset 1	Bit-9 to bit-2 of absolute single-turn.	0000-0000
0x0E	[7:6]	Zero Reset 0	LSB bit-1 to bit-0 of absolute single-turn.	00

Table 5: Advance Configuration (Page 2/5/8/11)

Address	Bit(s)	Name	Description	Default
0x00	[7:0]	Sin Static Gain [15:8]	Digital static gain multiplier value for sin/cos inputs, calculated using auto-calibration; to adjust digital sin/cos VPP to 1.8V equivalent. 0x0000 = 100% (exception) 0x0001 = ~0% : 0x4000 = 100% : 0xFFFF = 400%	0x00
0x01	[7:0]	Sin Static Gain [7:0]		0x00
0x02	[7:0]	Cos Static Gain [15:8]		0x00
0x03	[7:0]	Cos Static Gain [7:0]		0x00
0x04	[7:0]	Sin Static Offset [15:8]	Digital static offset value for sin/cos, calculated using auto-calibration; to adjust digital sin/cos Vmid to 1.0V equivalent. 0x8000 = –1.0V : 0x0000 = 0.0V : 0x7FFF = 1.0V	0x00
0x05	[7:0]	Sin Static Offset [7:0]		0x00
0x06	[7:0]	Cos Static Offset [15:8]		0x00
0x07	[7:0]	Cos Static Offset [7:0]		0x00
0x08	[7:4]	Sin Raw Gain	Analog raw gain configuration for sin.	0000
	[3:0]	Cos Raw Gain	Analog raw gain configuration for cos.	0000
0x09	[7:4]	Reserved	Reserved.	0000
	[3:0]	Hall Bias	Hall sensor bias current configuration.	Page 2: 1110 Others: 1101
0x0A	[7:0]	Reserved	Reserved.	0x00
0x0B	[7:0]	Reserved	Reserved.	0x00
0x0C	[7:0]	Cos Static Phase [15:8]	Digital static phase value for cos (w.r.t sin), calculated using auto-calibration; to maintain Cos/Sin phase delta per calibrated result. 0x0000 = 0 deg : 0x4000 = 90 deg : 0xFFFF = 360 deg	0x00
0x0D	[7:0]	Cos Static Phase [7:0]		0x00
0x0E	[7:0]	Reserved	Reserved.	0x00

Table 6: Advance Configuration (Page 3/6/9/12)

Address	Bit(s)	Name	Description	Default
0x00	[7:0]	ADC Configuration	Fixed ADC configuration.	0x08
0x01	[7]	Dynamic Offset Enable	Enable dynamic offset correction. 1: Enable dynamic offset correction. 0: Disable dynamic offset correction.	1
	[6:0]	Fixed Configuration	Fixed test configuration.	0000000
0x02	[7]	Dynamic Gain Enable	Enable dynamic gain correction. 1: Enable dynamic gain correction. 0: Disable dynamic gain correction.	1
	[6:5]	Phase Measure Configuration (dft_en)	Phase measure configuration. 00: No phase measurement. 01: Phase measurement always ON. 10: Phase measurement ON after Offset/Gain values stable. 11: Phase measurement ON after 10 iterations of Offset/Gain value evaluation.	Page 3: 00 Others: 10
0x03	[7]	Dynamic Phase Enable	Enable dynamic phase correction. 1: Enable dynamic phase correction. 0: Disable dynamic phase correction.	Page 3: 0 Others: 1
	[6:5]	Phase Hysteresis	Phase hysteresis for phase correction. 00: 0.04 deg 01: 0.08 deg 10: 0.17 deg 11: 0.34 deg	Page 3: 00 Others: 01
0x04	[7:0]	Fixed Configuration	Fixed test configuration.	0x55
0x05	[7]	Fixed Configuration	Fixed configuration.	0
	[6:4]	doc_st_delta	Dynamic offset stabilizer configuration. Acceptance range to consider as “stable” offset. Higher = Lower sensitivity.	001
	[3:2]	doc_st_step	Dynamic offset stabilizer configuration. Rate of switching of Stabilizer state. 00: No change of Stabilizer state upon power-up. Higher = Higher sensitivity.	11
	[1:0]	doc_st_init	Dynamic offset stabilizer configuration. State of stabilizer at power-up. 00: Very unstable (high sensitivity). 01: Slightly unstable (middle sensitivity). 10: Slightly stable (middle sensitivity). 11: Very stable (low sensitivity).	11

Table 6: Advance Configuration (Page 3/6/9/12) (Continued)

Address	Bit(s)	Name	Description	Default
0x06	[7]	Fixed Configuration	Fixed configuration.	0
	[6:4]	dgc_st_delta	Dynamic gain stabilizer configuration. Acceptance range to consider as “stable” gain. Higher = Lower sensitivity.	001
	[3:2]	dgc_st_step	Dynamic gain stabilizer configuration. Rate of switching of Stabilizer state. 00: No change of Stabilizer state upon power-up. Higher = Higher sensitivity.	11
	[1:0]	dgc_st_init	Dynamic gain stabilizer configuration. State of stabilizer at power-up. 00: Very unstable (high sensitivity). 01: Slightly unstable (middle sensitivity). 10: Slightly stable (middle sensitivity). 11: Very stable (low sensitivity).	11
0x07	[7]	Fixed Configuration	Fixed configuration.	0
	[6:4]	dpc_st_delta	Dynamic phase stabilizer configuration. Acceptance range to consider as “stable” phase. Higher = Lower sensitivity.	001
	[3:2]	dpc_st_step	Dynamic phase stabilizer configuration. Rate of switching of Stabilizer state. 00: No change of Stabilizer state upon power-up. Higher = Higher sensitivity.	11
	[1:0]	dpc_st_init	Dynamic phase stabilizer configuration. State of stabilizer at power-up. 00: Very unstable (high sensitivity). 01: Slightly unstable (middle sensitivity). 10: Slightly stable (middle sensitivity). 11: Very stable (low sensitivity).	11

Table 6: Advance Configuration (Page 3/6/9/12) (Continued)

Address	Bit(s)	Name	Description	Default
0x08	[7:4]	Filter Config2 (Level 2a)	Position filter configuration. 0000: Dynamic Filter 0001: 163 µs 0010: 237 µs 0011: 491 µs 0100: 655 µs 0101: 984 µs 0110: 1.3 ms 0111: 1.6 ms 1000: 2.0 ms 1001: 2.3 ms 1010: 2.6 ms 1011: 3.3 ms 1100: 3.9 ms 1101: 4.6 ms 1110: 5.2 ms 1111: 6.6 ms	0000
	[3:0]	Fixed Configuration	Fixed test configuration.	1011
0x09	[7:4]	Dyn. Filter Slope	Configuration for Dynamic Filter. See Dynamic and Static Filter Function for further explanation.	0101
	[3:0]	Dyn. Filter Y-intercept		0011
0x0A	[7:4]	Dyn. Filter Max		0001
	[3:0]	Dyn. Filter Min		0110
0x0B	[7:3]	Reserved		00000
	[2:0]	Dyn. Filter Hysteresis		011
0x0C	[7]	Reserved	Reserved.	0
	[6]	Acceleration Algorithm	1 to enable the acceleration algorithm.	1
	[5]	Stop Algorithm	1 to enable the break algorithm.	0
	[4]	Deceleration Algorithm	1 to enable the deceleration algorithm.	1
	[3]	Speed interpolation	1 to enable speed info interpolation.	1
	[2:0]	Filter Compensation	19b configuration for filter compensation. 0x78C5C: Default, optimize for constant speed application. 0x58C50: Optimize for high acceleration/deceleration application. 0x58C4C: Balance between constant speed and high acceleration/deceleration.	0x7
0x0D	[7:0]			0x8C
0x0E	[7:0]			0x5C

Table 7: Advance Configuration (Page 4/7/10/13)

Address	Bit(s)	Name	Description	Default
0x00	[7:0]	Fixed Configuration	Fixed configuration.	Page 13: 0x80 Others: 0xE6
0x01	[7:0]	Fixed Configuration	Fixed configuration.	0x80
0x02	[7:0]	Fixed Configuration	Fixed configuration.	0x44
0x03	[7:0]	Fixed Configuration	Fixed configuration.	Page 13: 0x77 Others: 0x44
0x04	[7:6]	Fixed Configuration	Fixed configuration.	01
	[5:4]	Accuracy Calibration Enable	00: Perform accuracy calibration as part of auto-calibration. 11: Do not perform accuracy calibration as part of auto-calibration. Etc: Invalid.	00
	[3:2]	Raw Gain Calibration Enable	10: Perform raw gain calibration as part of auto-calibration. 11: Do not perform raw gain calibration as part of auto-calibration. Etc: Invalid.	10
	[1]	Gain Calibration Enable	0: Perform digital gain calibration. 1: Do not perform digital gain calibration.	0
	[0]	Offset Calibration Enable	0: Perform digital offset calibration. 1: Do not perform digital offset calibration.	0
0x05	[7:0]	Fixed Configuration	Fixed configuration.	0x25
0x06	[7:0]	Fixed Configuration	Fixed configuration.	0x73
0x07	[7:0]	Fixed Configuration	Fixed configuration.	Page 4: 0x88 Others: 0x80

Table 7: Advance Configuration (Page 4/7/10/13) (Continued)

Address	Bit(s)	Name	Description	Default
0x08	[7:5]	Absolute Pos. Hysteresis Max	Configuration for absolute position hysteresis. 000: hys2_max = 0.02 deg 001: hys2_max = 0.04 deg 010: hys2_max = 0.08 deg 011: hys2_max = 0.17 deg 100: hys2_max = 0.35 deg 101: hys2_max = 0.70 deg 110: hys2_max = 1.4 deg 111: Turn OFF absolute position hysteresis See Position Data Hysteresis for further explanation.	110
	[4:2]	Absolute Pos. Hysteresis Min	Configuration for absolute position hysteresis. 000: hys2_min = 0 deg 001: hys2_min = 0.003 deg 010: hys2_min = 0.005 deg 011: hys2_min = 0.011 deg 100: hys2_min = 0.022 deg 101: hys2_min = 0.044 deg 110: hys2_min = 0.088 deg 111: hys2_min = 0.176 deg See Position Data Hysteresis for further explanation.	Page 4: 110 Others: 111
	[1:0]	Absolute Pos. Hysteresis Configuration	Configuration for absolute position hysteresis. 00: hys2_cfg = 0.5 01: hys2_cfg = 1 10: hys2_cfg = 2 11: hys2_cfg = 4 See Position Data Hysteresis for further explanation.	00
0x09	[7:0]	Filter Compensation Factor	Decimal 0 – 1023 for the lag compensation calculation. Each step increases/reduces the compensation equivalent to 80 ns.	Page 4: 0x02BC Others: 0x0443
0x0A	[7:0]			
0x0B	[7:0]	Reserved	Reserved.	0x00
0x0C	[7:0]	Fixed Configuration	Fixed configuration.	0x04
0x0D	[7:0]	Fixed Configuration	Fixed configuration.	0x06
0x0E	[7:0]	Fixed Configuration	Fixed configuration.	0x0A

Table 8: Advance Configuration (Page 14)

Address	Bit(s)	Name	Description	Default
0x00	[7:0]	Fixed Configuration	Fixed configuration.	0x00
0x01	[7:0]	Fixed Configuration	Fixed configuration.	0x00
0x02	[7:0]	Debug	Set to 0x80 to read out sin/cos information.	0x00
0x03	[7:0]	Fixed Configuration	Fixed configuration.	0x00
0x04	[7:5]	Fixed Configuration	Fixed configuration.	111
	[4]	Filter Enable	0: Disable filter. 1: Enable filter.	1
	[3]	Filter Compensation Enable	0: Disable filter compensation. 1: Enable filter compensation.	1
	[2]	Fixed Configuration	Fixed configuration.	0
	[1]	Dynamic Correction (dc_clip)	0: Allow abrupt change on dynamic offset/gain/phase correction values. 1: Limit to gradual change on dynamic offset/gain/phase correction values.	1
	[0]	Fixed Configuration	Fixed configuration.	1
0x05	[7]	Accuracy Correction Enable	0: Disable accuracy correction. 1: Enable accuracy correction.	1
	[6:5]	Forced Test Enable	When Safety feature enabled (Page 0, address 0x00 [bit 7] = 1). 00: Disable power-up auto alarm check. 11: Enable power-up auto alarm check.	11
	[4]	ST Error Enable	0: Disable ST error. 1: Enable ST error.	1
	[3]	MHI Error Enable	0: Disable MHI error. 1: Enable MHI error.	1
	[2]	MLO Error Enable	0: Disable MLO error. 1: Enable MLO error.	1
	[1]	OV Error Enable	0: Disable OV error. 1: Enable OV error.	1
	[0]	UV Error Enable	0: Disable UV error. 1: Enable UV error.	1
0x06	[7:0]	Fixed Configuration	Fixed configuration.	0x00
0x07	[7:0]	Fixed Configuration	Fixed configuration.	0x00
0x08	[7:0]	Fixed Configuration	Fixed configuration.	0x00
0x09	[7:0]	Fixed Configuration	Fixed configuration.	0x00
0x0A	[7:0]	Fixed Configuration	Fixed configuration.	0x00
0x0B	[7:0]	Fixed Configuration	Fixed configuration.	0x00
0x0C	[7:0]	Fixed Configuration	Fixed configuration.	0x00
0x0D	[7:0]	Fixed Configuration	Fixed configuration.	0x00
0x0E	[7:0]	Fixed Configuration	Fixed configuration.	0x00

EEPROM Passcode (Level 2 Memory Access)

Perform the following steps to set a memory passcode:

1. Write value 8'hAB to address 0x10 to unlock Level 1 memory access.
2. Write the desired passcode 7x8 bits to the memory address from 0x18 to 0x1E.
3. Write 8'hBA to address 0x1F to set the passcode.

NOTE: The factory/default passcode is h00-h00-h00-h00-h00-h00-h00.

EEPROM Unlock

The AEAT-9955 consists of three levels of memory:

1. Level 0: No unlock required.
2. Level 1: Unlock required. To unlock, write address 0x10 = 8'hAB.
3. Level 2: Unlock required. To unlock, after unlocking Level 1, write address 0x18-0x1E = <User Passcode>.
4. Level 2a: Unlock required. To unlock, after unlocking Level 2, write address 0x1F = 8'hCD.

NOTE:

- Default user passcode = All 0s, meaning that no additional write is required at these addresses to unlock Level 2 if the user passcode has not been created.
- Level 2a access is available for date codes starting from January 2025. This access refers to the advanced configuration settings as shown in Table 5, Table 6, Table 7, and Table 8. These products are marked with identification "E", as shown in the following figure. Refer to Broadcom sales or factory resources for confirmation of the date codes.

EEPROM Page

Perform the following steps to load the EEPROM page to the MTP register:

1. Perform the steps in EEPROM Unlock to unlock the EEPROM.
2. To change the EEPROM page, write the desired page number to address 0x16 to load the selected EEPROM page into the MTP shadow register. For example, writing the value 0x00 to address 0x16 loads the Customer Configuration Registers (Page 0).

NOTE: Upon power-up, the MTP shadow register is loaded with the Customer Configuration Registers (Page 0).

EEPROM Programming

Perform the following steps to program the MTP shadow register to EEPROM:

1. Write the desired values to the current MTP register (Customer Reserve / Configuration Shadow register).
2. Verify the written value by reading back all registers.
3. Write value 8'hA1 to address 0x14 to program the current MTP registers to EEPROM.
4. Read memory busy bit[7] address 0x2A:
   – 0: EEPROM programming completed
   – 1: EEPROM programming in progress

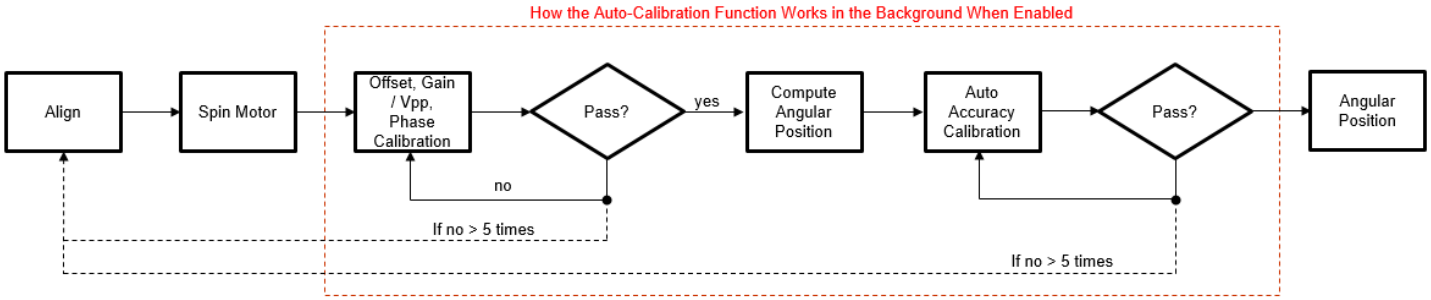
NOTE: EEPROM programming is required before changing the EEPROM page.

Encoder Calibration

Auto-Calibration Function

The AEAT-9955 encoder series comes with an Auto-Calibration function that utilizes a complex built-in algorithm to calibrate the encoder into achieving its most accurate angular accuracy. As it is designed for ease of use and cost-effectiveness by circumventing the need for a reference encoder, this calibration mode requires the users to simply align the magnet to the rotary shaft, rotate the magnet, and enable the Auto-Calibration function, and the AEAT-9955 encoder itself will perform the calibration and notify the user if the function is successfully completed. The following figure describes the sequence of this function.

Figure 2: AEAT-9955 Sequence of Auto-Calibration

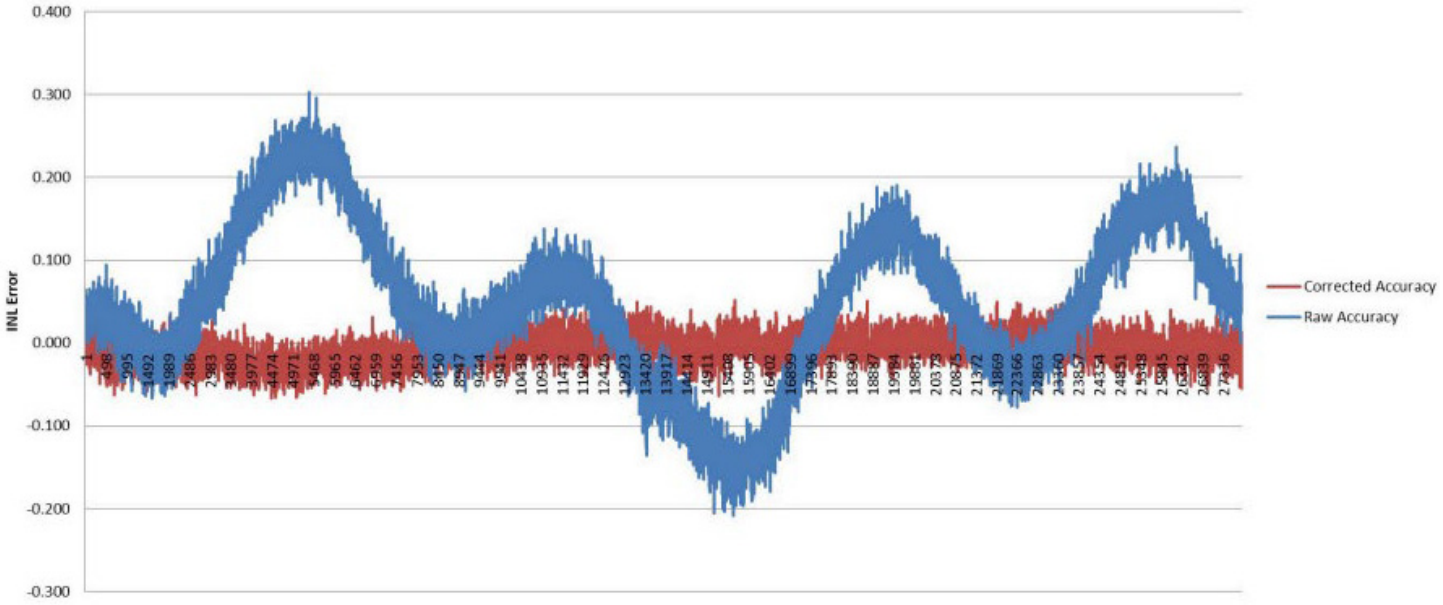


As shown in the preceding figure, upon enabling the Auto-Calibration function, the AEAT-9955 first calibrates the offset, gain, and phase of the sine/cosine signals that it receives from the magnet. This is the AEAT-9955 way of ensuring that the magnet is first properly aligned within an acceptable calibration range. If it is not, the AEAT-9955 will disqualify the calibration and notify the user that the calibration has failed. Otherwise, the AEAT-9955 will proceed to compute the angular position and perform the Auto-Calibration function.

The AEAT-9955 encoder series allows users to further adjust its internal settings in an attempt to pass this phase. In the case when either the magnet is not properly aligned or the magnet does not quite fit the specifications for an optimal performance, the user can adjust the AEAT-9955 internal settings to pass the calibration at the detriment of performance and overall accuracy.

The Auto-Calibration function first takes in the computed angular position and calculates the harmonics of the angular accuracy error present within a 360-degree rotation of a magnet and stores them as correction points within the AEAT-9955 internal memory. These correction points will then be used to compensate the errors to achieve an optimal accuracy. The following figure illustrates the before and after Auto-Calibration function and its accuracy difference.

Figure 3: AEAT-9955 Before and After Auto-Calibration



NOTE: For this function to be as effective as possible, the user must ensure that during calibration the speed of the rotation of the magnet is stable with as minimal of a speed ripple as possible.

Auto-Calibration without Lookup Table

The differences between the sampled actual positions and the calculated ideal positions are stored in the AEAT-9955's internal memory, referred to as the lookup table. Auto-calibration without the lookup table reflects the raw accuracy of the magnet system, as illustrated in Figure 3 (blue line: Raw Accuracy). This feature allows users to implement their own algorithms for lookup table compensation.

Auto-Calibration with Lookup Table

The lookup table represents the populated points of raw accuracy. Auto-calibration with the lookup table provides the corrected accuracy, calculated by subtracting the raw accuracy from the lookup table values, as illustrated in Figure 3 (red line: Corrected Accuracy).

Auto-calibration can be performed in two ways: either via an SPI register write-in or via hardware pin M1. The methods are described in the following two sections.

SPI Register Auto-Calibration

1. Mount the encoder to the motor system (with a magnet).
2. Rotate the magnet at a constant speed ranging from 10 rpm to 2000 rpm.
3. Once the speed stabilizes, write value 8'h2 to address 0x15 to initiate the calibration sequence.
4. Read the calibration status on bit [1:0] address 0x2A.
   – 10: Calibration pass
   – 11: Calibration fail
5. Write value 8'h0 to address 0x15 to exit the calibration sequence.
6. The calibration value is automatically stored in memory; no further programming is required.
   – To erase the calibration value, write value 8'h1 to address 0x15.
   – To return to operation mode, write value 8'h0 to address 0x15.

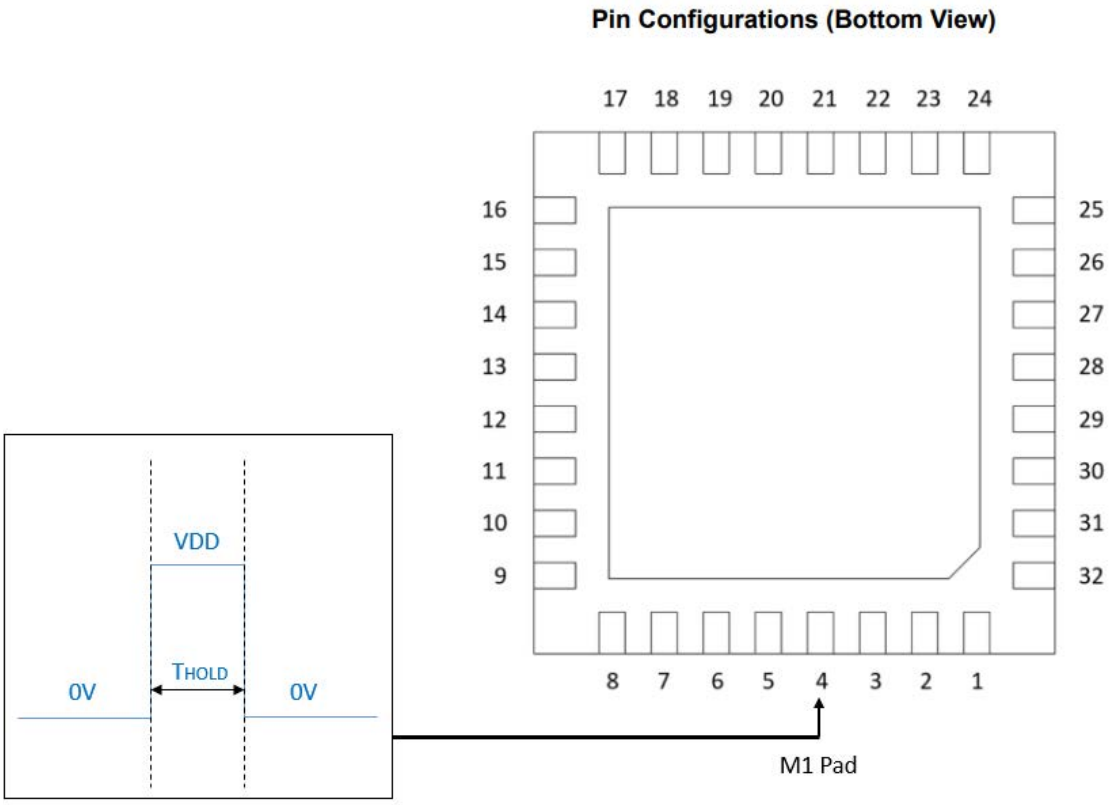
Hardware Pin M1 (Trigger) Calibration

1. Mount the encoder to the motor system (with a magnet).
2. Rotate the magnet at a constant speed ranging from 10 rpm to 2000 rpm.
3. Once the speed stabilizes, pull the signal high, M1 for more than 50 ms to initiate the calibration sequence.
4. Read the calibration status on output pin ABI.
   – If AB = 1, I = 0: Calibration pass
   – If AB = 1, I = 1: Calibration fail
5. The calibration value is automatically stored in memory; no further programming is required.

The AEAT-9955 not only allows users to perform its Auto-Calibration function through its various communication protocols via software means, it also allows users to perform the same calibration function via hardware through the use of one of its dedicated pads. This section explains how the hardware-based pad-initiated calibration can be performed and what settings can be changed to impact its behavior.

The following figure illustrates the pattern of signal necessary to trigger a pad-initiated calibration.

Figure 4: Method to Trigger Pad-Initiated Calibration



As per the preceding figure, to trigger a pad-initiated calibration, the user must send a signal into the pad 4 or M1 pad by triggering a valid VDD high for a T_{HOLD} duration of time while the magnet is rotating at stable speeds. Then the user must monitor the pad 8 or A pad, the pad 9 or B pad, and the pad 10 or I pad to know if the pad-initiated calibration is successful.

- If A/B/I = High/High/Low, calibration is successful.
- If A/B/I = High/High/High, calibration is not successful.

The flow of what occurs internally is as discussed earlier in the Auto-Calibration Function section. This means that should users want to modify the calibration steps, they may refer to the previous section. Although the internal calibration within the system is identical for both hardware- and software-triggered calibration, the method to initiate calibration differs. To further simplify pad-initiated calibration for customers, the AEAT-9955 offers several settings to adjust the criteria for triggering this function. See the settings in Table 3, Customer Configuration Registers (Page 0), which are as follows:

- Auto-calibration Hardware Hold Time (address 0x01 [bit 1])
- Multiple Auto-calibration Hardware (address 0x01 [bit 0])
- Auto-calibration Hardware (address 0x06 [bit 7])

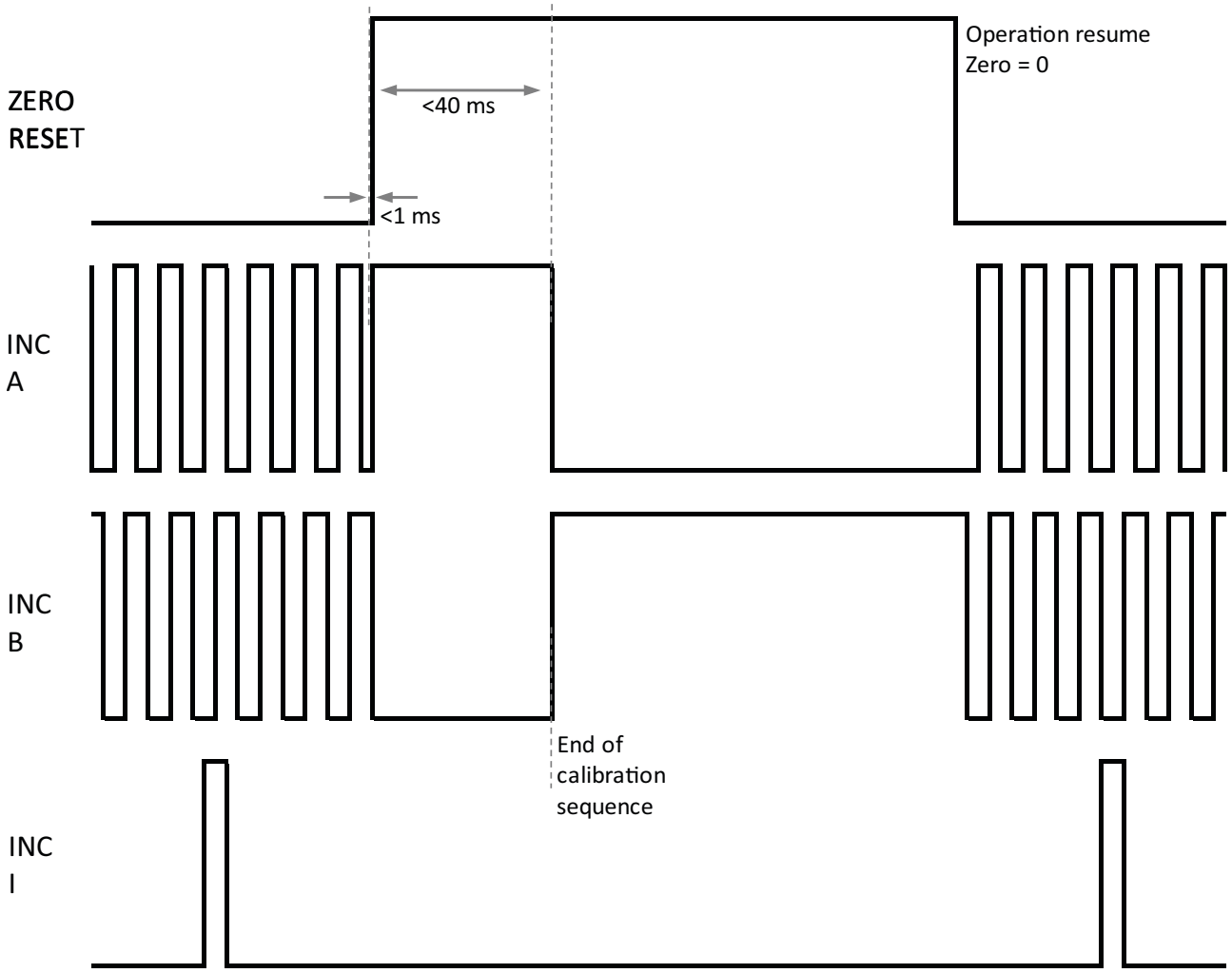
Zero Reset Calibration

The AEAT-9955 allows users to configure a zero reset position. The following is the calibration procedure.

Via an SPI Register

1. Stop the encoder to the motor system at the desired location.
2. Once it is stationary, write value 8'h8 to address 0x15 to reset the absolute single-turn position.
3. Read the calibration status on bit [3:2] address 0x2A.
   – 10: Calibration pass
   – 11: Calibration fail
4. Write value 8'h0 to address 0x15 to exit the calibration sequence.
5. The offset value is automatically stored in memory; no further programming is required.
   – To erase the calibration value, write value 8'h4 to address 0x15.
   – To return to operation mode, write value 8'h0 to address to 0x15.

Figure 5: Zero Reset Calibration



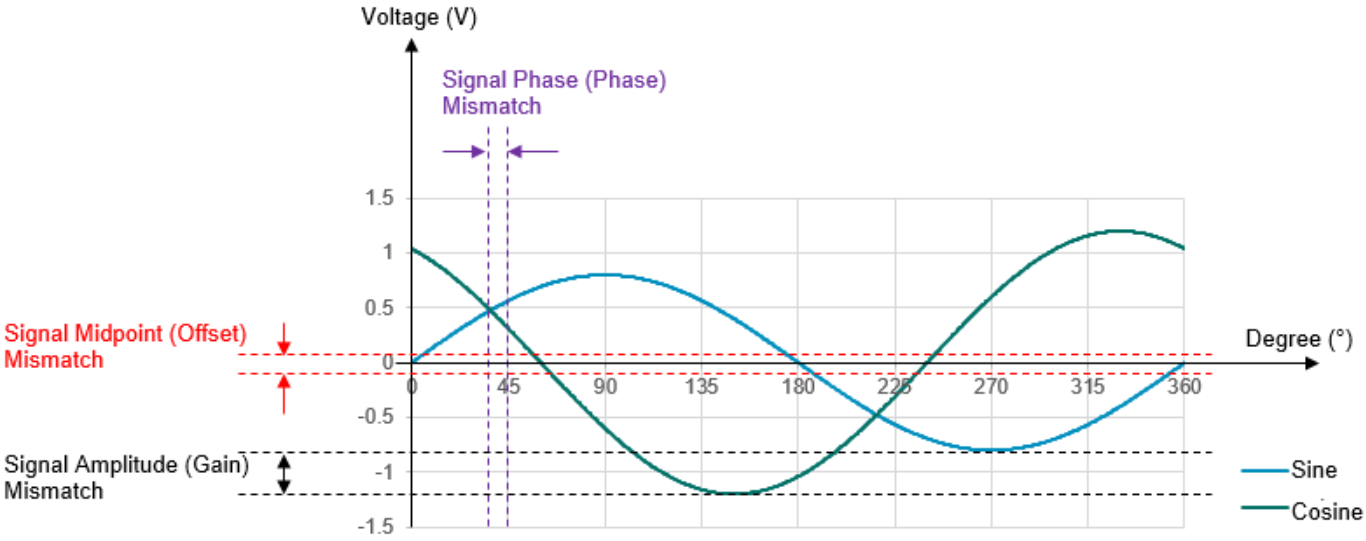
Compensation for Misalignment

The AEAT-9955 encoder actively detects magnetic flux in real time through its integrated Hall sensors. The detected magnetic flux is then converted into signals interpreted by the encoder to determine if any mechanical misalignment of the magnet has occurred during operation.

If any misalignment occurs, the AEAT-9955 encoder compensates in real time for imperfections in the sine and cosine signals generated by the misalignments. This compensation occurs in the background and improves the encoder's tolerance to magnet misalignment.

In an uncompensated system, misalignment can distort the critical sine and cosine signals generated from the magnetic flux, which are used in the encoder's positioning computation. An example of a poorly aligned magnet is shown in the following figure, where the signal perceived by the encoder exhibits errors in offset, gain, and phase.

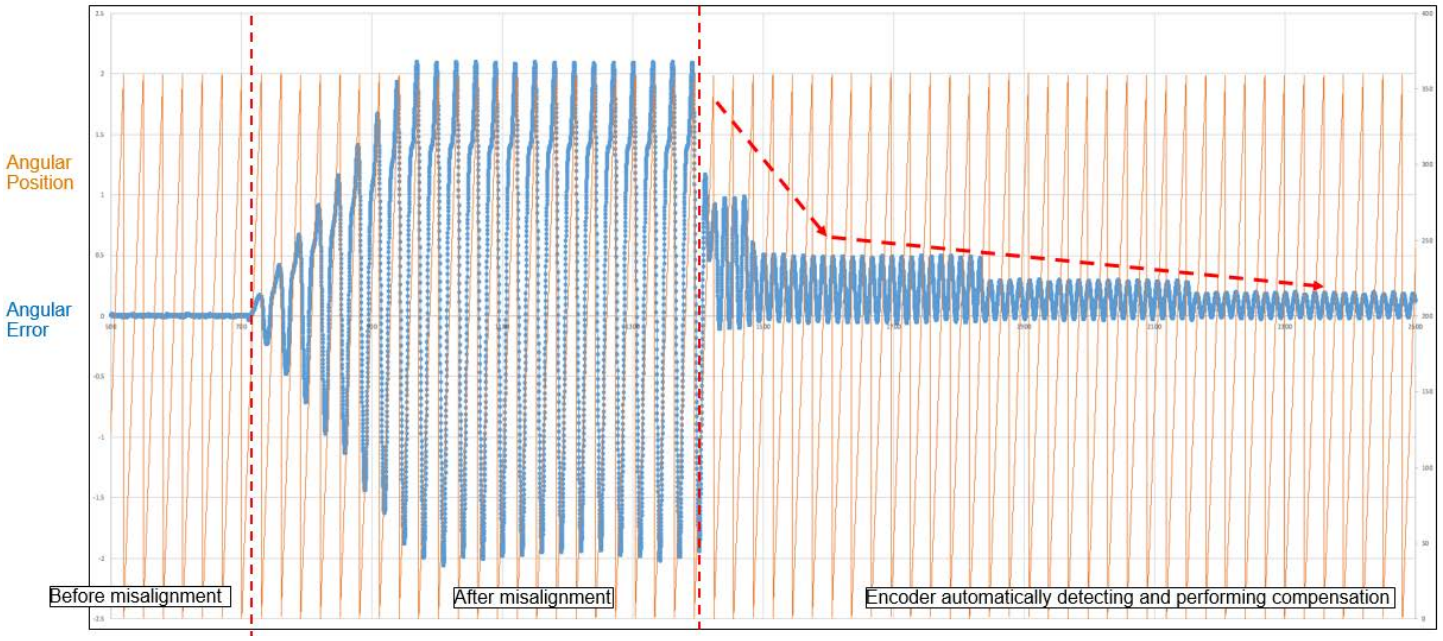
Figure 6: An Uncompensated Sine/Cosine Detected by the AEAT-9955 during Magnet Misalignment



Because compensation for any magnet misalignment occurs in real time, the system performs this adjustment in small increments. This means that whenever a misalignment happens, the AEAT-9955 encoder requires several magnet rotations, depending on the magnitude of the errors introduced, to detect and fully compensate for these inaccuracies.

The following figure demonstrates a typical angular error immediately after a misalignment occurs, up to the point when the system detects the error and begins compensation. In each magnetic turn, the error is calculated using a perfect optical reference encoder against our measured device under test (DUT).

Figure 7: AEAT-9955 Misalignment Compensation During Deliberate Misalignment



To ensure that the AEAT-9955 misalignment compensation meets the diverse needs of users with unique applications, each function within this feature can be adjusted or toggled on and off. This flexibility allows for a high degree of customization to better suit various user applications. The following is a list of adjustable functions for the AEAT-9955 misalignment compensation:

- Dynamic Offset Compensation (DOC)
  - Can be turned ON/OFF.
  - Can be tuned for higher or lower sensitivity. Higher sensitivity equals faster compensation but poorer performance against the encoder's effective number of bits (ENOB). (The settings are doc_st_init[1:0], doc_st_step[1:0], doc_st_delta[2:0], dc_clip.)
- Dynamic Gain Compensation (DGC)
  - Can be turned ON/OFF.
  - Can be tuned for higher or lower sensitivity. Higher sensitivity equals faster compensation but poorer performance against the encoder's effective number of bits (ENOB). (The settings are dgc_st_init[1:0], dgc_st_step[1:0], dgc_st_delta[2:0], dc_clip.)
- Dynamic Phase Compensation (DPC)
  - Can be turned ON/OFF.
  - Can be tuned for higher or lower sensitivity. Higher sensitivity equals faster compensation but poorer performance against the encoder's effective number of bits (ENOB). (The settings are dpc_st_init[1:0], dpc_st_step[1:0], dpc_st_delta[2:0], dc_clip.)
  - Can be tuned to cater to highly misaligned magnetic systems. This alters the correction sequence, rendering DPC correction to occur before DOC/DGC. (The setting is dft_en[1:0].)

Calibration on Signal Condition/Lookup Table

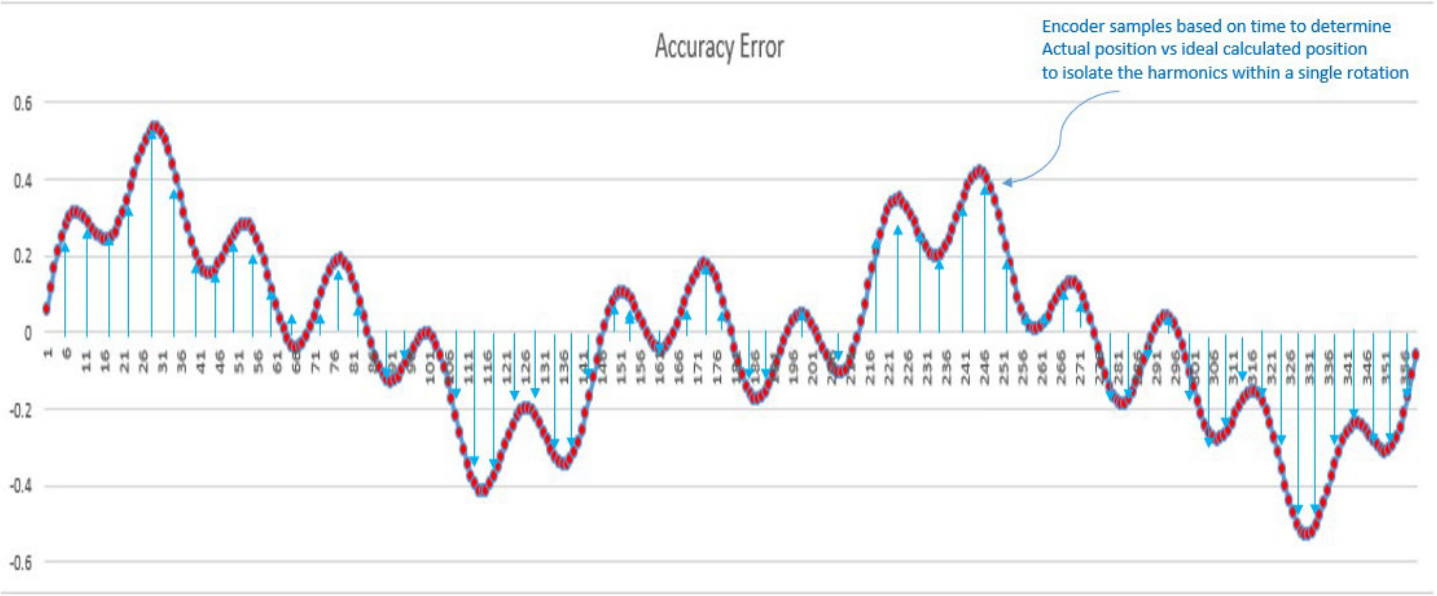
As discussed in the Auto-Calibration Function section, the AEAT-9955 encoder optimizes system performance whenever the Auto-Calibration function is activated. This function adjusts the magnetic signals received by the encoder to counteract potential negative effects from mechanical misalignment, magnet imperfections, or other external factors that could impact performance.

Although signal conditioning can enhance the encoder's performance to some degree, the AEAT-9955 encoder includes an additional process to automatically improve performance by further correcting harmonic errors. This section explains how the AEAT-9955 leverages its internal memory to compute and correct these errors.

The following is an overview of the full sequence of the lookup table harmonic correction. Once all signals have been adjusted and the initial accuracy calculated, the remaining harmonic error may appear as shown in Figure 8 after the AEAT-9955's first accuracy computation. These harmonics may vary depending on factors, such as the magnet, alignment, and system configuration, that could not be corrected by offset, Vpp, or phase correction in previous steps. With harmonic correction, the signal can be refined to an ideal state or to the encoder's base effective number of bits (ENOB).

During the Auto-Calibration function, the AEAT-9955 first assesses the computed accuracy as illustrated in Figure 8. The encoder then samples each computed position relative to an ideal position to determine the exact difference between the actual and ideal positions. Figure 8 shows this sampling process. Note that each sampled position in the figure is not to scale, because the actual sampling speed is much faster, based on system clock speeds of up to 100 MHz.

Figure 8: AEAT-9955 Sampling Position



The differences between the sampled actual positions and the calculated ideal positions are stored in the AEAT-9955's internal memory, known as a lookup table. This lookup table calibration is enabled by default in the AEAT-9955 but can be turned off if desired.

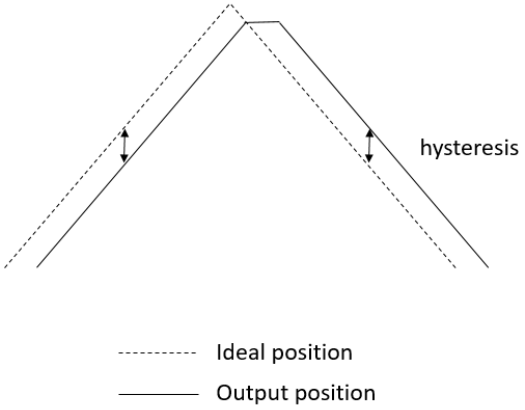
To enable or disable lookup table calibration:

1. Write value 8'h00 to address 0x16 to load the Customer Configuration register.
2. Go to address 0x01 bit[2] (Accuracy Cal. Skip). Write: 0 = Enable, 1 = Disable.

Position Data Hysteresis

The AEAT-9955 allows users to set hysteresis on a position to filter out noise components.

Figure 9: Hysteresis on a Position to Filter Out Noise Components

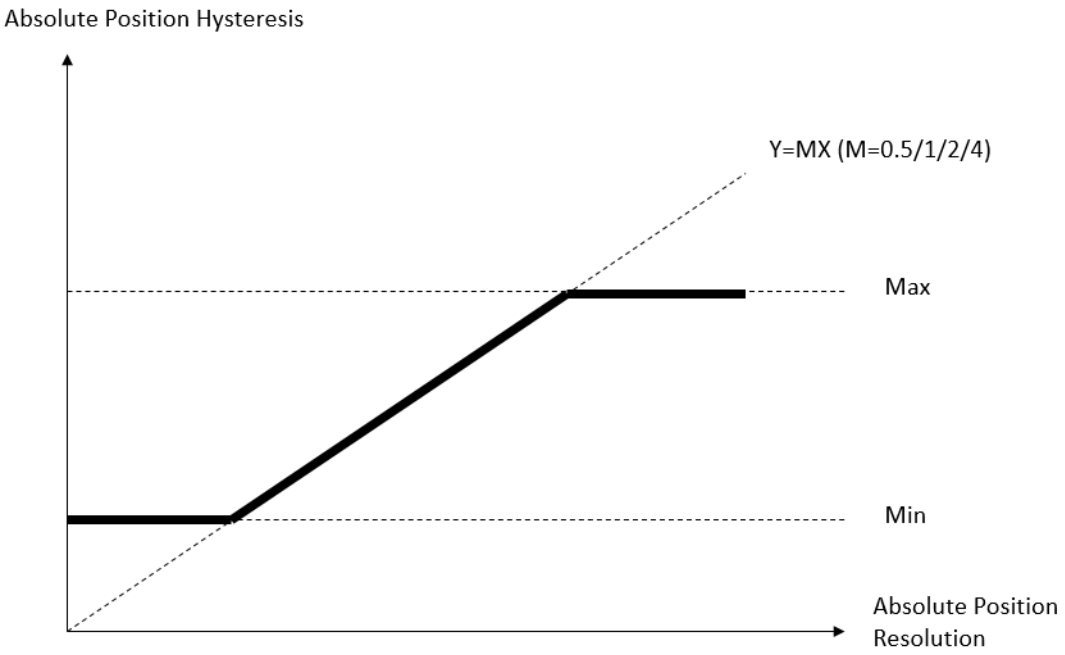


For an incremental position (ABI, UVW), hysteresis is configurable at page 0, 0x0B (Level 2 memory). Each hysteresis setting refers to its respective mechanical degree.

For an absolute position, hysteresis is configurable at page 4/7/10/13, 0x8 (Level 2a memory). Users can control absolute position hysteresis using four parameters, as illustrated by the following figure.

- Absolute position resolution.
- hys2_max: To set the Max limit or to turn OFF absolute position hysteresis if set to 111.
- hys2_min: To set the Min limit.
- hys2_cfg: To set the Y=MX line.

Figure 10: Absolute Position Hysteresis



Dynamic and Static Filter Function

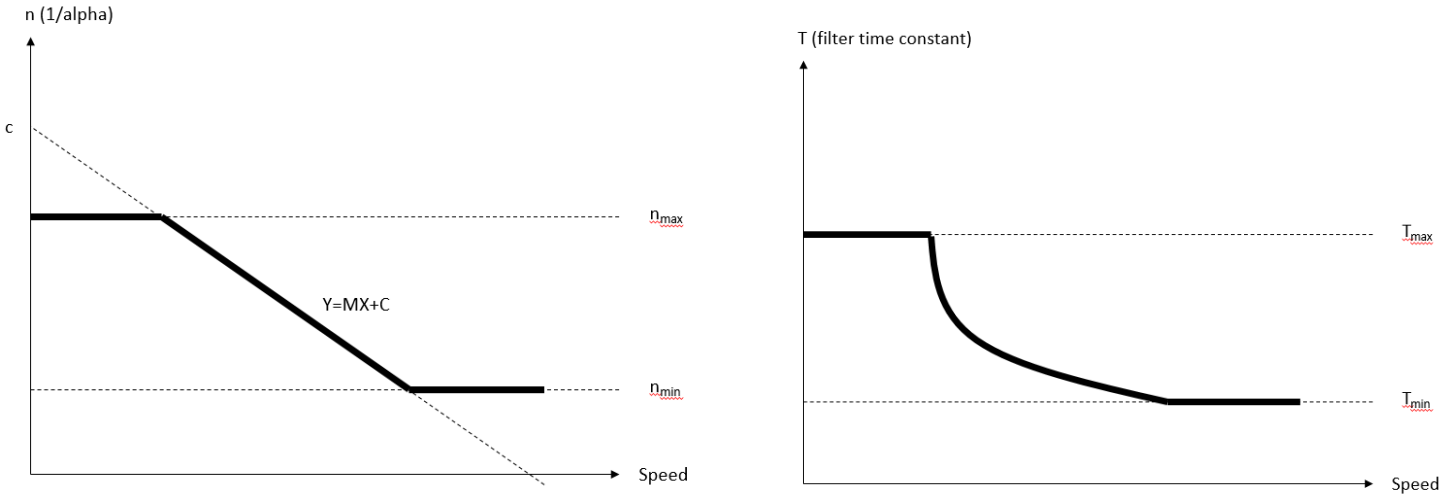
The AEAT-9955 allows users to set a position filter to reduce noise components. Two filter modes are available:

- Dynamic Filter (default)
- Static Filter

The Dynamic Filter applies a higher time constant (T) at lower speeds and a lower time constant at higher speeds. This filter is configurable at registers page 3/6/9/12, address 0x09 to 0x0A (Level 2a memory). Users can adjust the Dynamic Filter by setting four parameters to determine the value of “n”, where T is inversely proportional to n, as shown in the following figure.

- df_m1: Dynamic Filter slope (M) of n
- df_c: Dynamic Filter Y-intercept of n
- df_nmax: Dynamic Filter maximum limit for n
- df_nmin: Dynamic Filter minimum limit for n

Figure 11: Filter on a Position to Filter Out Noise Components



By default, the Dynamic Filter is enabled, with a maximum filter time constant (T_{max}) of 1.5 ms when the speed < 300 rpm and a minimum time constant (T_{min}) of 1.3 ms when the speed > 500 rpm.

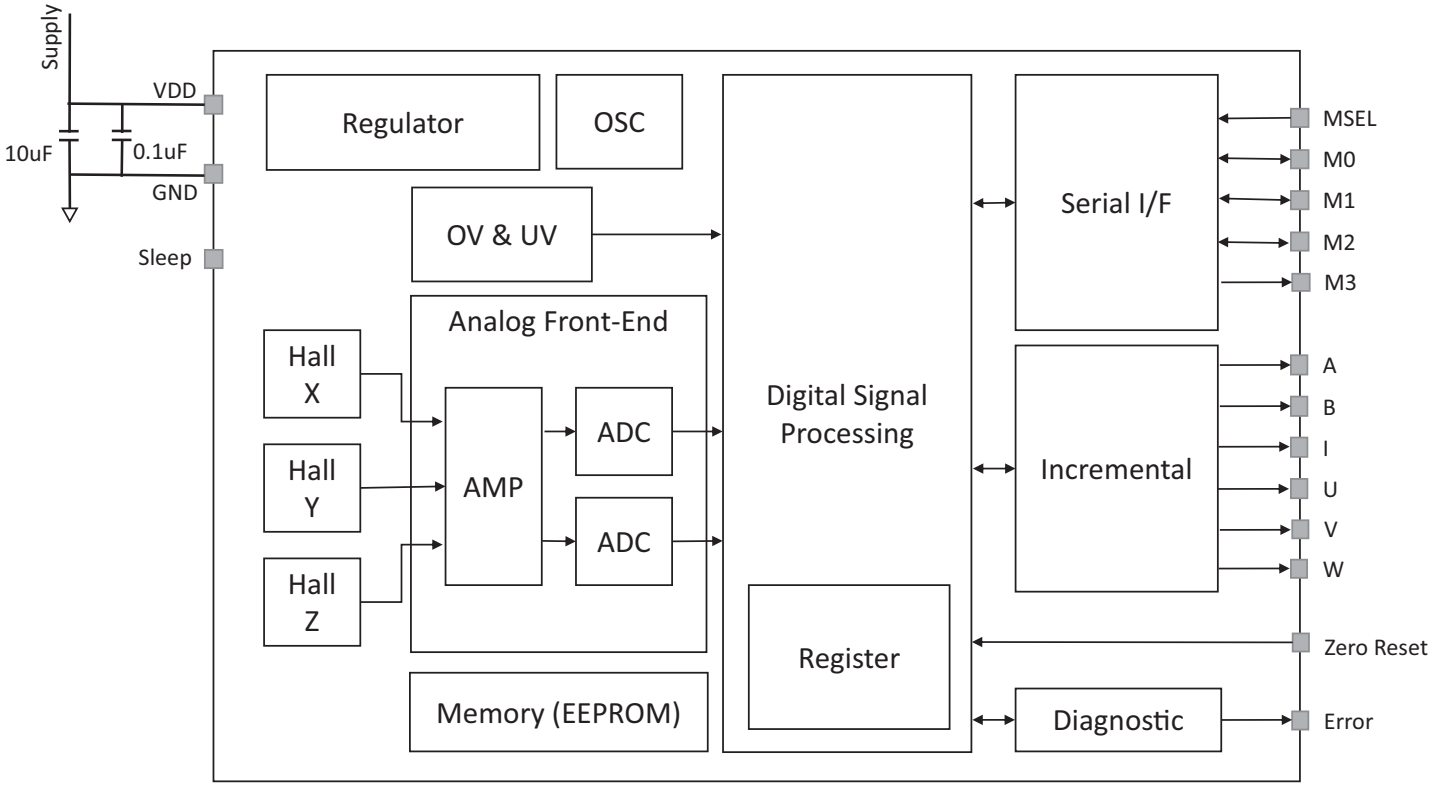
The Static Filter, on the other hand, applies a constant filter parameter regardless of speed.

The selection between Dynamic and Static Filter modes can be configured as follows:

1. If memory page 0, address 0x03 (Level 1 memory) static_ave2 is set to a nonzero value, then Static Filter = static_ave2.
2. Otherwise, if memory page 3/6/9/12, address 0x08 (Level 2a memory) static_ave is set to a nonzero value, then Static Filter = static_ave.
3. If neither setting is nonzero, the Dynamic Filter is applied.

Circuit Diagram

Figure 12: Recommended Circuit Diagram for the AEAT-9955

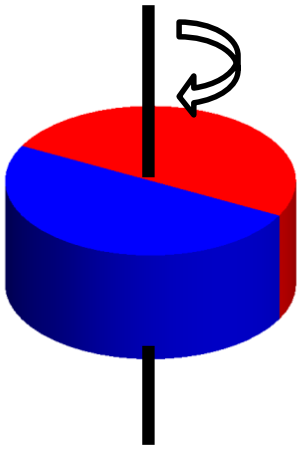


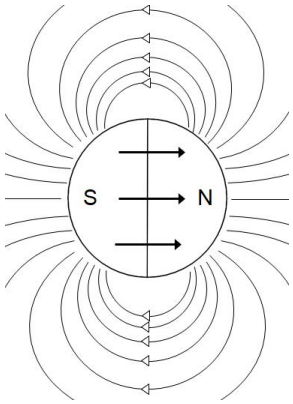
NOTE: Connect the 10-µF and 100-nF capacitors as close as possible to the individually assigned power and ground pins.

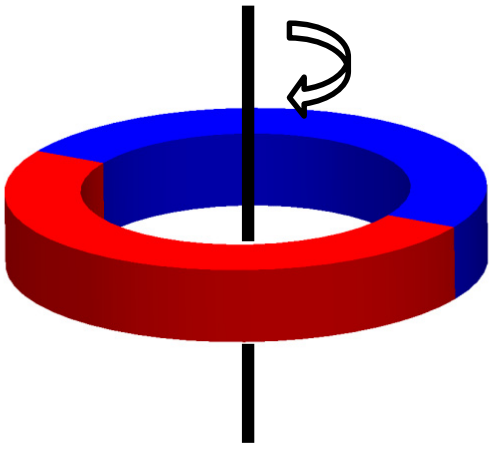
Recommended Magnetic Input Specifications

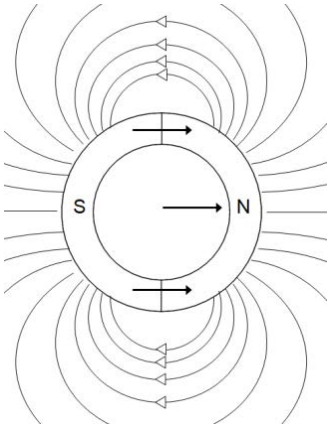
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Diameter Disc magnet Ring magnet ID /OD	d	 4 —	 6 ID,15 OD,25	 — —	 mm mm mm	Recommended magnet: Cylindrical magnet or ring magnet diametrically magnetized and one pole pair.
Thickness Disc magnet Ring magnet	t	 — 2	 2.5 6	 — —	 mm mm	
Magnetic input field magnitude On-axis (disc magnet) Off-axis (ring magnet)	Bpk	 45 30	 — —	 100 150	 mT mT	Required vertical/horizontal component of the magnetic field strength on the die's surface, measured along concentric circle.
Magnet displacement radius	R_m	—	—	0.25	mm	Displacement between the magnet axis and the device center.
Recommended magnet material and temperature drift	—	—	–0.12	—	%/K	NdFeB (Neodymium Iron Boron), grade N35SH.

Diametrically Magnetized Magnet





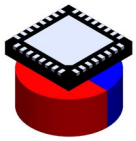
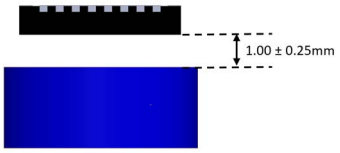
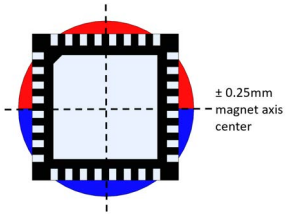
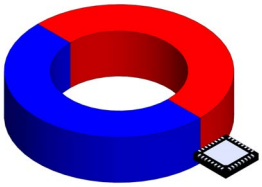
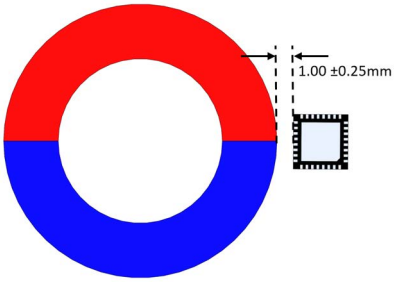
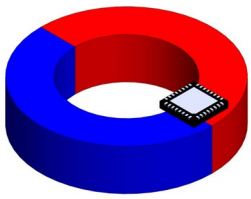
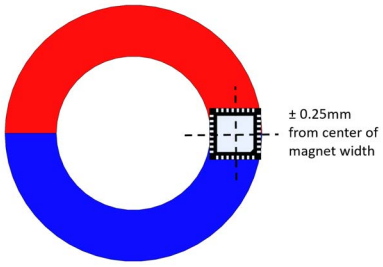
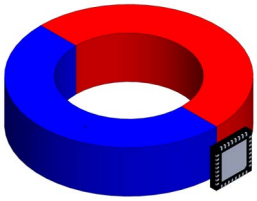
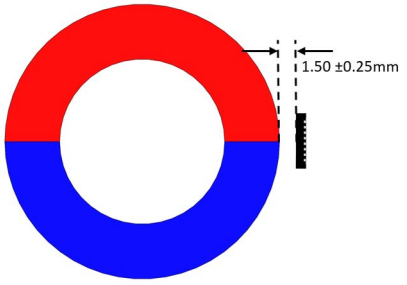




Magnet and IC Package Placement

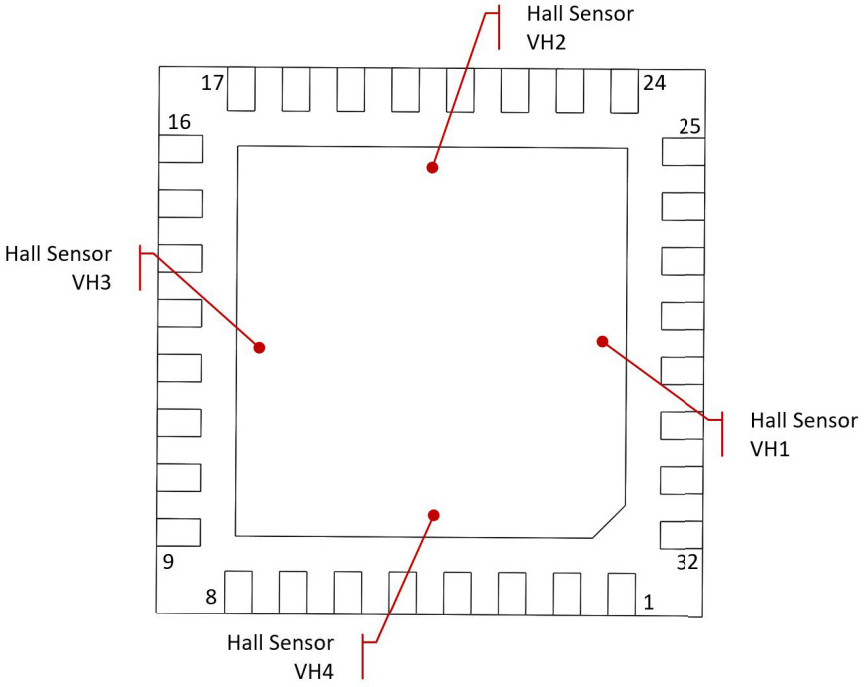
The AEAT-9955 multi-axis capability comes from multiple integrated Hall devices that allow flexibility on the sensor mounting with respect to the magnet. Generally, the shaft end configuration senses the vertical field (Z component perpendicular to the chip surface), and the rest of the configuration senses the horizontal field (X and Y components parallel to the chip surface).

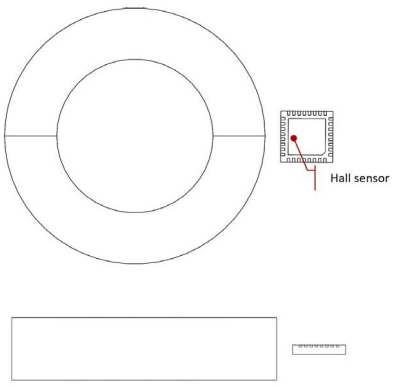
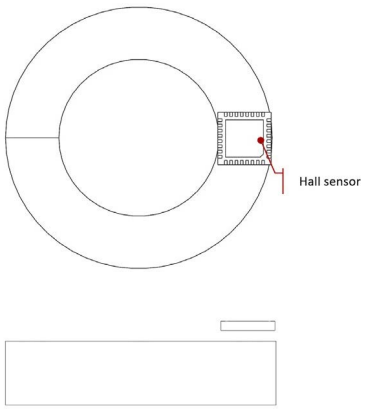
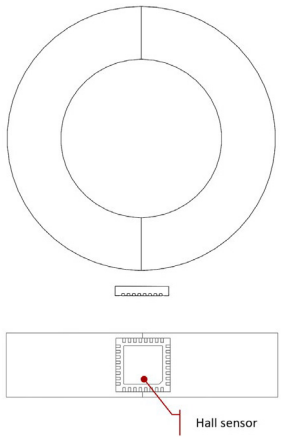
The nominal mounting tolerance is indicated in the following table.

Configuration	Gap Tolerance	X-Y Tolerance
Shaft End 		
Side Shaft 		
Axial 		
Radial 		

Off-Axis Sensing Orientation

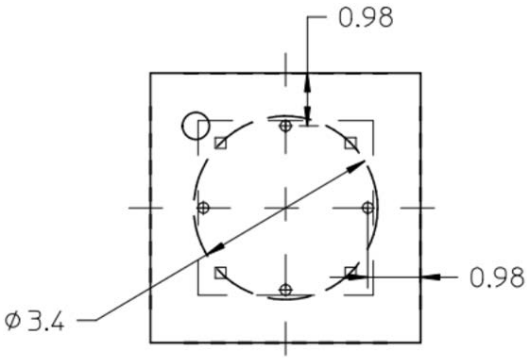
The off-axis configuration is sensed via the vertical Hall element. Each axis requires a specific vertical Hall orientation to be configured. Multiple vertical Hall sensors are built in to provide flexibility in the mounting configuration. The vertical Hall selections are available in the Customer Configuration 0 registers.



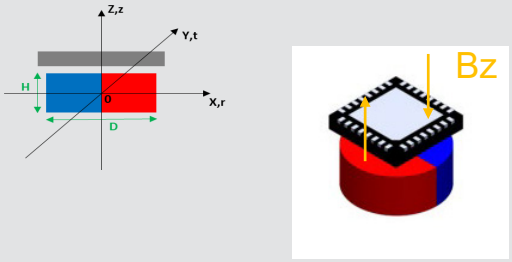
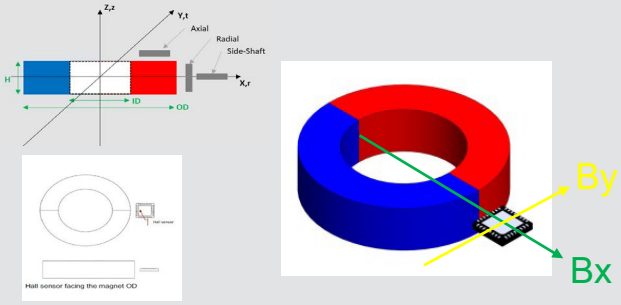
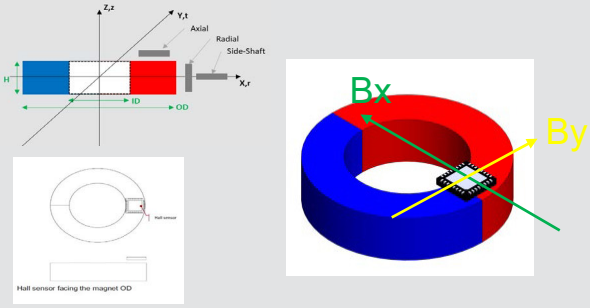
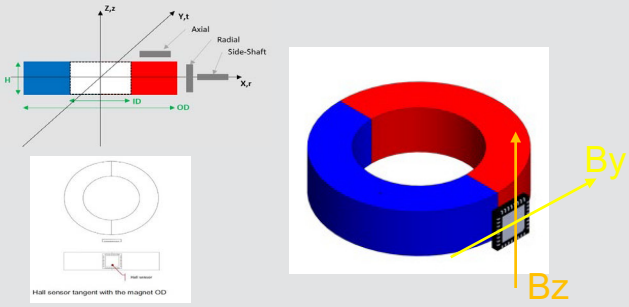
Side-Shaft	Axial	Radial
		
Hall sensor facing the magnet OD	Hall sensor facing the magnet OD	Hall sensor tanget with the magnet OD

Hall Sensor Location

There are a total of four on-axis sensors located along the 3.4-mm diameter with each sensor 90 degrees apart. The off-axis uses only a single pair of hall sensors at a time and is located 0.98 mm from each chip edge.



The following table illustrates the magnetic field of interest for each configuration.

ON Axis [End-Shaft]	OFF Axis [Side-Shaft]
	
OFF Axis [Axial]	**OFF Axis [Radial]**
	

Recommended Operation Circuit

Figure 13: Absolute and Incremental Output Operation

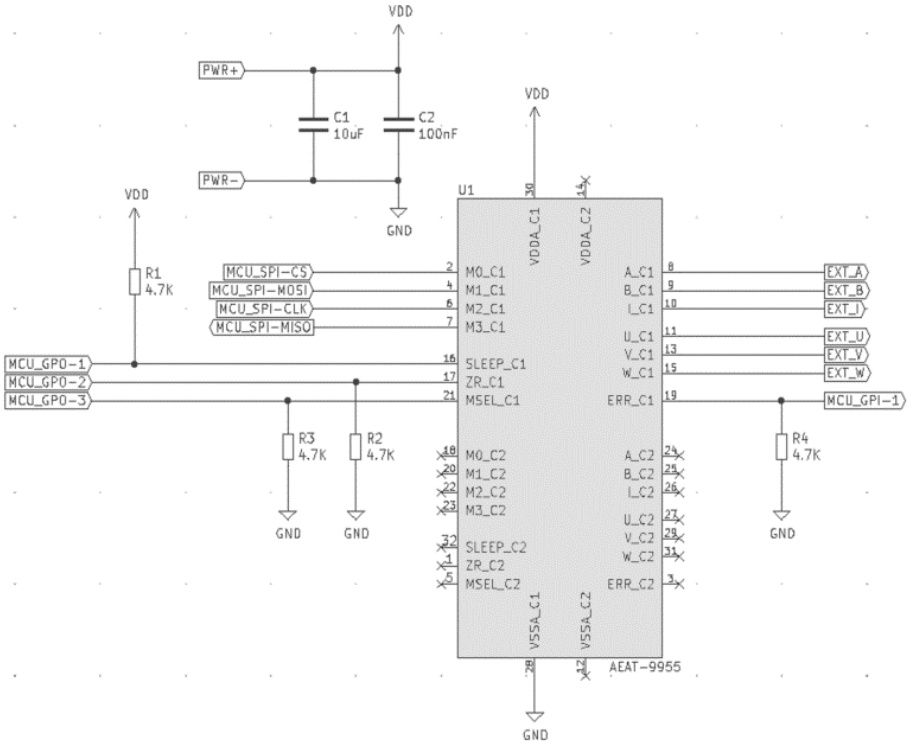


Figure 14: Absolute Operation Only

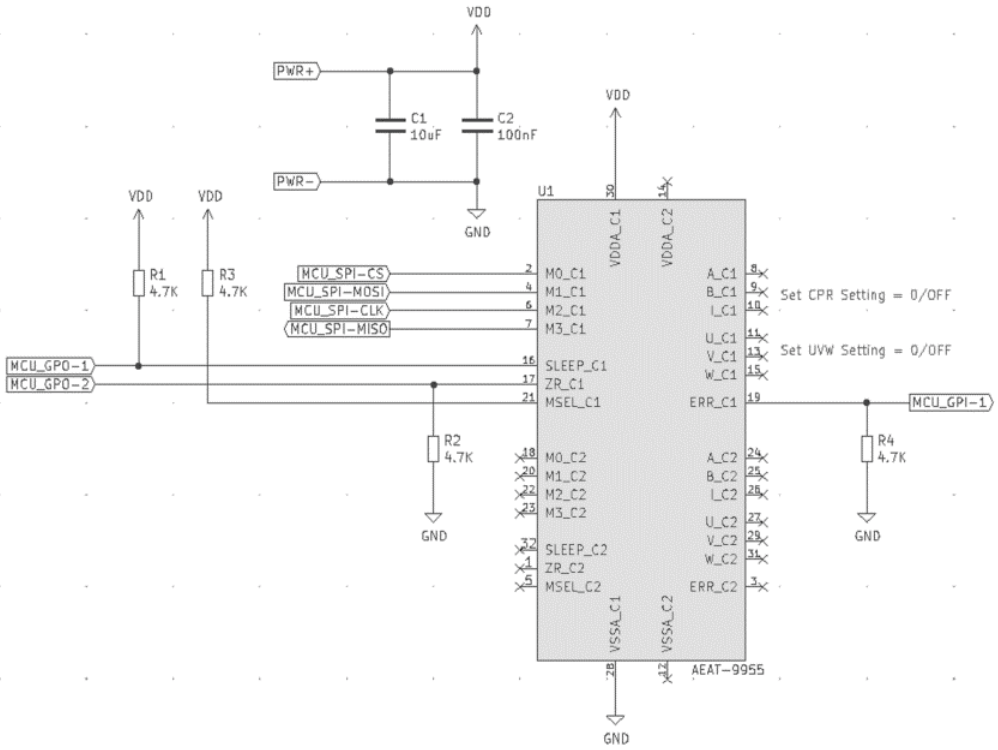
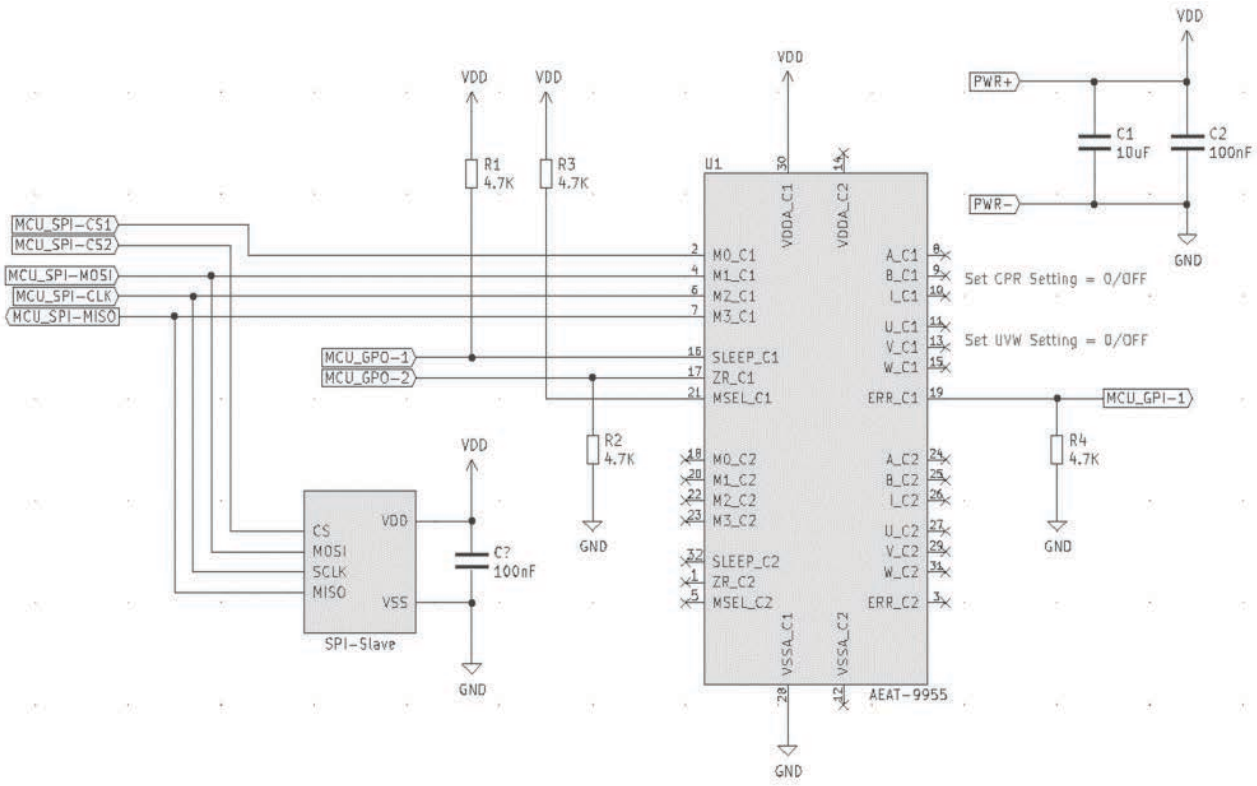


Figure 15: Multi-Client Operation



Serial Interface Format

The AEAT-9955 serial interface hosts up to 10 different protocols for position output and memory access. The protocol is configurable with the combination of the physical I/O MSEL and M0 and memory settings PSEL, SPI4[0], and SPI4[1]. The default factory setting is all zeros, which is either SPI3 or SPI4-16a depending on the MSEL state. The output pin can be configured to high impedance mode for multi-client connection or bus connection.

All protocol selection can be switched during operation.

MATS Table

Mode / Pin	SPI3	SSI3a	SSI3b	SSI2a	SSI2b	SPI4-16	SPI4-24a	SPI4-24b	SPI4-8	PWM
MSEL	0	0	0	0	0	1	1	1	1	1
PSEL	x	0	1	0	1	0	0	0	0	1
SPI4[1]	x	x	x	x	x	0	0	1	1	x
SPI4[0]	x	x	x	x	x	0	1	0	1	x
M0	0	1	1	1	1	NCS	NCS	NCS	NCS	-
M1	DIN	NSL	NSL	0	0	MOSI	MOSI	MOSI	MOSI	-
M2	SCK	SCL	SCL	SCL	SCL	SCK	SCK	SCK	SCK	-
M3	DO	DO	DO	DO	DO	MISO	MISO	MISO	MISO	PWM

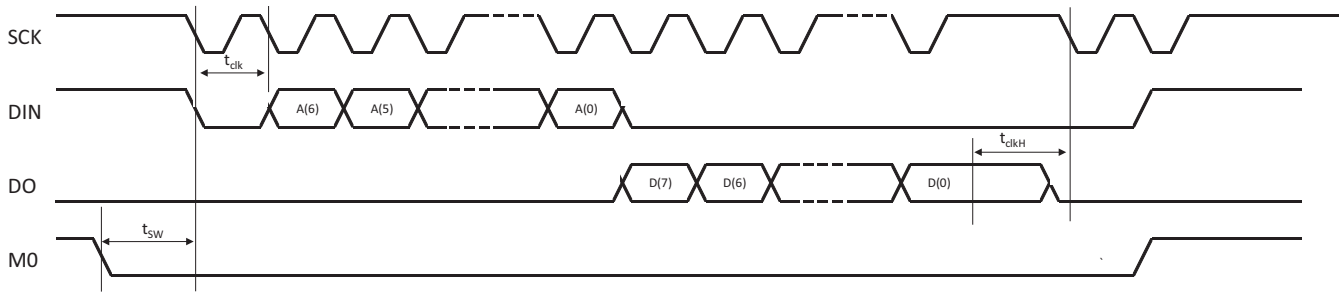
NOTE: PSEL, SPI4[1], and SPI4[0] are configured through memory. MSEL and M0 are configured through I/O pads.

Serial Peripheral Interface (SPI3)

SPI3 protocols allow access to memory read write only. Assert 0 on the MSEL and M0 pin to configure it. The SPI is implemented with CPOL = 0 and CPHA = 0; data is propagated on the clock falling edge.

- M1 → SPI_Data Input (DIN) signal for the SPI protocol, input to the AEAT-9955.
- M2 → SPI_Clock Input (SCK) signal for the SPI protocol, input to the AEAT-9955.
- M3 → SPI_Data Output (DO) signal for the SPI protocol, output from the AEAT-9955.

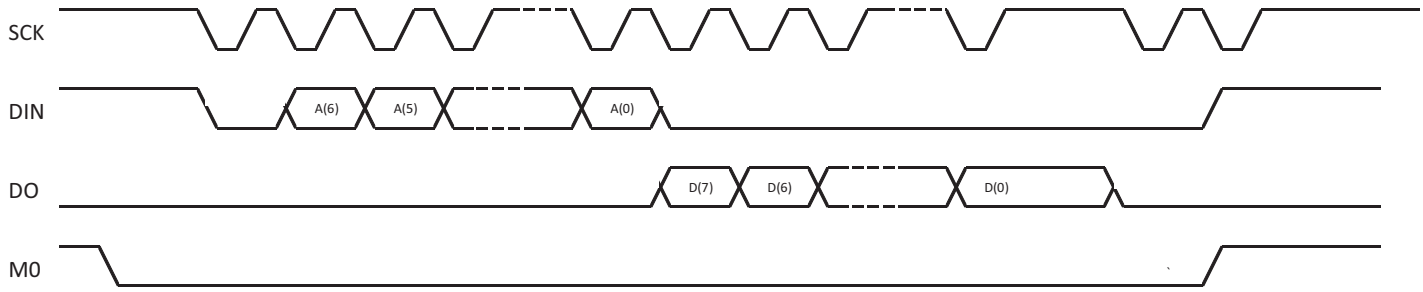
SPI3 Timing Diagram



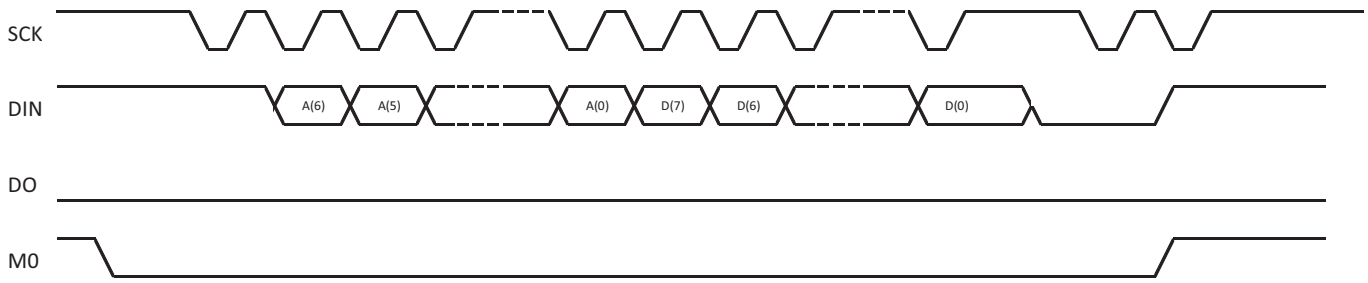
Symbol	Description	Min.	Typ.	Max.	Unit
t_{SW}	Time between the M0 falling edge and the CLK rising edge	1	—	—	µs
t_{clk}	Serial clock period	1	—	—	µs
t_{clkH}	CLK high time after the end of the last clock period	300	—	—	ns

NOTE: Read back data to confirm that it has been written successfully.

SPI3 Read



SPI3 Write



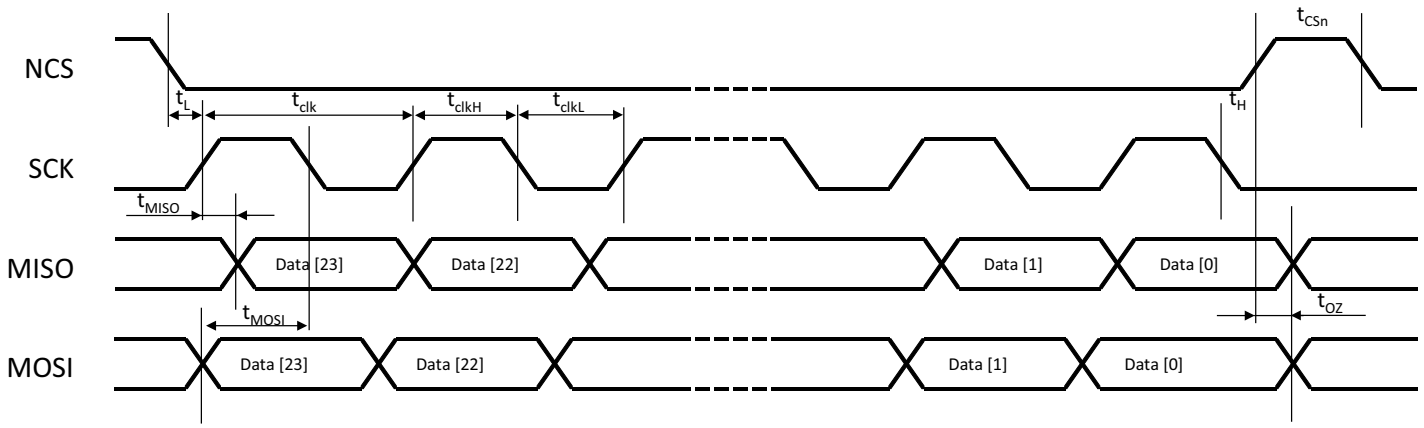
Serial Peripheral Interface (SPI4)

The SPI protocol uses four pins from the AEAT-9955. These four pins are shared between the UVW, SSI, and SPI protocols. To select the SPI4 protocol, assert 1 on the MSEL pin.

SPI4 protocols allow you to access memory read or write and position data. It uses CPOL = 0, CPHA = 1 for triggering.

- M0 → SPI_Chip Select (NCS) signal for the SPI protocol, input to the AEAT-9955.
- M1 → SPI_Data Input (MOSI) signal for the SPI protocol, input to the AEAT-9955.
- M2 → SPI_Clock Input (SCK) signal for the SPI protocol, input to the AEAT-9955.
- M3 → SPI_Data Output (MISO) signal for the SPI protocol, output from the AEAT-9955.

SPI4 Timing Diagram

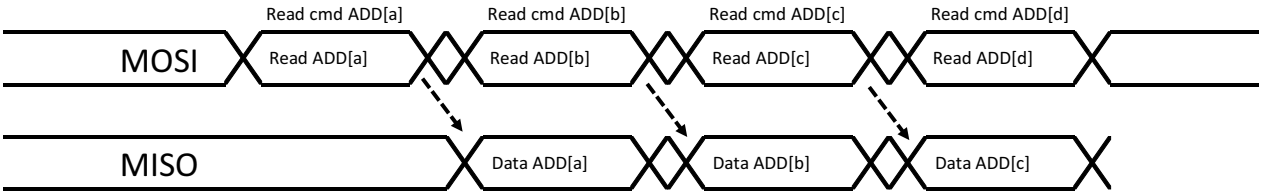


Symbol	Description	Min.	Typ.	Max.	Unit
t_L	Time between the SCn falling edge and the CLK rising edge	350	—	—	ns
t_{clk}	Serial clock period	100	—	—	ns
t_{clkL}	Low period of the serial clock	50	—	—	ns
t_{clkH}	High period of the serial clock	50	—	—	ns
t_H	Time between the last falling edge of CLK and the rising edge of CSn	$t_{clk}/2$	—	—	ns
t_{CSn}	High time of CS between two transmissions	350	—	—	ns
t_{MOSI}	Data input valid to clock edge	20	—	—	ns
t_{MISO}	CLK edge to data output valid	—	—	51	ns
t_{OZ}	Time between CSn rising edge and MISO HiZ	—	—	10	ns

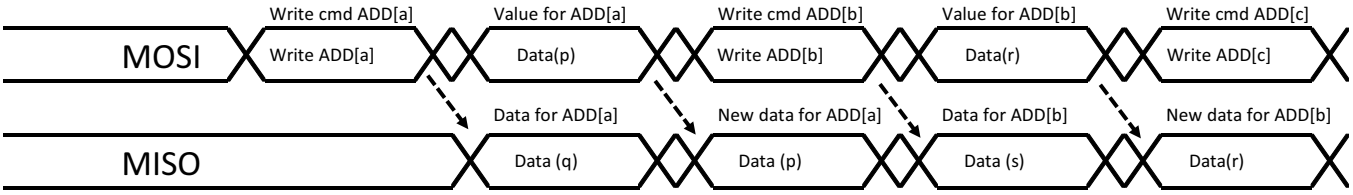
NOTE: Read back data to confirm that it has been written successfully.

SPI4 Command and Data Frame

SPI4 Read Sequence



SPI4 Write Sequence



SPI4-16: 16-Bit (Parity)

By default, the chip is configured to SPI4 16-bit selection; PSEL = 0, SPI4[1] = 0, SPI4[0] = 0 in the register setting.

	Data Format																			
	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Controller to Peripheral					P	RW	0	0	0	0	0	0	Addr/Data[7:0]							
Peripheral to Controller (memory)					P	EF	0	0	0	0	0	0	Data[7:0]							
Peripheral to Controller (pos 10b)					P	EF	Pos[9:0]										0	0	0	0
Peripheral to Controller (pos 11b)					P	EF	Pos[10:0]											0	0	0
Peripheral to Controller (pos 12b)					P	EF	Pos[11:0]												0	0
Peripheral to Controller (pos 13b)					P	EF	Pos[12:0]													0
Peripheral to Controller (pos 14b)					P	EF	Pos[13:0]													
Peripheral to Controller (pos 15b)				P	EF	Pos[14:0]														
Peripheral to Controller (pos 16b)			P	EF	Pos[15:0]															
Peripheral to Controller (pos 17b)		P	EF	Pos[16:0]																
Peripheral to Controller (pos 18b)	P	EF	Pos[17:0]																	

P: Parity
EF: Error Flag
RW: Read = 1, Write = 0

SPI4-24a: 24-Bit (Parallel CRC)

To configure the chip to SPI4 24-bit selection (Parallel CRC), set PSEL = 0, SPI4[1] = 0, SPI4[0] = 1 in the register setting.

Data Format

	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Controller to Peripheral					0	RW	0	0	0	0	0	0	Addr/Data[7:0]								CRC[7:0]							
Peripheral to Controller (memory)					W	E	0	0	0	0	0	0	Data[7:0]								CRC[7:0]							
Peripheral to Controller (pos 8b)					W	E	Pos[7:0]								0	0	0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 9b)					W	E	Pos[8:0]									0	0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 10b)					W	E	Pos[9:0]										0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 11b)					W	E	Pos[10:0]											0	0	0	CRC[7:0]							
Peripheral to Controller (pos 12b)					W	E	Pos[11:0]												0	0	CRC[7:0]							
Peripheral to Controller (pos 13b)					W	E	Pos[12:0]													0	CRC[7:0]							
Peripheral to Controller (pos 14b)					W	E	Pos[13:0]														CRC[7:0]							
Peripheral to Controller (pos 15b)				W	E	Pos[14:0]															CRC[7:0]							
Peripheral to Controller (pos 16b)			W	E	Pos[15:0]																CRC[7:0]							
Peripheral to Controller (pos 17b)		W	E	Pos[16:0]																	CRC[7:0]							
Peripheral to Controller (pos 18b)	W	E	Pos[17:0]																		CRC[7:0]							

Input for CRC Calculation

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
								0	RW	0	0	0	0	0	0	Addr/Data[7:0]								Data+CRC =24b
								W	E	0	0	0	0	0	0	Data[7:0]								Data+CRC =24b
								W	E	Pos[7:0]							0	0	0	0	0	0		Data+CRC =24b
								W	E	Pos[8:0]								0	0	0	0	0		Data+CRC =24b
								W	E	Pos[9:0]									0	0	0	0		Data+CRC =24b
								W	E	Pos[10:0]										0	0	0		Data+CRC =24b
								W	E	Pos[11:0]											0	0		Data+CRC =24b
								W	E	Pos[12:0]												0		Data+CRC =24b
								W	E	Pos[13:0]														Data+CRC =24b
W	E	Pos[14:0]															0	0	0	0	0	0		Data+CRC >24b
W	E	Pos[15:0]																0	0	0	0	0		Data+CRC >24b
W	E	Pos[16:0]																	0	0	0	0		Data+CRC >24b
W	E	Pos[17:0]																		0	0	0		Data+CRC >24b

When Data+CRC =24b, use Data (16b) to calculate CRC based

When Data+CRC >24b, pad 0 at behind Data until it is 24b, then calculate CRC

W: Warning
E: Error
RW: Read = 1, Write = 0

SPI4-24b: 24-Bit (Serial CRC)

To configure the chip to SPI4 24-bit selection (Serial CRC), set PSEL = 0, SPI4[1] = 1, SPI[0] = 0 in the register setting.

Data Format

	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Controller to Peripheral					0	RW	0	0	0	0	0	0	Addr/Data[7:0]								CRC[7:0]							
Peripheral to Controller (memory)					W	E	0	0	0	0	0	0	Data[7:0]								CRC[7:0]							
Peripheral to Controller (pos 8b)					W	E	Pos[7:0]								0	0	0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 9b)					W	E	Pos[8:0]									0	0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 10b)					W	E	Pos[9:0]										0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 11b)					W	E	Pos[10:0]											0	0	0	CRC[7:0]							
Peripheral to Controller (pos 12b)					W	E	Pos[11:0]												0	0	CRC[7:0]							
Peripheral to Controller (pos 13b)					W	E	Pos[12:0]													0	CRC[7:0]							
Peripheral to Controller (pos 14b)					W	E	Pos[13:0]														CRC[7:0]							
Peripheral to Controller (pos 15b)				W	E	Pos[14:0]															CRC[7:0]							
Peripheral to Controller (pos 16b)			W	E	Pos[15:0]																CRC[7:0]							
Peripheral to Controller (pos 17b)		W	E	Pos[16:0]																	CRC[7:0]							
Peripheral to Controller (pos 18b)	W	E	Pos[17:0]																		CRC[7:0]							

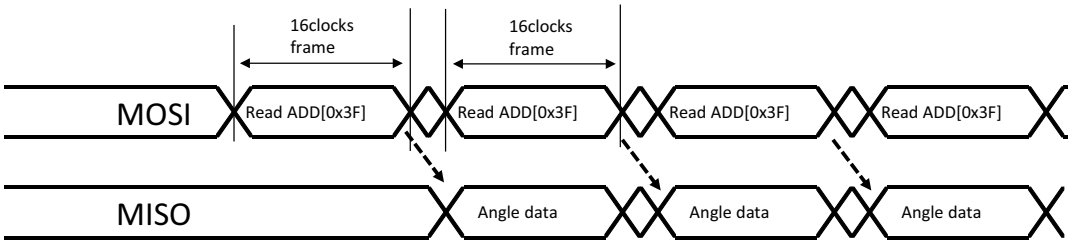
Input for CRC Calculation

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					0	RW	0	0	0	0	0	0	Addr/Data[7:0]							
					W	E	0	0	0	0	0	0	Data[7:0]							
					W	E	Pos[7:0]								0	0	0	0	0	0
					W	E	Pos[8:0]									0	0	0	0	0
					W	E	Pos[9:0]										0	0	0	0
					W	E	Pos[10:0]											0	0	0
					W	E	Pos[11:0]												0	0
					W	E	Pos[12:0]													0
					W	E	Pos[13:0]													
				W	E	Pos[14:0]														
			W	E	Pos[15:0]															
		W	E	Pos[16:0]																
	W	E	Pos[17:0]																	

W: Warning
E: Error
RW: Read = 1, Write = 0

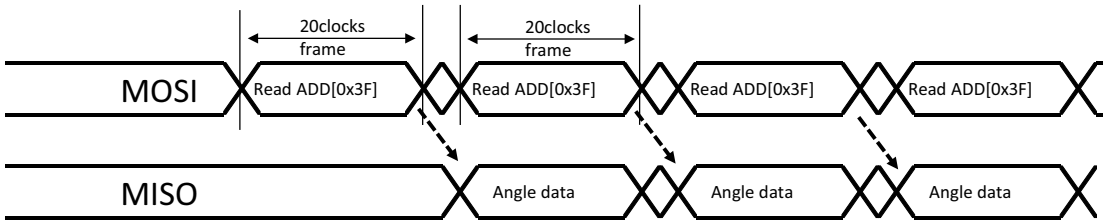
Position Read

Absolute position data can be obtained by sending a read command to address 0x3F.



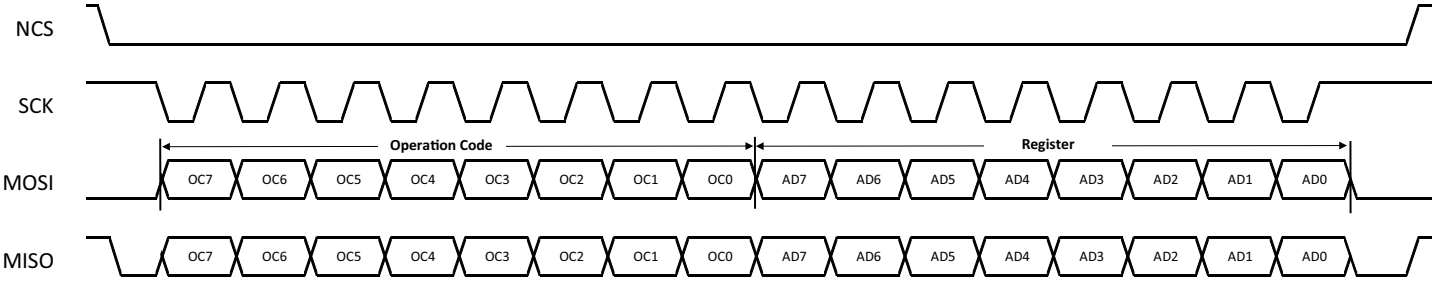
In the event of higher single-turn resolution (15-bit and above), the command and data frame size is adjusted accordingly.

Example: 18 bits + 2 bits (parity and error)



SPI4-8: 8-Bit

To configure the chip to SPI4 8-bit selection, set PSEL = 0, SPI4[1] = 1, SPI4[0] = 1 in the register setting.

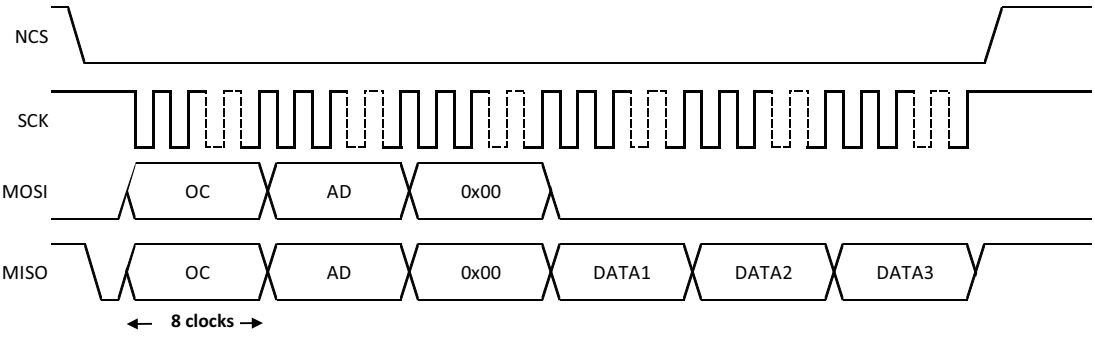


When NCS is low, the communication line is activated and the data is sampled on the rising edge of SCK.

The MISO state turns to high impedance mode (hi-Z) when NCS is high. The transmission works over specific operation code (OC).

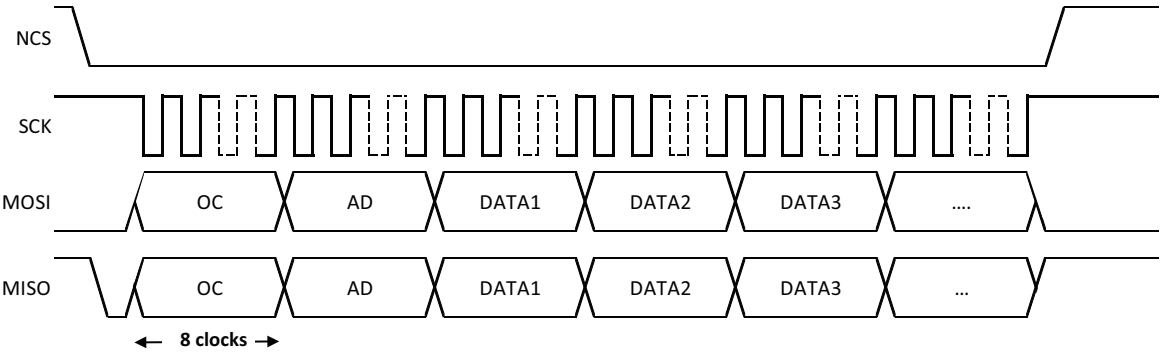
Register Read (OC = 0x81'h)

This operation is used to read data from the internal register of the chip. It can be performed consecutively starting from any register address. The data continues to be transmitted as long the clock (SCK) is sent and the chip select (NCS) remains active.



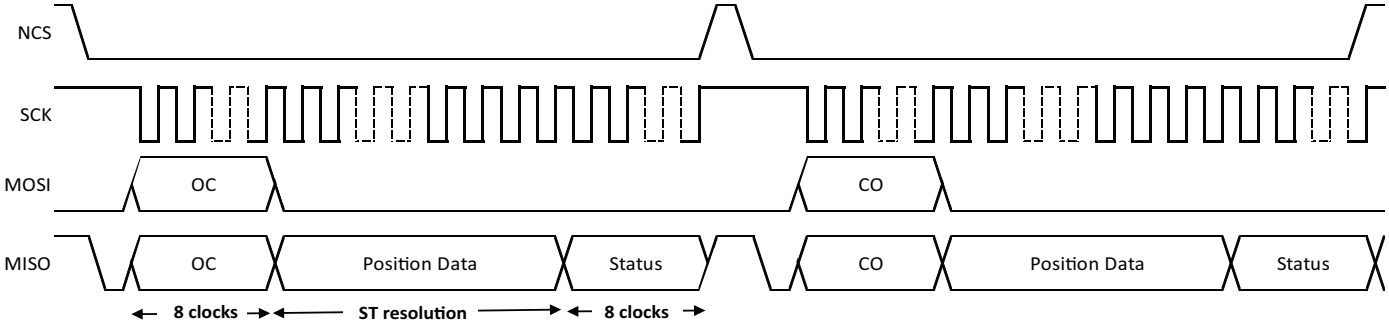
Register Write (OC = 0xCF'h)

This operation is used to write data into the internal register of the chip. It can be performed consecutively starting from any register address.The subsequent data byte is written into the next register address (AD+1), while the NCS signal stays active. Complete written data is transmitted back via MISO.

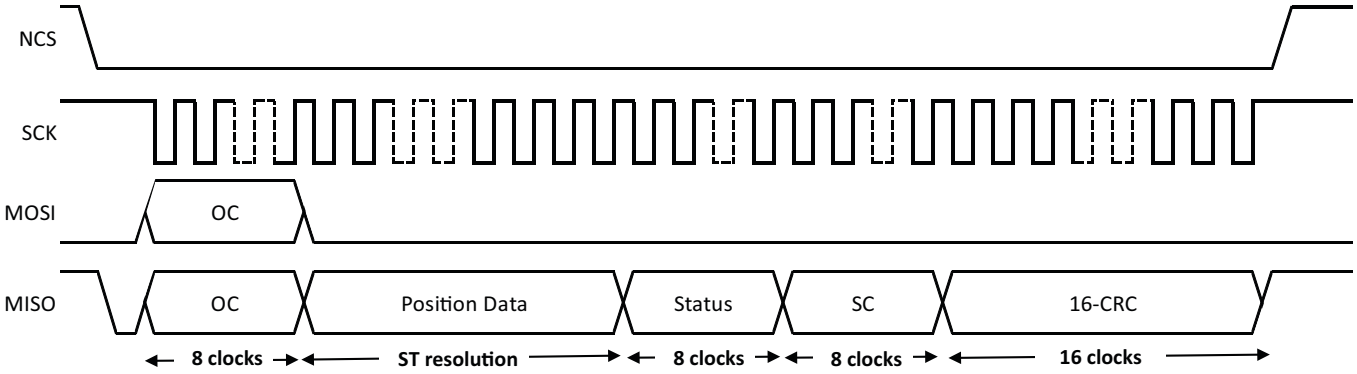


Position Read (OC = 0xA6'h)

Read the absolute position by sending the operation code, and the data will be transmitted on the MISO line. The position data consists of the single-turn position data length and status byte. The position data length follows the single-turn resolution setting.



For safety format, there are additional bytes: sequence counter (SC) and CRC.



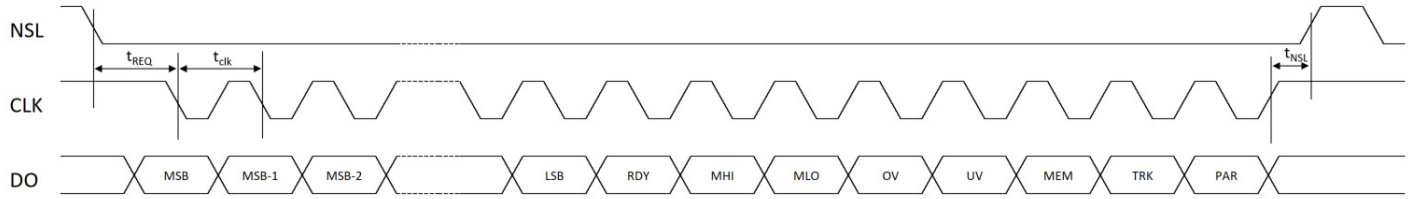
Serial Synchronous Interface 3-Wire (SSI3)

The SSI3 protocol uses three pins from the AEAT-9955. These three pins are shared between the UVW, SSI, and SPI protocols. To activate the SSI3 protocol, assert 0 on the MSEL pin and assert 1 on the M0 pin.

- M1 → SSI_NSL Input (NSL) signal for the SSI protocol, input to the AEAT-9955.
- M2 → SSI_Clock Input (CLK) signal for the SSI protocol, input to the AEAT-9955.
- M3 → SSI_Data Output (DO) signal for the SSI protocol, output from the AEAT-9955.

It is available in two options per PSEL register setting.

SSI Protocol Timing Diagram. Default: Data Output with 3-Wire SSI to 10-MHz Clock Rates

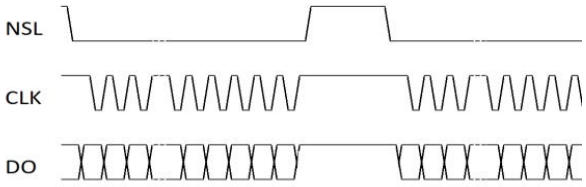


Symbol	Description	Min.	Typ.	Max.	Unit
t_{clk}	SSI_SPI_SEL switch time	1	—	—	µs
t_{REQ}	CLK high time between the NSL falling edge and the first CLK falling edge	300	—	—	ns
t_{NSL}	NSL high time between two successive SSI reads	200	—	—	ns

SSI-3(A)

By default, the chip is configured to SSI-3(A) selection; PSEL = 0 in the register setting.

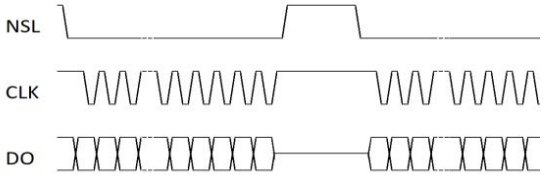
The DO pin is held at a high state once the NSL pin is high.



SSI-3(B)

To configure the chip to SSI-3(B) selection, set PSEL = 1 in the register setting.

The DO pin is at a tristate (high-impedance) state once the NSL pin is high.



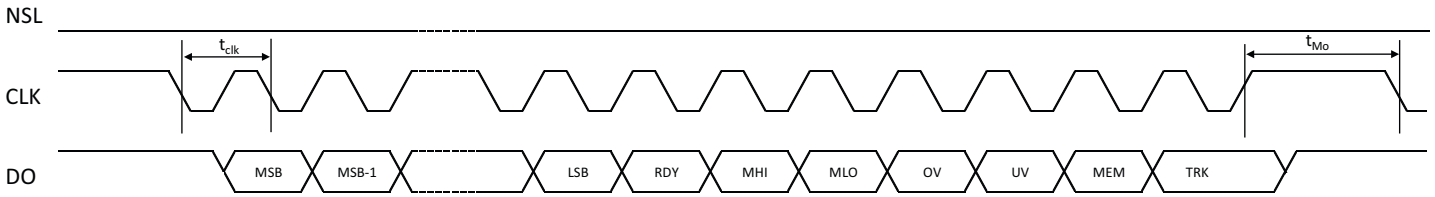
Serial Synchronous Interface 2-Wire (SSI2)

The SSI2 protocol uses two pins from the AEAT-9955. These two pins are shared between the SSI and SPI protocols. To activate the SSI2 protocol, assert 0 on the MSEL and M1 pins and assert 1 on the M0 pin upon power-up.

- M2 → SSI_Clock Input (CLK) signal for the SSI protocol, input to the AEAT-9955.
- M3 → SSI_Data Output (DO) signal for the SSI protocol, output from the AEAT-9955.

Depending on the PSEL setting, it can be configured as SSI2(A) Ring Mode or SSI2(B) No Ring Mode.

Data is latched on the first CLK falling edge and is transmitted on the next rising edge.

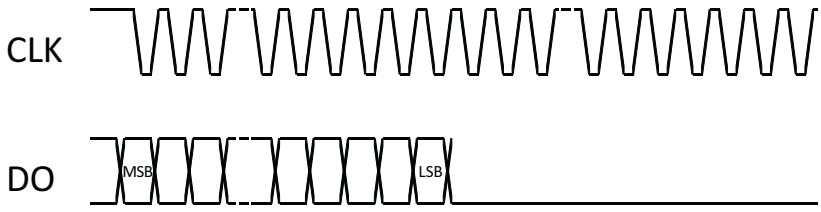


Symbol	Description	Min.	Typ.	Max.	Unit
t_{Clk}	Serial clock period	250	—	$t_M/2$	ns
t_M	Time required to place the chip in standby mode	—	16.5	18.0	µs

SSI-2(A)

By default, the chip is configured to SSI-2(A) selection; PSEL = 0 in the register setting.

Outputs single data position and remains low after LSB until the next monoflop (t_M) expires.

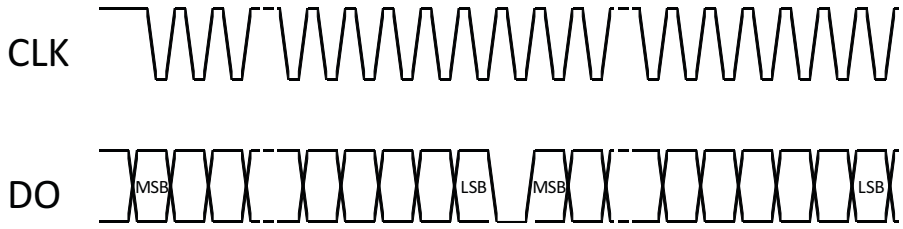


SSI-2(B)

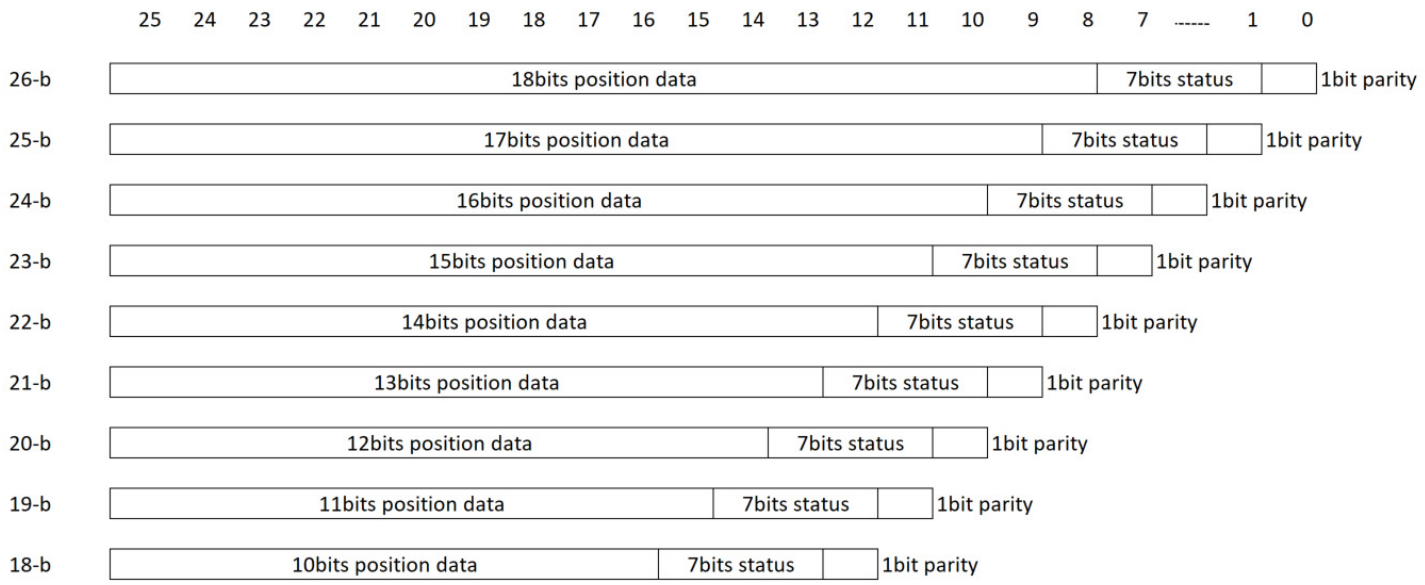
To configure the chip to SSI-2(B) selection, set PSEL = 1 in the register setting.

The same position data can be continuously output by sending clock train, and the data is separated by a single low pulse.

Data will be refreshed when the next monoflop (t_M) expires.



SSI Read Data Format



NOTE:

- 7-b status: {Ready, MHI, MLO, OV, UV, Mem, Trck}
- See Alarm for more details.

Safety and Non-safety Protocol Format

The position serial interface is available in Safety and Non-safety format; applicable for SSI3, SSI2, and SPI-8.

Position (n-bit)	Status / Alarm (7-bit)							Parity (1-bit)
Position[(n-1):0]	READY	MHI	MLO	OV	UV	MEM	TRK	parity

Position (n-bit)	Status / Alarm (8-bit)							SC (8-bit)	CRC (8/16-bit)
Position[(n-1):0]	Status[1:0] (1)	MHI	MLO	OV	UV	MEM	TRK	SC [7:0] (2)	CRC [7/15:0] (3)

NOTE:

1. 2-bit status to indicate the safety status:
   - Status = 2b'00 – Encoder not ready.
   - Status = 2b'01 – Encoder ready, Force test failed.
   - Status = 2b'10 – Encoder ready.
   - Status = 2b'11 – Encoder ready, Force test passed.
2. SC denotes as "Sequence Count" or life counter that automatically increments on every position transmission. The counting starts from 1 to 255, and the initial value upon power-up is configurable.
3. CRC poly 0x1021 or 0x1D, initial value is configurable (0x0000, 5555, AAAA, FFFF).

Alarm

Details of the alarm bit are available in the following register.

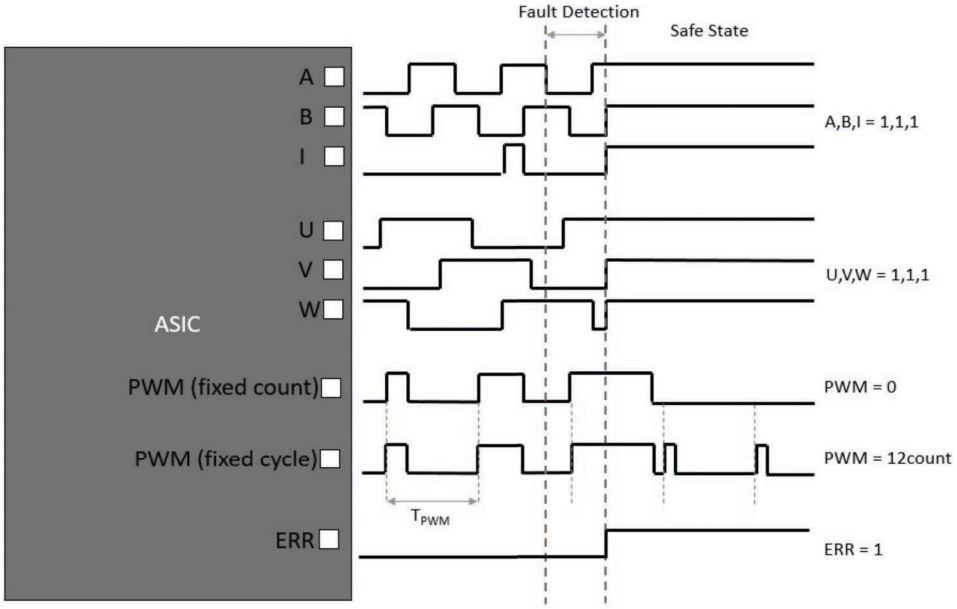
Address	Bit							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x29	RDY[1]	RDY[0]	MHI	MLO	OV	UV	MEM	TRACK

- **Ready:** The chip is ready, and the ready value is 1.
- **Parity:** 1-b parity is even parity.
- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is set high consistently, change to a weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error:** This indicates that the magnet strength detected by the chip is too weak. When this is set low consistently, change to a stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Overvoltage (OV) Error:** This indicates that the input supply has exceeded the limit. When this is set high consistently, check the supply line. The value for this alarm is represented as 1.
- **Undervoltage (UV) Error:** This indicates that the input supply has dropped below the limit. When this is set high consistently, check the supply line. The value for this alarm is represented as 1.
- **Memory Error (MEM) Error:** This indicates that memory corruption has occurred. When this is set high, perform a power-cycle to reload the memory. The value for this alarm is represented as 1.
- **Tracker (TRK) Error:** This indicates that the angular error has exceeded 5° within 5 ms. When this is set high consistently, perform a power-cycle to re-initialize the sensor. The value for this alarm is represented as 1.

The ERR pin is a dedicated hardware pin for error indication, which automatically clears once all error bits in the register are cleared. It features a push-pull output configuration and should be left floating if unused. The ERR pin output operates with OR logic, meaning that it will go high if any of the alarm bits (MHI, MLO, OV, UV, MEM, TRACK) is high.

In safety mode, once a fault is detected, the ERR pin flags high after 3 ms, and the incremental ABI, commutation UVW, and PWM outputs enter a safe state. Alternatively, users can disable the ABI/UVW safe state behavior by setting bit [3] (Inc. Safety Off) to 1 at Page 0, address 0x01'h.

Figure 16: Safe State Diagram

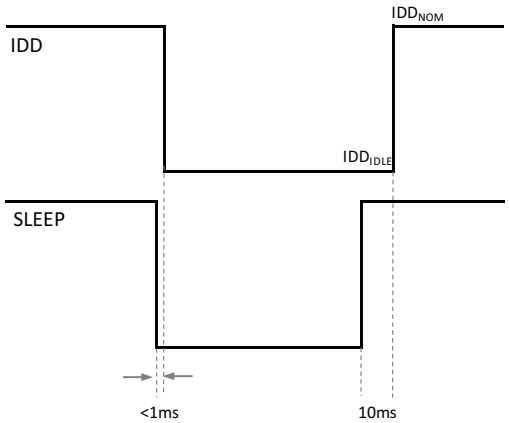


Power Modes

The AEAT-9955 is designed with two power modes:

- **Active Mode** where the chip operates under full functions with normal current consumption, IDD_{NOM}.
- **Sleep Mode** powers down the chip front-end and digital processing blocks, leaving only the detection block to track on user input with low current consumption, IDD_{IDLE}.
- The SLEEP pin is an active low, tied to VDD if unused.

Figure 17: Sleep Mode Timing



PWM

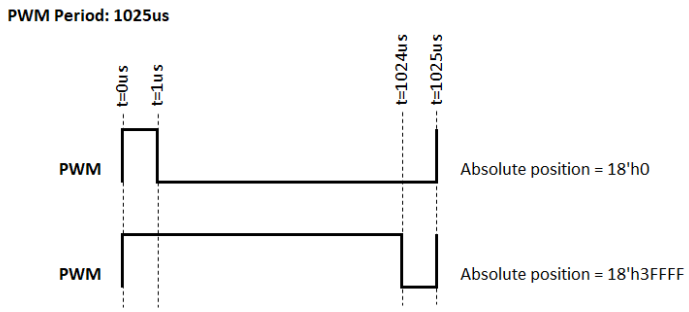
The PWM protocol uses one output pin (W_PWM) from the AEAT-9955. Note that the W_PWM pin is shared between the UVW and PWM protocols.

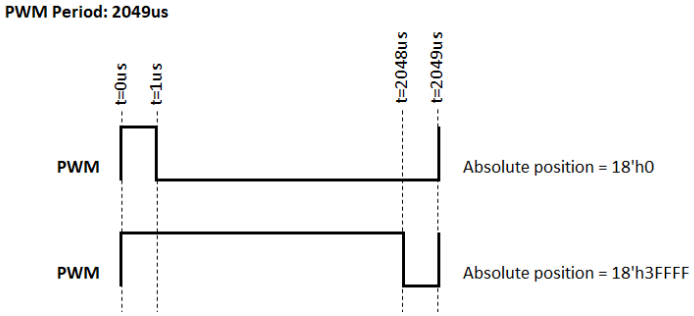
PWM Fixed Clock

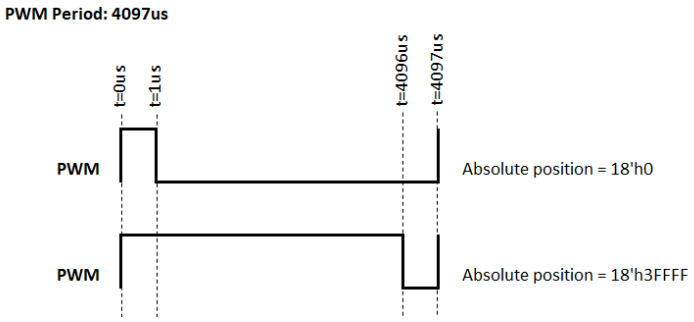
The PWM signals are configurable to have a period of 1025, 2049, 4097, 8193, or 16385 µs. During power-up, the PWM signal is 0 before chip ready.

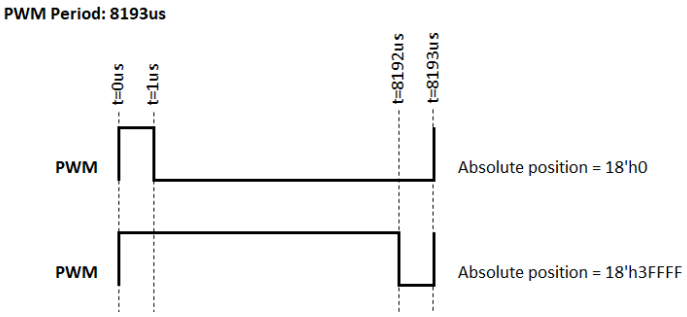
PWM Signals (Period = 1025/2049/4097/8193/16385 µs)

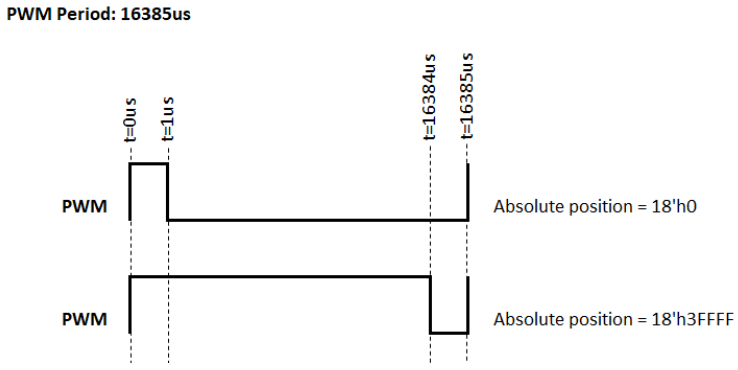
PWM Period: 1025, 2049, 4097, 8193, 16385 µs









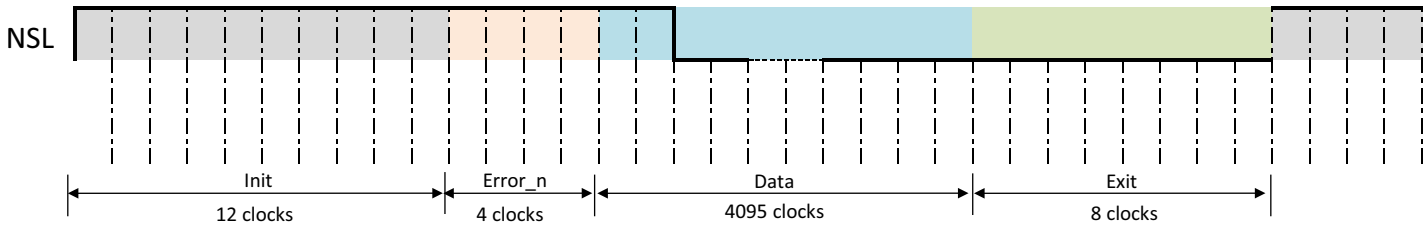


PWM Fixed Period

The PWM protocol is also available with Init, Error_n, and Exit along with Data information.

PWM Signals (Period = 1047/2071/4119/8215/16407 µs)

PMW Period: 4119 µs



Incremental Output Format

The AEAT-9955 provides ABI and UVW signals to indicate the incremental position of the motor.

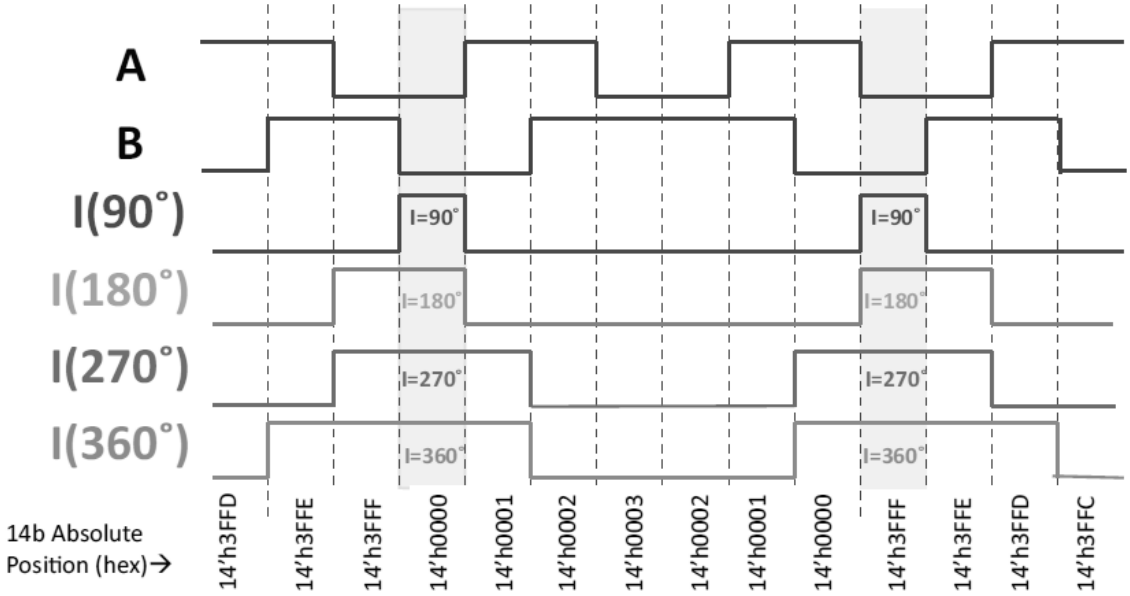
ABI

The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B, and I).

The index signal marks the absolute angular position and typically occurs once per revolution. The ABI signal is configurable using the memory map registers. It supports the following configuration:

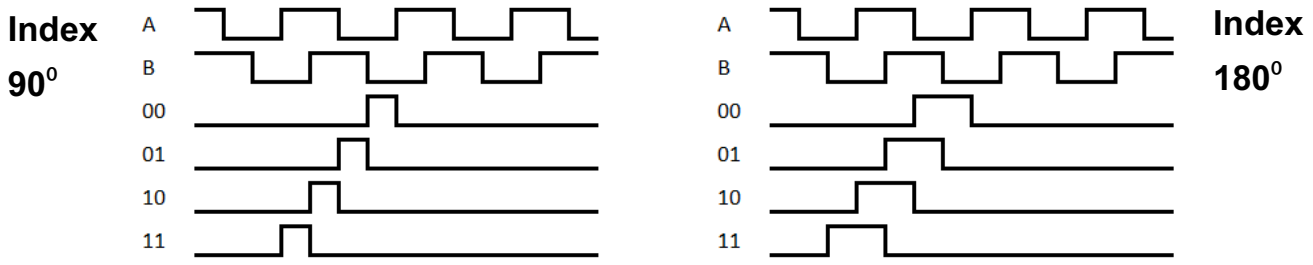
- Programmable CPR: 1 to 20,000 CPR
- Programmable I-width: 90, 180, 270, or 360 electrical degrees (edeg)
- Programmable I-state: 90, 180, 270, or 360 electrical degrees (edeg)

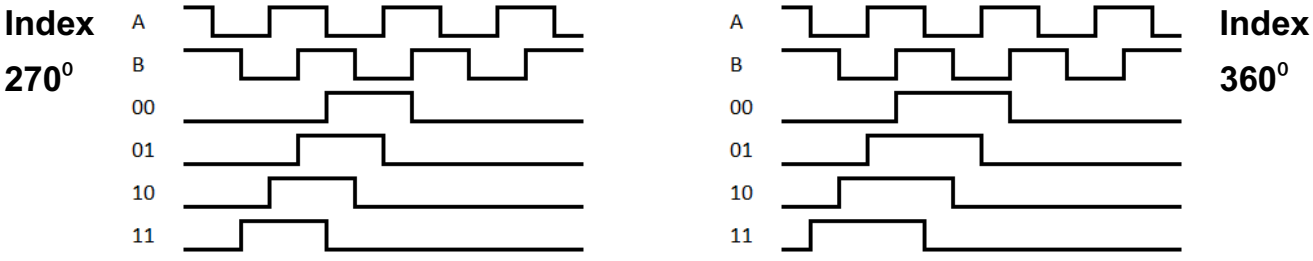
Figure 18: ABI Signal (4096 CPR, with Different I-Width Settings), Assuming Hysteresis Is Set at 0.02 Mechanical Degrees



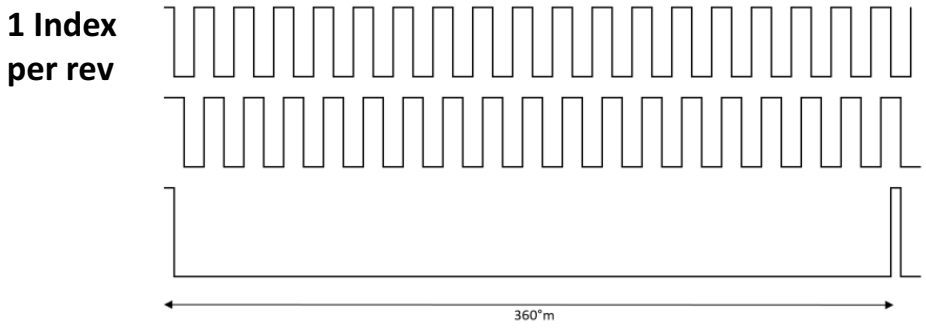
The index position is configurable among the incremental states.

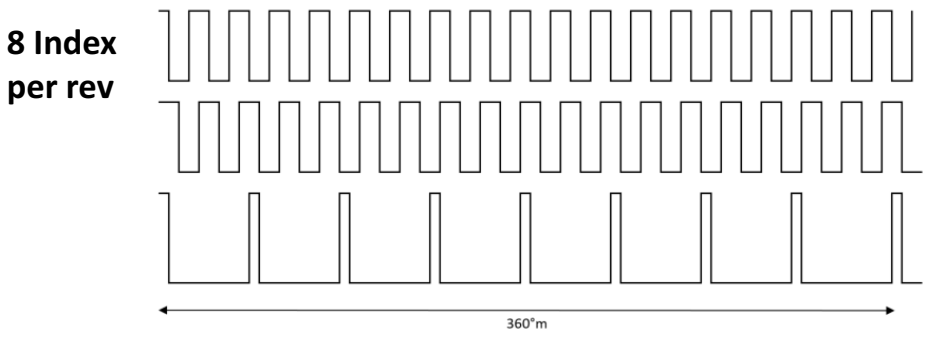
The index signal rises high once per turn at the absolute zero position.





The number of indexes per revolutions is configurable from 1 pulse up to 128 pulses.

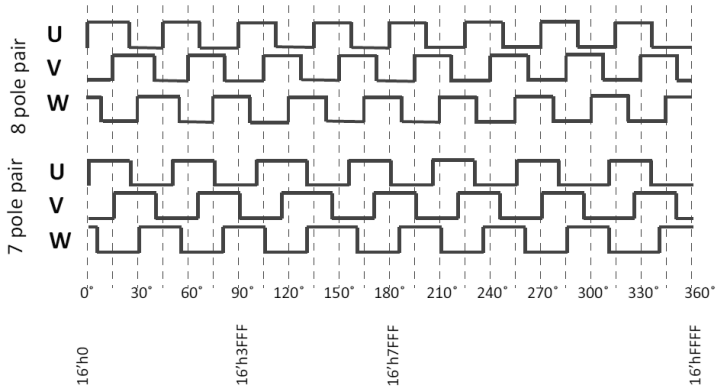


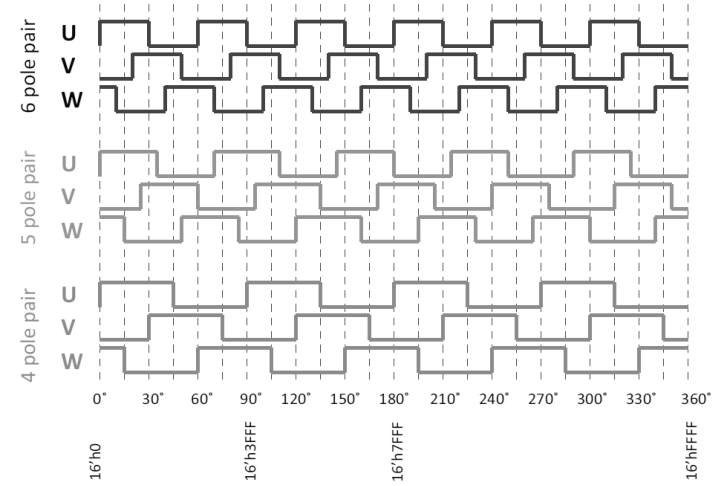


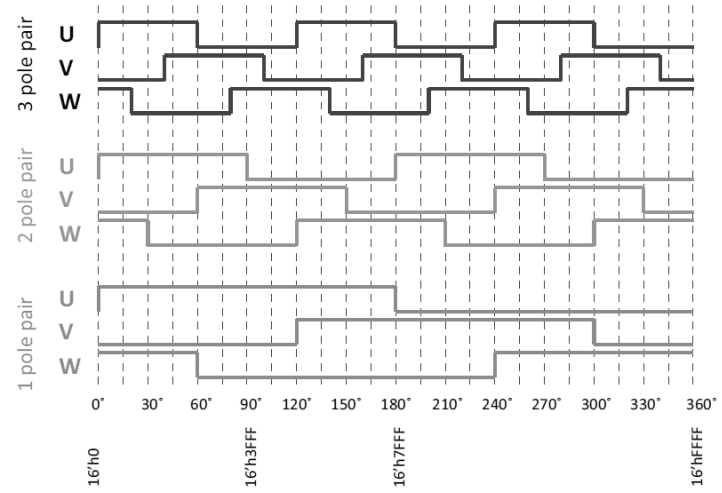
UVW

Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback and is available using three output pins. Note that the W_PWM pin is shared between the UVW and PWM protocols.

The AEAT-9955 can configure pole pairs from 1 to 32 (equivalent to 2 to 64 poles).

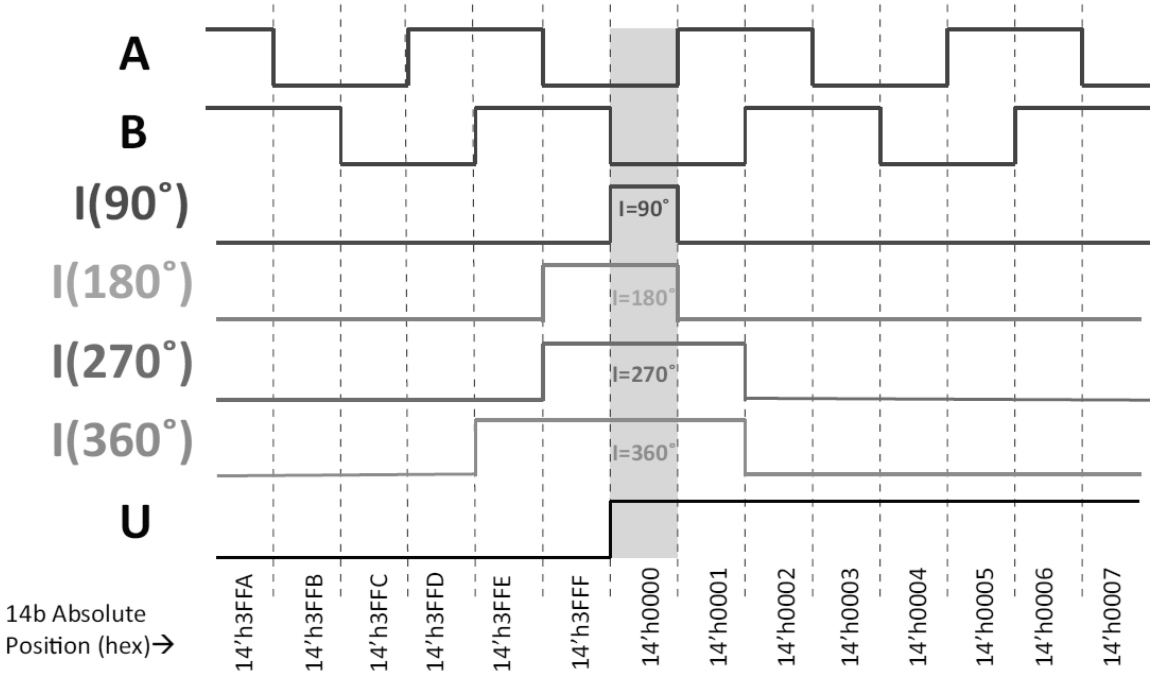






Note that signal U from the UVW protocol is tagged to signal I from the ABI protocol as shown in the following figure.

Figure 19: U-to-I Tagging



Recommended PCB Land Pattern (in mm)

Figure 20: Land Pattern Dimensions and Tolerance

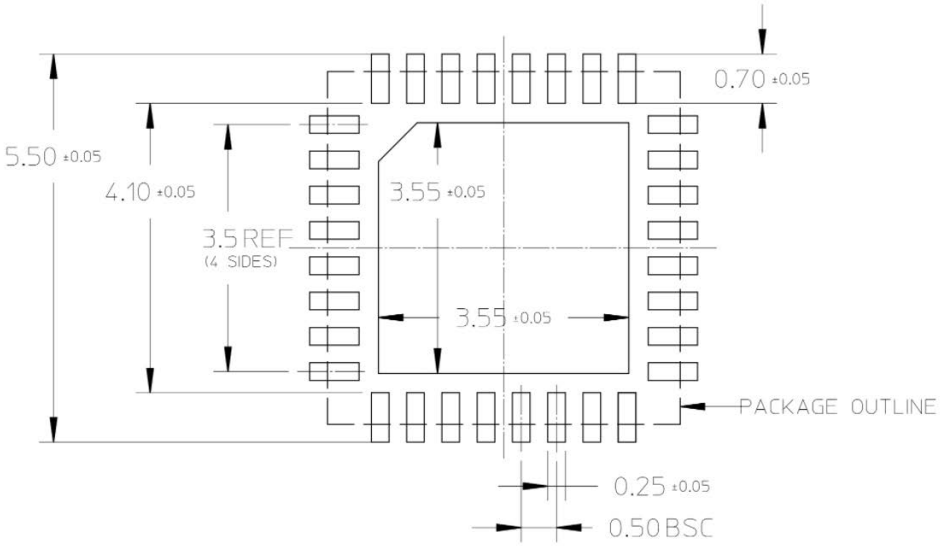
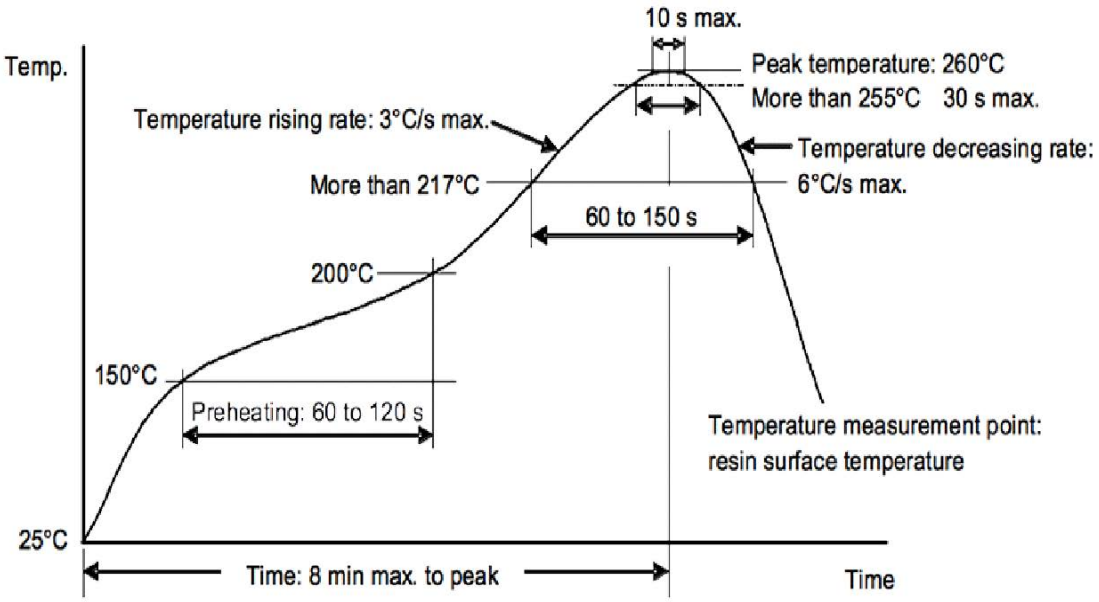


Figure 21: Recommended Lead-Free Solder Reflow Temperature Profile



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