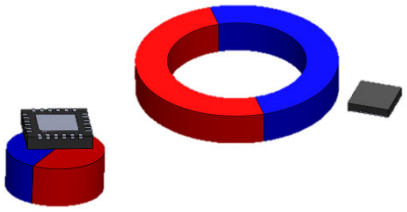
Application Note

AEAT-9922-Q24

10-Bit to 18-Bit Programmable Angular Magnetic Encoder IC



Description

The Broadcom® AEAT-9922-Q24 is a CMOS magnetic sensor structure suitable for contactless 360° encoding based on the Hall Effect technology. It provides an angle output up to 18 bits of resolution and simultaneous incremental output of up to 10,000 CPR. An integrated Hall structure at the core of the device uses a single 2-pole disc or ring magnet to convert the magnetic field vector in the chip plane into an AC signal whose amplitude and phase correspond to the magnitude and direction of the field.

An internal digital signal-processing unit then processes and conditions the raw AC signal from the sensor. The output signals are available in three different forms:

- Pulse Width Modulation (PWM)
- Absolute 18-bit position through the 3-wire or 2-wire Serial Synchronous Interface (SSI) and 4-wire Serial Protocol Interface (SPI)
- Incremental output (ABI and UVW signals)

These features can be programmed by configuring the internal registers in the Configuration mode.

More information about the product specifications of the AEAT-9922-Q24 is available in the product data sheet.

Operation Mode

The AEAT-9922-Q24 features two types of operational modes, which are normal operation mode and configuration mode.

Normal Operation Mode

This is the normal operating mode of the encoder chip. The absolute output (10-bit to 18-bit absolute position data) is available through serial protocol pins (M0, M1, M2, and M3). The following are the output signal conditions during AEAT-9922 initialization:

- PWM signals all 0s.
- ABI signals all 1s.
- UVW signals all 0s.

The incremental positions are indicated on ABI and UVW signals with user-configurable CPR from 1 to 10,000 of ABI signals and pole pairs from 1 to 32 (2 to 64 poles) for UVW commutation signals.

Configuration Mode

The AEAT-9922-Q24 has a built-in nonvolatile memory for user data and encoder configurations. Programming of the AEAT-9922-Q24 can be performed with the HEDS-9922 programming kit or any tester or programmer device using the guidelines provided.

Absolute and Incremental Programming

The absolute resolution can be set to 10, 11, 12, 13, 14, 15, 16, 17, or 18 bits. For incremental selection, ABI or UVW can be selected by following the instructions in the following sections. The PWM output is available as well.

The shadow registers are programmable using the SPI protocol. Writing specific commands to specific addresses of the internal registers will program values of shadow registers to memory. The memory can be programmed multiple times (up to 1000 times).

Customer Configuration Registers

The AEAT-9922 encoder IC uses nonvolatile EEPROM with 8 bits data per address to store the encoder settings and user Data. For EEPROM programming, the process can be performed at 3.3V or 5V supply.

There are 7 bytes (7 × 8 bits) of Customer Reserved Memory that can be used to store any application information.

Table 1: Customer Reserved Memory

Address	Bits	Name	Description	Default
0x00	[7:0]	Customer Reserve 0	User programmable	8'h00
0x01	[7:0]	Customer Reserve 1	User programmable	8'h00
0x02	[7:0]	Customer Reserve 2	User programmable	8'h00
0x03	[7:0]	Customer Reserve 3	User programmable	8'h00
0x04	[7:0]	Customer Reserve 4	User programmable	8'h00
0x05	[7:0]	Customer Reserve 5	User programmable	8'h00
0x06	[7:0]	Customer Reserve 6	User programmable	8'h00

EEPROM Memory Access

- The AEAT-9922 encoder IC uses Multiple-Time Programmable (MTP) shadow registers to access the built-in EEPROM within the IC.
- MTP registers are volatile (upon power-up, reload the corresponding values from EEPROM) and are not written to the EEPROM automatically.
- To write MTP shadow registers values to EEPROM (nonvolatile) memory, see EEPROM Programming.
- The MTP shadow registers addresses 0x07 to 0x0E are available for users to configure the encoder as required.
- All bits (addresses 0x00 to 0x0E) are in lock mode upon power-up.
- Users are required to write a hexadecimal value of 8'hAB to address 0x10 to unlock the registers.
- In UNLOCK mode, you may write to any MTP shadow registers or registers. Values written will remain until power off.
- The UNLOCK state is maintained until the power supply is turned off or any value (except 8'hAB) is written to address 0x10.
- Other addresses are factory reserved or with factory preconfigured values. Do not overwrite these values.

Table 2: Customer Configuration-0 Registers

Address	Bits	Name	Description	Default
0x07	[7]	Hardware ST Zero	**1: Enable external pin** 0: Disable external pin	1
	[6]	Hardware Accuracy Calibration	**1: Enable external pin** 0: Disable external pin	1
	[5]	Axis Mode	1: Off-axis **0: On-axis**	0
	[4]	Reserved	0: Reserved	0
	[3:2]	I-Width Setting (ABI)	**00: 90 electrical degrees (°e)** 01: 180 electrical degrees (°e) 10: 270 electrical degrees (°e) 11: 360 electrical degrees (°e)	00
	[1:0]	I-Phase Setting (ABI)	**00: 90 electrical degrees (°e)** 01: 180 electrical degrees (°e) 10: 270 electrical degrees (°e) 11: 360 electrical degrees (°e)	00
0x08	[7:5]	Hysteresis Setting	000: 0.00 mechanical degree (m°) 001: 0.01 mechanical degree (m°) 010: 0.02 mechanical degree (m°) 011: 0.04 mechanical degree (m°) **100: 0.08 mechanical degree (m°)** 101: 0.17 mechanical degree (m°) 110: 0.35 mechanical degree (m°) 111: 0.70 mechanical degree (m°)	100
	[4]	Direction Setting	1: Count up at counterclockwise rotation top view **0: Count up at clockwise rotation**	0
	[3:0]	Absolute Resolution[a]	**0000: 18-b absolute resolution (SSI)** 0001: 17-b absolute resolution (SSI) 0010: 16-b absolute resolution (SSI) 0011: 15-b absolute resolution (SSI) 0100: 14-b absolute resolution (SSI) 0101: 13-b absolute resolution (SSI) 0110: 12-b absolute resolution (SSI) 0111: 11-b absolute resolution (SSI) 1000: 10-b absolute resolution (SSI) 1001 to 1111: Reserved	0000

a. Flexible 18-bit absolute resolution from 10-bit to 18-bit. Combinations lower than 10-bit are invalid.

Table 3: Customer Configuration-1 Registers

Address	Bits	Name	Description	Default
0x09	[7:6]	Reserved	00 ~11: Reserved	01
	[5:0]	Incremental Resolution [13:8][a]	00-0000-0000-0000: 0 CPR (OFF)	00
0x0A	[7:0]	Incremental Resolution [7:0][a]	00-0000-0000-0001: 1 CPR	0100
			00-0000-0000-0010: 2 CPR	0000
			00-0000-0000-0011: 3 CPR	0000
			...	
			00-0000-1000-0000: 128 CPR	
			...	
			00-0100-0000-0000: 1024 CPR	
			...	
			10-0000-0000-0000: 8192 CPR	
			...	
			10-0111-0001-0000: 10,000 CPR	

a. Flexible 14-bit Incremental resolution up to 10000CPR. Combination above 10000 is invalid.

Table 4: Customer Configuration-2 Registers

Address	Bits	Name	Description	Default
0x0B	[7]	Reserved	0: Reserved	0
	[6:5]	PSEL [1:0][a]	**00: SSI3a/SPI4a** 01: SSI3b/SPI4b 10: SSI2a/UVW 11: SSI2b/PWM	00
	[4:0]	UVW, PWM Setting[b]	**00000: UVW = 1 pole pairs/PWM fixed period = 10 bits** 00001: UVW = 2 pole pairs/PWM fixed period = 11 bits 00010: UVW = 3 pole pairs/PWM fixed period = 12 bits 00011: UVW = 4 pole pairs/PWM fixed period = 13 bits 00100: UVW = 5 pole pairs/PWM fixed period = 14 bits 01000: UVW = 9 pole pairs/PWM fixed clock = 10 bits 01001: UVW = 10 pole pairs/PWM fixed clock = 11 bits 01010: UVW = 11 pole pairs/PWM fixed clock = 12 bits 01011: UVW = 12 pole pairs/PWM fixed clock = 13 bits 01100: UVW = 13 pole pairs/PWM fixed clock = 14 bits	00000

a. In conjunction with the table for input/output configuration; see Table 9, Configurable Interface I/O and Selection Table.

b. UVW: Flexible 5-bit UVW resolution up to 32 pole pairs.
PWM: Only shown settings are available, other combinations are invalid.

Table 5: Customer Single-Turn Reset

Address	Bits	Name	Description	Default
0x0C	[7:0]	Zero Reset 2	MSB bit-17 to bit-10 of Absolute Single-turn	0000-0000
0x0D	[7:0]	Zero Reset 1	Bit-9 to bit-2 of Absolute Single-turn	0000-0000
0x0E	[7:6]	Zero Reset 0	LSB bit-1 to bit-0 of Absolute Single-turn	00

EEPROM Programming

Perform the following steps to program the MTP shadow register to EEPROM.

1. Write the desired values to the Customer Configuration MTP registers (0x00 to 0x0E).
2. Verify the written value by reading back all Customer Configuration MTP registers (0x00 to 0x0E).
3. Write value 8'hA1 to address 0x11 to program all Customer Configuration MTP registers to EEPROM.
   Memory busy bit[8] address 0x22 flags high for 40 ms.
4. When done, perform a power cycle and check for Memory Error bit[4] address 0x21.
   – 0: No memory error
   – 1: Memory error

Table 6: Memory Unlock and Program

Address	Value	Name	Description	Default
0x10	8'hAB	Unlock	Unlock register addresses 0x00 to 0x0E	0000-0000
0x11	8'hA1	Program	Program all Customer Configuration MTP registers to EEPROM	0000-0000

Warning and Error Bit

Error bit is triggered if a Magnet High (MHI), Magnet Low (MLO), Memory Error (MEM_Err), or communication error occurs.

Details of error bits are available in the following register address.

Table 7: Error Bits Register

Address	Bit								
[decimal]	[hex]	7	6	5	4	3	2	1	0
33	0x21	RDY	MHI	MLO	MEM_Err				

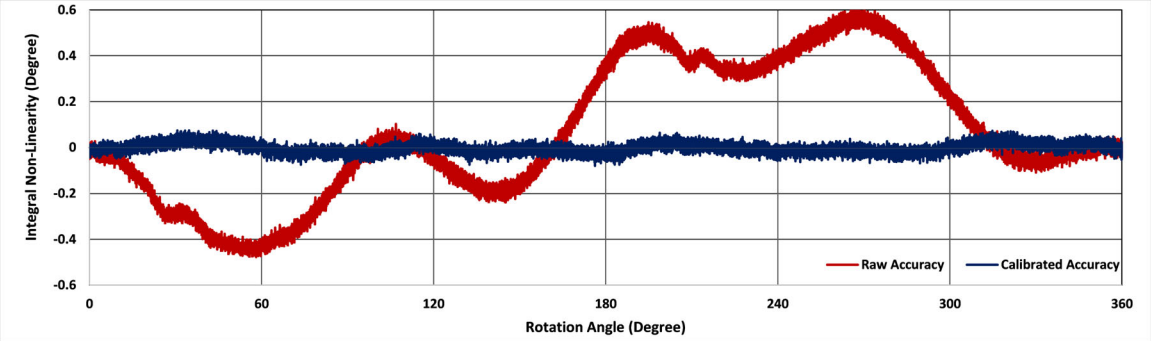
- **Magnet High (MHI) Error**: This indicates that the magnet strength detected by the chip is too strong. When this is flagged high consistently, change to a weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error**: This indicates that the magnet strength detected by the chip is too weak. When this is flagged high consistently, change to a stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Ready (RDY)**: The chip is ready, and the ready value is 1.
- **Memory Error (MEM_Err)**: The chip memory content is corrupted (per CRC check).

Encoder Calibration

Accuracy Angle Calibration

To achieve high degree of angle accuracy, AEAT-9922-Q24 comes with a built-in correction algorithm. This algorithm will correct the error upon installation of encoder to the motor. The following figure shows the comparison between raw and corrected accuracy over one rotation.

Figure 1: Example of Raw and Corrected Accuracy (Mechanical Degree) over One Rotation (360 Degrees)



Calibration Procedure Using the SPI Register

1. Mount the encoder to the motor system (with the magnet).
2. Rotate the magnet at constant speed ranging from 60 RPM to 2000 RPM.
3. When the speed stabilizes, write value 8'h02 to address 0x12 to initiate the calibration sequence.
4. Read the calibration status on bit [1:0] of address 0x22.
   - 10: Calibration Pass
   - 11: Calibration Fail
5. Write value 8'h00 to address 0x12 to exit the calibration sequence.

   The calibration value is automatically stored in memory; no further programming is required.
   - To erase the calibration value, write value 8'h01 to address 0x12.
   - Write value 8'h00 to address 0x12 to return to operation mode.

Calibration Procedure Using Hardware Pin M1

1. Mount the encoder to the motor system (with magnet).
2. Rotate the magnet at a constant speed ranging from 60 RPM to 2000 RPM.
3. When the speed stabilizes, pull the M1 signal to High for more than 50 ms to initiate the calibration sequence.
4. Read the calibration status on output pin ABI.
   - If AB=1, I=0: Calibration Pass
   - If AB=1, I=1: Calibration Fail

   The calibration value is automatically stored in memory; no further programming is required.

NOTE: Hardware pin calibration is automatically disabled upon completion. To reenable this function, write value 8'h40 to address 0x07.

Zero Reset Calibration

AEAT-9922-Q24 allows users to configure the zero reset position.

Calibration Procedure Using the SPI Register

1. Stop the motor system at the desired encoder zero position.
2. When the motor shaft is stationary, write a value 8'h08 to address 0x12 to reset the absolute single-turn position.
3. Read the calibration status on bit [3:2] of address 0x22.
   - 10: Calibration Pass
   - 11: Calibration Fail
4. Write value 8'h00 to address 0x12 to exit the calibration sequence.

   The offset value is automatically stored in memory; no further programming is required.
   - To erase the calibration value, write value 8'h04 to address 0x12.
   - Write value 8'h00 to address 0x12 to return to operation mode.

Calibration Procedure Using Hardware Pin M2

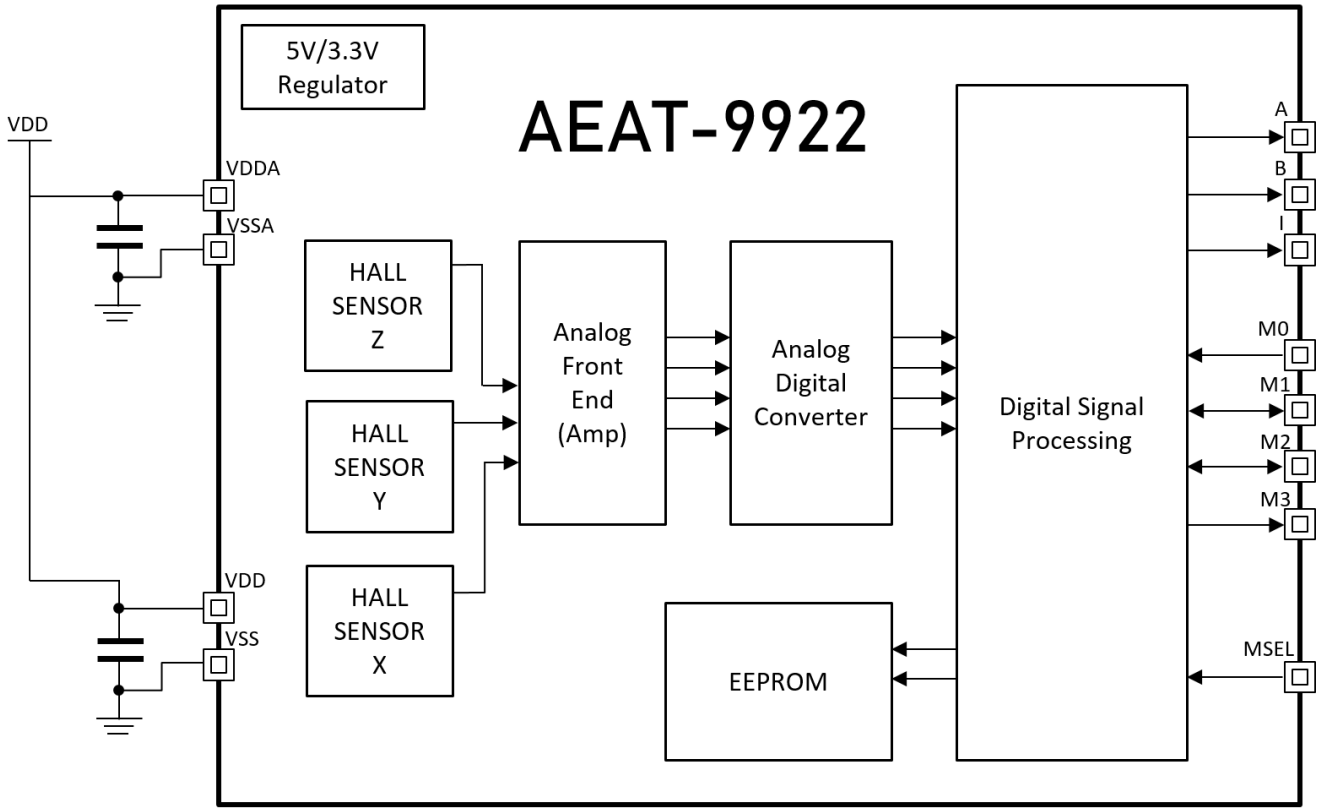
1. Stop the motor system at the desired encoder zero position.
2. When the motor shaft is stationary, pull the M2 signal to High for more than 50 ms to reset the absolute single-turn position.
3. Read the calibration status on output pin ABI.
   - If AB=1, I=0: Calibration Pass
   - If AB=1, I=1: Calibration Fail

   The calibration value is automatically stored in memory; no further programming is required.

NOTE: Hardware pin calibration is automatically disabled upon completion. To reenable this function, write value 8'h80 to address 0x07.

AEAT-9922-Q24 Circuit Diagram

Figure 2: Recommended Circuit Diagram for AEAT-9922-Q24



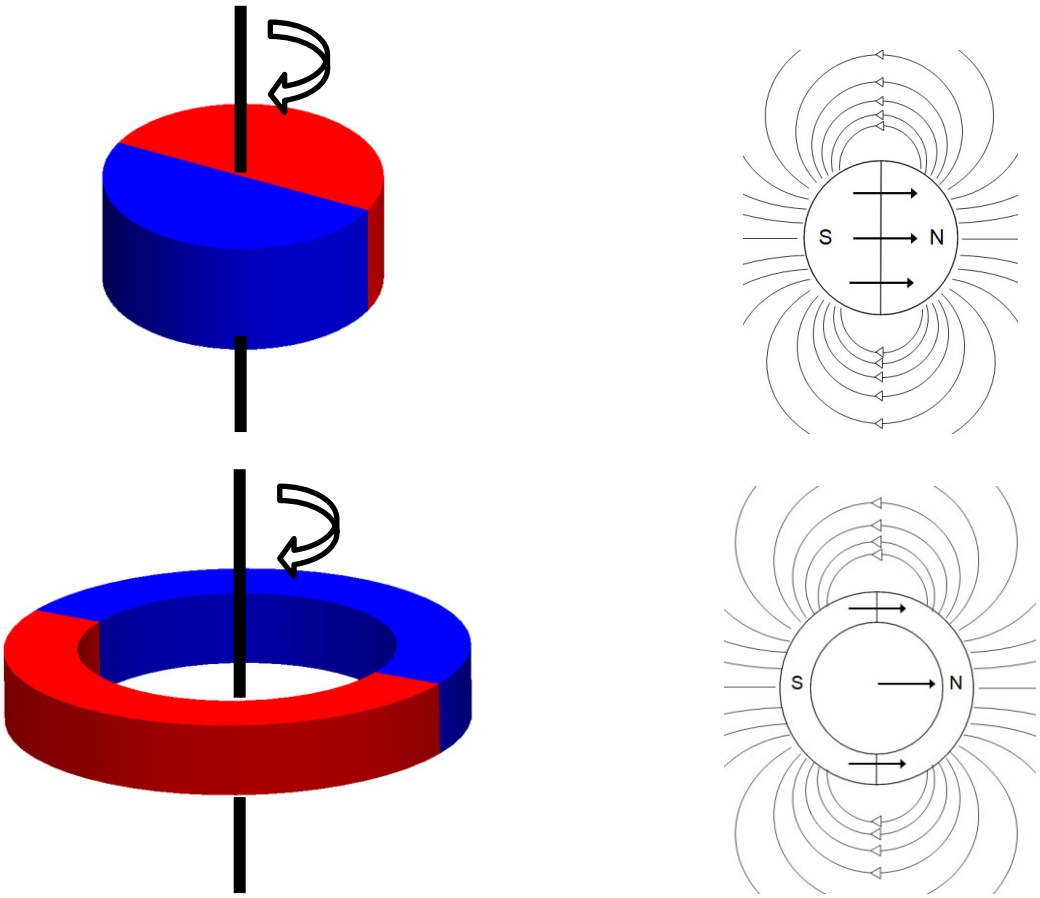
NOTE: Connect the 10-µF and 100-nF capacitors as close to the individually assigned power and ground pins as possible.

Magnetic Input Specifications

Table 8: Magnet Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Diameter	d	4				Recommended magnet: Cylindrical magnet or ring magnet diametrically magnetized & 1 pole pair.
Disc magnet		—	6	—	mm	
Ring magnet ID			ID,15	—	mm	
Ring magnet OD			OD, 25	—	mm	
Thickness	t					
Disc magnet		—	2.5	—	mm	
Ring magnet		2	6	—	mm	
Magnetic input field magnitude	Bpk					Required vertical/horizontal component of the magnetic field strength on the die's surface, measured along concentric circle.
On-axis (Disc Magnet)		45	—	100	mT	
Off-axis (Ring Magnet)		30	—	150	mT	
Magnet displacement radius	R_m	—	—	0.25	mm	Displacement between the magnet axis to the device center.
Recommended magnet material and temperature drift		—	–0.12	—	%/K	NdFeB (Neodymium Iron Boron), grade N35SH.

Figure 3: Diametrically Magnetized Magnet



Magnet and IC Package Placement

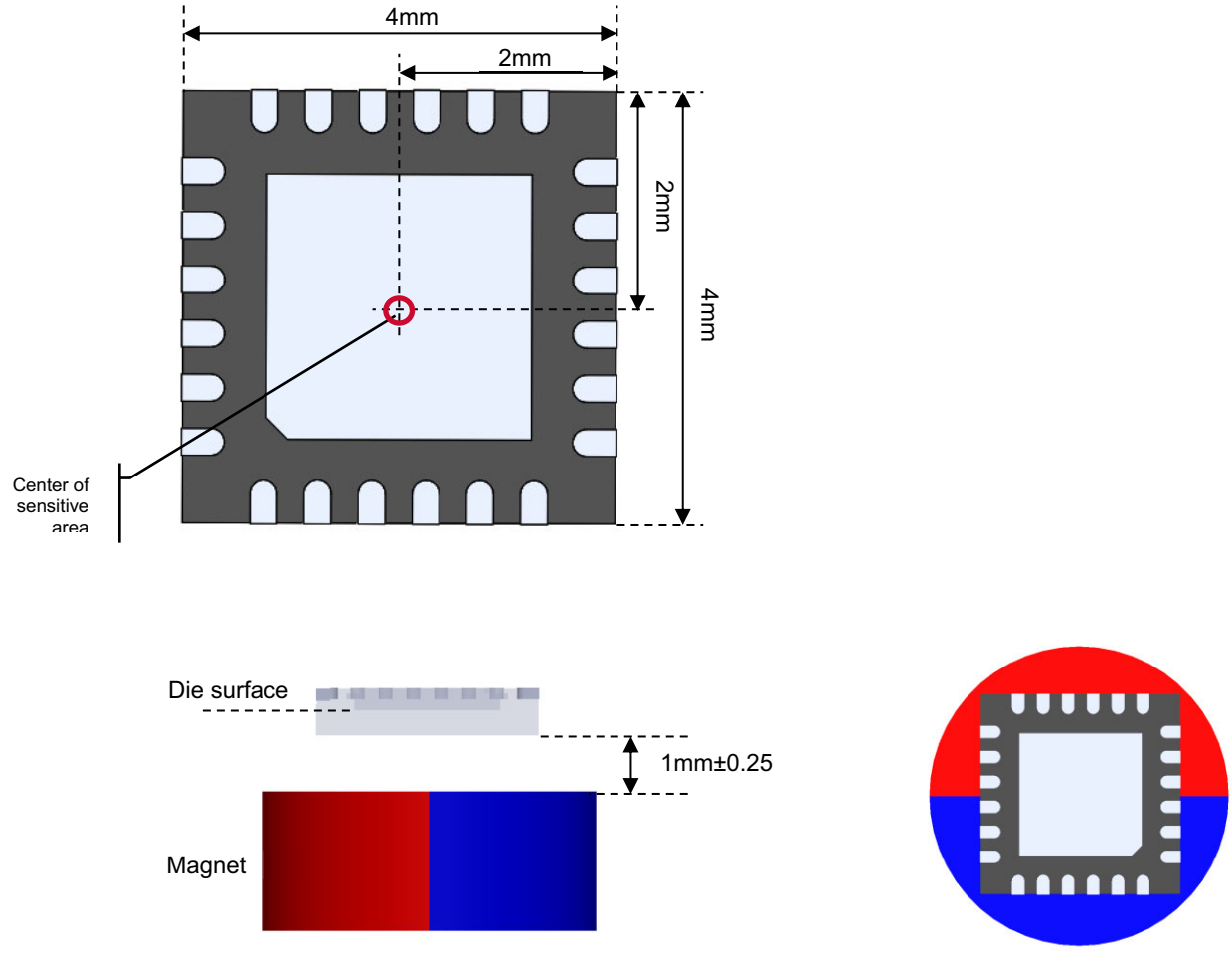
On-Axis Configuration

Align the magnet's center axis within a displacement radius of 0.25 mm from the defined Hall sensor center.

Place the magnet so that it faces the sensor. The magnet must be mounted on a non-magnetic part. The Z gap varies depending on the magnetic strength on the die surface, with the recommended magnet material and dimensions.

The typical distance Z is 0.75 mm to 1.25 mm (1 mm ± 0.25 mm). Do not put magnetic material close to the magnet because it will affect the magnetic field and increase the INL.

Figure 4: Defined Chip Sensor Center and Magnet Displacement



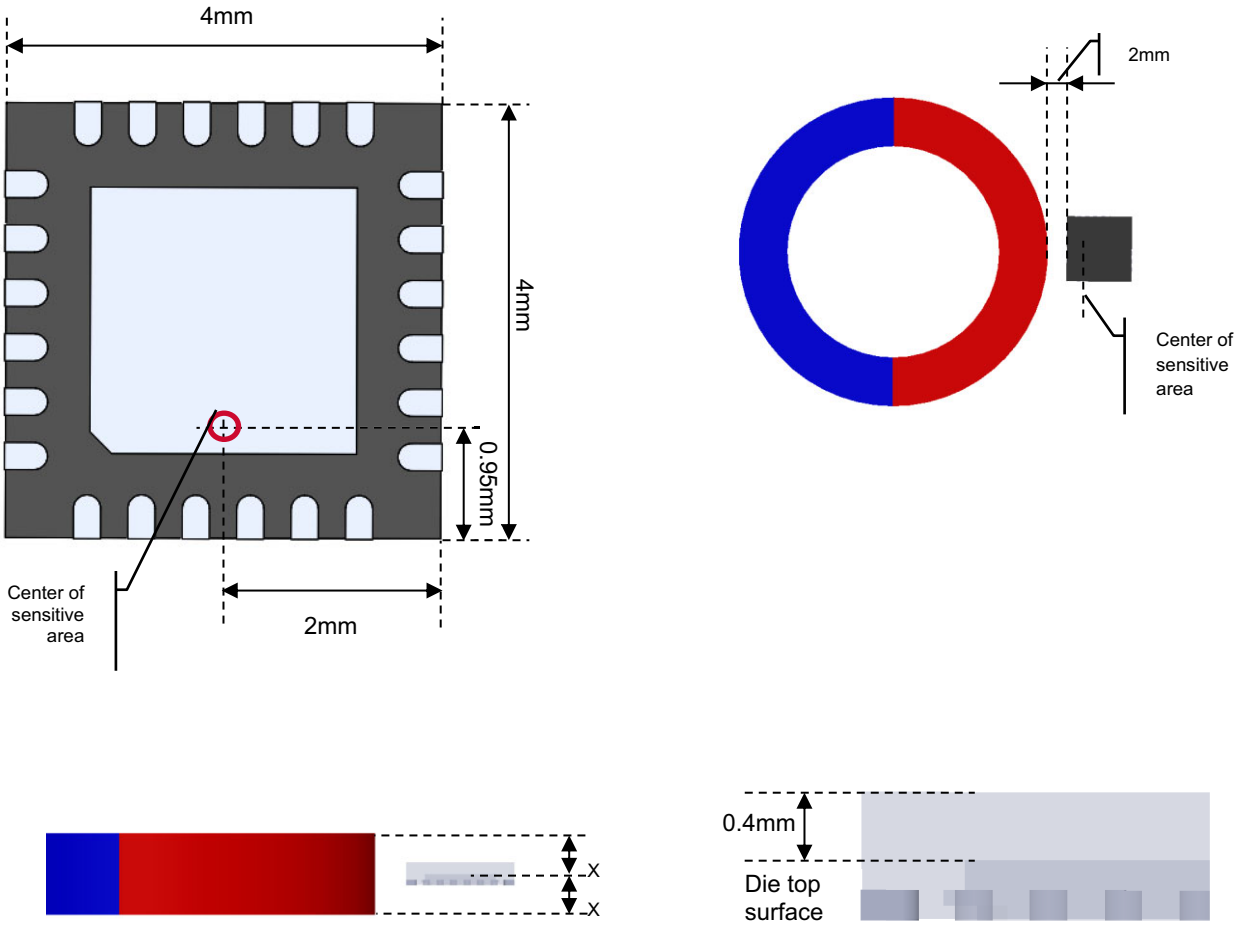
Off-Axis Configuration

Align the magnet's edge within a displacement of 2 mm from the chip edge with the center of sensitive area orientated to it.

Place the magnet next to the sensor. The magnet must be mounted on a non-magnetic part. The air gap varies depending on the magnetic strength on the die surface, with the recommended magnet material and dimensions.

The height placement of chip is in the middle of magnet thickness. Do not put magnetic material close to the magnet because it will affect the magnetic field and increase the INL.

Figure 5: Defined Chip Sensor Center and Magnet Displacement



NOTE: The magnet center should align to the die top surface.

Absolute Output Format

AEAT-9922 has a total of 10 interfaces; one is dedicated for incremental ABI and remaining are multiplexed to I/O pins M0, M1, M2, and M3. Each output is configurable using the M0 pin, the MSEL pin and the PSEL registers as shown in the following table.

Table 9: Configurable Interface I/O and Selection Table

Pin	Mode									
	SPI-3	SSI-3(A)	SSI-3(B)	SSI-2(A)	SSI-2(B)	SPI-4(A)	SPI-4(B)	UVW	PWM	Remarks
MSEL	0	0	0	0	0	1	1	1	1	I/O Pin
PSEL[1]	x	x	x	x	x	0	0	1	1	Memory
PSEL[0]	x	0	1	0	1	0	1	0	1	Memory
M0	0	1	1	1	1	NCS	NCS	ERR	ERR	I/O Pin
M1	DIN	NSL	NSL	0	0	MOSI	MOSI	U	N/A	I/O Pin
M2	SCK	SCL	SCL	SCL	SCL	SCK	SCK	V	N/A	I/O Pin
M3	DO	DO	DO	DO	DO	MISO	MISO	W	PWM	I/O Pin

NOTE:

1. PSEL[1], PSEL[0] is configurable through memory, see Table 4, Customer Configuration-2 Registers.
2. MSEL, M0, M1, M2, M3 are configurable through the I/O pads.

SPI4 Protocol

SPI4 protocol uses four pins from AEAT-9922. These four pins are shared among the UVW, SSI, SPI protocols. MSEL (input pin) selects either protocol at a time. Assert 1 on MSEL pin to select the SPI4 protocol.

SPI4 protocols allow users to access memory read or write and position data. They use CPOL=0, CPHA=1 for triggering.

- M0 → SPI_Chip Select (NCS) signal for SPI protocol, input to AEAT-9922
- M1 → SPI_Data Input (MOSI) signal for SPI protocol, input to AEAT-9922
- M2 → SPI_Clock Input (SCK) signal for SPI protocol, input to AEAT-9922
- M3 → SPI_Data Output (MISO) signal for SPI protocol, output from AEAT-9922

Figure 6: SPI4 Timing Diagram

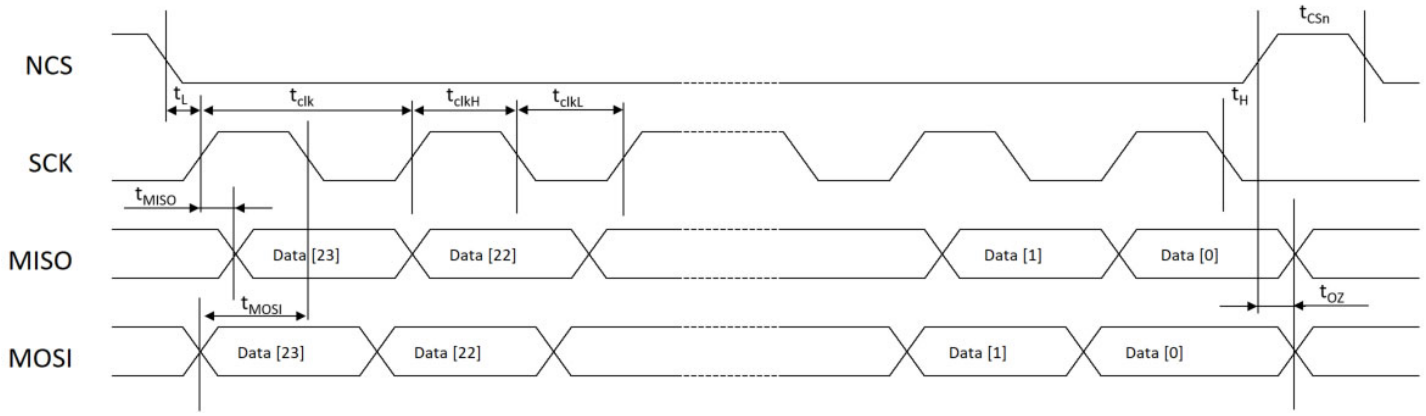


Table 10: SPI4 Timing Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
t_L	Time between NCS falling edge and SCK rising edge	350	—	—	ns
t_{clk}	Serial clock period	100	—	—	ns
t_{clkL}	Low period of serial clock	50	—	—	ns
t_{clkH}	High period of serial clock	50	—	—	ns
t_H	Time between last falling edge of SCK and rising edge of NCS	t_{clk} / 2	—	—	ns
t_{CSn}	High time of NCS between two transmission	350	—	—	ns
t_{MOSI}	Data input valid to clock edge	20	—	—	ns
t_{MISO}	SCK edge to data output valid	—	51	—	ns
t_{OZ}	Time between NCS rising edge and MISO Hi-Z	—	10	—	ns

NOTE: Users should read back the data to confirm it is written successfully.

SPI4 Command and Data Frame

Figure 7: SPI4 Read Sequence

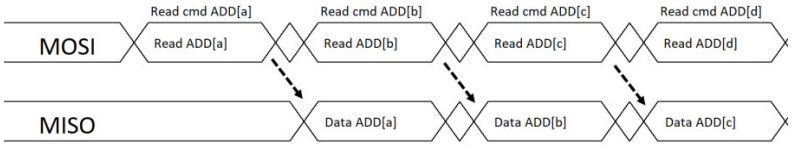
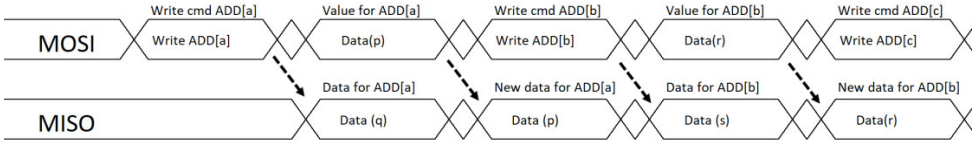


Figure 8: SPI4 Write Sequence



By default, the chip is configured to SPI4 16-bit selection, **PSEL [1] = 0**, **PSEL [0] = 0** in the register setting.

Figure 9: SPI-4(A) 16-Bit (Parity)

	Data Format																			
	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Master to Slave					P	RW	0	0	0	0	0	0	Addr/Data[7:0]							
Slave to Master (memory)					P	EF	0	0	0	0	0	0	Data[7:0]							
Slave to Master (pos 10b)					P	EF	Pos[9:0]									0	0	0	0	
Slave to Master (pos 11b)					P	EF	Pos[10:0]										0	0	0	
Slave to Master (pos 12b)					P	EF	Pos[11:0]											0	0	
Slave to Master (pos 13b)					P	EF	Pos[12:0]												0	
Slave to Master (pos 14b)					P	EF	Pos[13:0]													
Slave to Master (pos 15b)				P	EF	Pos[14:0]														
Slave to Master (pos 16b)			P	EF	Pos[15:0]															
Slave to Master (pos 17b)		P	EF	Pos[16:0]																
Slave to Master (pos 18b)	P	EF	Pos[17:0]																	

P: Parity; EF: Error Flag; RW: Read = 1, Write = 0

To configure the chip to SPI4 24-bit selection, set **PSEL [1] = 0**, **PSEL [0] = 1** in the register setting.

Figure 10: SPI4-(B) 24-Bit (CRC)

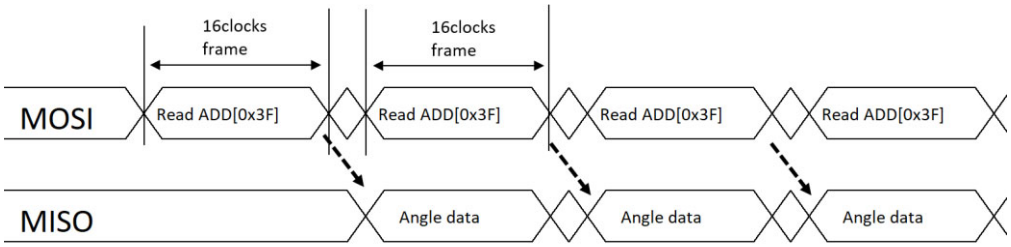
	Data Format																											
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Master to Slave					0	RW	0	0	0	0	0	0	Addr/Data[7:0]								CRC[7:0]							
Slave to Master (memory)					W	E	0	0	0	0	0	0	Data[7:0]								CRC[7:0]							
Slave to Master (pos 10b)					W	E	Pos[9:0]										0	0	0	0	CRC[7:0]							
Slave to Master (pos 11b)					W	E	Pos[10:0]											0	0	0	CRC[7:0]							
Slave to Master (pos 12b)					W	E	Pos[11:0]												0	0	CRC[7:0]							
Slave to Master (pos 13b)					W	E	Pos[12:0]													0	CRC[7:0]							
Slave to Master (pos 14b)					W	E	Pos[13:0]														CRC[7:0]							
Slave to Master (pos 15b)				W	E	Pos[14:0]															CRC[7:0]							
Slave to Master (pos 16b)			W	E	Pos[15:0]																CRC[7:0]							
Slave to Master (pos 17b)		W	E	Pos[16:0]																	CRC[7:0]							
Slave to Master (pos 18b)	W	E	Pos[17:0]																		CRC[7:0]							

NOTE: W: Warning; E: Error; RW: Read = 1, Write = 0

Position Read

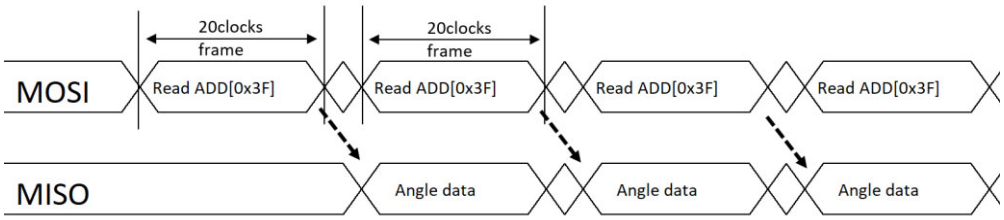
Absolute position data can be obtained by sending read command to address 0x3F.

Figure 11: Read Command



In the event of higher single turn resolution (15-bit and above), the command and data frame size is adjusted accordingly.

Figure 12: Command and Data Frame Example for 18 Bits + 2 Bits (Parity and Error)



SPI3 Protocol

SPI3 protocols only allow access to memory read write. Assert 0 on the **MSEL** pin and the **M0** pin to configure it.

- M1 → SPI_Data Input (DIN) signal for SPI protocol, input to AEAT-9922
- M2 → SPI_Clock Input (SCK) signal for SPI protocol, input to AEAT-9922
- M3 → SPI_Data Output (DO) signal for SPI protocol, output from AEAT-9922

Figure 13: SPI3 Timing Diagram

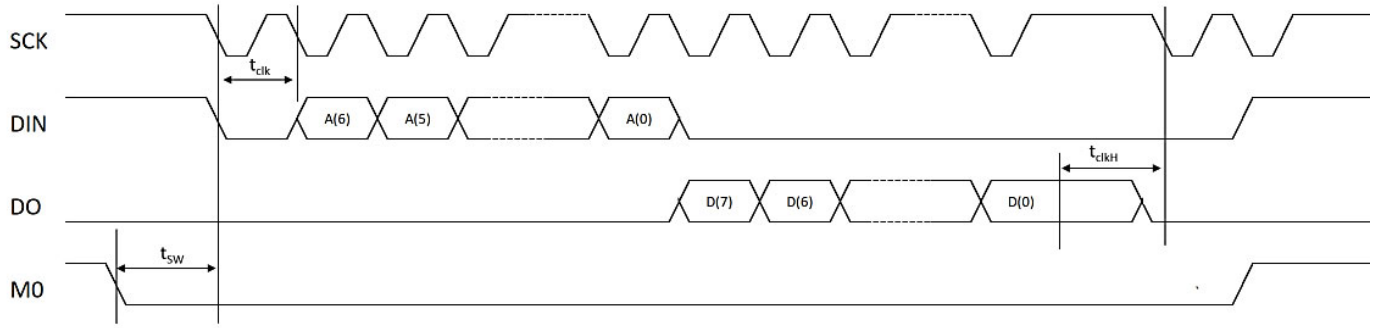


Table 11: SPI3 Timing Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
t_{SW}	Time between M0 falling edge and SCK falling edge	1	—	—	µs
t_{clk}	Serial clock period	—	—	100	ns
t_{clkH}	SCK clock high time after end of last clock period	300	—	—	ns

NOTE: The user should read back data to confirm data is written successfully.

Figure 14: SPI3 Read

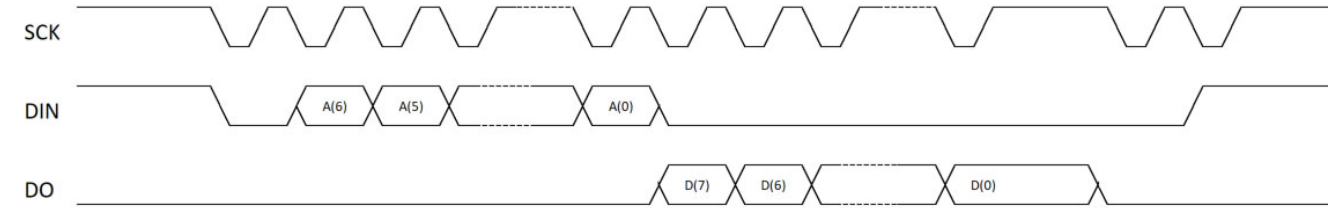
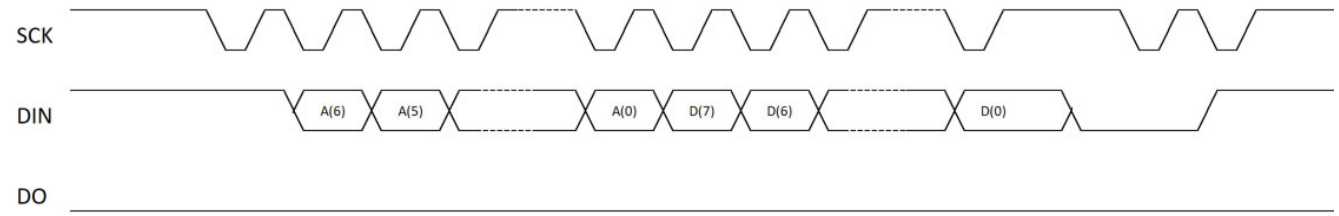


Figure 15: SPI3 Write

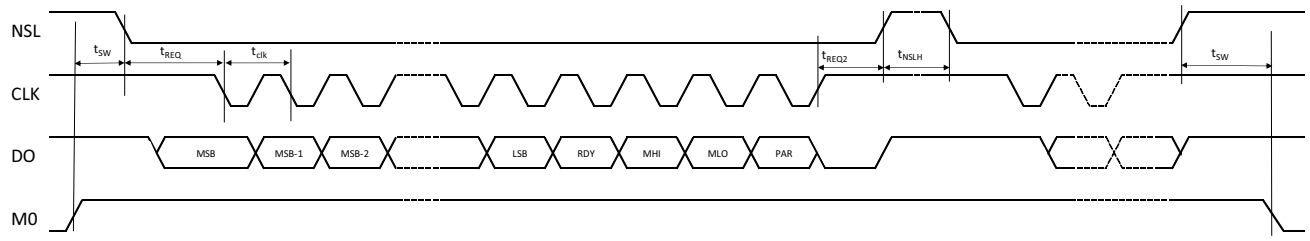


Serial Synchronous Interface 3-Wire (SSI3)

SSI3 protocol uses three pins from AEAT-9922. These three pins are shared among the UVW, SSI, and SPI protocols. MSEL (input pin) selects the protocol one at a time. Assert 0 on the **MSEL** pin and 1 on the **M0** pin to select the SSI protocol.

- M1 → SSI_NSL Input (NSL) signal for SSI protocol, input to from AEAT-9922
- M2 → SSI_Clock Input (CLK) signal for SSI protocol, input to AEAT-9922
- M3 → SSI_Data Output (DO) signal for SSI protocol, output from AEAT-9922

Figure 16: SSI3 Protocol Timing Diagram



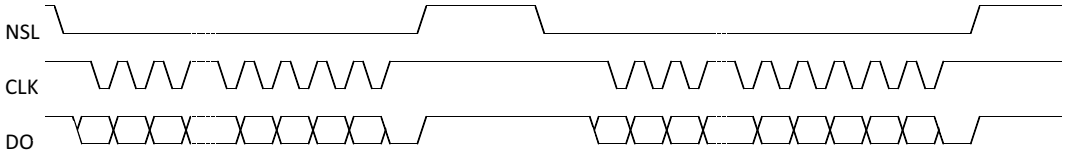
Default: Data output with 3-wire SSI up to 10-MHz clock rates.

Table 12: SSI3 Protocol Timing

Symbol	Description	Min.	Typ.	Max.	Unit
t_{sw}	Time between M0 and NSL switching edges	1	—	—	µs
t_{clk}	Serial clock period	100	—	—	ns
t_{REQ}	CLK high time between NSL falling edge and first CLK falling edge	300	—	—	ns
t_{REQ2}	NSL low time after rising edge of last clock period for an SSI read	200	—	—	ns
t_{NSLH}	NSL high time between two successive SSI reads	200	—	—	ns

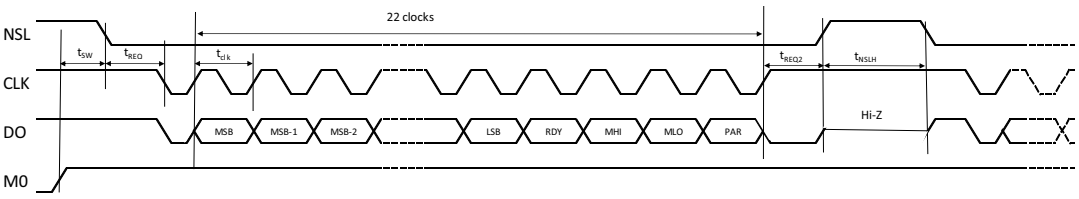
SSI3 is available in two options per the PSEL register setting.

Figure 17: SSI-3(A)



The DO pin is held at high state when the NSL pin is high.

Figure 18: SSI-3(B)



The DO pin is at tristate (high impedance) when the NSL pin is high.

Serial Synchronous Interface 2-Wire (SSI2)

SSI2 protocol uses two pins from AEAT-9922. These two pins are shared among the UVW, SSI, and SPI protocols. MSEL (input pin) selects one protocol at a time. Assert 0 on the **MSEL** pin and the **M1** pin and 1 on the **M0** pin upon power up.

- M2 → SSI_Clock Input (CLK) signal for SSI protocol, input to AEAT-9922
- M3 → SSI_Data Output (DO) signal for SSI protocol, output from AEAT-9922

Figure 19: SSI 2-Wire Timing Diagram

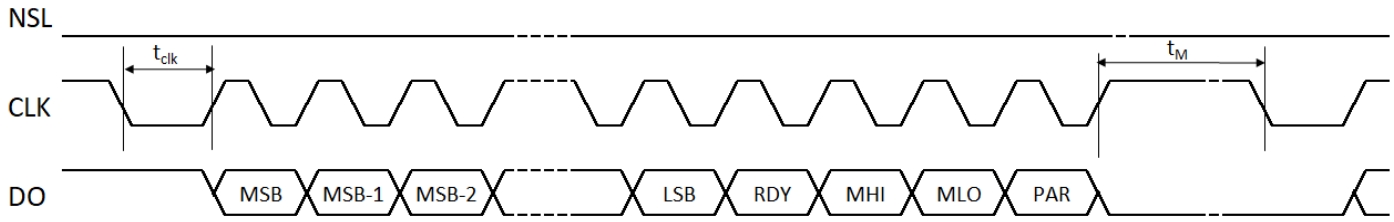
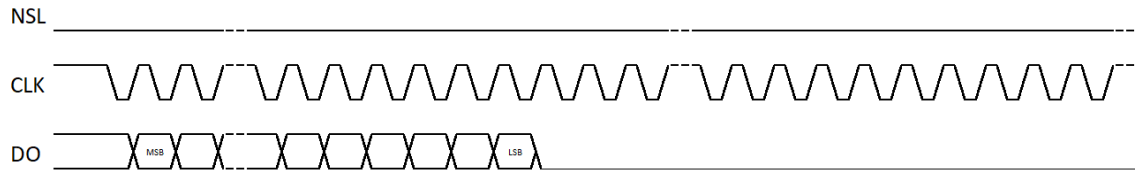


Table 13: SSI 2-Wire Timing Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
t_{clk}	CLK low time after the first falling edge for an SSI read	250	—	t_M / 2	ns
t_M	CLK high time between two successive SSI reads	—	16.5	18.0	µs

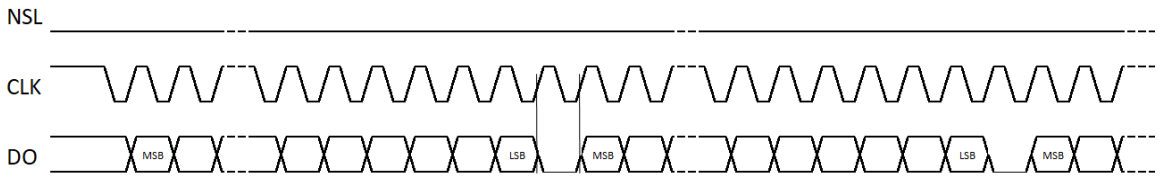
SSI2 is available in two options per the PSEL register setting:

Figure 20: SSI-2(A)



Output single data position and remains low after LSB until the next monoflops (t_M) expires.

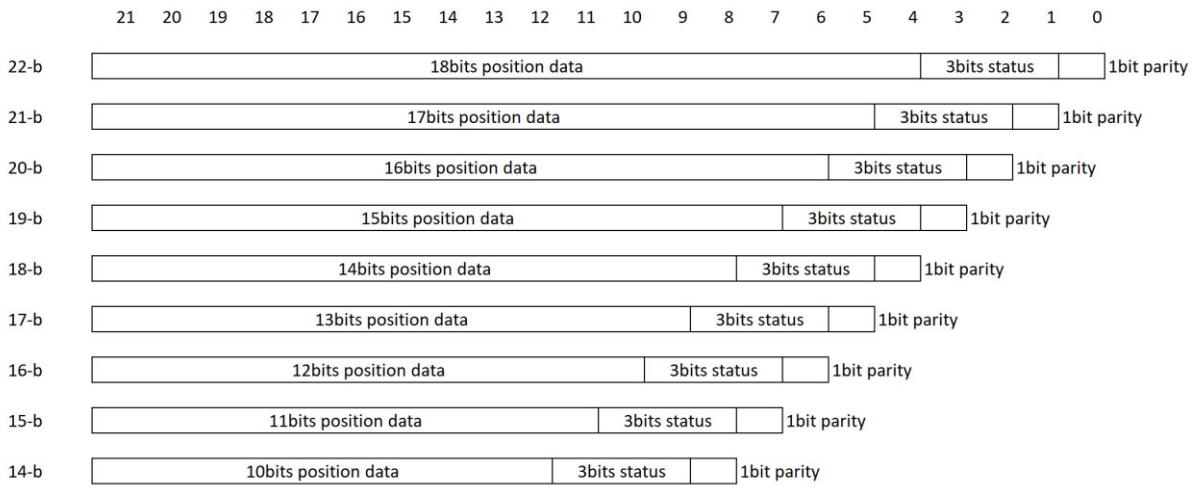
Figure 21: SSI-2(B)



The same position data can be continuously output by sending clock train and data is separated by a single low pulse.

Data will be refreshed on the next monoflop (t_M) expires.

Figure 22: SSI2 READ Data Format



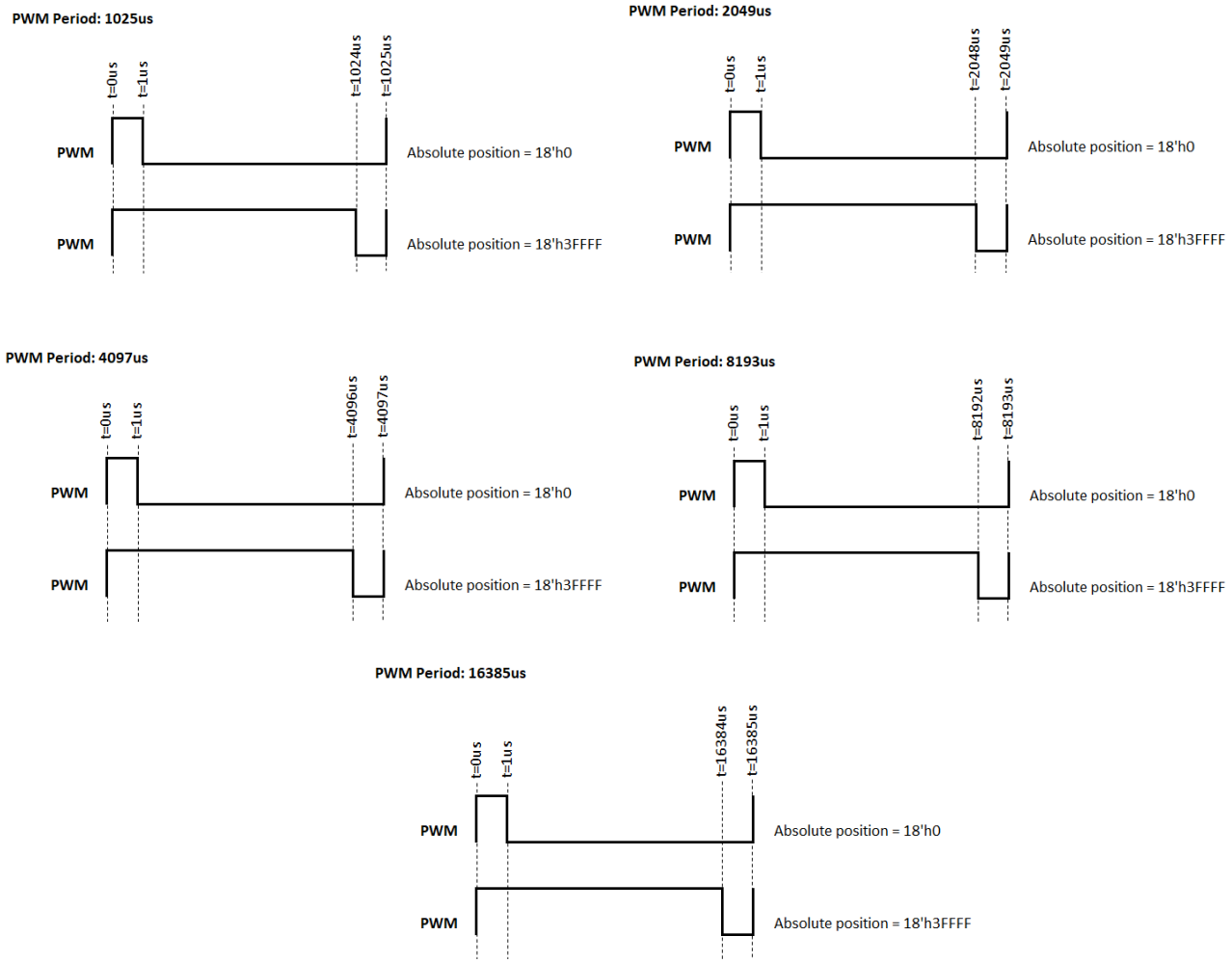
NOTE: 3-b status: {Ready, MHI, MLO}

- **Magnet High (MHI) Error**: This indicates that the magnet strength detected by the chip is too strong. When this is flagged high consistently, change the weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error**: This indicates that the magnet strength detected by the chip is too weak. When this is flagged high consistently, change the stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Ready**: The chip is ready, and the ready value is 1.
- **Parity**: 1-b parity is even parity.

PWM

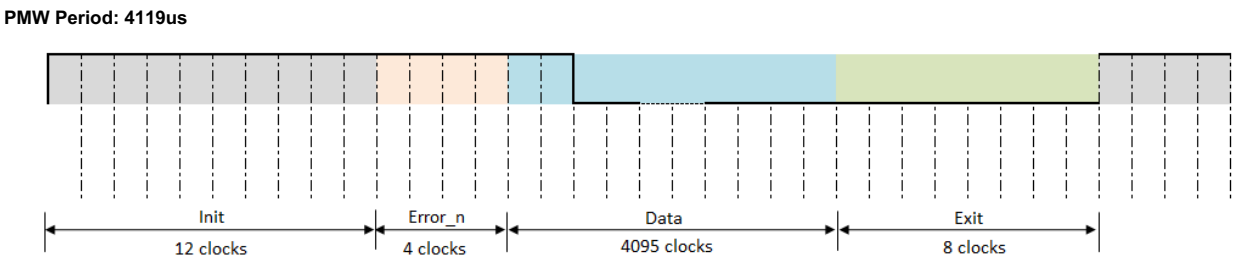
PWM protocol uses one output pin (W_PWM) from AEAT-9922. Note that W_PWM pin is shared between the UVW and PWM protocols. The PWM signals are configurable to have period of 1025, 2049, 4097, 8193 or 16385 µs. During power-up, the PWM signal is 0 before chip ready.

Figure 23: PWM Signals (Period = 1025/2049/4097/8193/16385 µs)



PWM protocols are also available in with Init, Error_n, and Exit along with Data information.

Figure 24: PWM Signals (Period = 1047/2071/4119/8215/16407 µs)



Incremental Output Format

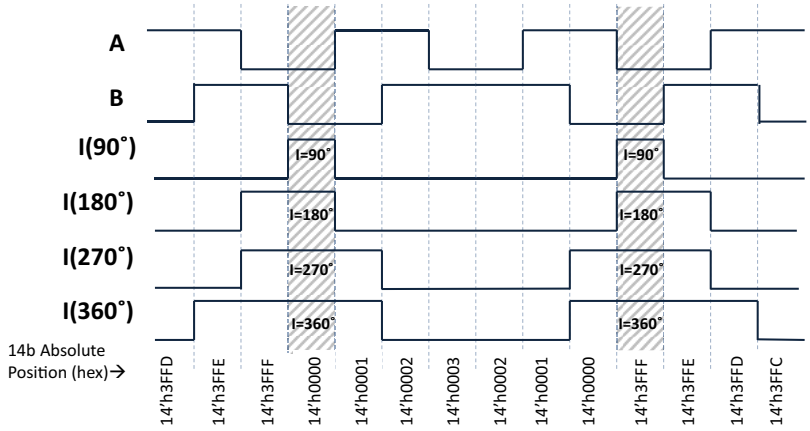
ABI

The AEAT-9922 provides ABI and UVW signals to indicate incremental position of the motor. The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B, and I).

The index signal marks the absolute angular position and typically occurs once per revolution The ABI signal is configurable using the memory map registers. It supports the following configurations:

- Programmable CPR: 1 to 10000CPR
- Programmable I-width: 90, 180, 270, or 360 electrical degrees (°e)
- Programmable I-State: 90, 180, 270, or 360 electrical degrees (°e)

Figure 25: ABI Signal (4096 CPR, with Different I-Width Settings)

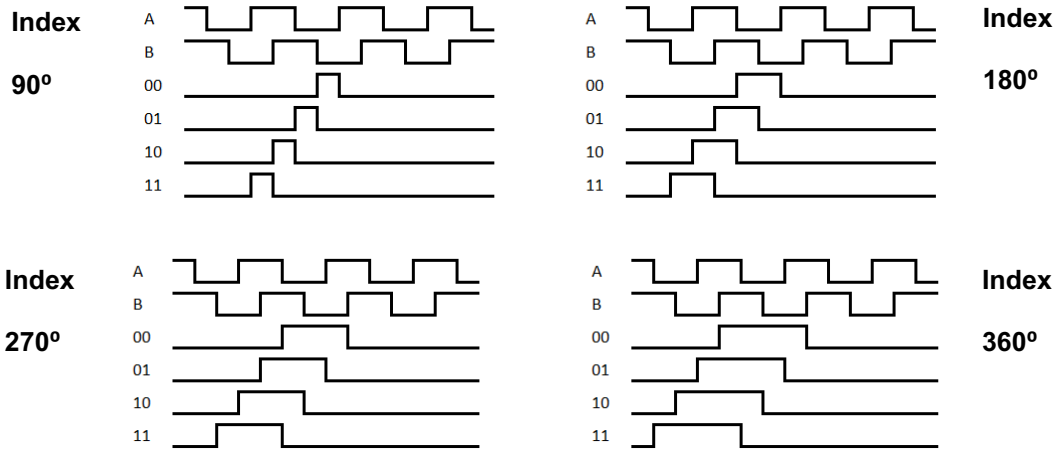


NOTE: Assuming User Sets Hysteresis at 0.02 Mechanical Degree

The Index position is configurable among the incremental state.

The Index signal rises high once per revolution at the absolute zero position.

Figure 26: Index Signal Configuration

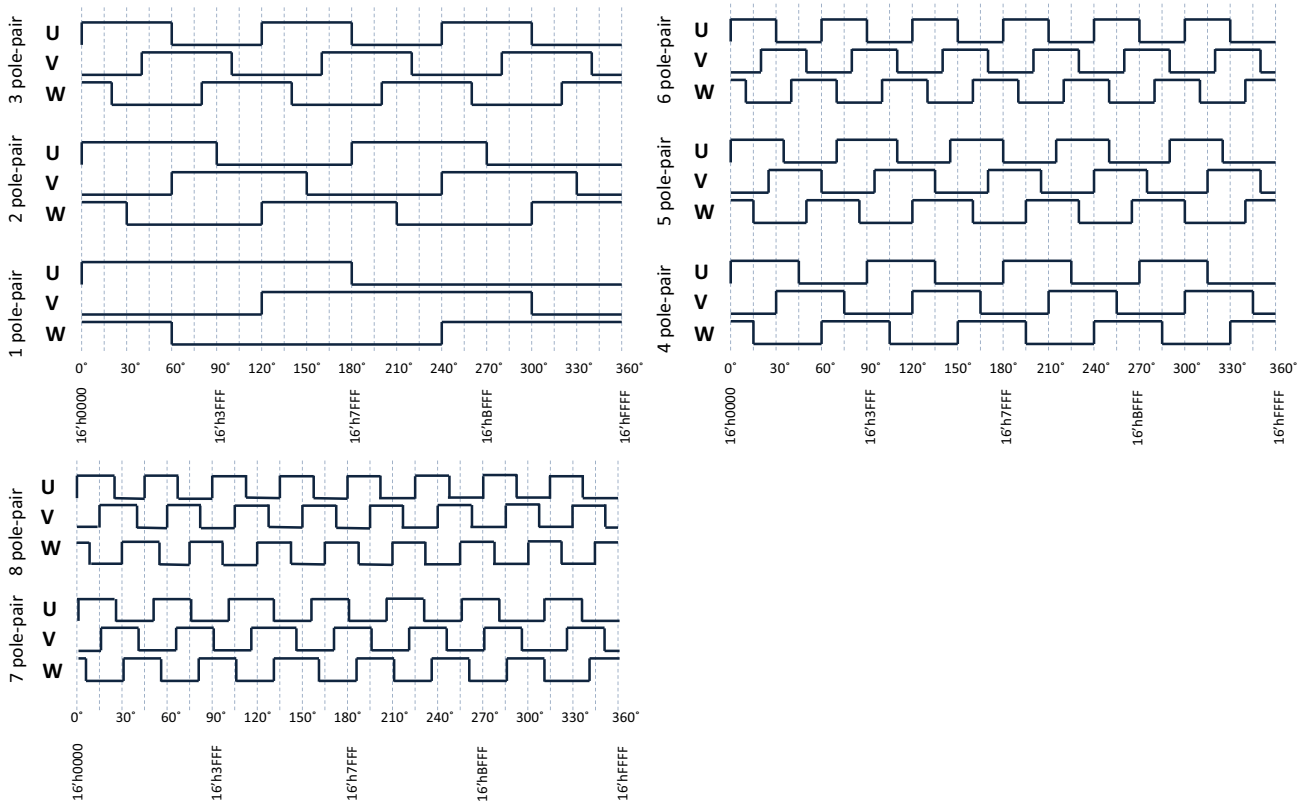


UVW

Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback and is available using three output pins. The AEAT-9922 can configure from 1 to 32 pole pairs, equivalents to 2 to 64 poles.

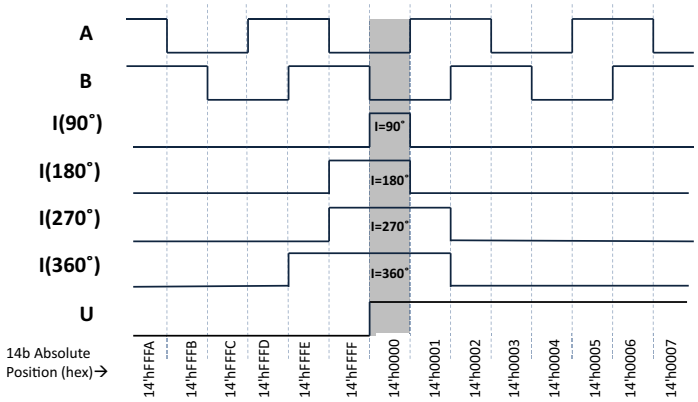
Note that W_PWM pin is shared between the UVW and PWM protocols.

Figure 27: Commutation Output



Note that signal U from UVW protocol is tagged to signal I from the ABI protocol as shown in the following figure.

Figure 28: U-to-I Tagging



Recommended PCB Land Pattern and Soldering Profile

Figure 29: Land Pattern Dimensions in mm

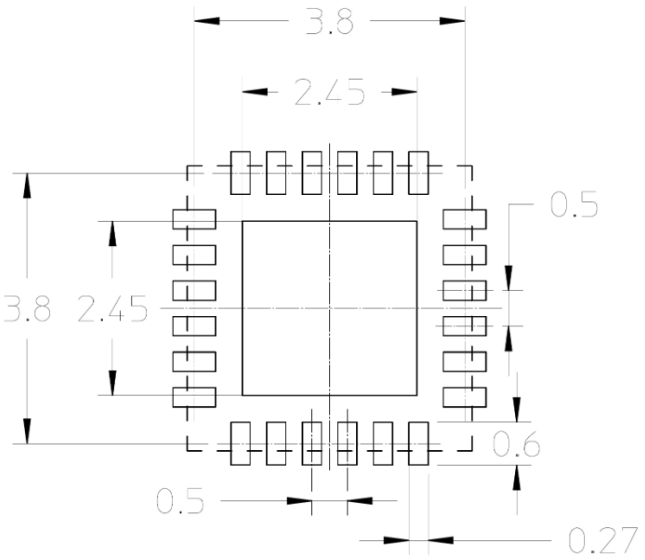
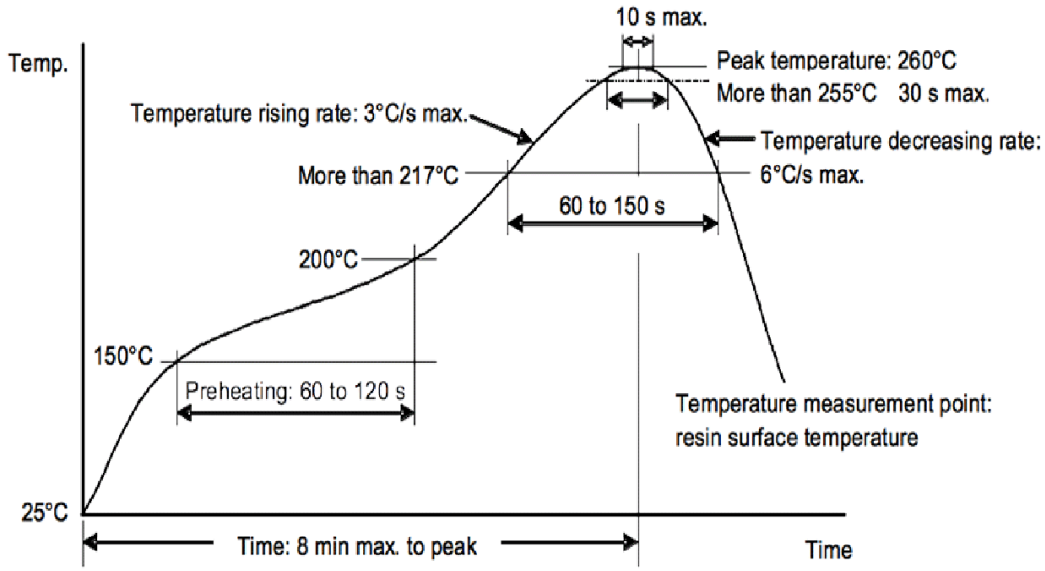


Figure 30: Recommended Lead-Free Solder Reflow Soldering Temperature Profile



Accessories Ordering Information

Ordering Part Number	Product Description	Remarks
HEDS-9922PRGEVB	AEAT-9922 Programming Kit, Evaluation Board and Magnet Evaluation Set	1 unit of SPI programming kit, 2 units of sensor board, 2 pieces of on-axis magnets, USB cable for PC interface and the associated software
HEDS-9922EVB	AEAT-9922 Evaluation Board	1 unit of sensor board