

ACPL-P346

GaN Systems GaN E-HEMT GS66508T Half Bridge Evaluation Board

Introduction

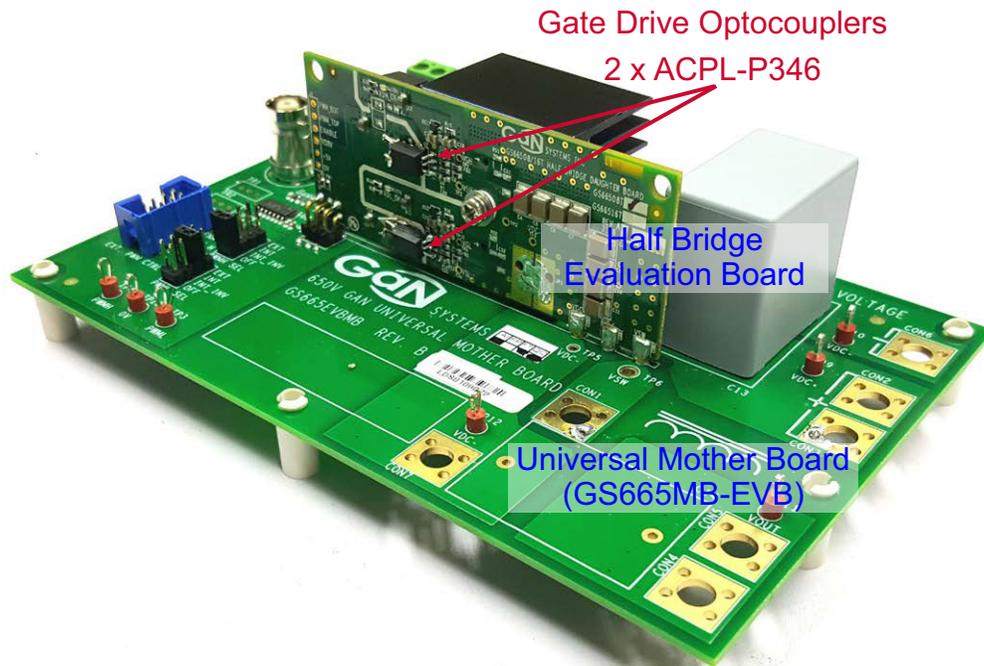
GaN Power Semiconductors

Gallium Nitride (GaN) power semiconductors are rapidly emerging into the commercial market delivering huge benefits over conventional Silicon-based power semiconductors. GaN can improve overall system efficiency with lower on-resistance and the higher switching capability can reduce the overall system size and costs. The technical benefits coupled with lower costs have increased the fast adoption of GaN power semiconductors in applications like industrial power supplies and renewable energy inverters.

Broadcom[®] gate drive optocouplers have been used extensively in driving Silicon-based semiconductors like IGBT. This reference manual will describe how gate drive optocoupler, ACPL-P346 can also be used to drive GaN devices.

A half-bridge evaluation board featuring GaN Systems 650V E-HEMT GS66508T (30A/50mΩ) transistor and 2.5A gate drive optocoupler, ACPL-P346 will be used to perform the slew rate, switching power loss and efficiency test.

Figure 1: Half Bridge Evaluation Board



Description of Half Bridge Evaluation Board

Figure 2 shows the block diagram of the half bridge evaluation board. The universal mother board (GS665MB-EVB) from GaN systems is used to provide the input PWM signals and power to the half bridge evaluation board.

Figure 2: Half Bridge Evaluation Board Block Diagram

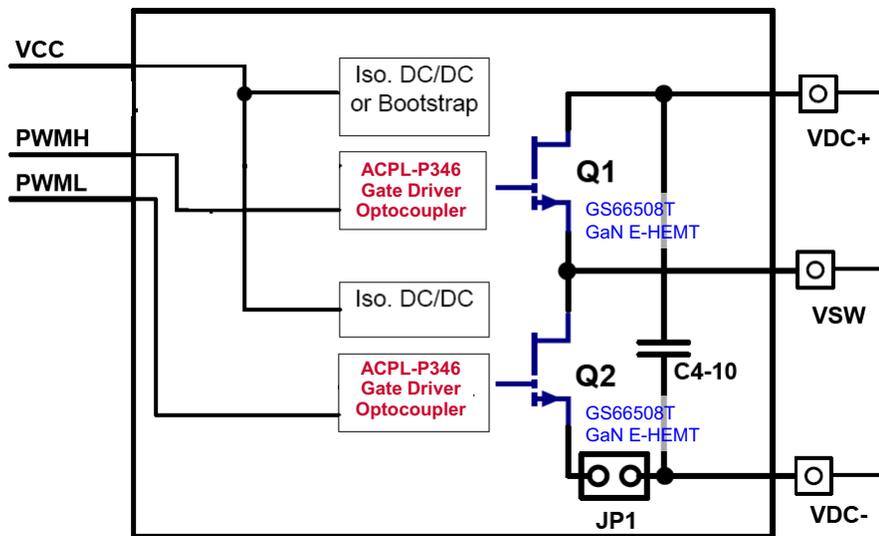


Figure 3: Gate Bias and Driver Circuit

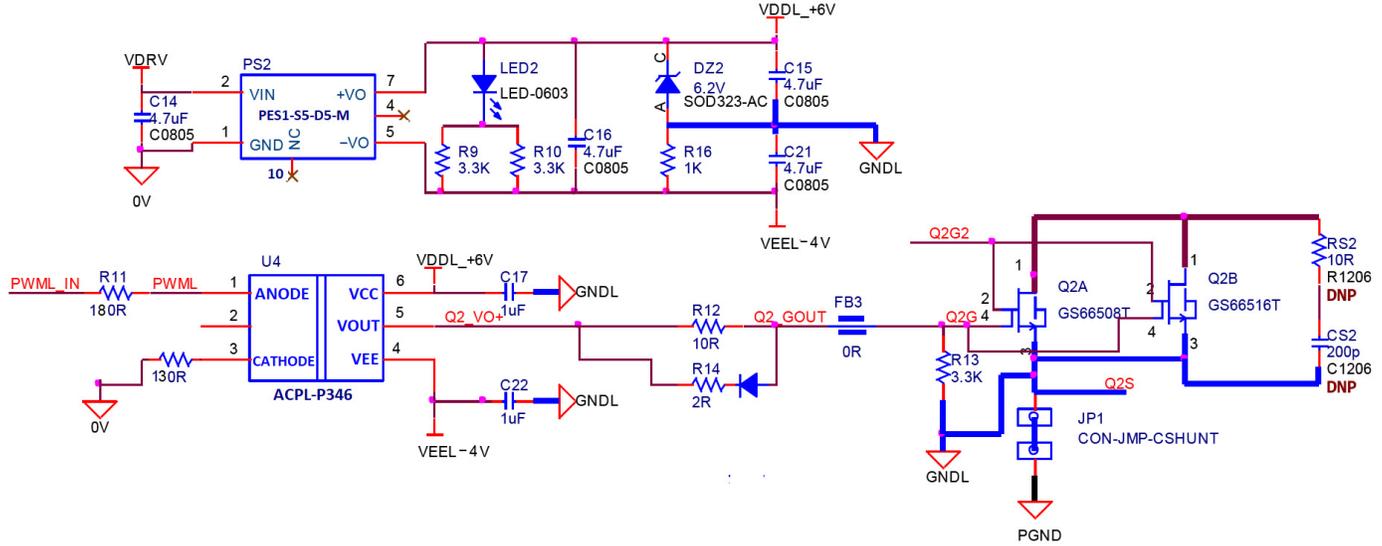


Figure 3 shows the schematic of the gate bias and driver circuit. The isolated DC-DC 5V to 10V converters (PES1-S5-D5-M) are used to provide +6V and -4V bipolar gate drive bias for more robust gate drive and better noise immunity. The 10V is then split into +6V and -4V bias by using 6V Zener diode.

The half bridge evaluation board uses two gate drive optocouplers (ACPL-P346) to drive the GaN transistor directly. The ACPL-P346 is a basic gate driver optocoupler used to isolate and drive the GaN operating at high DC bus voltage. It has a rail-to-rail output with 2.5A maximum output current to provide fast switching high voltage and driving current to turn-on and off the GaN efficiently and reliably. The drive output is separated by a diode and a 10Ω gate resistor is used to limit the current for sourcing and another 2Ω for sinking.

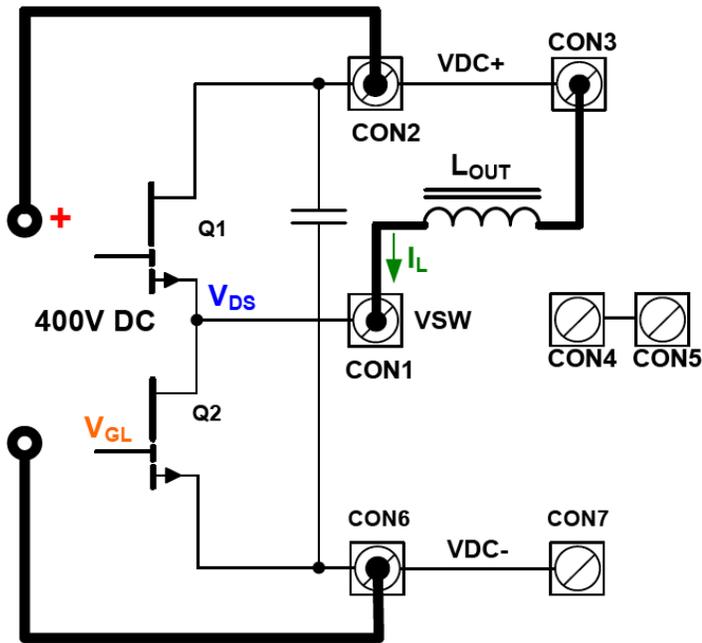
The ACPL-P346 has a propagation delay of less than 110 ns and typical rise and fall times around 8 ns. The very high CMR, common mode rejection of 100kV/μs (min.) is required to isolate high transient noise during the high frequency operation from causing erroneous outputs. It can provide isolation certified by UL 1577 for up to V_{ISO} 3750V_{RMS}/min and IEC 60747-5-5 for working voltage, V_{IORM} up to 891V_{PEAK}.

Test Circuits and Results

Slew Rate Test Circuit

Two 60-μH/40A inductors are connected between VDC+ and VSW to form the boost configuration also known as low side test. The low side GaN transistor QA is active in boost mode. 400V Bus voltage is applied to VDC+/VDC-.

Figure 4: Low Side Slew Rate Test Circuit



The double pulse test is used for easy evaluation of device switching performance at high voltage/current without the need of actually running at high power as shown in Figure 5. The period of first pulse T_{ON1} defines the switching current $I_{SW} = (V_{DS} \times T_{ON1}) / L$. t_1 (turn-off) and t_2 (turn-on) are of interest for this test as they are the hard switching transients for the half bridge circuit when Q2 is under high switching stress. The slew rate tests are conducted at 400V DC and 30A hard switching as shown in Figure 6.

Figure 5: Input Double Pulse Test Pattern

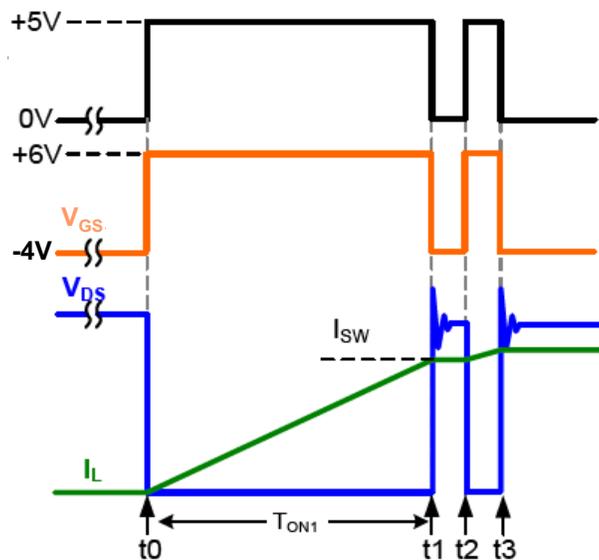
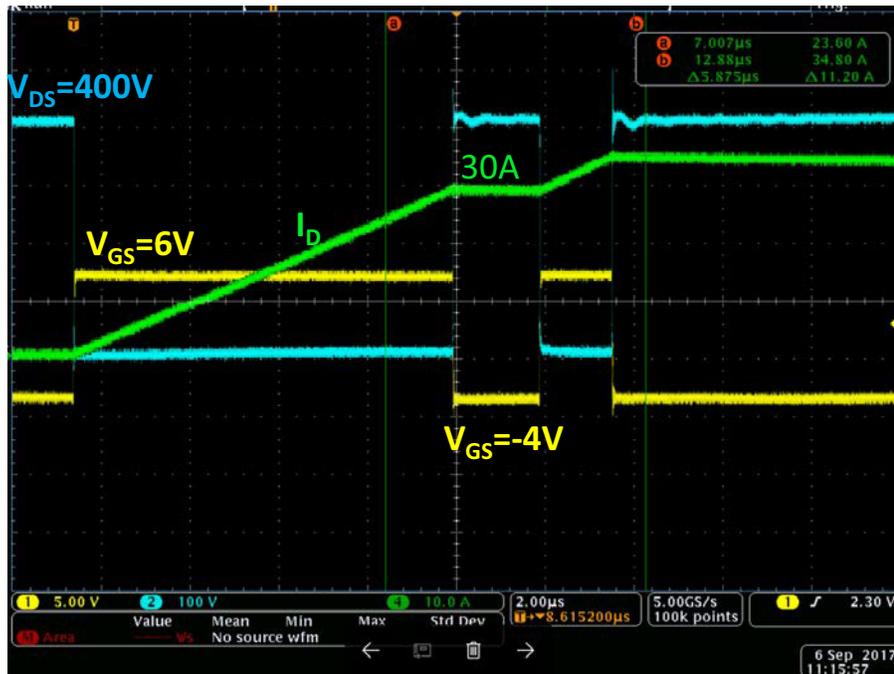


Figure 6: 400V-30A Double Pulse Test



Slew Rate Test Results

The turn on and off slew rates (dv/dt) are measured at t_1 (turn-off) and t_2 (turn-on) respectively. The highest slew rate of more than $110kV/\mu s$ was measured when the GaN transistor hard turned off at 30A.

Figure 7: Turn-On Slew Rate at 400V-30A Hard Switching

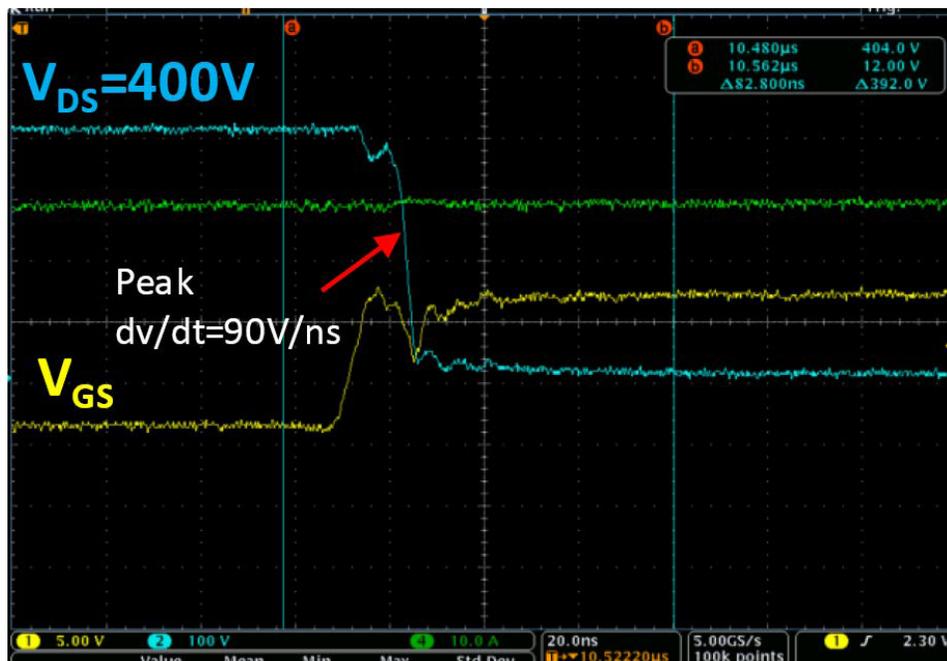
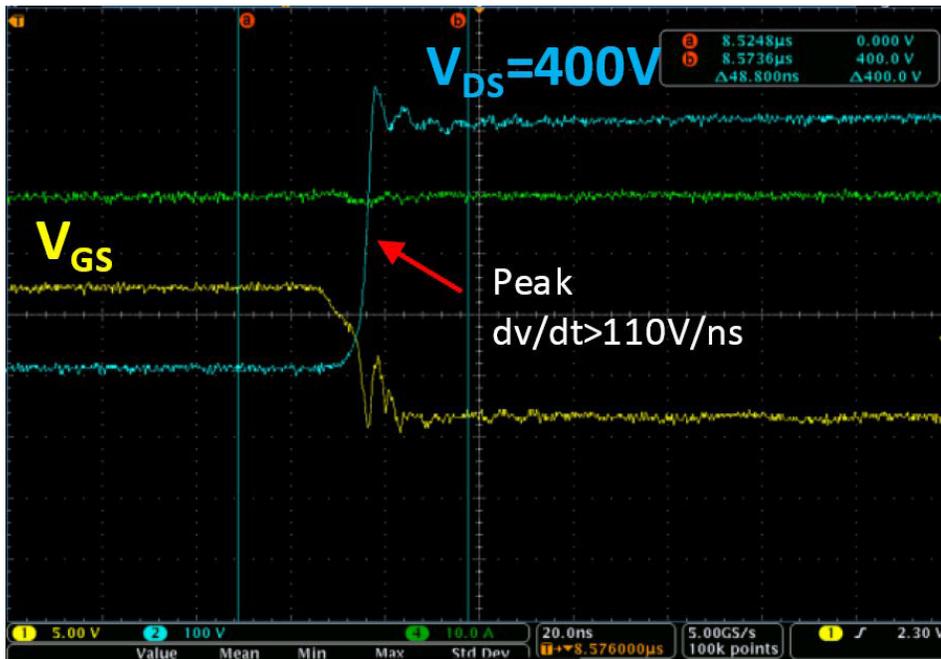


Figure 8: Turn-Off Slew Rate at 400V-30A Hard Switching



Switching Loss Test Circuit

The switching loss test uses the same boost configuration or the low side test. A current shunt (recommended P/N: SDN-414-10, 2-GHz B/W, 0.1Ω) is installed at JP1 (see Figure 2 and Figure 3) for I_D measurement. The switching energy can be calculated from the measured switching waveform $P_{sw} = V_{ds} \times I_d$. The integral of the P_{sw} during switching period is the measured switching loss.

Figure 9: Switching Loss Test Circuit

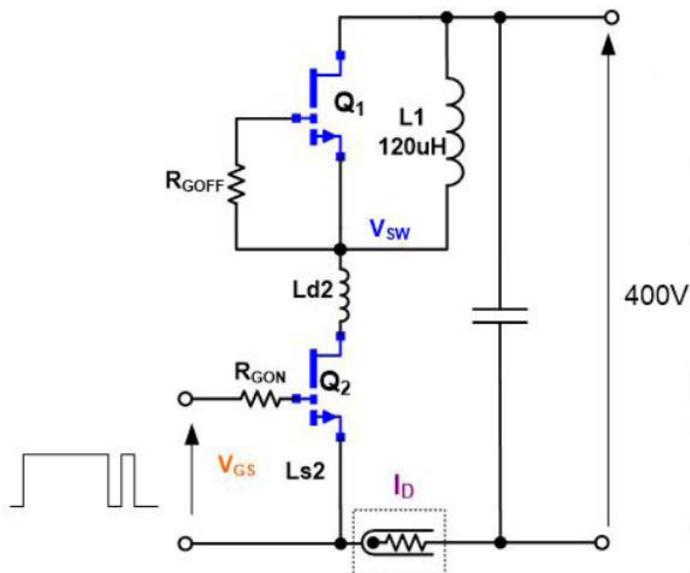


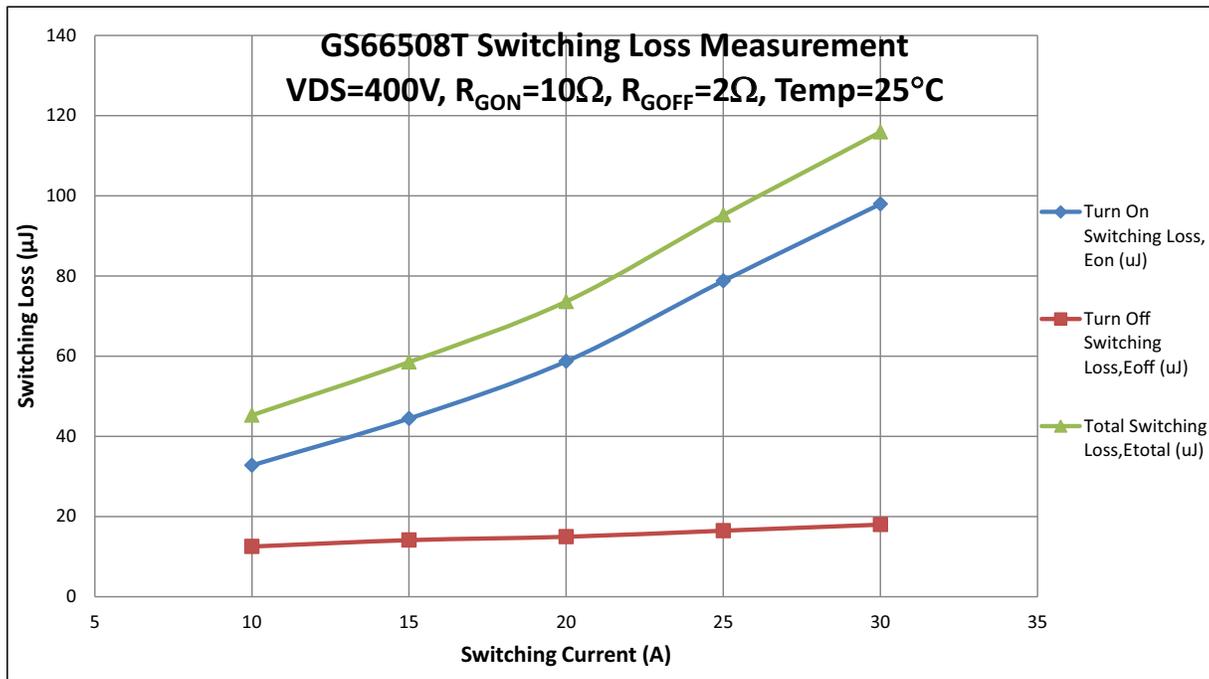
Figure 10: Turn-On Switching Loss Measurement



Switching Loss Test Results

The turn off switching loss is kept at below 20μJ regardless of inductor load current. The turn on switching loss is less than 100μJ at a load current of 30A. Total switching loss is kept within 120μJ.

Figure 11: Turn On/Off Switching Loss vs. Inductor Current

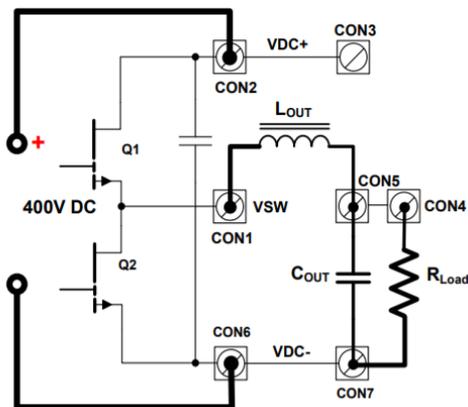


Efficiency Test Circuit

To test the efficiency of GaN transistor in hard switching operation, the board is connected as DC-DC converter in synchronous buck configuration. The converter is operated at high frequency 100 kHz.

Figure 12: Efficiency Test Circuit

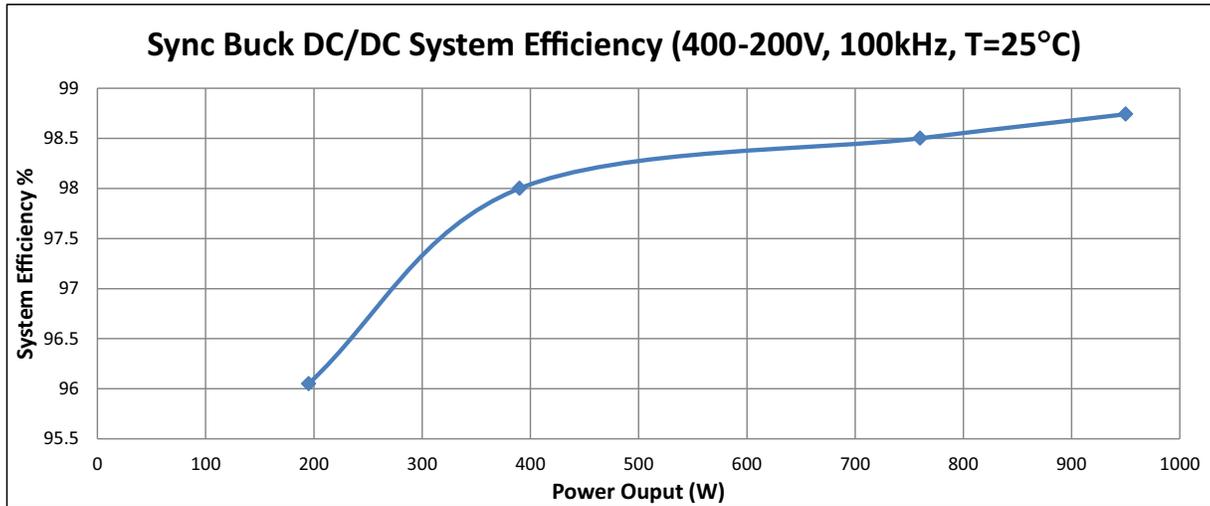
Buck/Standard half bridge mode



Efficiency Test Results

A very high DC-DC conversion efficiency of more than 98.5% is achieved using 650V E-HEMT GS66508T (30A/50mΩ) transistor and gate drive optocoupler, ACPL-P346 at 100 kHz.

Figure 13: Efficiency Test Results



Acknowledgement

Broadcom acknowledges the technical support on the testing of the half bridge evaluation board by the Application Team from GaN Systems.

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