BROADCOM®

Data Sheet

ACPL-K378

Isolated Voltage/Current Detector with Adjustable Upper/Lower Threshold

Description

The Broadcom® ACPL-K378 is a voltage/current detection optocoupler with adjustable upper and lower thresholds. The devices utilize threshold-sensing input buffer ICs, which permit control of threshold levels over a wide range of input voltages with a single external resistor.

The input buffer incorporates several features: hysteresis for extra noise immunity and switching immunity, a diode bridge for easy use with AC input signals, and internal clamping diodes to protect the buffer and LED from a wide range of overvoltage and overcurrent transients. Because threshold sensing is done before driving the LED, variations in optical coupling from the LED to the detector have no effect on the threshold levels.

The ACPL-K378's input buffer IC has a nominal turn-on threshold of 1.3 mA (I_{TH+}) and 3.8V (V_{TH+}).

The high gain output stage features an open collector output that provides both TTL-compatible saturation voltages and CMOS-compatible breakdown voltages.

By combining several unique functions in a single package, the user is provided with an ideal component for industrial control computer input boards and other applications where a predetermined input threshold level is desirable.

Features

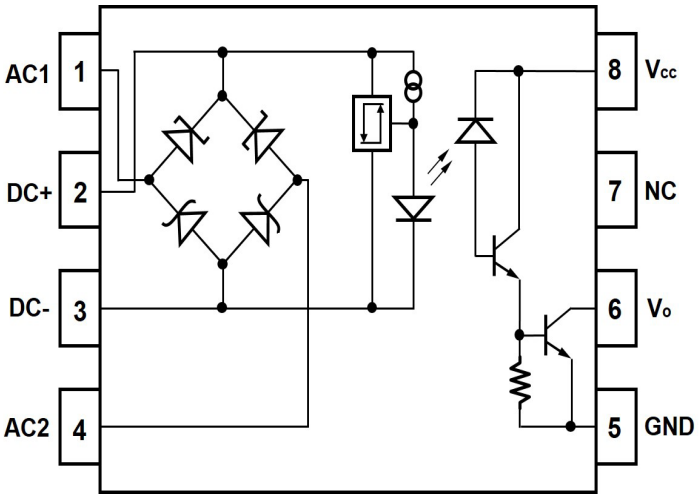
- Wide AC or DC detection range
- User-configurable single/dual detection levels
- Built-in hysteresis that improves noise immunity
- Logic-compatible output
- Wide output supply voltage: 2V to 18V
- –40°C to +105°C operating temperature range
- Package selection: SSO-8
- Safety and regulatory approval:
  - UL 1577 recognized: 5000 V_{rms} for 1 minute
  - CSA approval
  - IEC/EN/DIN EN 60747-5-5 approval for reinforced insulation

Applications

- Limit switch sensing
- Low-voltage detectors
- AC mains and DC link voltage detection
- Relay contact monitors
- Relay coil voltage monitors
- Current sensing
- Microprocessor interfacing

CAUTION! It is advised that normal static precautions be taken in the handling and assembly of this component to prevent damage and/or degradation that may be induced by ESD.

Functional Diagram



Pin Description

Pin No.	Symbol	Description
1	AC1	AC input
2	DC+	DC positive input
3	DC-	DC negative input
4	AC2	AC input
5	GND	Output side ground
6	Vo	Output voltage
7	NC	Not connected
8	Vcc	Output side supply voltage

Ordering Information

The ACPL-K378 is UL recognized with a 5000 V_{rms}/1 minute rating per UL 1577.

Table 1: Ordering Information

Part Number	Option (RoHS Compliant)	Package	Gull Wing Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-K378	-000E	Stretched SO-8	X			80 per tube
	-060E		X		X	80 per tube
	-500E		X	X		1000 per reel
	-560E		X	X	X	1000 per reel

To form an order entry, choose a part number from the Part Number column and combine it with the desired option from the Option column.

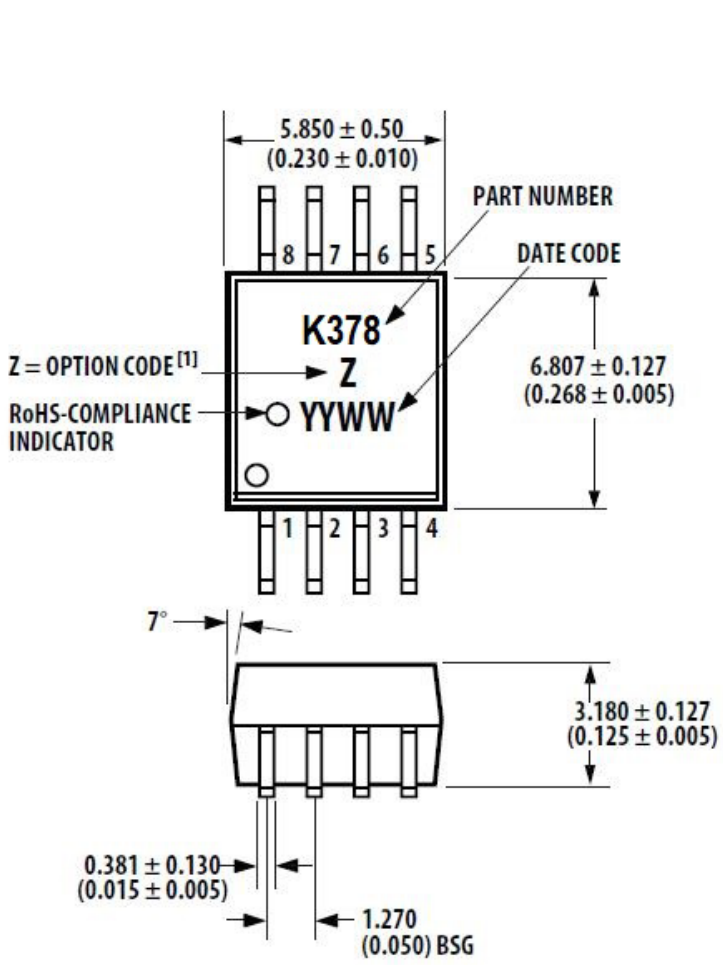
Example:

ACPL-K378-560E is used to order the product with a stretched SO-8 surface-mount package in tape-and-reel packaging with IEC/EN/DIN EN 60747-5-5 safety approval and RoHS compliance.

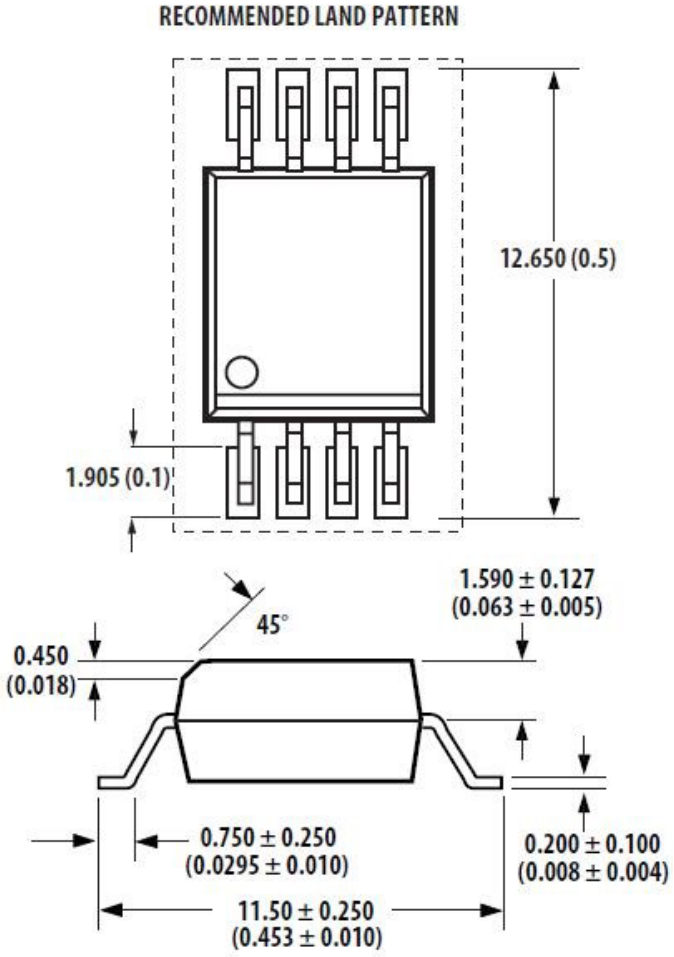
Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawing

Stretched SO-8 Package



Note 1. "V" = Options comprise 060; other options are not marked.



Dimensions in millimeters and (inches).
Lead coplanarity = 0.1 mm (0.004 inches).

Recommended Pb-Free IR Profile

A reflow condition as per the JEDEC standard J-STD-020 (latest revision) is recommended. Non-halide flux should be used.

Regulatory Information

The ACPL-K378 is approved by the following organizations.

IEC/EN/DIN EN 60747-5-5 (with Option 060)	Approval with maximum working insulation voltage V_{IORM} = 1140 V_{peak}.
UL	Approval under the UL 1577 component recognition program up to V_{ISO} = 5000 V_{rms}/1 minute. File 55361.
CSA	Approval under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Specifications

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.0	mm	Measured from input terminals to output terminals, shortest distance through the air.
Minimum External Tracking (External Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along the body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.08	mm	Measured insulation thickness between the emitter and the detector, conductor to conductor, usually the straight line distance thickness between the emitter and the detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group	—	IIIa	—	Material Group (DIN VDE 0110, 1/89, Table 1).

NOTE: All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended land pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques, such as grooves and ribs, that may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances also change depending on factors such as pollution degree and insulation level.

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics [a] (Option 060)

Description	Symbol	Value	Unit
Installation Classification per DIN VDE 0110/39, Table 1	—		—
For rated mains voltage ≤ 300 V_{rms}		I-IV	
For rated mains voltage ≤ 600 V_{rms}		I-III	
Climatic Classification	—	40/105/21	—
Pollution Degree (DIN VDE 0110/39)	—	2	—
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{peak}
Input to Output Test Voltage, Method b V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	2137	V_{peak}
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage [t_{ini}] = 60 seconds)	V_{IOTM}	8000	V_{peak}
Safety-Limiting Values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current [b]	$I_{S,INPUT}$	230	mA
Output Power [b]	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	≥ 10^9	Ω

a. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.

b. Safety-limiting parameters are dependent on case temperature. The input current, $I_{S,INPUT}$, should be derated linearly above a 25°C free-air case temperature at a rate of 1.53 mA/°C; the output power, $P_{S,OUTPUT}$, should be derated linearly above a 25°C free-air case temperature at a rate of 4 mW/°C.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	–55	125	°C	
Ambient Operating Temperature	T_A	–40	105	°C	
Input and Output IC Junction Temperature	T_J	—	125	°C	
Input Current, Average	I_{IN}	—	50	mA	a
Input Current, Surge	I_{IN}	—	140	mA	a, b
Input Current, Transient	I_{IN}	—	500	mA	a, b
Input Voltage (Pin 2–3)	V_{IN}	–0.5	—	V	
Input Power Dissipation	P_{IN}	—	200	mW	c
Total Package Power Dissipation	P_T	—	269	mW	d
Output Power Dissipation	P_O	—	163	mW	e
Output Current, Average	I_O	—	30	mA	f
Supply Voltage (Pins 8–5)	V_{CC}	–0.5	20	V	
Output Voltage (Pins 6–5)	V_O	–0.5	20	V	
Lead Solder Temperature	260°C for 10 seconds, 1.6 mm below the seating plane				

a. Current into or out of any single lead.

b. The surge input current duration is 3 ms at a 120-Hz pulse repetition rate. The transient input current duration is 10 µs at a 120-Hz pulse repetition rate. Note that the maximum input power, P_{IN}, must be observed.

c. Derate linearly above a 105°C free-air temperature at a rate of 10 mW/°C. The maximum input power dissipation of 200 mW allows an input IC junction temperature of 125°C at an ambient temperature of T_A = 105°C. Excessive P_{IN} and T_J may result in IC chip degradation.

d. Derate linearly above a 105°C free-air temperature at a rate of 13.5 mW/°C.

e. Derate linearly above a 105°C free-air temperature at a rate of 8.2 mW/°C. A maximum output power dissipation of 163 mW allows an output IC junction temperature of 125°C at an ambient temperature of T_A = 105°C.

f. Derate linearly above a 105°C free-air temperature at a rate of 1.5 mA/°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Supply Voltage	V_{CC}	2	18	V	
Operating Temperature	T_A	–40	105	°C	
Operating Frequency, V_{CC} = 5V	f	0	9	kHz	a
Operating Frequency, V_{CC} = 3.3V	f	0	5	kHz	a

a. The maximum operating frequency is defined when the output waveform at pin 6 obtains only 90% of V_{CC} with R_L = 4.7 kΩ, C_L = 30 pF using a 5V square wave input signal.

Electrical Specifications

Unless otherwise noted, T_A = –40°C to +105°C and V_{CC} = 3V to 5.5V.

Parameter	Symbol	Min.	Typ.[a]	Max.	Unit	Test Conditions/Notes	Fig.
Upper Threshold Voltage, DC Input (Pins 2, 3)	V_{TH+}	3.6	3.8	4	V	T_A = 25°C, $V_{IN} = V_{DC+} – V_{DC–}$; AC1 and AC2 open	2, 3
		3.35	—	4.05	V	$V_{IN} = V_{DC+} – V_{DC–}$; AC1 and AC2 open	2, 3
Lower Threshold Voltage, DC Input (Pins 2, 3)	V_{TH-}	2.45	2.6	2.75	V	T_A = 25°C, $V_{IN} = V_{DC+} – V_{DC–}$; AC1 and AC2 open	2, 3
		2.01	—	2.96	V	$V_{IN} = V_{DC+} – V_{DC–}$; AC1 and AC2 open	2, 3
Upper Threshold Voltage, AC Input (Pins 1, 4)	V_{TH+}	4.7	4.9	5.1	V	T_A = 25°C, $V_{IN} = V_{AC1} – V_{AC2}$; DC+ and DC– open; Note [b]	2, 3
		4.23	—	5.5	V	$V_{IN} = V_{AC1} – V_{AC2}$; DC+ and DC– open	2, 3
Lower Threshold Voltage, AC Input (Pins 1, 4)	V_{TH-}	3.5	3.7	3.86	V	T_A = 25°C, $V_{IN} = V_{AC1} – V_{AC2}$; DC+ and DC– open; Note [b]	2, 3
		2.87	—	4.42	V	$V_{IN} = V_{AC1} – V_{AC2}$; DC+ and DC– open	2, 3
Upper Threshold Current	I_{TH+}	1.03	1.32	1.50	mA	T_A = 25°C	2, 3
		0.87	—	1.56	mA	—	2, 3
Lower Threshold Current	I_{TH-}	0.48	0.68	0.77	mA	T_A = 25°C	2, 3
		0.43	—	0.85	mA	—	2, 3
Current Hysteresis	I_{HYS}	—	0.6	—	mA	$I_{HYS} = I_{TH+} – I_{TH–}$	2
Voltage Hysteresis	V_{HYS}	—	1.2	—	V	$V_{HYS} = V_{TH+} – V_{TH–}$	2
Input Clamp Voltage	V_{IHC1}	5.4	6.1	6.9	V	$V_{IHC1} = V_{DC+} – V_{DC–}$, I_{IN} = 10 mA, AC1 and AC2 connected to DC–	1
	V_{IHC2}	6.1	6.8	7.6	V	$V_{IHC2} = \lvert V_{AC1} – V_{AC2} \rvert$, $\lvert I_{IN} \rvert$ = 10 mA, DC+ and DC– open	1
	V_{IHC3}	5.4	6.1	6.9	V	$V_{IHC3} = V_{DC+} – V_{DC–}$, I_{IN} = 15 mA, AC1 and AC2 open	1
	V_{ILC}	—	–0.76	—	V	$V_{ILC} = V_{DC+} – V_{DC–}$, I_{IN} = –10 mA	
Input Current	I_{IN}	1.5	1.9	2.3	mA	$V_{DC+} – V_{DC–}$ = 5V, AC1 and AC2 open	5
Bridge Diode Forward Voltage	$V_{D1,2}$	—	0.73	—	V	I_{IN} = 1.5 mA	
	$V_{D3,4}$	—	0.47	—	V	I_{IN} = 1.5 mA	
Logic Low Output Voltage	V_{OL}	—	0.05	0.4	V	V_{CC} = 4.5V, I_{OL} = 4.2 mA; Note [c]	5
Logic High Output Current	I_{OH}	—	—	100	µA	$V_{OH} = V_{CC}$ = 18V; Note [d]	
Logic Low Supply Current	I_{CCL}	—	0.5	3	mA	$V_{DC+} – V_{DC–}$ = 5V, V_O open	6
Logic High Supply Current	I_{CCH}	—	0.002	4	µA	V_{CC} = 18V, V_O open	4
Input Capacitance	C_{IN}	—	50	—	pF	f = 1 MHz, V_{IN} = 0V	

a. All typical values are at T_A = 25°C unless otherwise stated.

b. AC voltage is instantaneous voltage.

c. A logic “Low” output level at pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH–}$ once V_{IN} has exceeded V_{TH+}.

d. A logic “High” output level at pin 6 occurs under the conditions of $V_{IN} \leq V_{TH–}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.

Switching Specifications

Unless otherwise noted, T_A = –40°C to +105°C.

Parameter	Symbol	Min.	Typ.[a]	Max.	Unit	Test Conditions/Notes	Fig.
V_{CC} = 4.5V							
Propagation Delay Time to Logic Low at Output	t_{PHL}	—	6.2	12.5	µs	R_L = 4.7 kΩ, C_L = 30 pF; Note [b]	7
		—	6.3	12.5	µs	R_L = 1.8 kΩ, C_L = 15 pF; Note [b]	
Propagation Delay Time to Logic High at Output	t_{PLH}	—	13.3	70	µs	R_L = 4.7 kΩ, C_L = 30 pF; Note [c]	7
		—	6.4	45	µs	R_L = 1.8 kΩ, C_L = 15 pF; Note [c]	
Output Rise Time (10–90%)	t_R	—	24	—	µs	R_L = 4.7 kΩ, C_L = 30 pF	8
Output Fall Time (90–10%)	t_F	—	0.4	—	µs	R_L = 4.7 kΩ, C_L = 30 pF	8
V_{CC} = 3.3V							
Propagation Delay Time to Logic Low at Output	t_{PHL}	—	6.8	12.5	µs	R_L = 4.7 kΩ, C_L = 30 pF; Note [b]	7
		—	6.9	12.5	µs	R_L = 1.8 kΩ, C_L = 15 pF; Note [b]	
Propagation Delay Time to Logic High at Output	t_{PLH}	—	18.5	90	µs	R_L = 4.7 kΩ, C_L = 30 pF; Note [c]	7
		—	12.5	70	µs	R_L = 1.8 kΩ, C_L = 15 pF; Note [c]	
Output Rise Time (10–90%)	t_R	—	26	—	µs	R_L = 4.7 kΩ, C_L = 30 pF	8
Output Fall Time (90–10%)	t_F	—	0.5	—	µs	R_L = 4.7 kΩ, C_L = 30 pF	8
V_{CC} = 3V to 5.5V							
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	—	10	—	kV/µs	I_{IN} = 0 mA, R_L = 4.7 kΩ, $V_{O,MIN}$ = 2V, V_{CM} = 1500V; Notes [d, e]	
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	—	1	—	kV/µs	I_{IN} = 1.56 mA, R_L = 4.7 kΩ, $V_{O,MAX}$ = 0.8V, V_{CM} = 500V; Notes [d, e]	

a. All typical values are at T_A = 25°C unless otherwise stated.

b. The t_{PHL} propagation delay is measured from the 2.5V level of the leading edge of a 5.0V input pulse (1-µs rise time) to the 1.5V level on the leading edge of the output pulse. C_L includes the probe and stray wiring capacitance.

c. The t_{PLH} propagation delay is measured from the 2.5V level of the trailing edge of a 5.0V input pulse (1-µs fall time) to the 1.5V level on the trailing edge of the output pulse. C_L includes the probe and stray wiring capacitance.

d. Common mode transient immunity with a logic “High” level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to ensure that the output will remain in a logic “High” state (that is, V_O > 2.0V). Common mode transient immunity in a logic “Low” level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to ensure that the output will remain in a logic “Low” state (that is, V_O < 0.8V).

e. In applications where dV_{CM}/dt may exceed 50 kV/µs (such as when a static discharge occurs), a series resistor, R_{CC}, should be included to protect the detector IC from destructive high surge currents. The recommended value for R_{CC} is 240Ω per volt of allowable drop in V_{CC} (between pin 8 and V_{CC}) with a minimum value of 240Ω.

Package Characteristics

Over recommended temperature range of T_A = –40°C to 105°C unless otherwise specified.

Parameter	Symbol	Min.	Typ.[a]	Max.	Unit	Test Conditions/Notes
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{rms}	RH ≤ 50%, t = 1 minute; T_A = 25°C; Notes [a, b]
Input-Output Resistance	R_{I-O}	—	10^{12}	—	Ω	V_{I-O} = 500 Vdc; Note [c]
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f = 1 MHz, V_{I-O} = 0 Vdc; Note [c]

a. The input-output momentary withstand voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable), your equipment level safety specification, or Avago Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.

b. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA).

c. The device is considered a two-terminal device: pins 1, 2, 3, and 4 are connected together, and pins 5, 6, 7, and 8 are connected together.

Typical Performance Plots

Unless otherwise noted, T_A = 25°C.

Figure 1: Typical Input Characteristics (I_{IN}) vs. V_{IN} (AC Voltage Is an Instantaneous Value)

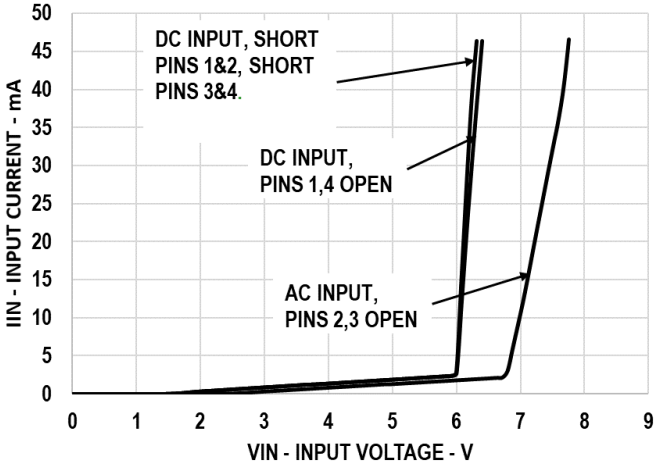
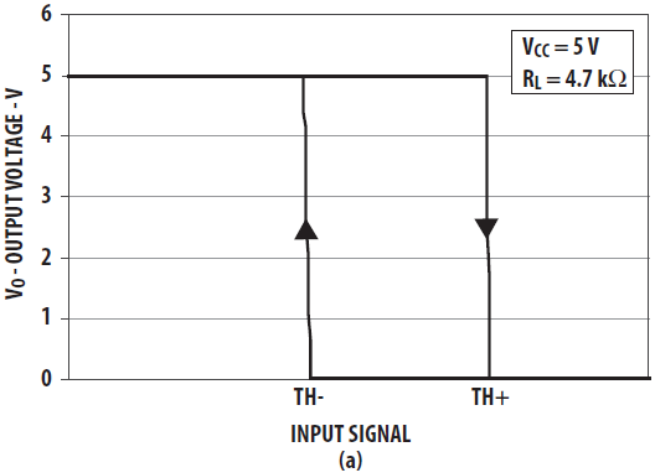


Figure 2: (a) Typical Transfer Characteristics and (b) Input Threshold Levels



Input Signal	TH+	TH-	Input Connection
I_{TH}	1.32 mA	0.68 mA	Pins 2, 3 or 1, 4
$V_{TH(DC)}$	3.8V	2.59V	Pins 2, 3
$V_{TH(AC)}$	5V	3.8V	Pins 2, 3

Figure 3: Typical DC Threshold Levels vs. Temperature

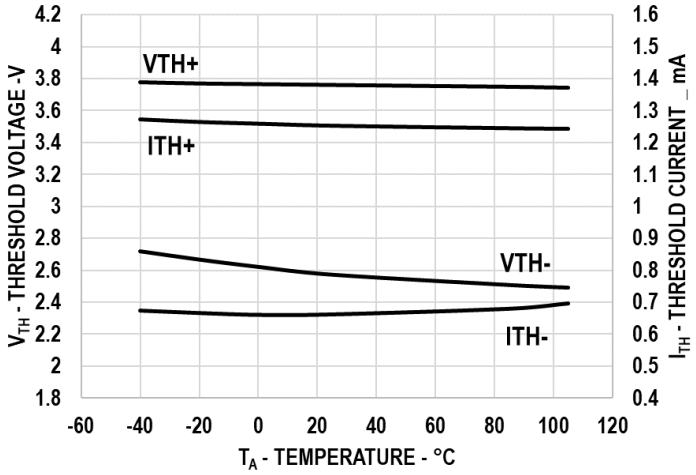


Figure 4: Typical High-Level Supply Current (I_{CCH}) vs. Temperature

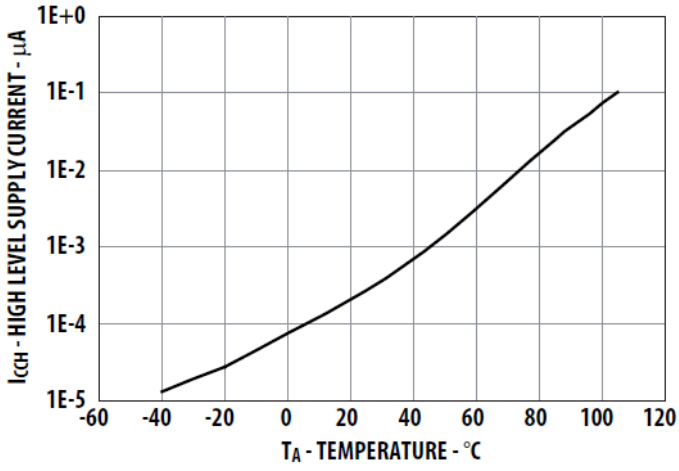


Figure 5: Typical Input Current (I_{IN}) and Low-Level Output Voltage (V_{OL}) vs. Temperature

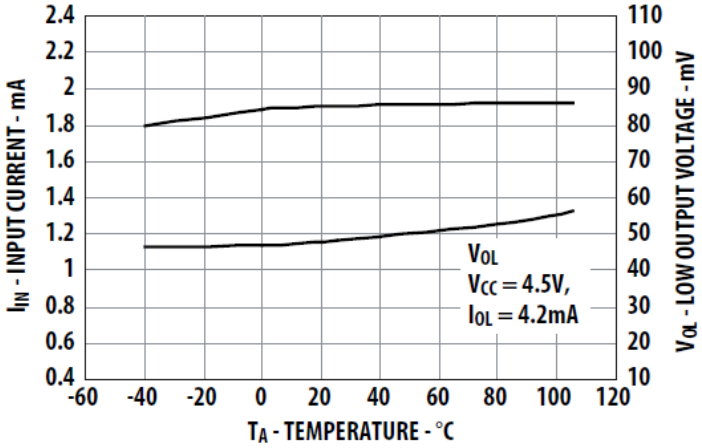


Figure 6: Typical Logic Low Supply Current vs. Supply Voltage

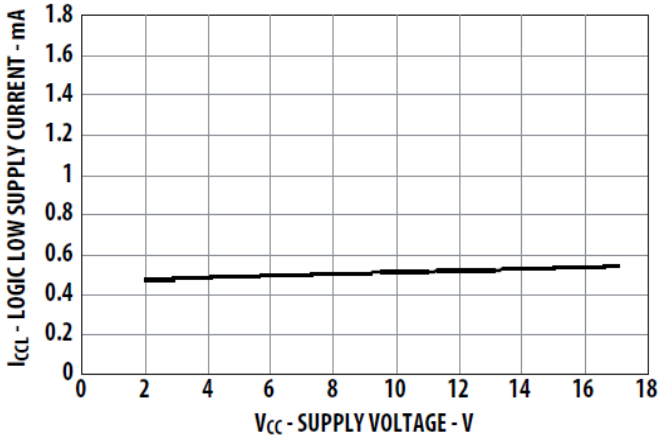


Figure 7: Typical Propagation Delay vs. Temperature

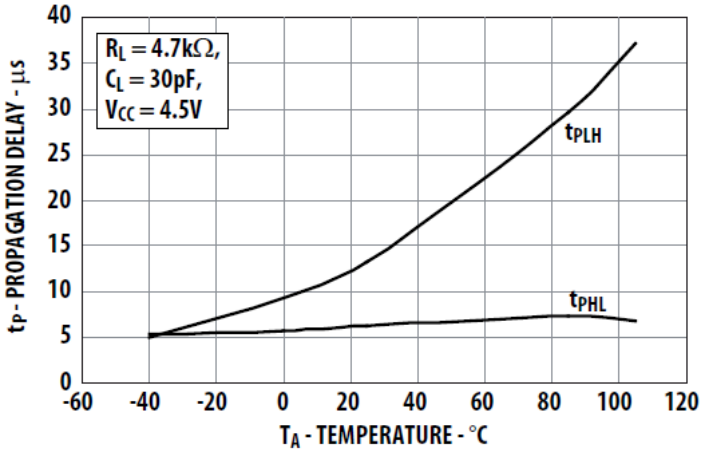


Figure 8: Typical Rise and Fall Times vs. Temperature

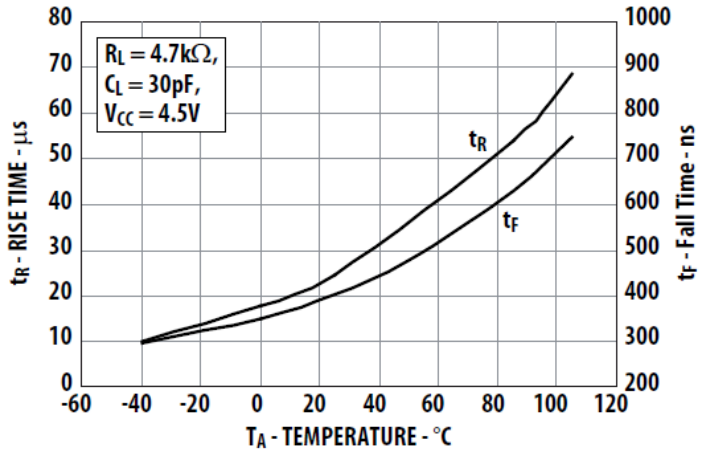


Figure 9: Typical External Threshold Characteristics ($V_{\pm}$) vs. R_X