User Guide

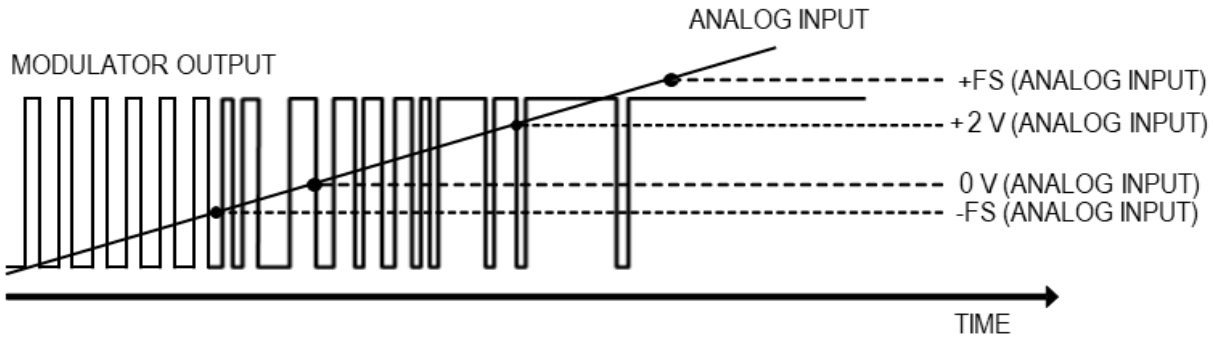
ACPL-C877

Isolated Sigma-Delta Modulator Evaluation Kit Board

The Broadcom® ACPL-C877 isolated sigma-delta (Σ-Δ) modulator converts an analog input signal into a high-speed (10 MHz typical) single-bit data stream by means of a sigma-delta over-sampling modulator. The time average of the modulator data is directly proportional to the input signal voltage. The modulator uses an internal speed of 10 MHz. The modulator data are encoded and transmitted across the isolation boundary where they are recovered and decoded into high-speed data stream of digital ones and zeros. The original signal information is represented by the density of ones in the data output.

The input signal information is contained in the modulator output data stream, represented by the density of ones and zeros. The density of ones is proportional to the input signal voltage, as shown in Figure 1. A differential input signal of 0V ideally produces a data stream of ones 50 percent of the time and zeros 50 percent of the time. A differential input of –100 mV corresponds to 48.44 percent density of ones, and a differential input of +2.0V is represented by 81.25 percent density of ones in the data stream. A differential input of +3.2V or higher results in ideally all ones in the data stream, while any input lower than –100 mV is undefined. Table 1 shows this relationship.

Figure 1: Modulator Output vs. Analog Input



NOTE: This User Guide is provided to assist you in the evaluation of product(s) currently under development. Until Broadcom releases this product for general sales, Broadcom reserves the right to alter prices, specifications, features, capabilities, functions, release dates, and remove availability of the product(s) at any time.

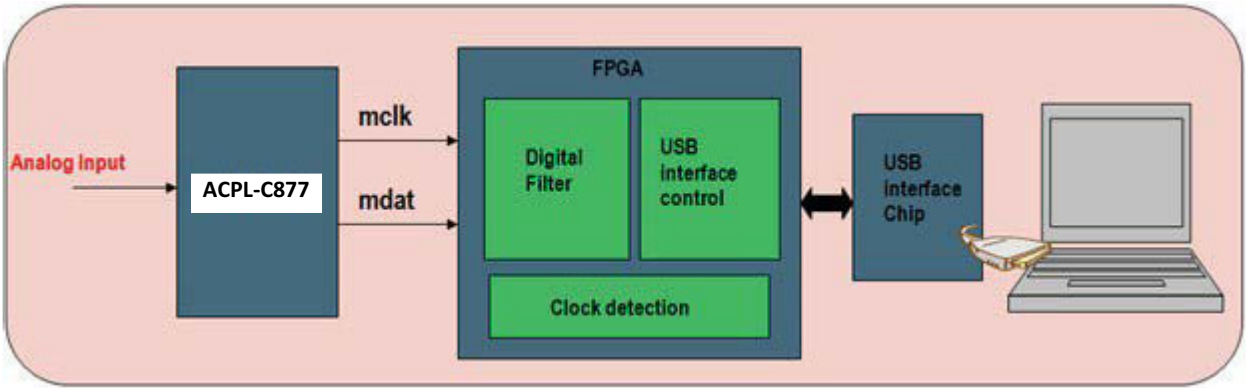
Table 1: Input Voltage with Ideal Corresponding Density of 1s at Module Data Output, and ADC Code

Analog Input	Voltage Input	Density of 1s	Density of 0s	ADC Code (16-bit unsigned decimation)
+Full-Scale	+3.2V	100%	0%	65,535
+Recommended Input Range	+2.0V	81.25%	18.75%	53,248
Zero	0V	50%	50%	32,768
–Full-Scale	–0.1V	48.44%	51.56%	31,744

A digital filter converts the single-bit data stream from the modulator into a multi-bit output word similar to the digital output of a conventional A/D converter. With this conversion, the data rate of the word output is also reduced (decimation). A Sinc3 filter is recommended to work together with the ACPL-C877. With a 10-MHz internal clock frequency, 256 decimation ratio and 16-bit word settings, the output data rate is 39 kHz (= 10 MHz/256). This filter can be implemented in an ASIC, an FPGA, or a DSP.

In this evaluation board, Sinc3 filter is implemented using Xilinx Spartan XC3S250E FPGA. The FPGA hardware is designed in Verilog/VHDL environment. The major building block are the Digital Filter and USB interface control as shown in Figure 2. The design is synthesized and implemented using Xilinx Tool to a bitstream file. This bitstream file can be loaded to FPGA through USB, which is already done for each evaluation board kit shipped to the customer.

Figure 2: Digital Filter and USB Interface Control

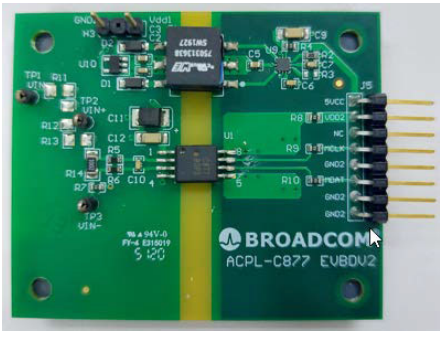


Preparation and Setup

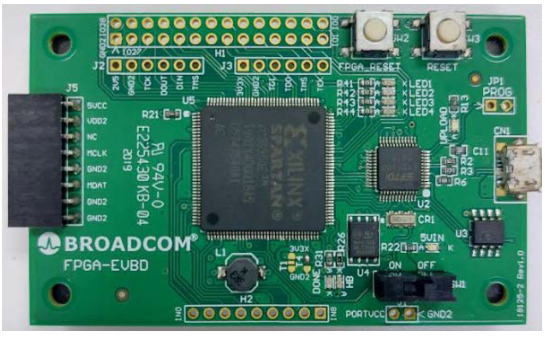
1. Each complete ACPL-C877 evaluation kit shipment includes the following items:
   – ACPL-C877 evaluation board
   – Cable with USB/mini USB terminations
   – Softcopy folder containing drivers and application software programs
2. The softcopy folder contains the following documents or software programs:
   – `ACPL-C877 Xilinx FPGA Evbd Kit User Guide.pdf` - Evaluation board user guide
   – `CDM21228_Setup.exe` - FTDI USB chipset driver for Windows 32-bit and 64-bit operating systems. For other operating systems, you can download from the manufacturer's website: http://ftdichip.com/Drivers/VCP.htm
   – `dig_filter_2020.exe` - Broadcom application GUI software
   – `DigFil_2000mvINcmosOUT_2019.bit` - FPGA bit file
   – `Sinc3_verilog.txt` - Sinc3 filter codes in Verilog
   – `Sinc3_VHDL.txt` - Sinc3 filter codes in VHDL
3. Save the softcopy folder into a PC directory locations. See the appendix for descriptions of the major components on the evaluation board, the schematic diagrams, and PCB layout.
4. Connect the FPGA-EVBD board to the PC using the provided USB cable.
   a. Turn on switch SW1. The red **5VIN** LED lights up indicating the presence of a USB connection.
   b. Install the `CDM21228_Setup.exe` USB chipset driver file. The driver will install two ports, USB Serial Converter A and USB Serial Converter B.
   c. To verify that the installation is successful, open Device Manager. Under **Universal Serial bus controllers**, the two ports **USB Serial Converter A** and **USB Serial Converter B** should appear.
5. Each time the evaluation board SW1 is turned on, the board goes through a series of power-on sequences. When completed, the green **DONE** LED comes on to indicate completion of the power-on sequences.

   Then connect the C877-SDM-EVBD board to the FPGA-EVBD. Once connected, LED1 to LED4 will light up in an undefined sequence to indicate that the board connections are properly done. The following figure shows the C877-SDM-EVBD and FPGA-EVBD boards.

Figure 3: C877-SDM-EVBD and FPGA-EVBD Boards



C877-SDM-EVBDV2



FPGA-EVBD

6. Go to the PC directory, and run the `dig_filter_2020.exe` application program. Refer to the application GUI screen capture as shown in Figure 5. If the evaluation board is connected and SW1 is switched on, a `Broadcom-System` text message will appear on the right of the **Search** button. If SW1 is not switched on, an error message will appear as shown in Figure 4.

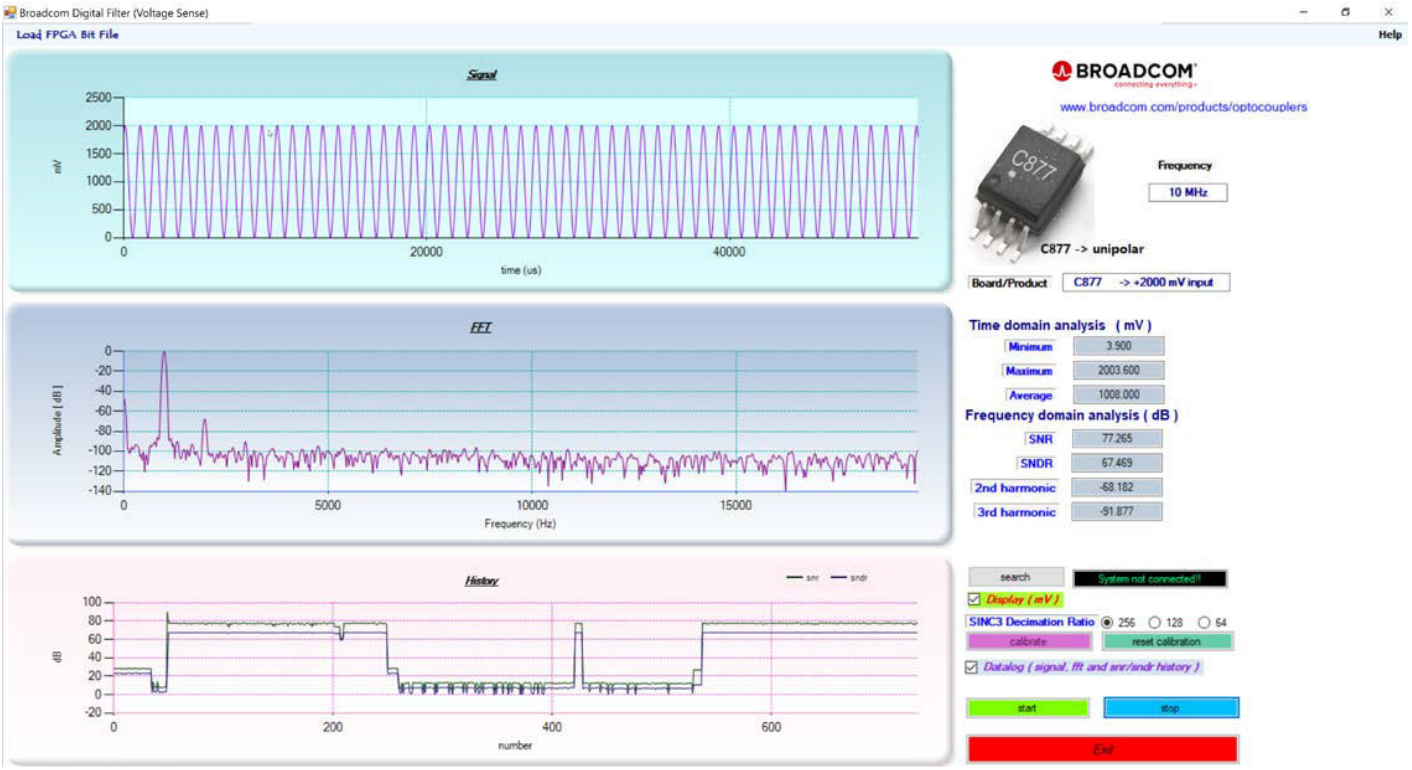
   Click **OK** once, and the application GUI appears. The text message `System not connected!!` appears instead.

Figure 4: Error Message

7. Switch on SW1. Go to the application GUI, and click the **Search** button. Now the text message changes to `Broadcom-System` to indicate that the connection is established.

Application GUI

Figure 5: Application GUI

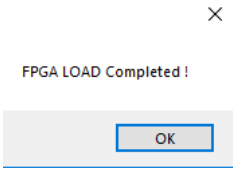


The application GUI has three displays. Two of the displays show the signal in time domain and frequency domain, and the third shows SNR and SNDR historical plots. The time domain signal can be displayed in terms of ADC count or voltage level (mV) by checking the **Display (mV)** box.

On the right of the displays, real time minimum, maximum, and average signal levels are shown in the time domain in terms of either mV or ADC count. SNR, SNDR, 2nd harmonic and 3rd harmonic levels are displayed in the frequency domain.

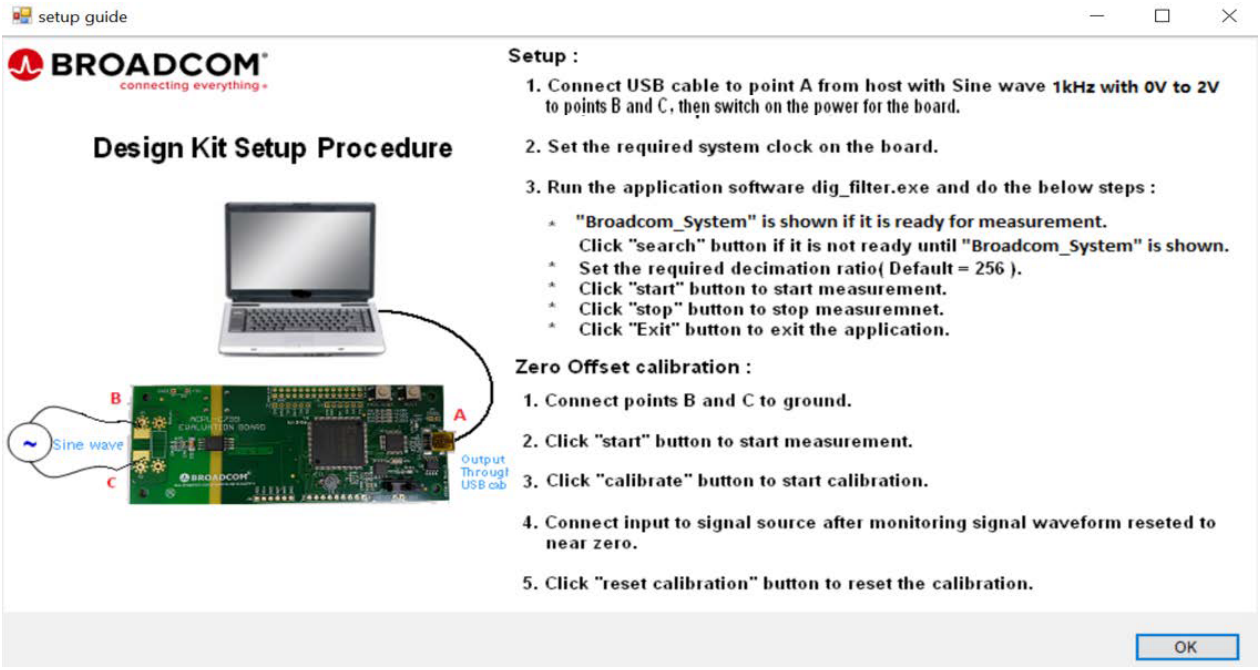
1. Click **Start** to start capturing the input signal. The configured board frequency is displayed in the **Frequency** box and the type of sigma-delta modulator in terms of input range and output signal type is displayed in the **Board/Product** box.
2. The signal, FFT and SNR/SNDR history data can be saved into text files that are readable and compatible to Microsoft Excel by checking the **Datalog (signal, fft and snr/sndr history)** box. The `snr.txt`, `signal.txt`, and `fft.txt` files are stored in the same file directory as the application GUI.
3. If there is an updated FPGA bitfile or you have configured a new bitstream file, this can be uploaded easily by clicking the **Load FPGA Bit File** on the top-left corner of the application GUI. When the bitfile is being uploaded, the green DONE LED goes off and the red UPLOAD LED lights up. When uploading is completed, the red UPLOAD LED goes off, while the green DONE LED lights up again to signal completion. The **FPGA LOAD Completed!** pop-up window appears, as shown in the following figure.

Figure 6: FPGA LOAD Completed!



4. For the quick help guide, click **Help** on the top-right corner of the application GUI, then select the **setup guide**. The help guide also describes the calibration procedure to zero the offset.

Figure 7: Help - setup guide



Output Measurement

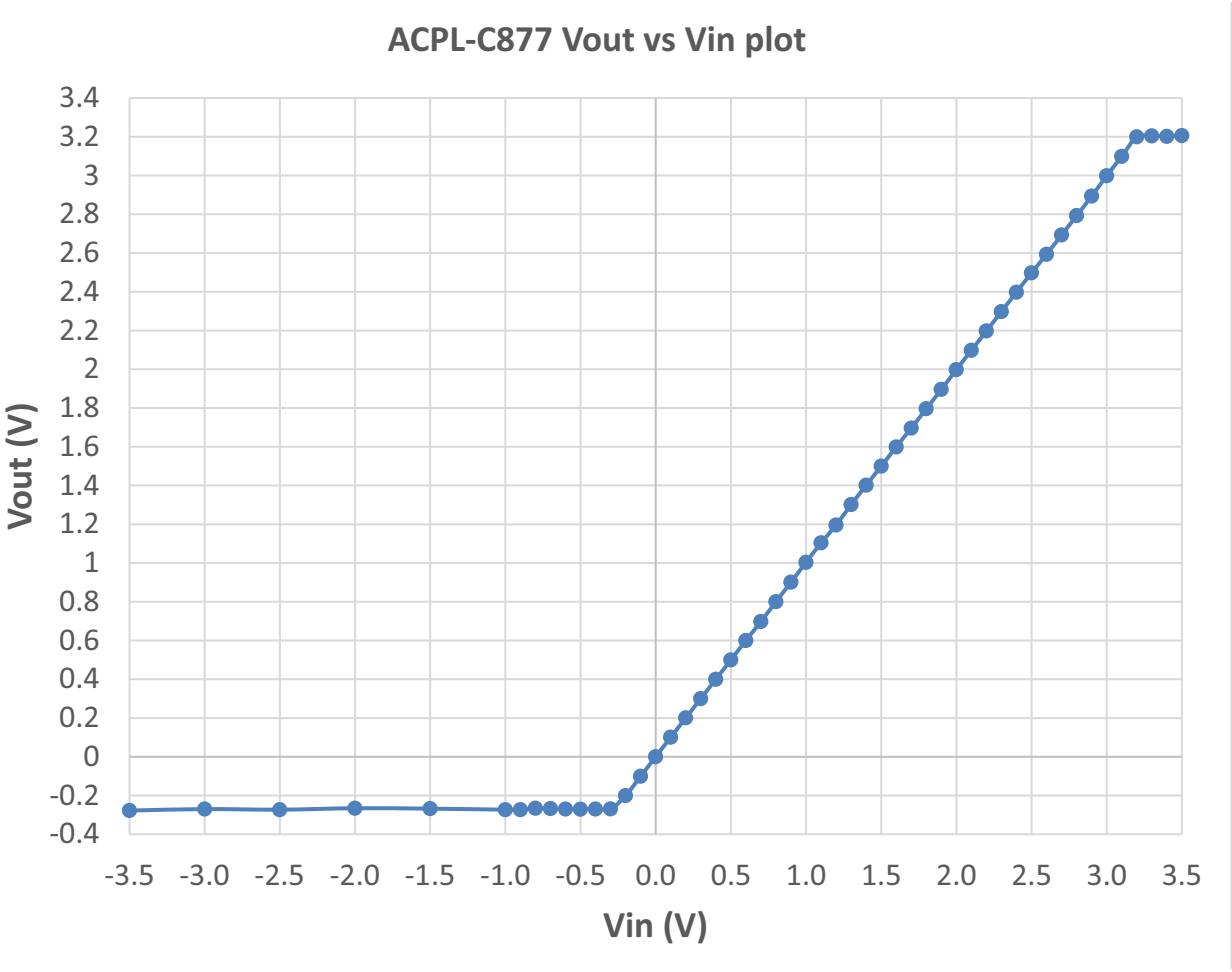
Figure 8: Output Measurement Evaluation Board Setup

Using the evaluation board:

1. Apply a 1 kHz sine wave input voltage signal to TP2 Vin+ and TP3 Vin– from a function generator such as the ultra-low distortion DS360 function generator from Stanford Research Systems. There is a 10 kΩ shunt resistor (R14) mounted between TP2 Vin+ and TP3 Vin–. Refer to the C877-SDM-EVBD Schematic Diagram. R11, R12 and R13 are for resistor network dividers to divide down the high voltage to about 2V input linear range of ACPL-C877. The sizes for R11, R12 and R13 resistors is SMD1206.
2. Adjust the input voltage signal to near +2000 mV or +20,000 ADC counts for best SNR/SNDR performance. The SNR and SNDR should be around 76 dB and 66 dB.
   The performance of SNR/SNDR is dependent on the following factors:
   – The evaluation board.
   – The sigma-delta modulator used, in this case, the ACPL-C877.
   – Input signal frequency used.
   – The decimation ratio, which can be set at the application GUI to 256, 128, or 64.
   – The input signal level. The recommended ACPL-C877 input voltage range is from 0 mV to 2000 mV. To achieve the best SNR/SNDR, design the maximum input signal range near to +2000 mV (selection of input current range and shunt resistor value).
   – The input signal source.

The following graph shows a plot of Vout vs. Vin measurements of ACPL-C877.

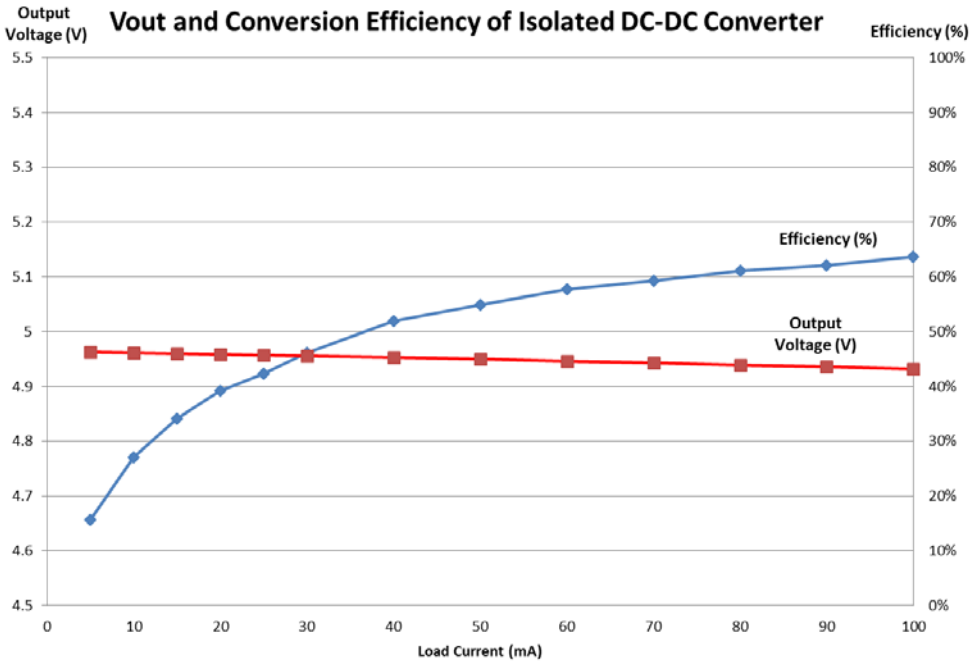
- The applied input voltage Vin is from –3.5V to 3.5V and the frequency of the sine wave is 1 kHz.
- The output voltage Vout is linear with Vin from Vin = 0V to 3.2V. However, the data sheet electrical specifications such as linearity, SNR/SNDR, and gain error are only guaranteed from Vin = 0V to 2V.



Isolated DC-DC Converter

The isolated DC-DC converter circuitry is designed based on push-pull transformer method to provide isolated Vdd1 = 5V for the Broadcom ACPL-C877 sigma-delta modulator from the 5V power supply directly from the micro USB type B connector of the FPGA-EVBD board. The design incorporate the push-pull transformer driver, PE22100 from pSemi, which is built in a small form factor of 2 x 2 x 0.5mm QFN package and can operate from –40°C to +125°C. The device consist of an on-chip oscillator where switching frequency can be set by an external capacitor. The oscillator output is divided by two in frequency to create anti-phase clock signals that drive two power switches. In this design, Cset of the PE22100 is selected as 100 pF, and that results in switching frequency of around 200 kHz. This frequency is outside the operating bandwidth of ACPL-C877 sigma-delta modulator and the Sinc3 filter FFT bandwidth used for filtering and decimating the sigma-delta bitstream from the ACPL-C877.

The PE22100 drives the Wurth pn: 750313638 push-pull transformer coil. The transformer coil can withstand isolation voltage of Viso = 5 kVrms per 1 minute, and built into a package with creepage and clearance distance of 8 mm. The transformer coil operates at ambient temperature from –40°C to +125°C. The two outputs of the transformer coil are then combined after the schottky diodes. The output voltage needs to be regulated through 5V-5V LDO regulator. The following plot shows measurement conversion efficiency vs. output load current.



For further technical support and pricing inquiry, contact pSemi at sales_europe@psemi.com and Wurth at midcom@we-online.com.

PCB Modifications

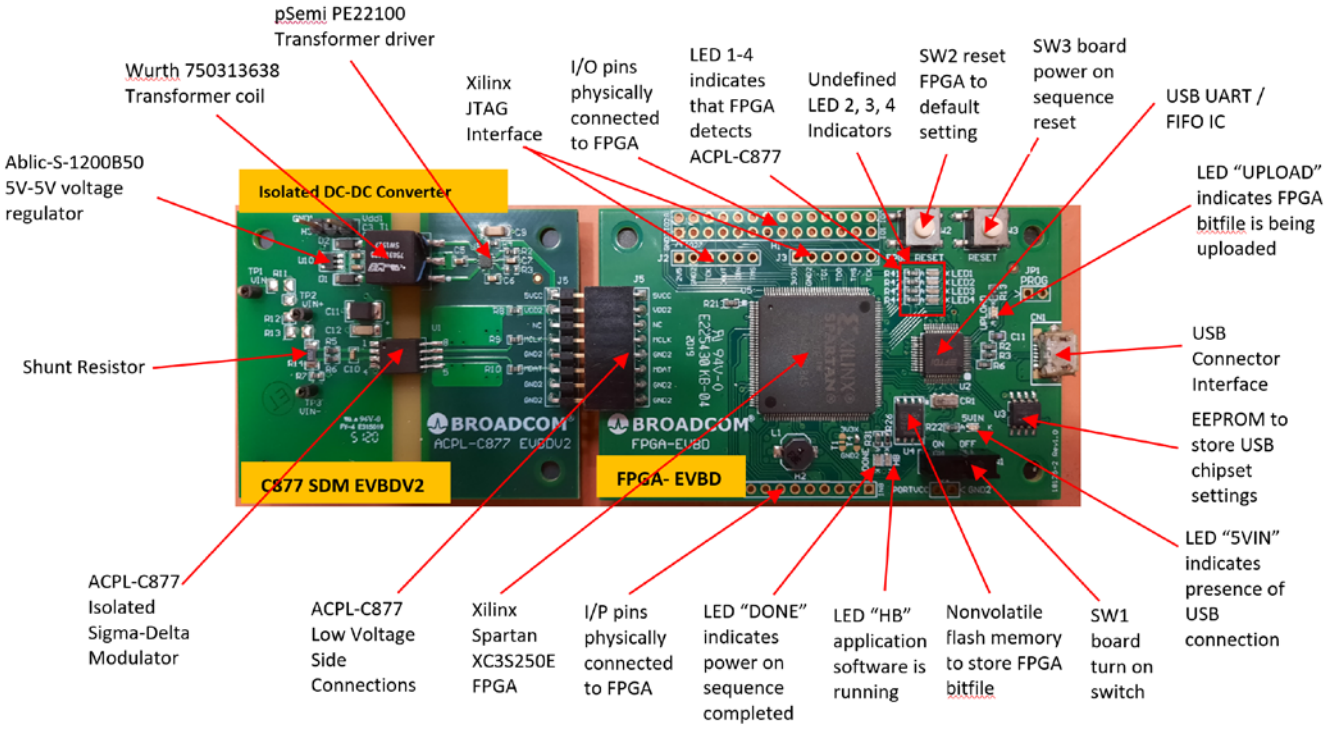
- Vdd1 is supplied from the 5V/5V isolated dc/dc converter using push-pull transformer method. Vdd1 can also be supplied externally. To do that, ensure that R1 is disconnected.
- The ACPL-C877 Vdd2 is supplied from the 3.3V regulator. If there is a need to check the performance or troubleshoot the ACPL-C877 component only at Vdd2 = 5V, Pin 1 and Pin2 of J5 connector on the C877-SDM-EVBDv2 board can be shorted. The Vdd2 is then supplied directly from the USB power, 5VCC. R18 would need to be removed on the FPGA-EVBD board.
- The green LED1-4 signals the detection of ACPL-C877. These LED indicators can be used for other functions if there is a need to modify the FPGA.
- The H1 and H2 connector pins are physically connected to the FPGA. These connector pins can also be used for input (I/P) or input/output (I/O) if there is a need to modify the FPGA.

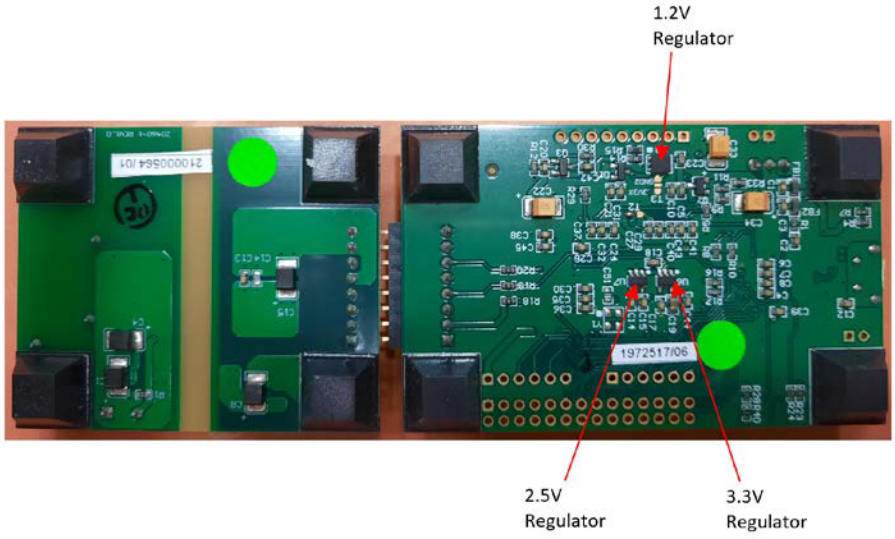
Troubleshooting

- After switching on SW1, if the green DONE LED does not come on, reset the FPGA by pressing SW2 once. If the problem still does not go away, perform a full board reset by pressing SW3 once.
- Each evaluation board sent to the customer is functionally checked and tested. If the problem does not go away, consult a Broadcom Application Engineer. If need be, Broadcom will send a new board.

Appendix

PCB Description

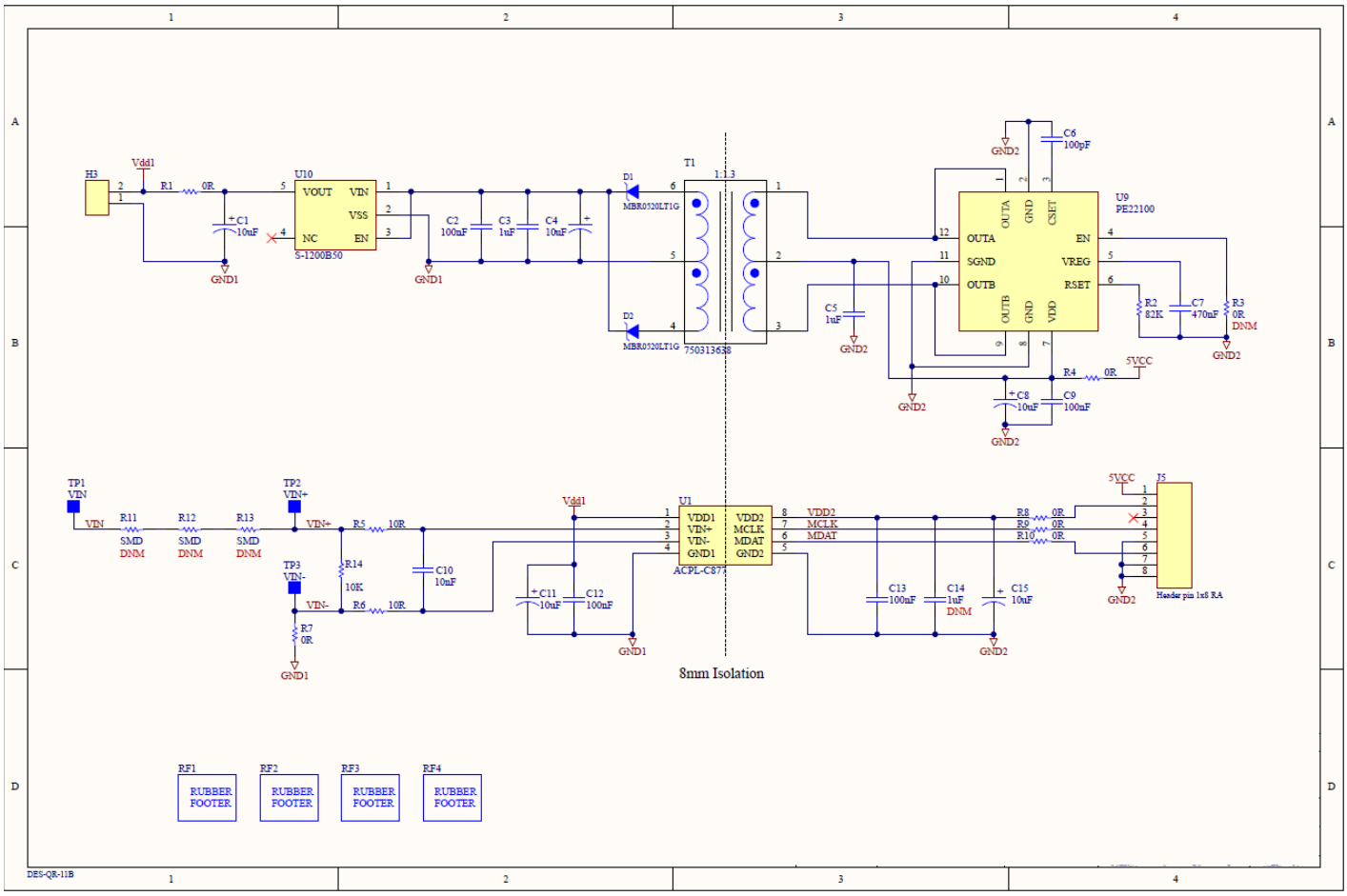




C877-SDM-EVBD Schematic Diagram

The schematic of the Evaluation Board is shown in the following figure.

Figure 9: Schematic of the ACPL-C877 Evaluation Board



C877-SDM-EVBD PCB Layout

Figure 10: Top Layer

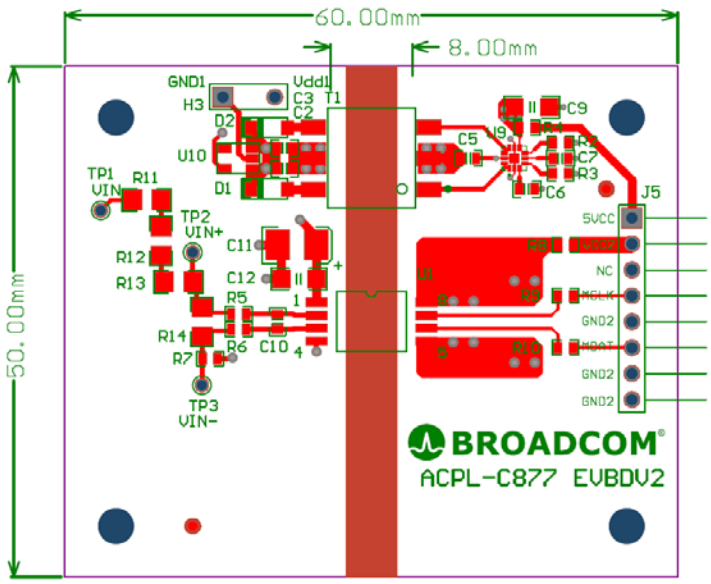


Figure 11: Second Layer

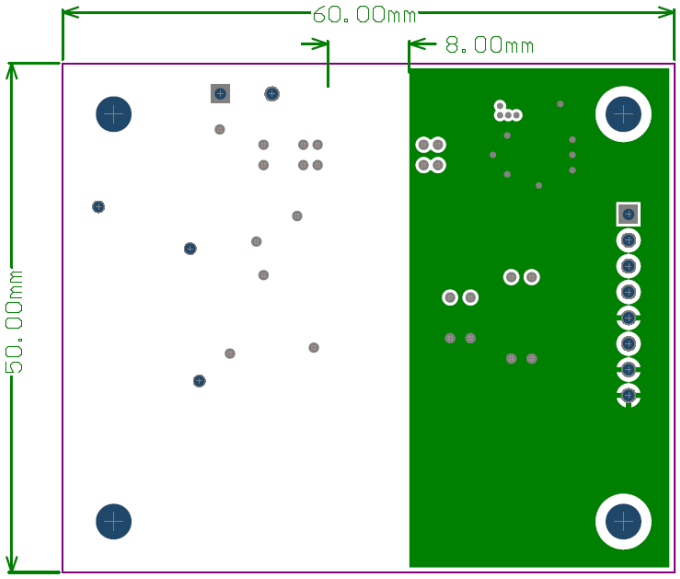


Figure 12: Third Layer

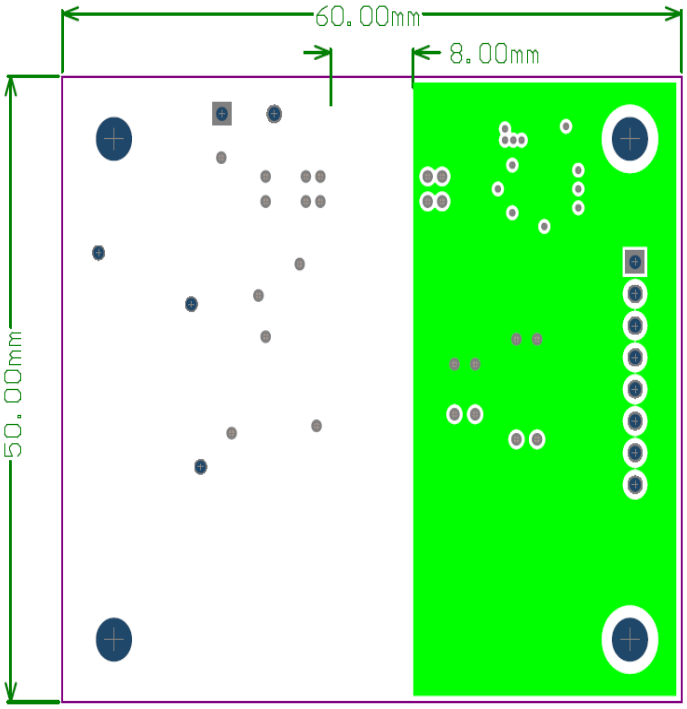
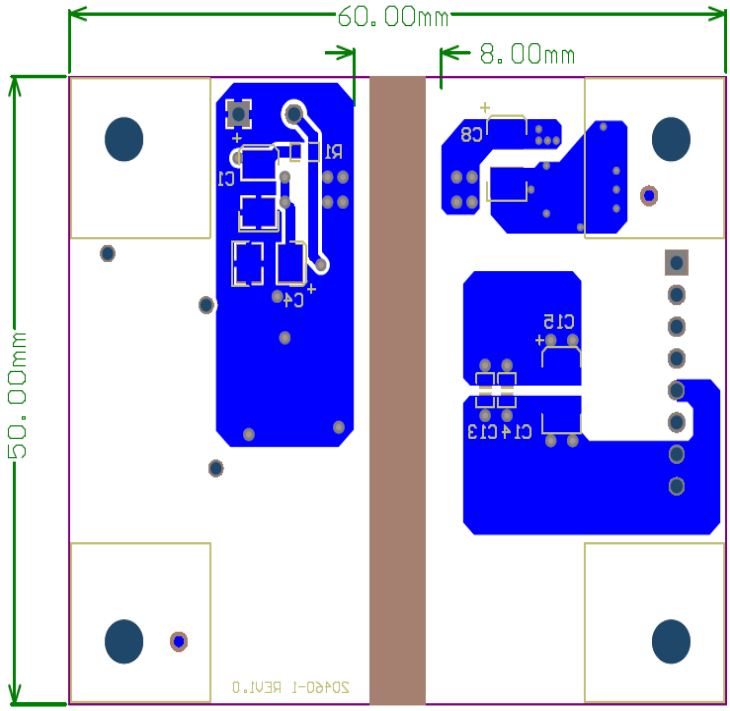
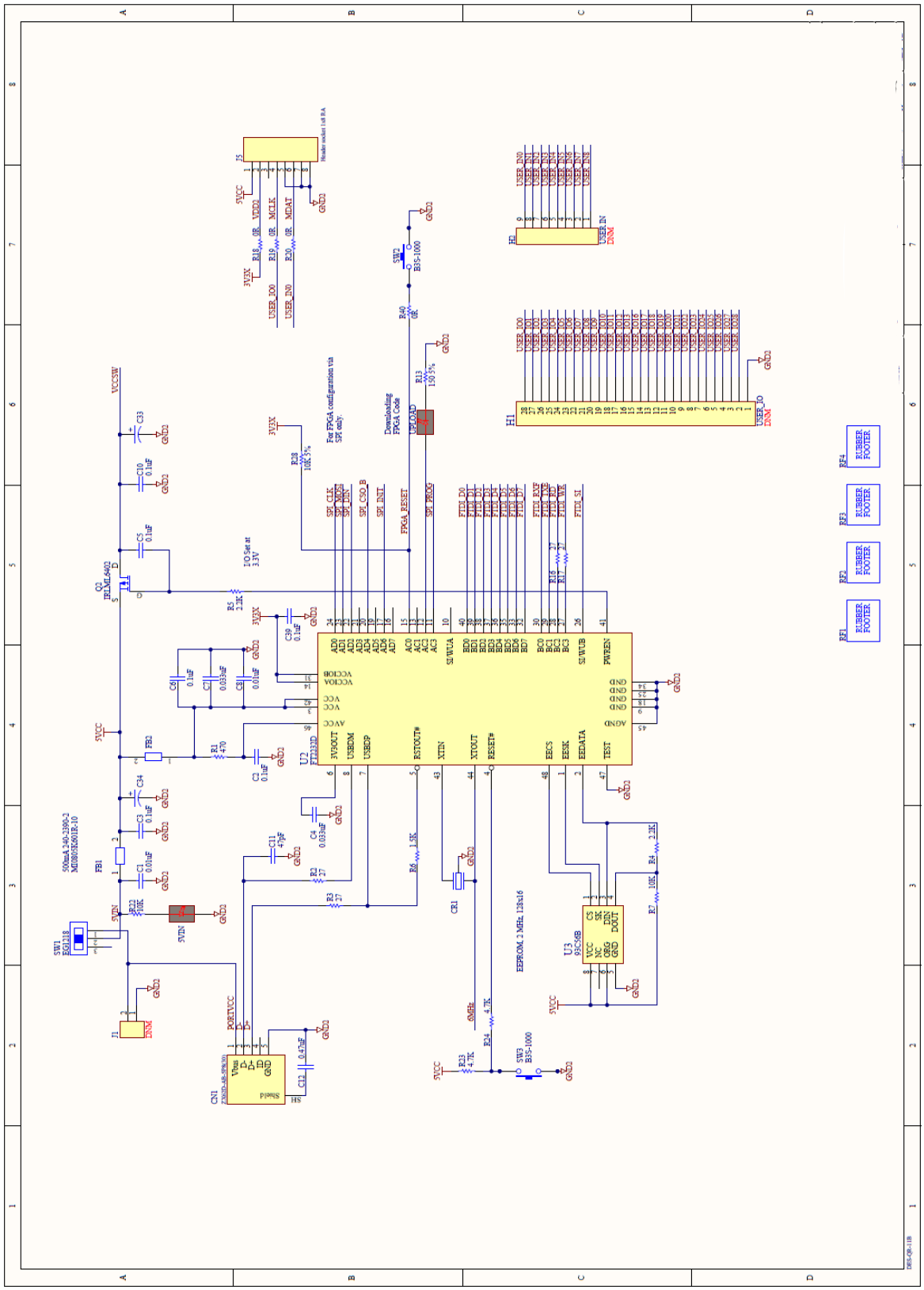
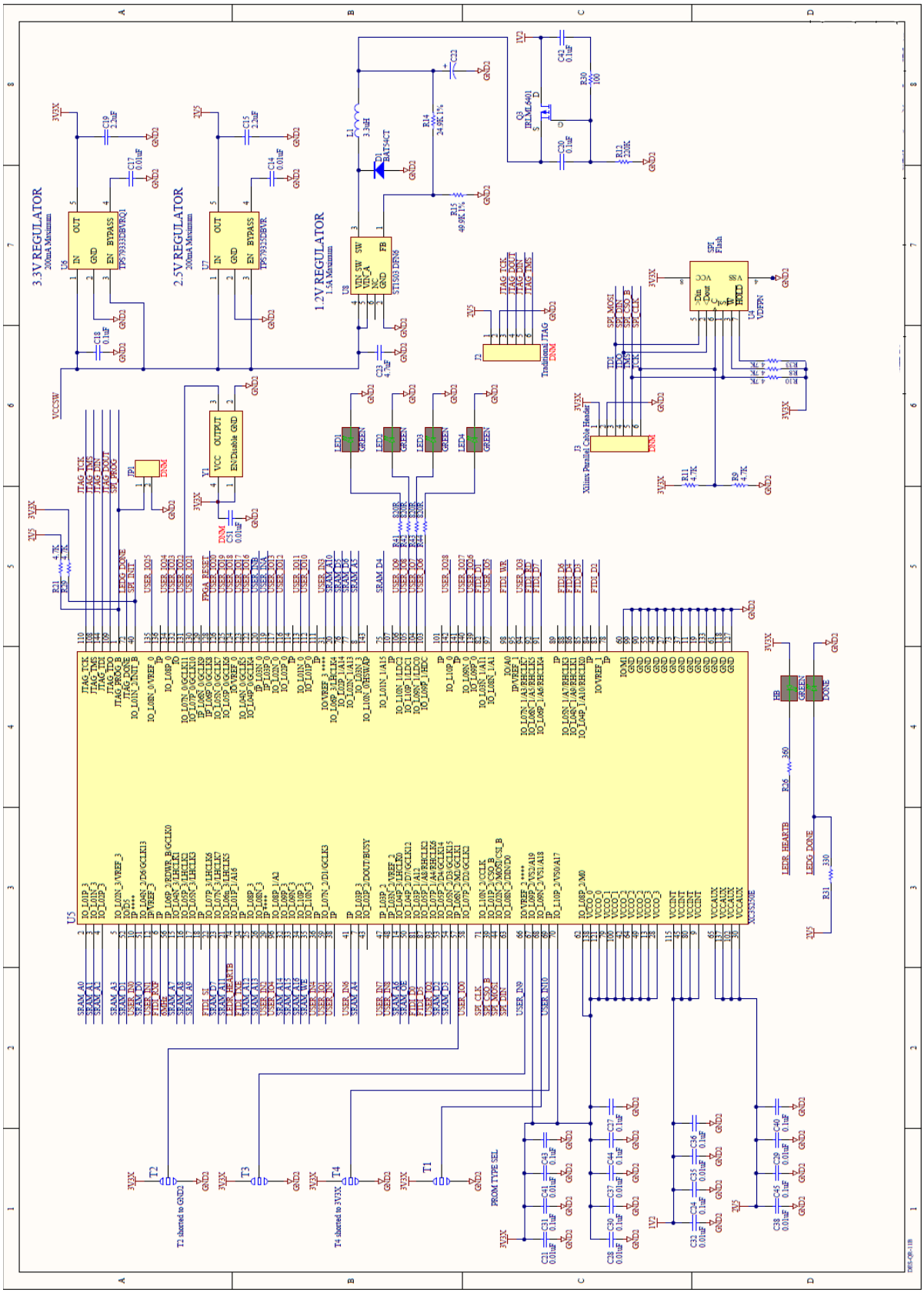


Figure 13: Bottom Layer



FPGA-EVBD Schematic Diagram




3.3V REGULATOR
200mA Maximum
2.5V REGULATOR
200mA Maximum
1.2V REGULATOR
1.5A Maximum
U5
XC3S250E
U6
U7
U8
J2
Traditional JTAG
J3
Xilinx Parallel Cable Header
U4
SPI Flash
LED1
LED2
LED3
LED4
HB
DONE
LEDR_HEARTB
LEDG_DONE
T1
T2
T3
T4
T2 shorted to GND
T4 shorted to 3V3X
PROM TYPE SEL

FPGA-EVBD PCB Layout

Figure 14: Top Layer

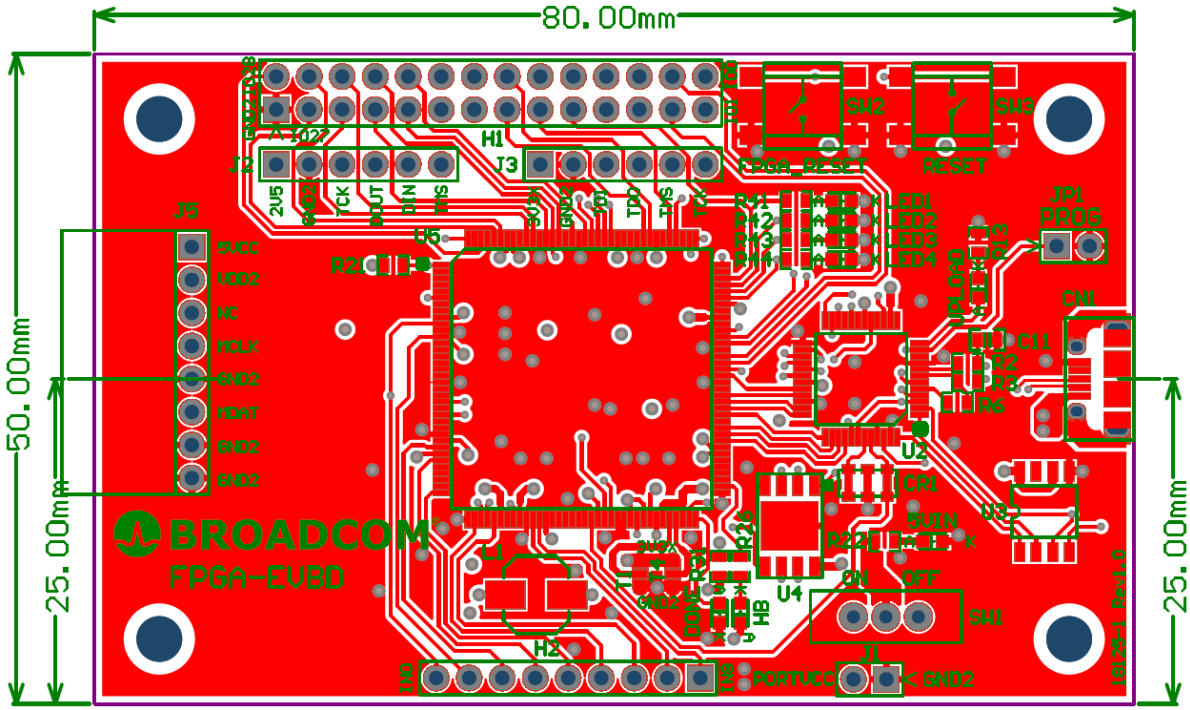


Figure 15: Second Layer

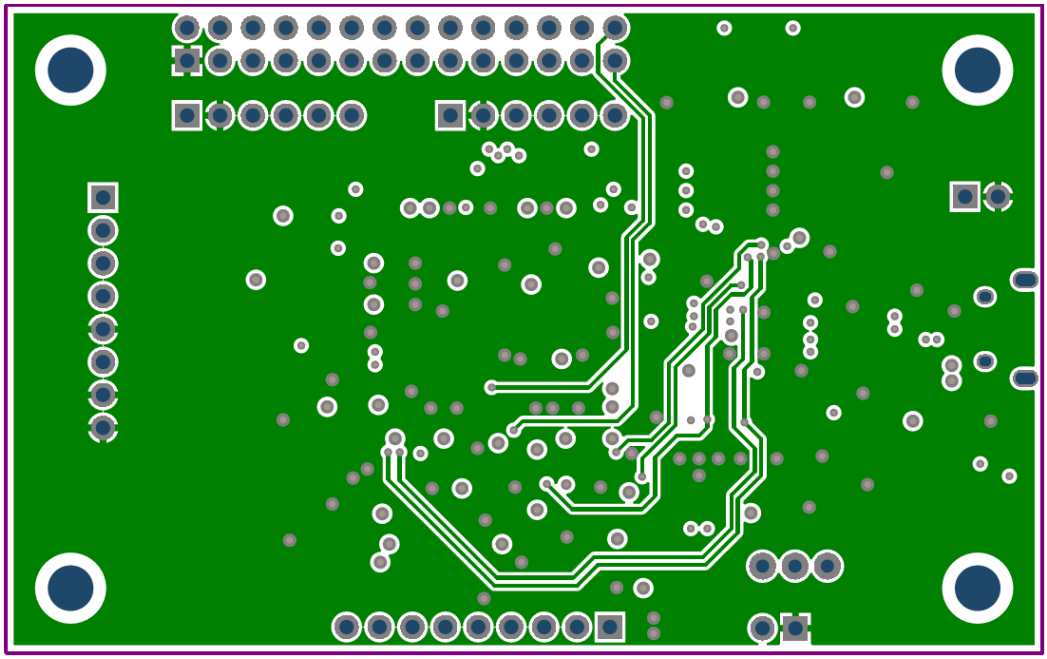


Figure 16: Third Layer

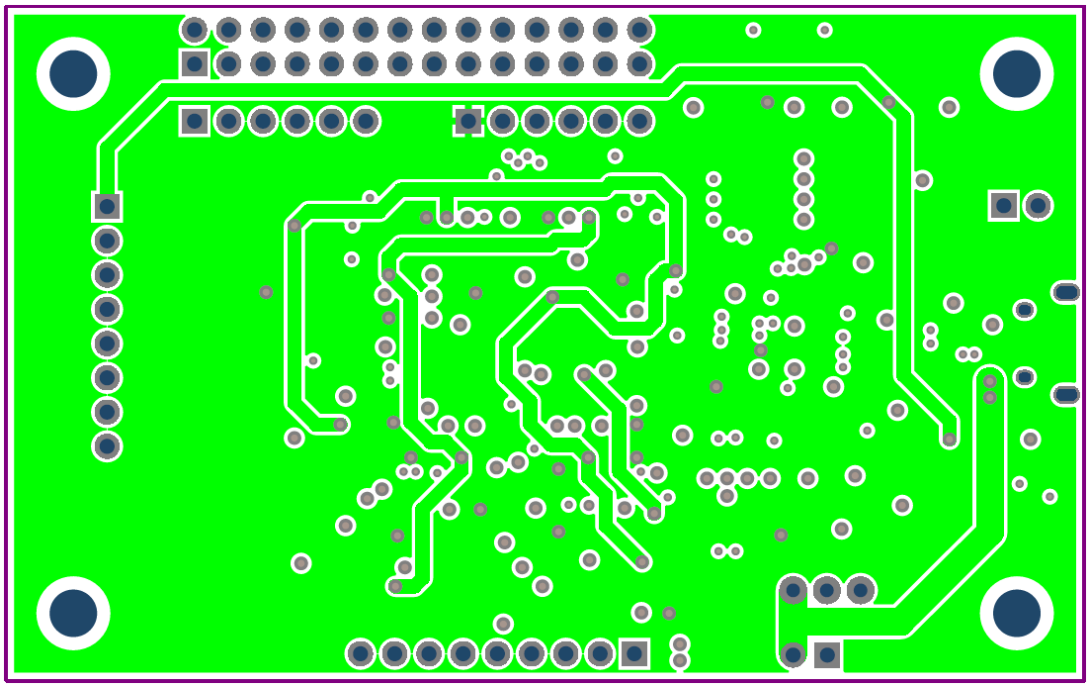
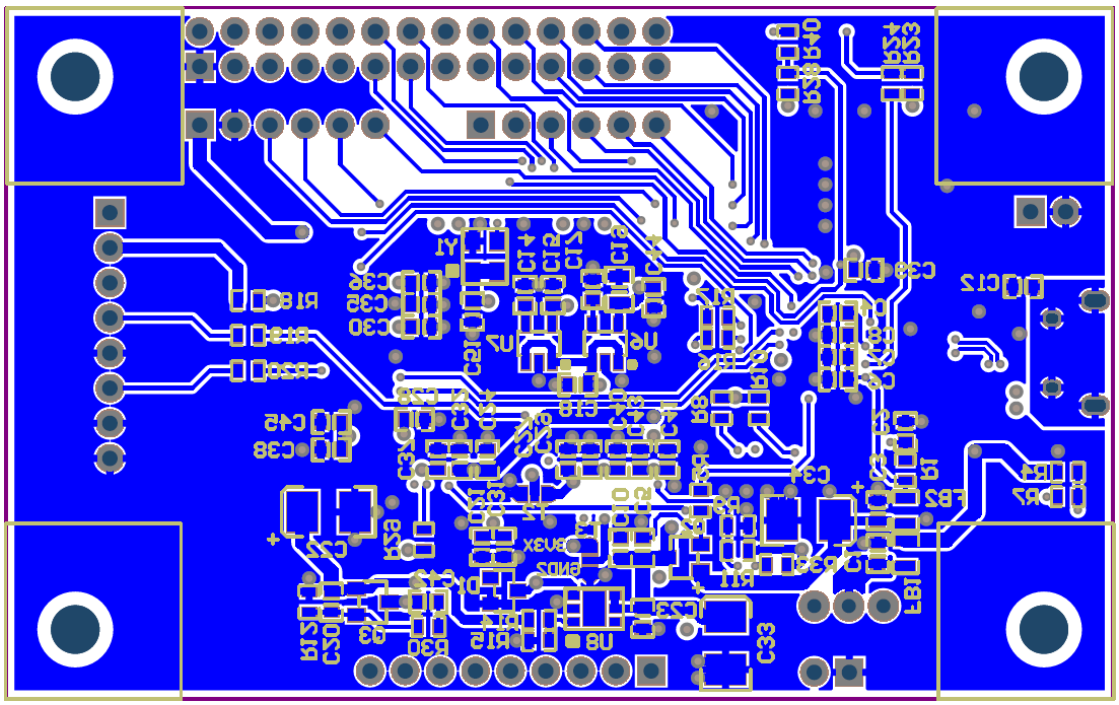


Figure 17: Bottom Layer



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