User Guide

ACPL-C740 Evaluation Kit Board

Isolated Sigma-Delta Modulator

Description

The Broadcom ACPL-C740 isolated sigma-delta (Σ-Δ) modulator converts an analog input signal into a high-speed (20 MHz typical) single-bit data stream by means of a sigma-delta over-sampling modulator. The time average of the modulator data is directly proportional to the input signal voltage. The modulator uses an internal speed of 20 MHz. The modulator data are encoded and transmitted across the isolation boundary where they are recovered and decoded into a high-speed data stream of digital ones and zeros. The original signal information is represented by the density of ones in the data output.

The input signal information is contained in the modulator output data stream, represented by the density of ones and zeros. The density of ones is proportional to the input signal voltage, as shown in Figure 1. A differential input signal of 0V ideally produces a data stream of ones 50% of the time and zeros 50% of the time. A differential input of –200 mV corresponds to an 18.75% density of ones, and a differential input of +200 mV is represented by an 81.25% density of ones in the data stream. A differential input of +320 mV or higher results in ideally all ones in the data stream, while an input of –320 mV or lower results in all zeros, ideally. Table 1 shows this relationship.

Figure 1: Modulator Output vs. Analog Input

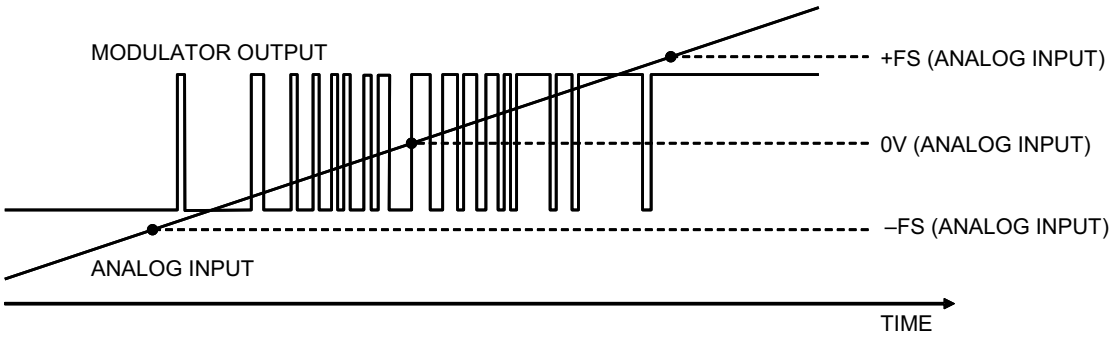


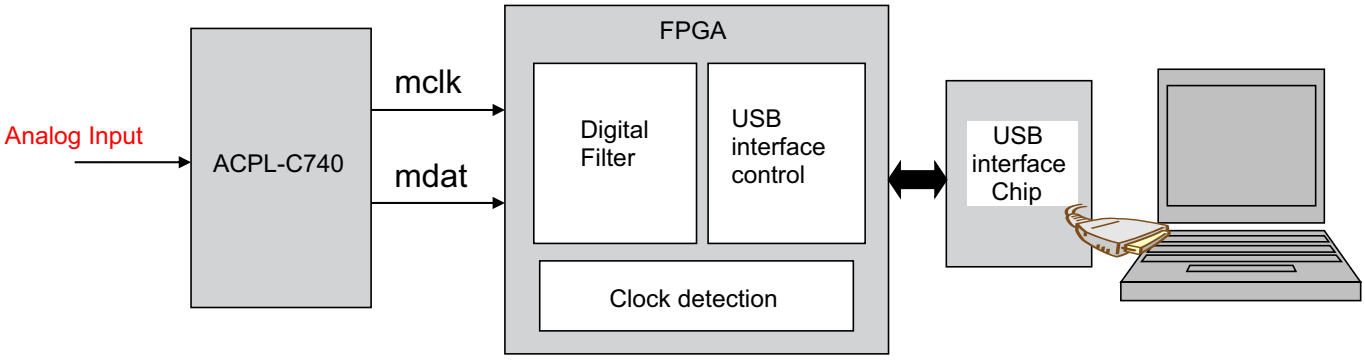
Table 1: Input Voltage with Ideal Corresponding Density of 1s at Module Data Output, and ADC Code

Analog Input	Voltage Input	Density of 1s	Density of 0s	ADC Code (16-bit unsigned decimation)
+Full-Scale	+320 mV	100%	0%	65,535
+Recommended Input Range	+200 mV	81.25%	18.75%	53,248
Zero	0 mV	50%	50%	32,768
–Recommended Input Range	–200 mV	18.75%	81.25%	12,288
–Full-Scale	–320 mV	0%	100%	0

A digital filter converts the single-bit data stream from the modulator into a multi-bit output word similar to the digital output of a conventional A/D converter. With this conversion, the data rate of the word output is also reduced (decimation). A Sinc3 filter is recommended to work together with the ACPL-C740. With a 20-MHz internal clock frequency, 256 decimation ratio, and 16-bit word settings, the output data rate is 78 kHz (20 MHz/256). This filter can be implemented in an ASIC, FPGA, or DSP.

In this evaluation board, a Sinc3 filter is implemented using the Xilinx Spartan XC3S250E FPGA. The FPGA hardware is designed in a Verilog/VHDL environment. The major building blocks are the Digital Filter and USB interface control, as shown in Figure 2. The design is synthesized and implemented using the Xilinx Tool to a bitstream file. This bitstream file can be loaded to FPGA through USB, a step already done for each evaluation board kit.

Figure 2: Digital Filter and USB Interface Control



Preparation and Setup

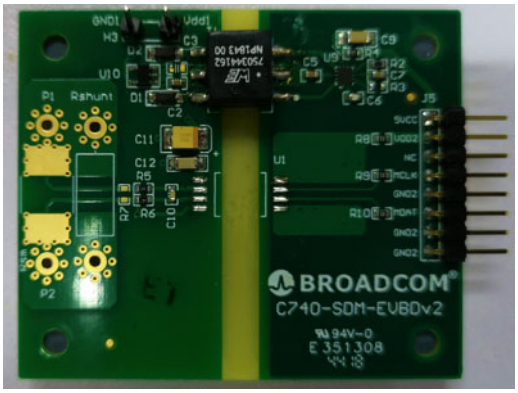
Each complete ACPL-C740 evaluation kit shipment includes the following items:

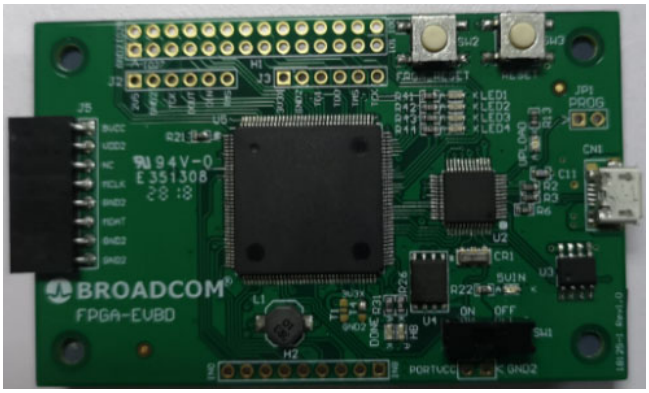
- ACPL-C740 evaluation board
- Cable with USB/mini-USB terminations
- Softcopy folder containing drivers and application software programs. The softcopy folder contains the following document or software programs:
  - ACPL-C740 Xilinx FPGA Evbd Kit User Guide.pdf: Evaluation board user guide
  - CDM21228_Setup.exe: FTDI USB chipset driver for Windows 32-bit and 64-bit operating systems. For other operating systems, download from the manufacturer's website (http://www.ftdichip.com/Drivers/VCP.htm)
  - dig_filter.exe: Broadcom application GUI software
  - DigFil_200mvINcmosOUT.bit: FPGA bitfile
  - Sinc3_verilog.txt: Sinc3 filter codes in Verilog
  - Sinc3_VHDL.txt: Sinc3 filter codes in VHDL
  - Sine wave files: Sine waves configured to different frequencies 500 Hz, 1000 Hz, and 2000 Hz that can be played from any audio player

1. Save the softcopy folder to a PC directory location. See the appendix for descriptions of the major components on the evaluation board, the schematic diagrams, and PCB layout.
2. Connect the FPGA-EVBD board to the PC using the provided USB cable.
3. Turn on switch SW1. The red *5VIN* LED lights up, indicating the presence of a USB connection.
4. Install the CDM21228_Setup.exe USB chipset driver file. The driver installs two ports: USB Serial Converter A and USB Serial Converter B.

5. To verify that the installation is successful, open the Device Manager. Under Universal Serial bus controllers, the two ports USB Serial Converter A and USB Serial Converter B should appear.
6. Each time the evaluation board SW1 is turned on, the board goes through a series of power-on sequences. When completed, the green DONE LED comes on to indicate completion of the power-on sequences.
7. Connect the C740-SDM-EVBD board to the FPGA-EVBD. Once connected, LED1 to LED4 light up in an undefined sequence to indicate that the board connections are properly done.

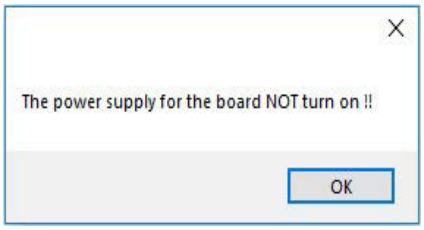
   The C740-SDM-EVBD and FPGA-EVBD boards are shown, respectively, below:





8. Go to the PC directory and run the dig_filter.exe application program. Refer to the application GUI screen capture as shown in Figure 3. If the evalboard is connected and SW1 switched on, a Broadcom-System message appears on the right of the Search button. If SW1 is not turned on, an error message appears, as shown below.

   Click **OK** and the application GUI appears. The message *System not connected!!* displays instead.

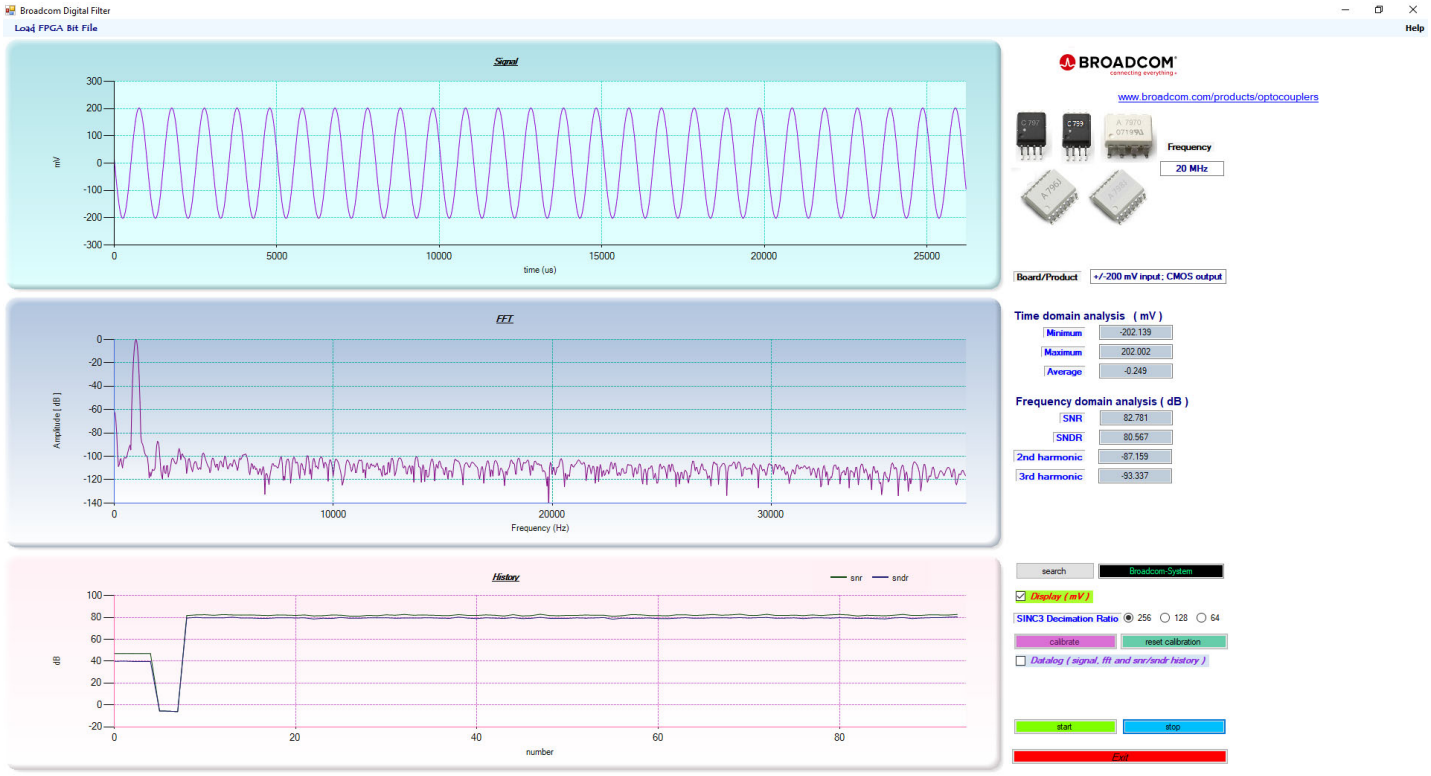


9. Switch on SW1. Go to the application GUI, and click **Search**. Now, the message changes to Broadcom-System to indicate that the connection is established.

Application GUI

The application GUI has three displays: two showing the signal in the time domain and frequency domain, and a third showing SNR and SNDR historical plots. The time domain signal can be displayed in terms of ADC count or voltage level (mV) by checking the Display (mV).

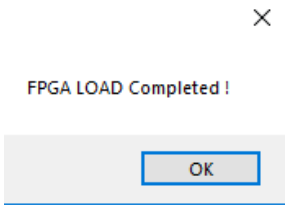
Figure 3: Application GUI Example



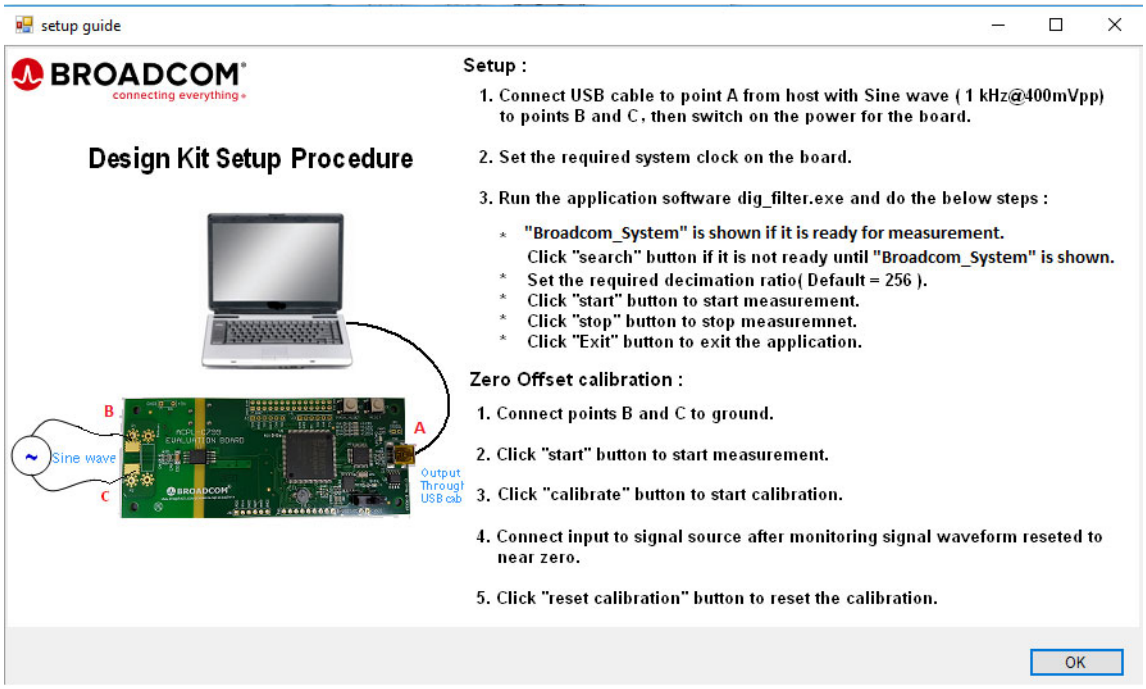
To the right of the displays, real-time minimum, maximum, and average signal levels are shown in the time domain in terms of either mV or ADC count. SNR, SNDR, 2nd harmonic, and 3rd harmonic levels are displayed in the frequency domain.

1. Click **Start** to begin capturing the input signal. The configured board frequency is captured under the Frequency box and the type of sigma-delta modulator in terms of input range and output signal type displays in the Board/Product.
2. Save the signal, FFT, and SNR/SNDR history data into text files that are readable and compatible to Microsoft Excel by selecting the Datalog (signal, fft, and snr/sndr history) box. The snr.txt, signal.txt, and fft.txt files are stored in the same file directory as the application GUI.

3. If there is an updated FPGA bitfile or a newly configured bitstream file, this can be can be uploaded by clicking **Load FPGA Bit File** on the top-left corner of the application GUI. When the bitfile is being uploaded, the green DONE LED goes off and the red UPLOAD LED displays. When uploading is completed, the red UPLOAD LED goes off, while the green DONE LED displays again to signal completion. The FPGA LOAD Completed! pop-up appears, as shown below.



4. For quick help, click **Help** from the top-right corner of the application GUI, then select the setup guide. The help guide also describes the calibration procedure to zero the offset.



Measurement

There are a few ways to apply an input signal to the evaluation board:

- Apply input current signal with a shunt resistor.

  Example: Select the shunt resistor value is shown below:

  If maximum RMS current through the motor = 30A, 20% overloads during normal operation, then, peak current is 51A (30 × 1.414 × 1.2). The recommended maximum input voltage for ACPL-C740 is ±200 mV.

  Shunt resistor value = V/I = 200 mV/51A ≈ 4 mΩ

  Power dissipation = $I^2 \times R = (30)^2 \times 4\ m\Omega = 3.6W$

The shunt resistor mounting pad is designed to accommodate various shunt resistor package types. The Kelvin connection PCB trace connects from the center of the pad to the inputs of ACPL-C740 through the anti-aliasing filters (AAFs). Connecting from the center of the pads is usually the optimum location for most shunt resistor designs. The evaluation board also provides pads P1 and P2 for soldering thick cables to the motor driving board.

- Apply an input voltage signal without a shunt resistor.

  Connect the audio cable with the audio 3.5-mm jack connected to either a PC, smart phone, tablet, MP3 player, or any kind of audio player device. Then, connect the crocodile clips to the shunt resistor mounting pads.

  Check the 1 kHz sine test signal and supply a 1 kHz sine wave voltage signal to the evaluation board. Other methods include playing any of the three provided sine wave files on a music player software program from the audio player devices described previously. Adjust the volume until the signal level is near ±200 mV or ±20,000 ADC counts for best SNR/SNDR performance.

  The performance of SNR/SNDR is dependent on a few factors:

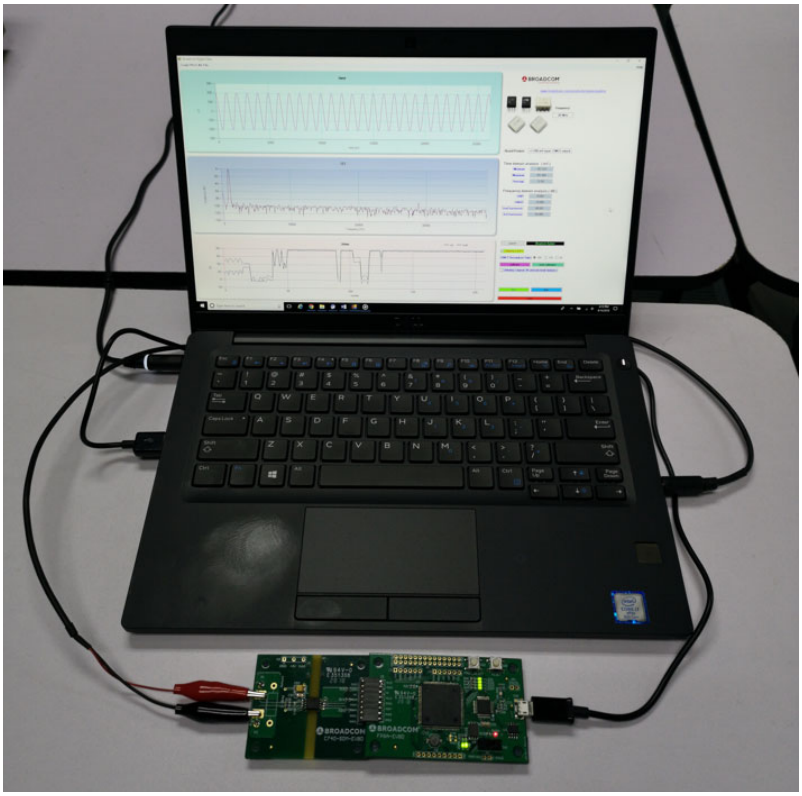
  – The evaluation board
  – The sigma-delta modulator used, in this case, the ACPL-C740
  – Input signal frequency used
  – The decimation ratio, which can be set at the application GUI to 256, 128, or 64.
  – The input signal level. The ACPL-C740 recommended input voltage range is from –200 mV to 200 mV. To achieve the best SNR/SNDR, design the maximum input signal range nearest ±200 mV (using the selection of the input current range and shunt resistor value).
  – The input signal source.

  Table 2 shows a comparison of the SNR/SNDR performance between audio signal sources coming from a laptop.

Table 2: SNR/SNDR Comparison

Filter Configuration	Signal Source from Audio Jack of Laptop					
	Signal Freq. = 500 Hz		Signal Freq. = 1000 Hz		Signal Freq. = 2000 Hz	
	SNR(dB)	SNDR(dB)	SNR(dB)	SNDR(dB)	SNR(dB)	SNDR(dB)
Sinc3 DR = 64	not enough sampling sinewave cycles		66	64	61	59
Sinc3 DR = 128	76	73	74	73	70	63
Sinc3 DR = 256	77	75	78	77	73	63

Figure 4: Measurement Setup



- Lab bench test: Apply input voltage signal from a function generator with one shunt resistor mounted on the input of evaluation board.

  A more accurate method to measure the performance of the ACPL-C740 evaluation board is to connect a 1-shunt resistor, then supply the voltage signal from a function generator that can drive sufficient current through the 1-shunt resistor until an input signal level of ±200 mV is reached. One such function generator is the ultra low distortion DS360 function generator from Standford Research Systems.

  Table 3 shows the SNR/SNDR performance using this method.

Table 3: SNR/SNDR Performance

Filter Configuration	Signal Source from Audio Jack of Laptop					
	Signal Freq. = 500 Hz		Signal Freq. = 1000 Hz		Signal Freq. = 2000 Hz	
	SNR(dB)	SNDR(dB)	SNR(dB)	SNDR(dB)	SNR(dB)	SNDR(dB)
Sinc3 DR = 64	not enough sampling sinewave cycles		75	72	72	71
Sinc3 DR = 128	81	77	79	76	79	76
Sinc3 DR = 256	82	78	82	78	81	77

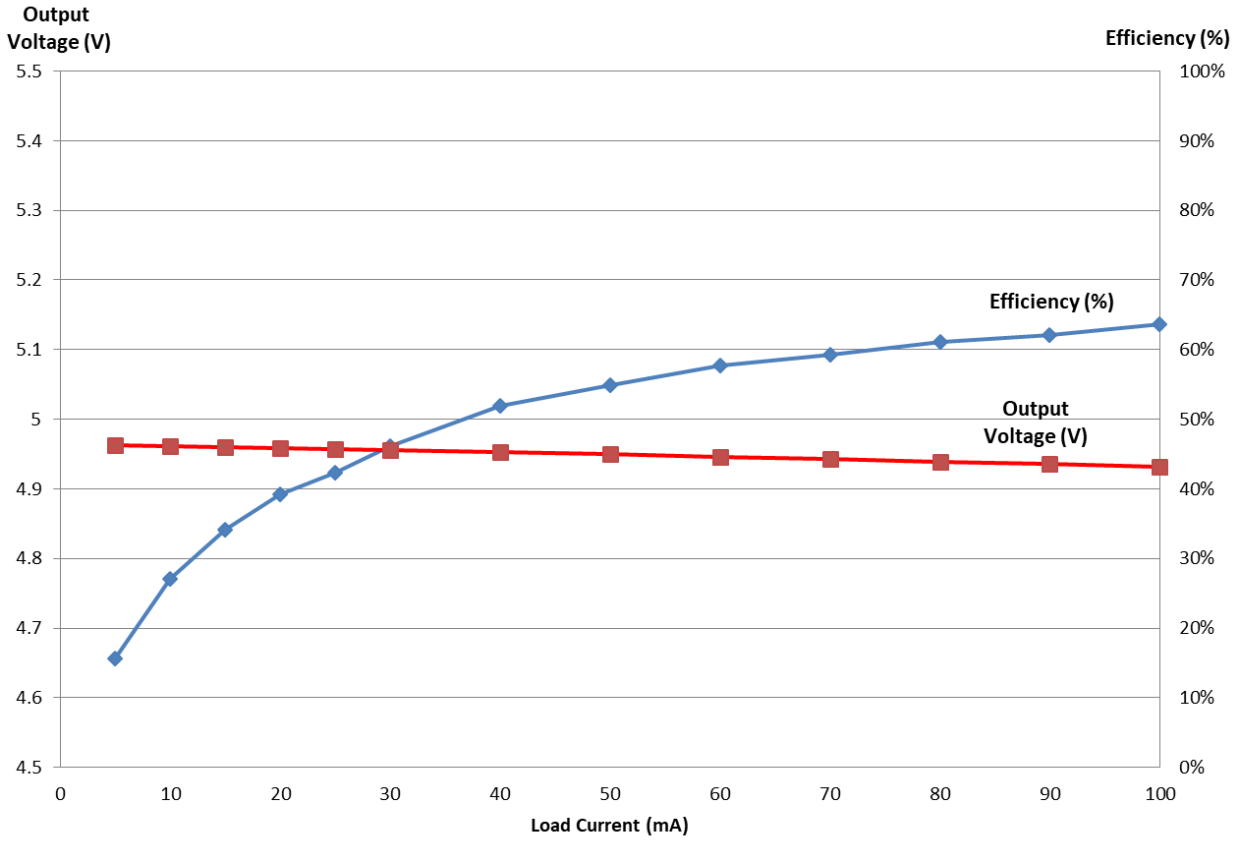
If such a function generator is not available, it is best to connect an actual shunt resistor and connect to the current-sensing system directly.

Isolated DC-DC Converter

The isolated DC-DC converter circuitry is designed based on the push-pull transformer method to provide isolated Vdd1=5V for the Broadcom ACPL-C740 sigma-delta modulator from the 5V power supply directly from the micro-USB type B connector of the FPGA-EVBD board. The design incorporates the push-pull transformer driver, PE22100 from pSemi, which is built in a small form factor of 2 x 2 x 0.5 mm^3 QFN package and can operate from –40°C to +125°C. The device consists of an on-chip oscillator where switching frequency can be set by an external capacitor. The oscillator output is divided by two in frequency to create anti-phase clock signals that drive two power switches. In this design, Cset of the PE22100 is selected as 100 pF, which results in a switching frequency of around 200 kHz. This frequency is outside the operating bandwidth of the ACPL-C740 sigma-delta modulator and the Sinc3 filter FFT bandwidth used for filtering and decimating the sigma-delta bitstream from the ACPL-C740.

The PE22100 drives the Wurth push-pull transformer coil (PN 750313638). The transformer coil can withstand isolation voltage of Viso = 5 kVrms per 1 min., and built into a package with creepage and clearance distance of 8 mm. The transformer coil operates at an ambient temperature from –40°C to +125°C. The two outputs of the transformer coil are then combined after the Schottky diodes. The output voltage must be regulated through a 5V/5V LDO regulator. The plot below shows measurement conversion efficiency versus output load current.

Figure 5: Vout and Conversion Efficiency of the Isolated DC-DC Converter



For further technical support and pricing enquiries, contact pSemi at sales_europe@psemi.com or Wurth at midcom@we-online.com.

PCB Modifications

1. Vdd1 is supplied from the 5V/5V isolated DC-DC converter using the push-pull transformer method. Vdd1 can also be supplied externally. To do that, ensure that R1 is disconnected.
2. The ACPL-C740 Vdd2 is supplied from the 3.3V regulator. To check the performance or troubleshoot the ACPL-C740 component only at Vdd2 = 5V, short Pin 1 and Pin2 of the J5 connector on the C740-SDM-EVBDv2 board. The Vdd2 is then supplied directly from the USB power, 5VCC.

   Note that R18 must be removed on the FPGA-EVBD board.
3. Green LED1–4 signals the detection of ACPL-C740. To modify the FPGA, use these LED indicators for other functions.
4. The H1 and H2 connector pins are physically connected to the FPGA. To modify the FPGA, use these connector pins for input (I/P) or input/output (I/O).

Troubleshooting

If the green DONE LED does not come on after switching on SW1, reset the FPGA by pressing SW2 once. If the problem arises, perform a full board reset by pressing SW3 once.

Each evaluation board is functionally checked and tested. before being sent to the customer. If a problem continues to arise, consult a Broadcom Application Engineer. If need be, Broadcom will send a new board.

Appendix

Figure 6: PCB Description

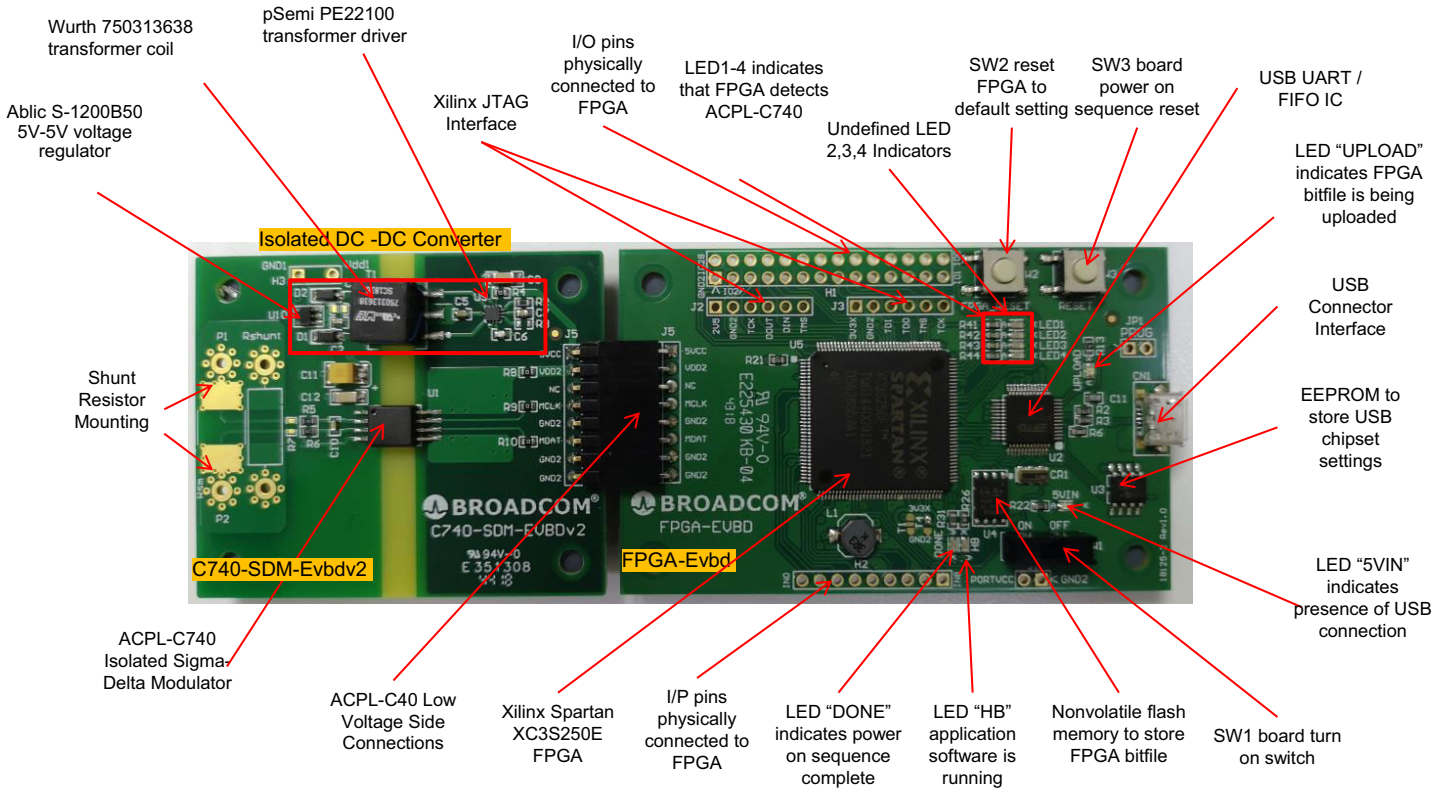
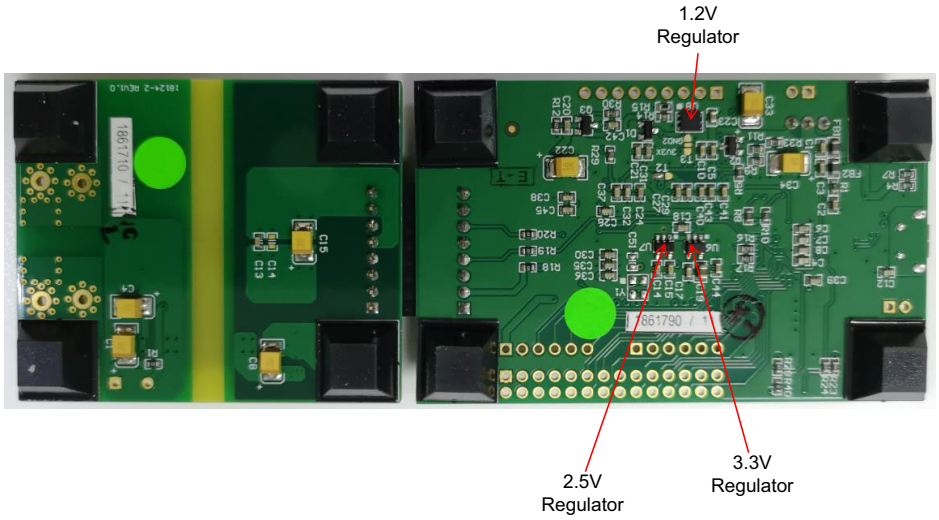
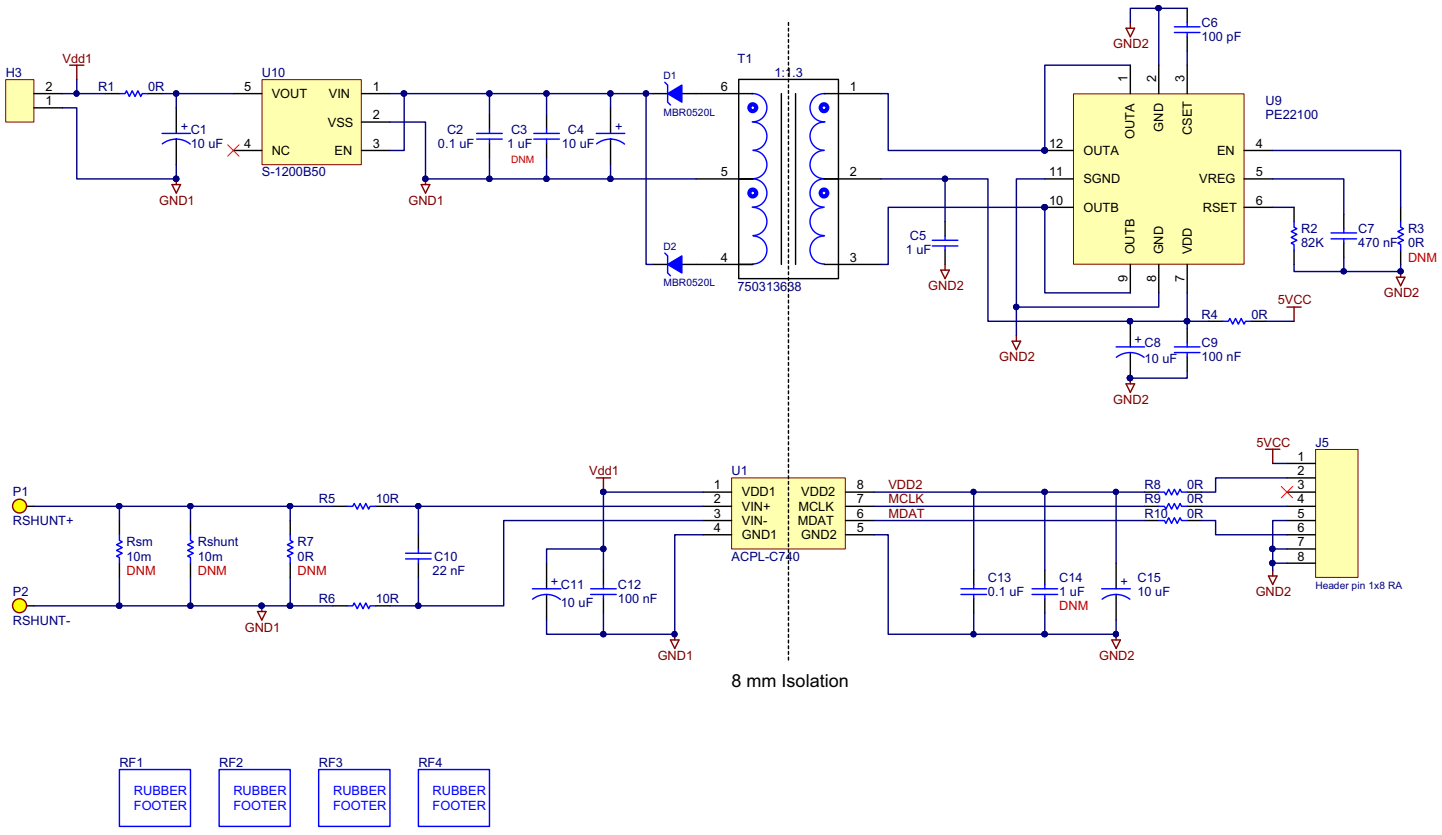


Figure 7: PCB Description



C740-SDM-EVBD Schematic Diagram

Figure 8: C740-SDM-EVBD Schematic Diagram



C740-SDM-EVBD PCB Layout

Figure 9: C740-SDM-EVBD PCB Top Layer

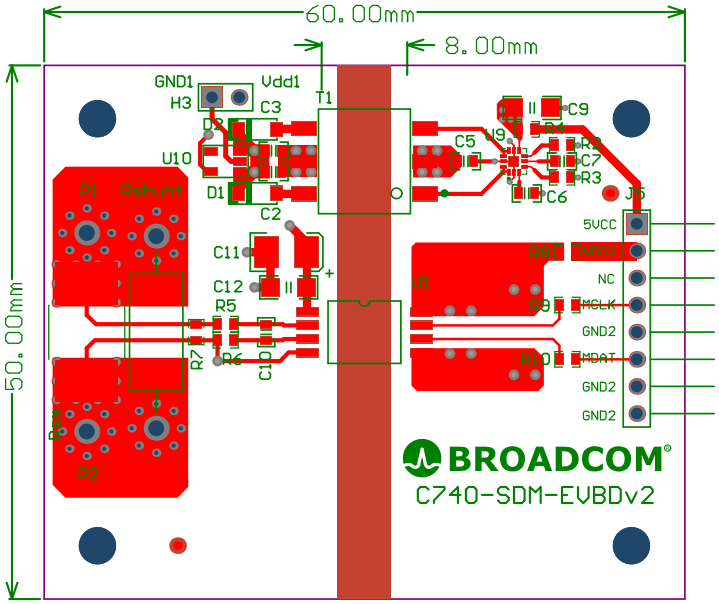


Figure 10: C740-SDM-EVBD PCB Second Layer

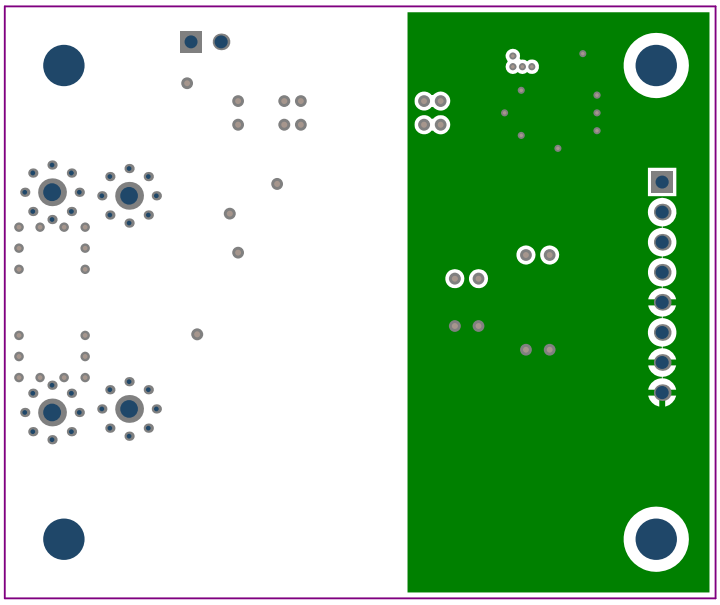


Figure 11: C740-SDM-EVBD PCB Third Layer

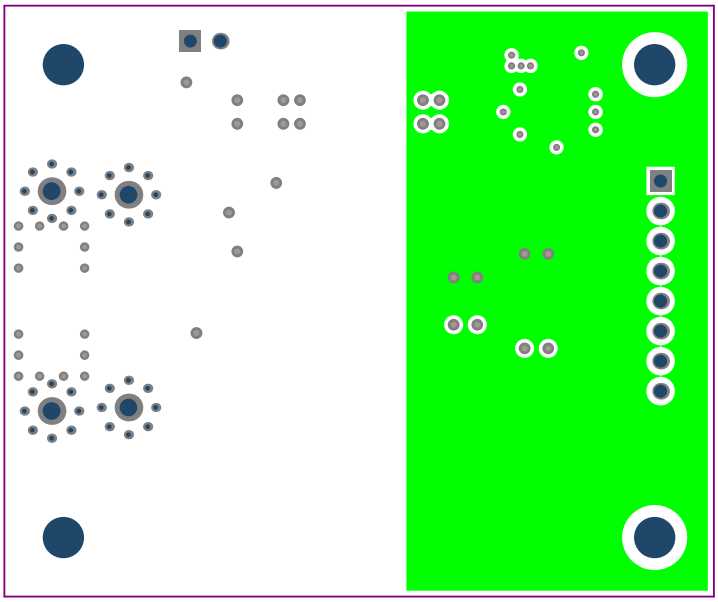
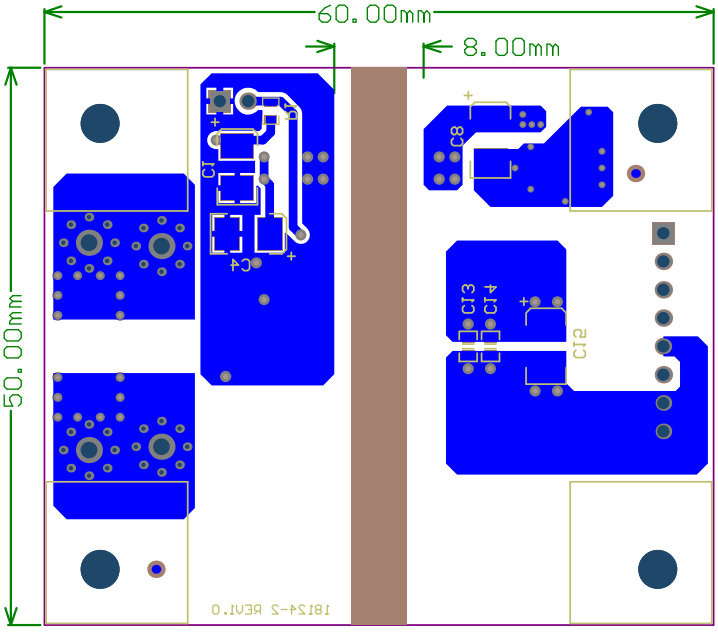


Figure 12: C740-SDM-EVBD PCB Bottom Layer



FPGA-EVBD Schematic Diagram

Figure 13: FPGA-EVBD Schematic Diagram (Part 1)

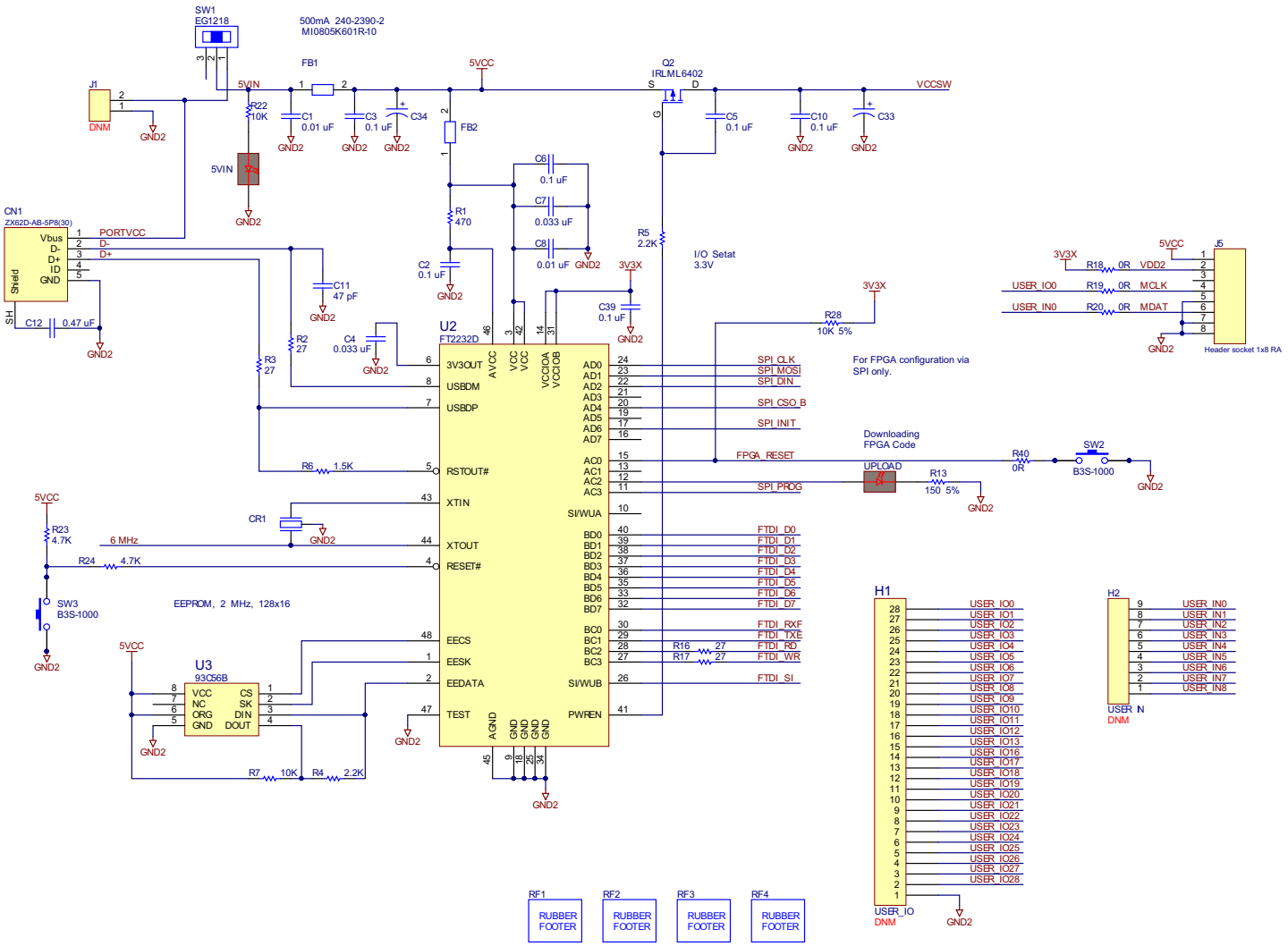
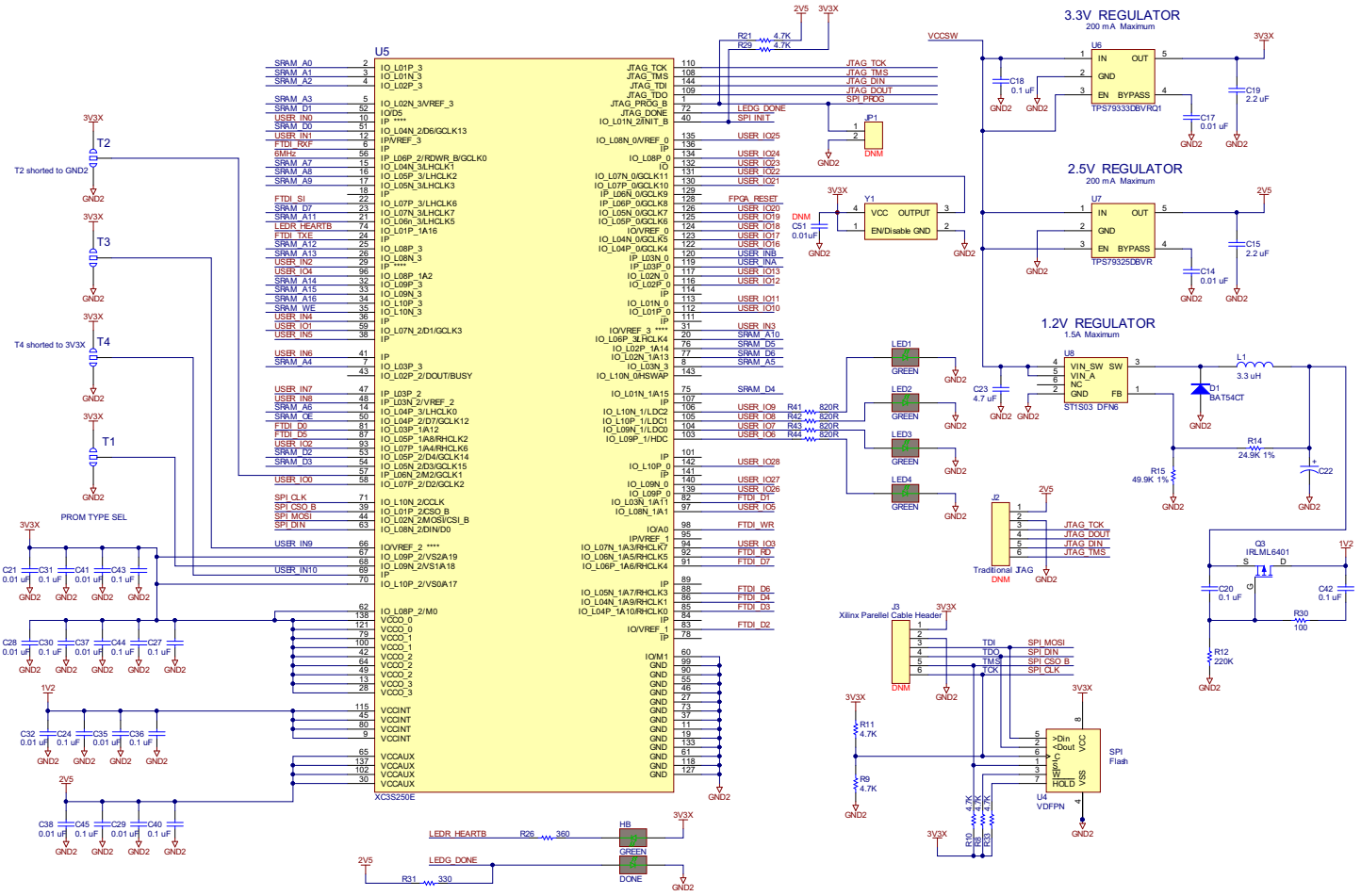


Figure 14: FPGA-EVBD Schematic Diagram (Part 2)



FPGA-EVBD PCB Layout

Figure 15: FPGA-EVBD PCB Top Layer

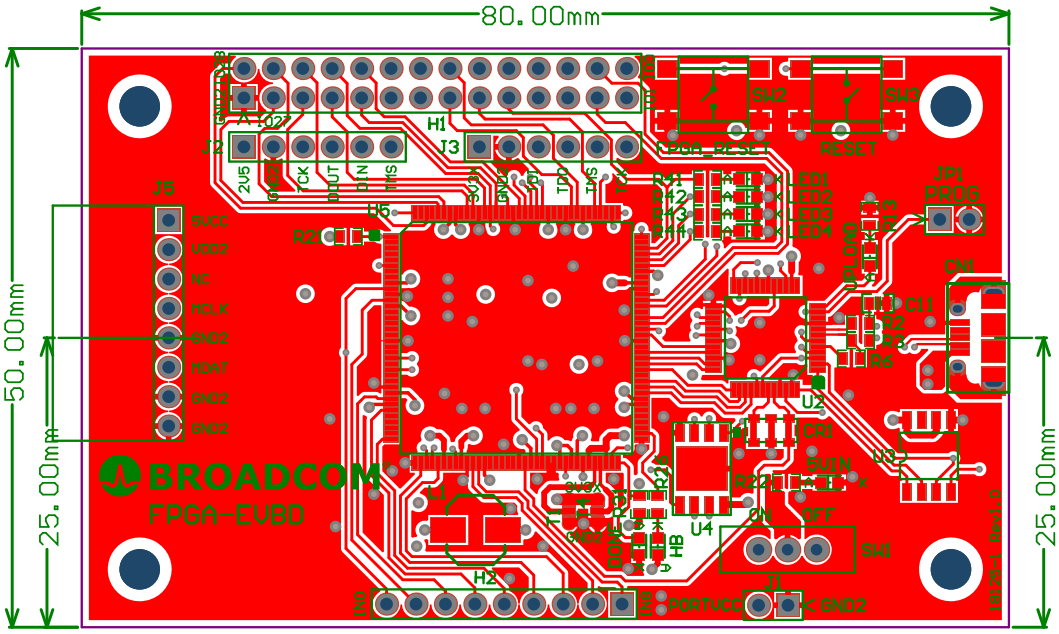


Figure 16: FPGA-EVBD PCB Second Layer

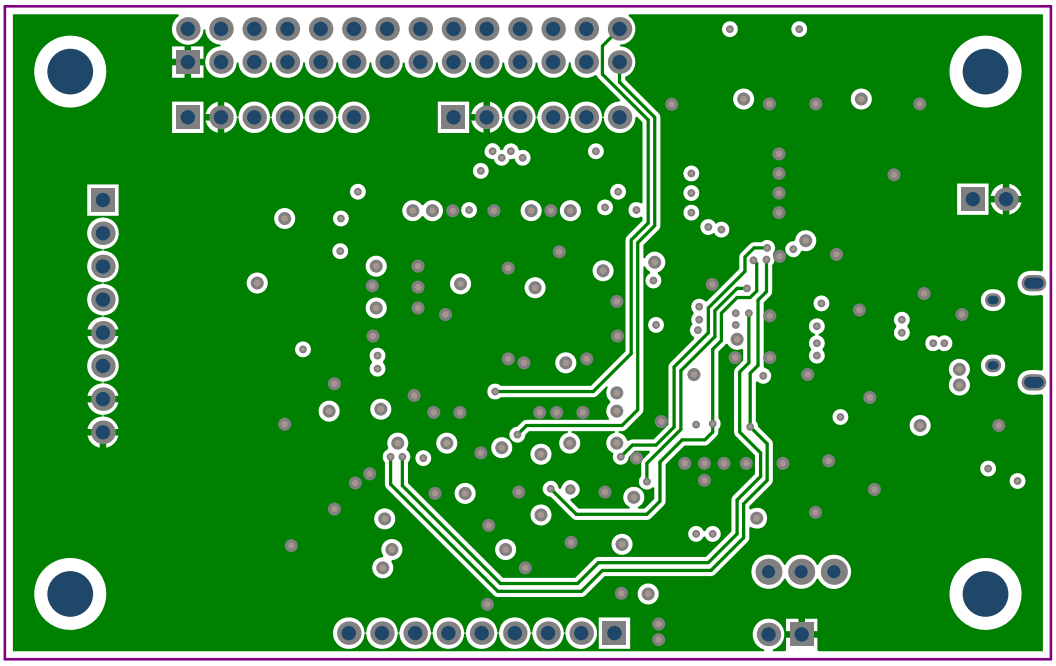


Figure 17: FPGA-EVBD PCB Third Layer

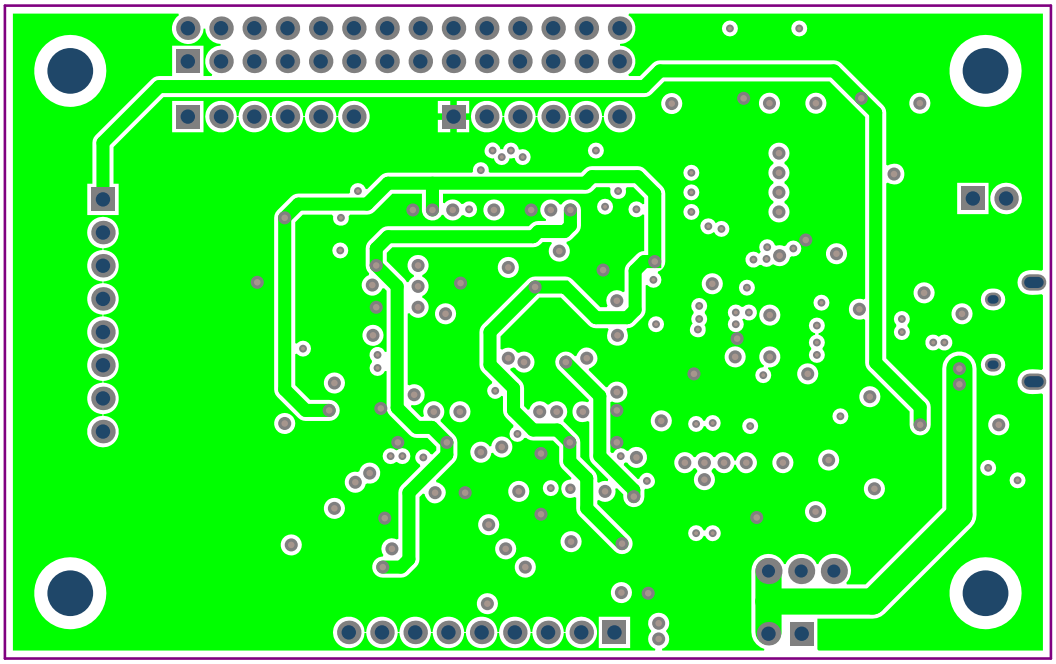
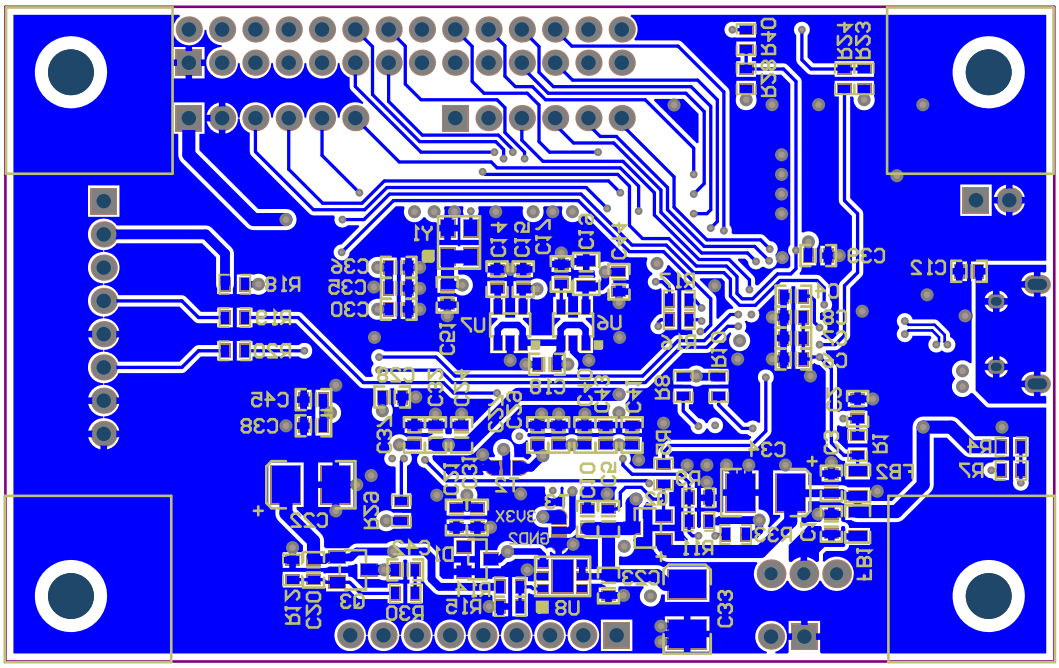


Figure 18: FPGA-EVBD PCB Bottom Layer



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