BROADCOM®

Data Sheet

ACPL-C72B, ACPL-C72A, ACPL-C720

Precision Miniature Isolation Amplifiers

Description

The Broadcom® ACPL-C72B, ACPL-C72A, and ACPL-C720 isolation amplifiers are designed for current sensing in electronic power converters in applications including motor drives and renewable energy systems. In a typical motor drive implementation, current flows through an external shunt resistor and the resulting analog voltage drop is sensed by the isolation amplifier. A differential output voltage that is proportional to the current is created on the other side of the optical isolation barrier.

Designed to reduce power loss on the shunt resistor, the ACPL-C72x series are optimized to accept a ±50-mV input voltage range. For general applications, the ACPL-C72A (±1% gain tolerance) and the ACPL-C720 (±3% gain tolerance) are recommended. For high-precision applications, the ACPL-C72B (±0.5% gain tolerance) can be used. The product operates from a single 5V supply and provides excellent linearity and dynamic performance of 65-dB SNR. The high common-mode transient immunity (25 kV/µs) of the ACPL-C72x series provides the precision and stability needed to accurately monitor motor current in high-noise motor control environments, providing for smoother control (less “torque ripple”) in various types of motor control applications.

Combined with superior optical coupling technology, the ACPL-C72x series implements a sigma-delta (Σ-Δ) analog-to-digital converter, chopper-stabilized amplifiers, and a fully differential circuit topology to provide unequaled isolation-mode noise rejection, low offset, high gain accuracy, and stability. This performance is delivered in a compact, auto-insertable Stretched SO-8 (SSO-8) package that meets worldwide regulatory safety standards.

Features

- ±0.5% high gain accuracy (ACPL-C72B)
- 0.5-mV input offset voltage
- Excellent 0.03% linearity
- 65-dB SNR
- 200-kHz wide bandwidth
- 3V to 5.5V wide supply range
- –40°C to +110°C operating temperature range
- Advanced sigma-delta (Σ-Δ) A/D converter technology
- Fully differential isolation amplifier
- 25-kV/µs common-mode transient immunity
- Compact, auto-insertable Stretched SO-8 package
- Suitable for functional safety design with V_{DD1} supply lost indication
- Safety and regulatory approvals:
  - IEC/EN/DIN EN 60747-5-5: 1414 V_{peak} working insulation voltage
  - UL 1577: 5000 V_{rms}/1 min. double protection rating
  - CAN/CSA-C22.2 No. 62368-1

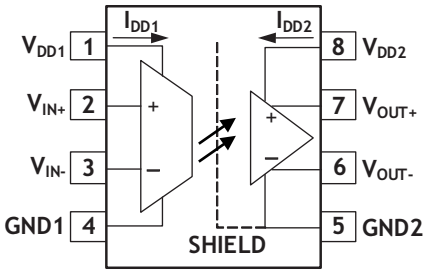
Applications

- Current sensing in AC and servo motor drives
- Solar inverters, wind turbine inverters
- Industrial process control
- Data acquisition systems
- Switching power supply signal isolation
- General-purpose analog signal isolation
- Traditional current transducer replacements

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The component featured in this data sheet is not to be used in military or aerospace applications or environments. The component is also not AEC-Q100 and not recommended for automotive applications.

Functional Block Diagram

Figure 1: Pin Configuration



NOTE: Connect 10-µF in parallel with the 0.1-µF bypass capacitors between pins 1 and 4 and between pins 5 and 8.

Table 1: Pin Description

Pin Number	Symbol	Description
1	V_{DD1}	Supply voltage for the input side (3V to 5.5V), relative to GND1
2	V_{IN+}	Positive input, ±50 mV recommended
3	V_{IN-}	Negative input, normally connected to GND1
4	GND1	Input-side ground
5	GND2	Output-side ground
6	V_{OUT-}	Negative output
7	V_{OUT+}	Positive output
8	V_{DD2}	Supply voltage for the output side (3V to 5.5V), relative to GND2

Ordering Information

Part Number	Option (RoHS-Compliant)	Package	Tape and Reel	IEC/EC/DIN EN 60747-5-5	Quantity
ACPL-C72B	-000E	Stretched SO-8	—	X	80 per tube
ACPL-C72A ACPL-C720	-500E		X	X	1000 per reel

NOTE:

- ACPL-C72B, ACPL-C72A, and ACPL-C720 are UL recognized with 5000 V_{rms}/1 minute rating per UL 1577.
- Gain accuracy is as follows: ACPL-C72B, ±0.5%; ACPL-C72A, ±1%; ACPL-C720 = ±3%.

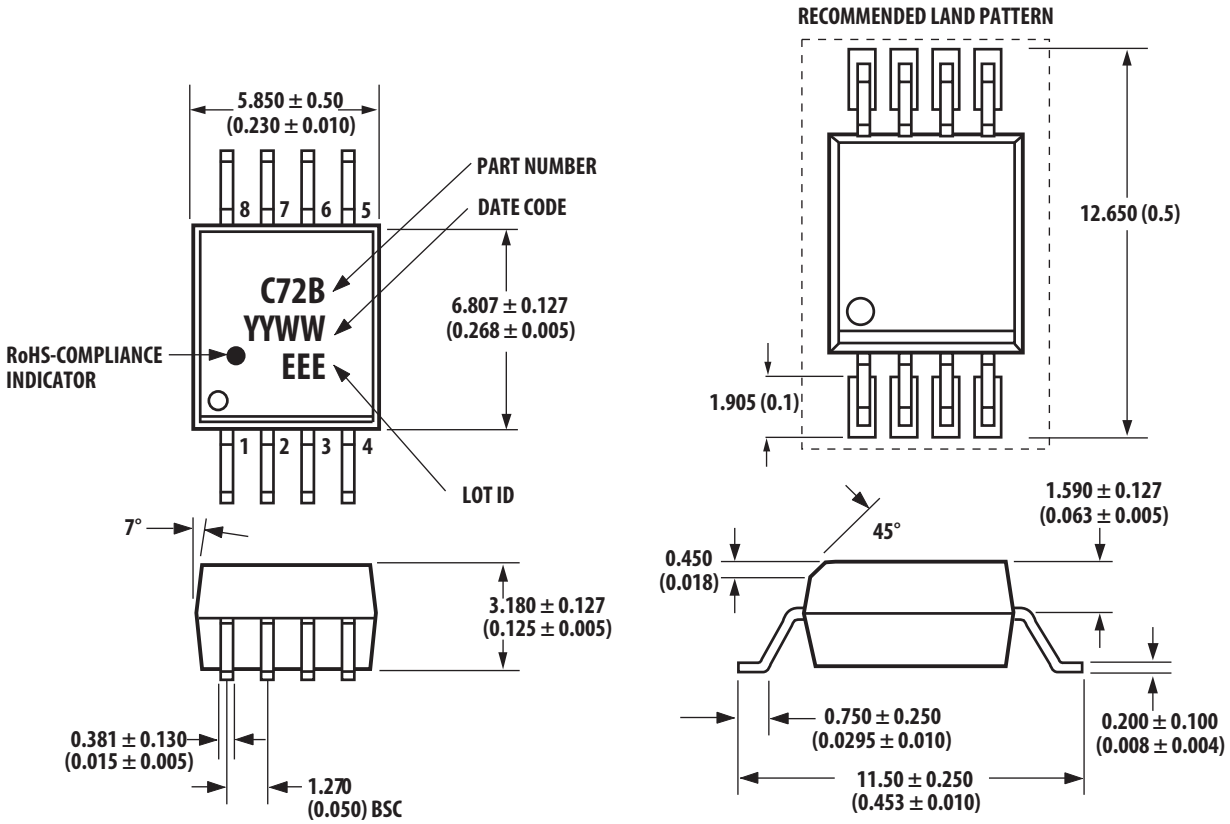
To form an order entry, choose a part number from the part number column and combine it with the desired option from the option column.

Example: Specify ACPL-C72B-500E to order the product comprised of a surface-mount package in tape-and-reel packaging with the IEC/EN/DIN EN 60747-5-5 safety approval and RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawings

Figure 2: Stretched SO-8 Package (SSO-8)



Dimensions in millimeters and (inches).
Lead coplanarity = 0.1 mm (0.004 inches).

Recommended Lead-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Use non-halide flux.

Regulatory Information

The ACPL-C72B, ACPL-C72A, and ACPL-C720 are approved by the following organizations:

IEC/EN/DIN EN 60747-5-5	Maximum working insulation voltage V_{IORM} = 1414 V_{peak}.
UL	Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{rms}. File E55361.
CSA	Approval under CAN/CSA-C22.2 No. 62368-1.

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description[a]	Symbol	Value	Units
Installation Classification per DIN VDE 0110/1.89, Table 1			
For Rated Mains Voltage ≤ 150 V_{rms}	—	I-IV	—
For Rated Mains Voltage ≤ 300 V_{rms}	—	I-IV	—
For Rated Mains Voltage ≤ 450 V_{rms}	—	I-IV	—
For Rated Mains Voltage ≤ 600 V_{rms}	—	I-IV	—
For Rated Mains Voltage ≤ 1000 V_{rms}	—	I-III	—
Climatic Classification	—	55/110/21	—
Pollution Degree (DIN VDE 0110/1.89)	—	2	—
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method[b] V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	2652	V_{peak}
Input to Output Test Voltage, Method[a] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage, tini = 60 seconds)	V_{IOTM}	8000	V_{peak}
Safety-Limiting Values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current[b]	$I_{S,INPUT}$	230	mA
Output Power[b]	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	≥ 10^9	Ω

a. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.

b. Safety-limiting parameters are dependent on ambient temperature. The input current, $I_{S,INPUT}$, derates linearly above a 25°C free-air temperature at a rate of 2.53 mA/°C; the output power, $P_{S,OUTPUT}$, derates linearly above a 25°C free-air temperature at a rate of 4 mW/°C.

Insulation-Related and Safety-Related Specifications

Parameter	Symbol	Conditions	Value	Unit
Minimum External Air Gap, External Clearance	L(101)	Measured from input terminals to output terminals, shortest distance through air.	8.0	mm
Minimum External Tracking, External Creepage	L(102)	Measured from input terminals to output terminals, shortest distance path along body.	8.0	mm
Minimum Internal Plastic Gap, Internal Clearance	—	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.	0.5	mm
Tracking Resistance, Comparative Tracking Index	CTI	DIN IEC 112/VDE 0303 Part 1.	>175	V
Isolation Group	—	Material Group (DIN VDE 0110, 1/89, Table 1).	IIIa	—

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	+125	°C
Ambient Operating Temperature	T_A	–40	+110	°C
Junction Temperature	T_J	—	+125	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	6.0	V
Steady-State Input Voltage[a, b]	V_{IN+}, $V_{IN–}$	–2	V_{DD1} + 0.5	V
Two-Second Transient Input Voltage[c]	V_{IN+}, $V_{IN–}$	–6	V_{DD1} + 0.5	V
Digital Output Voltages	V_{OUT+}, $V_{OUT–}$	–0.5	V_{DD2}+0.5	V
Input Power Dissipation	P_{IN}	—	124	mW
Output Power Dissipation	P_O	—	72	mW
Total Power Dissipation	P_T	—	196	mW
Lead Solder Temperature	260°C for 10 seconds, 1.6 mm below seating plane			

a. DC voltage of up to –2V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.

b. Absolute maximum DC current on the inputs = 100 mA, no latch-up or device damage occurs.

c. Transient voltage of 2 seconds up to –6V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	+110	°C
V_{DD1} Supply Voltage[a]	V_{DD1}	3	5.5	V
V_{DD2} Supply Voltage	V_{DD2}	3	5.5	V
Analog Input Voltage[b]	V_{IN+}, V_{IN-}	–50	+50	mV

a. When V_{DD1} falls below 2.2V (supply lost), the device will stop functioning normally and trigger failsafe outputs.

b. ±50 mV is the nominal input range. The full scale input range (FSR) is ±80 mV; exceeding this range can cause output signal clipping. The functional input range is ±2V.

Electrical Specifications

Unless otherwise noted, T_A = –40°C to +110°C, V_{DD1} = 3V to 5.5V, V_{DD2} = 3V to 5.5V, V_{IN+} = –50 mV to +50 mV, and $V_{IN–}$ = 0V (single-ended connection).

Parameter	Symbol	Min.	Typ.[a]	Max.	Units	Test Conditions/Notes	Figure
DC Characteristics							
Input Offset Voltage	V_{OS}	–0.5	0	0.5	mV	T_A = 25°C	3, 4
Magnitude of Input Offset Change vs. Temperature	$\lvert dV_{OS}/T_A \rvert$	—	0.6	2.4	µV/°C	T_A = –40°C to +110°C; absolute value	5
Gain, ACPL-C72B, ±0.5%	G0	34.825	35	35.175	V/V	T_A = 25°C[b]	6, 7
Gain, ACPL-C72A, ±1%	G1	34.65	35	35.35	V/V	T_A = 25°C[b]	6, 7
Gain, ACPL-C720, ±3%	G2	33.95	35	36.05	V/V	T_A = 25°C[b]	6, 7
Magnitude of Gain Change vs. Temperature	dG/T_A	—	–0.003	—	V/V/°C	T_A = –40°C to +110°C[c]	8
Nonlinearity over ±50 mV Input Voltage	NL50	–0.036	0.03	0.092	%	V_{IN+} = –50 mV to +50 mV, T_A = 25°C[b]	9, 10
Magnitude of NL50 Change vs. Temperature	$dNL50/T_A$	—	0.00013	—	%/°C	T_A = –40°C to +110°C	11
Inputs and Outputs							
Full-Scale Differential Voltage Input Range	FSR	—	±80	—	mV	$V_{IN} = V_{IN+} – V_{IN-}$[d]	12
Input Bias Current	I_{IN+}	–170	–140	—	µA	V_{IN+} = 0V, $V_{IN–}$ = 0V[e]	13
Magnitude of I_{IN+} Change vs. Temperature	dI_{IN+}/T_A	—	65.5	—	nA/°C	—	—
Equivalent Input Impedance	R_{IN}	—	1.8	—	kΩ	V_{IN+} = 0V, $V_{IN–}$ = 0 V; single-ended	14
Common-Mode Input Overvoltage Detection Level	V_{CMINOV}	—	2	—	V	$V_{IN+} = V_{IN–}$, with reference to GND1	—
Output Common-Mode Voltage	V_{OCM}	1.438	1.5	1.589	V	V_{OUT+} or $V_{OUT–}$	—
Output Voltage Range in Normal Operation	V_{OUT}	—	0.1 to 2.9	—	V	V_{OUT+} or $V_{OUT–}$	12
Fail-Safe Differential Output Voltage	$V_{FAILSAFE}$	—	$–V_{DD2}$	$–V_{DD2+0.05}$	V	$V_{CMIN} \geq V_{CMINOV}$, or V_{DD1} < 2.2V	—
Output Short-Circuit Current	$\lvert I_{OSC} \rvert$	—	20	—	mA	V_{OUT+} or $V_{OUT–}$, shorted to GND2 or V_{DD2}	—
Output Resistance	R_{OUT}	—	0.92	—	Ω	V_{OUT+} or $V_{OUT–}$	—
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$	—	76	—	dB	[b]	—

Parameter		Symbol	Min.	Typ.[a]	Max.	Units	Test Conditions/Notes	Figure
AC Characteristics								
Signal-to-Noise Ratio		SNR	—	65	—	dB	V_{IN+} = 100 mVpp, 10 kHz sine wave	15, 16
Signal-to-Noise and Distortion Ratio		SNDR	—	63	—	dB	V_{IN+} = 100 mVpp, 10 kHz sine wave	15, 16
Small-Signal Bandwidth, –3 dB		f_{-3dB}	200	250	—	kHz	—	17, 18
Input to Output Propagation Delay	10%-10%	t_{PD10}	—	1.5	2.3	µs	50 mV/µs step input	19
	50%-50%	t_{PD50}	—	1.7	2.5	µs		
	90%-90%	t_{PD90}	—	1.9	3.0	µs		
Output Rise/Fall Time (10% to 90%)		$t_{R/F}$	—	1.2	—	µs	Step input	19
Common-Mode Transient Immunity		CMTI	15	25	—	kV/µs	V_{CM} = 1 kV; T_A = 25°C[b]	—
Power Supply Rejection		PSR	—	–78	—	dB	1 Vpp, 1 kHz sine wave ripple on V_{DD1}, differential output[f]	—
Power Supply								
Minimum Power Supply for Functional Operation		V_{DD1}	—	2.2	2.9	V	V_{DD2} = 3V to 5.5V[g]	—
Input-Side Supply Current		I_{DD1}	—	16	22.5	mA	V_{DD1} = 5V supply, V_{IN+} = 100 mV[h]	20
Output-Side Supply Current		I_{DD2}	—	9.5	13	mA	V_{DD2} = 5V supply	20
			—	9	12.5	mA	V_{DD2} = 3.3V supply	20

a. All typical values are under typical operating conditions at T_A = 25°C, V_{DD1} = 5V, V_{DD2} = 3.3V.

b. See Definitions.

c. The gain temperature drift can be normalized and expressed as the temperature coefficient of gain (TCG) of –86 ppm/°C.

d. When FSR is exceeded, outputs saturate.

e. Because of the switched-capacitor nature of the input sigma-delta converter, time-averaged values are shown.

f. Ripple voltage applied to V_{DD1} with a 0.1-µF bypass capacitor connected; differential amplitude of the ripple outputs measured. See Definitions.

g. Below this level, the differential output level may go to fail-safe mode.

h. The input supply current decreases as the differential input voltage ($V_{IN+} – V_{IN–}$) decreases.

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{rms}	RH ≤ 50%, t = 1 minute; T_A = 25°C	a, b
Input-Output Resistance	R_{I-O}	—	$>10^{12}$	—	Ω	V_{I-O} = 500 Vdc	c
Input-Output Capacitance	C_{I-O}	—	0.5	—	pF	f = 1 MHz	c

a. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics table.

b. The input-output momentary withstand voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics table and your equipment level safety specification.

c. This is a two-terminal measurement: pins 1–4 are shorted together, and pins 5–8 are shorted together.

Typical Performance Plots

Unless otherwise noted, T_A = 25°C, V_{DD1} = 5V, V_{DD2} = 3.3V.

Figure 3: Input Offset vs. Supply V_{DD1}

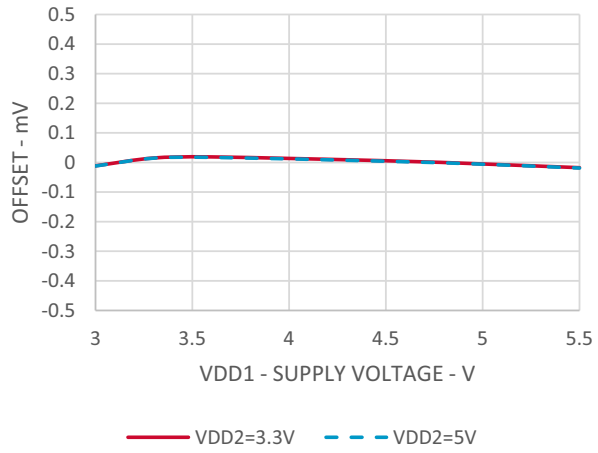


Figure 4: Input Offset vs. Supply V_{DD2}

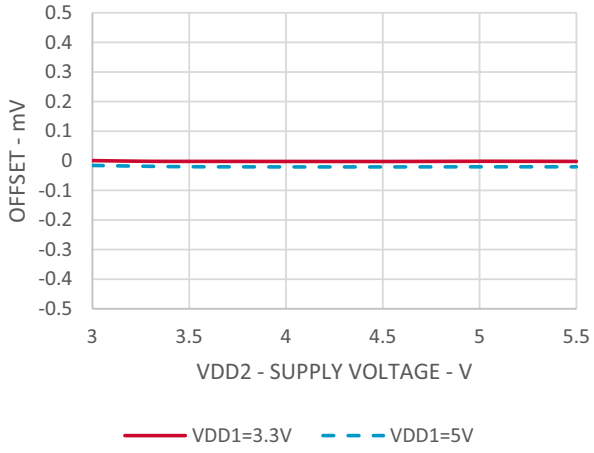


Figure 5: Input Offset vs. Temperature

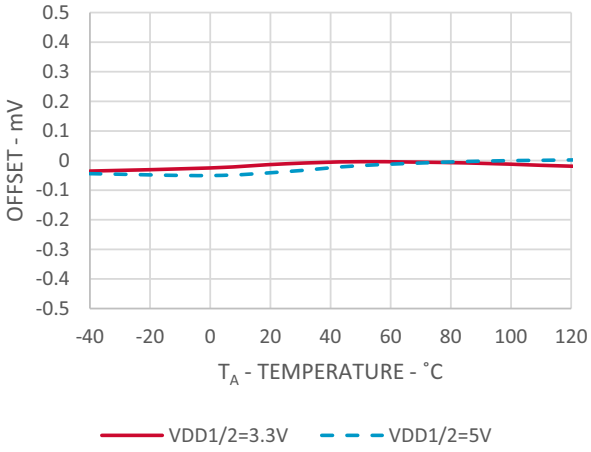


Figure 6: Gain vs. Supply V_{DD1}

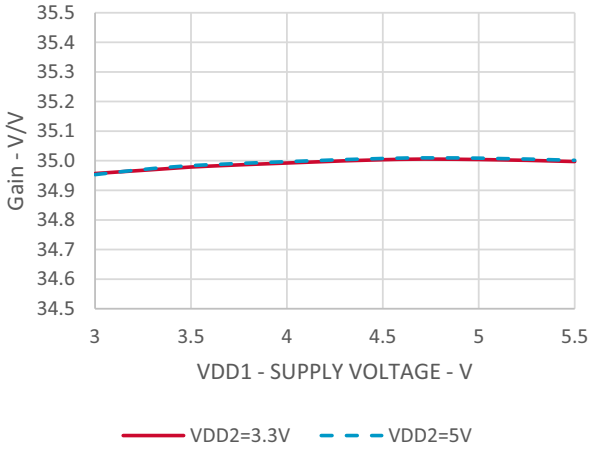


Figure 7: Gain vs. Supply V_{DD2}

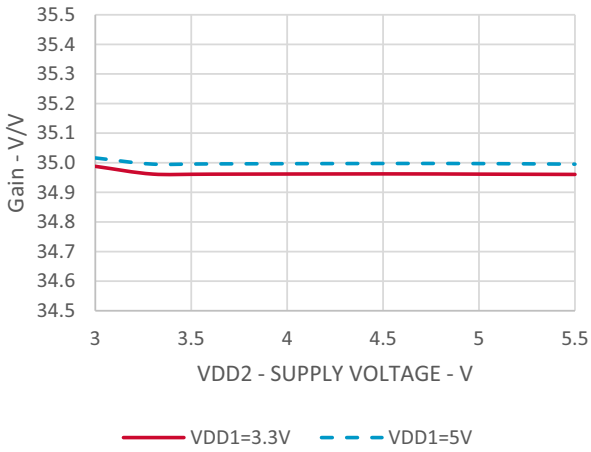


Figure 8: Gain vs. Temperature

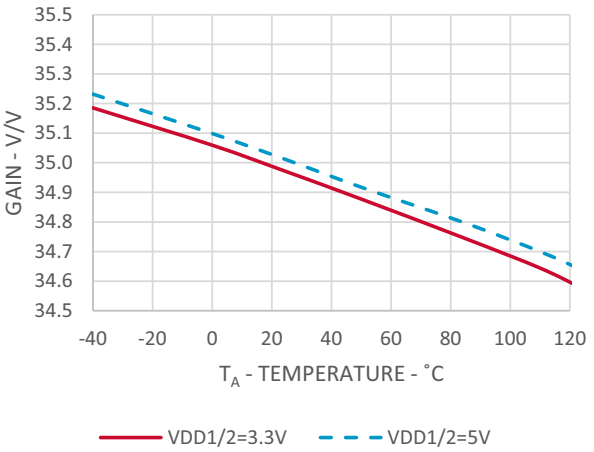


Figure 9: Nonlinearity vs. Supply V_{DD1}

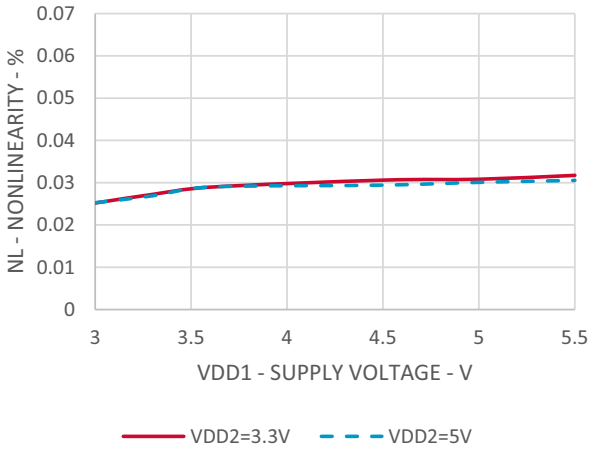


Figure 10: Nonlinearity vs. Supply V_{DD2}

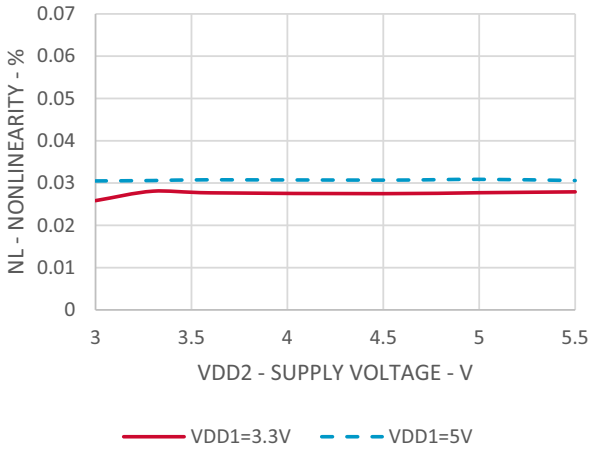


Figure 11: Nonlinearity vs. Temperature

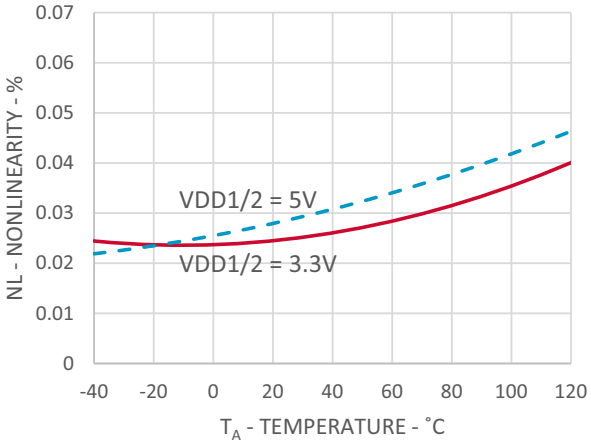


Figure 12: Output Voltage vs. Input Voltage

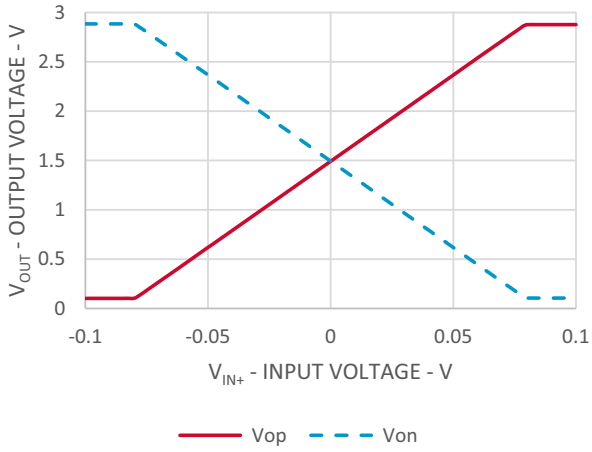


Figure 13: Input Current vs. Input Voltage

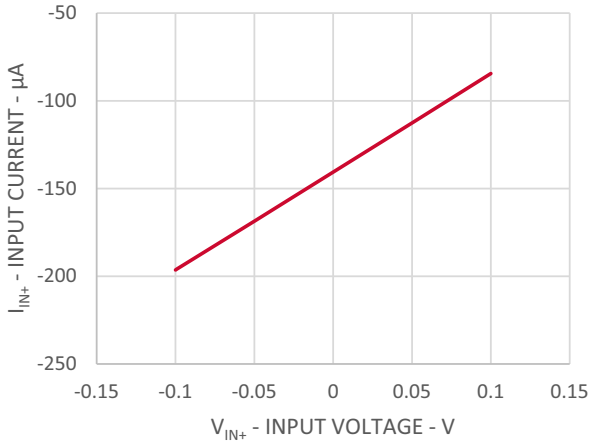


Figure 14: Input Impedance vs. Temperature

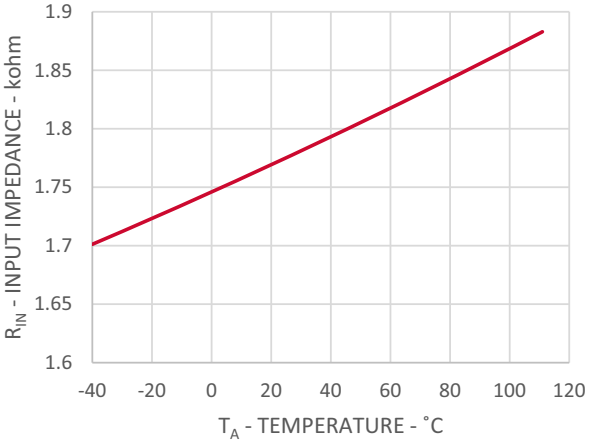


Figure 15: SNR, SNDR vs. Temperature

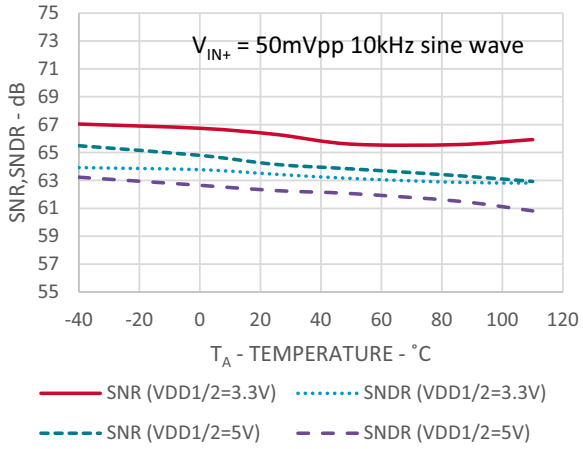


Figure 16: SNR, SNDR vs. Input Voltage

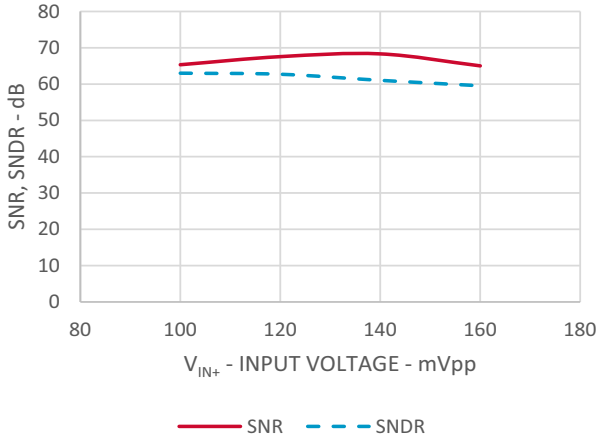


Figure 17: Gain Frequency Response

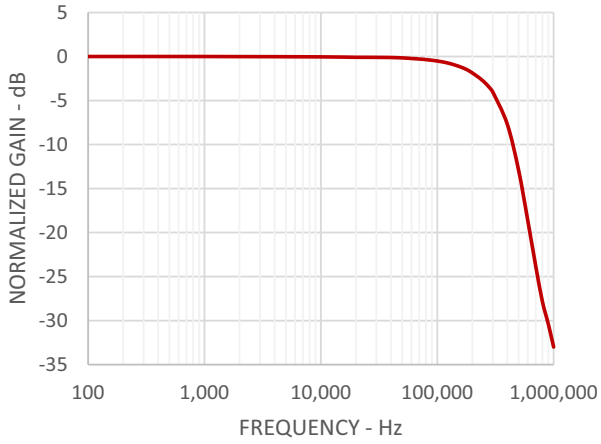


Figure 18: Phase Frequency Response

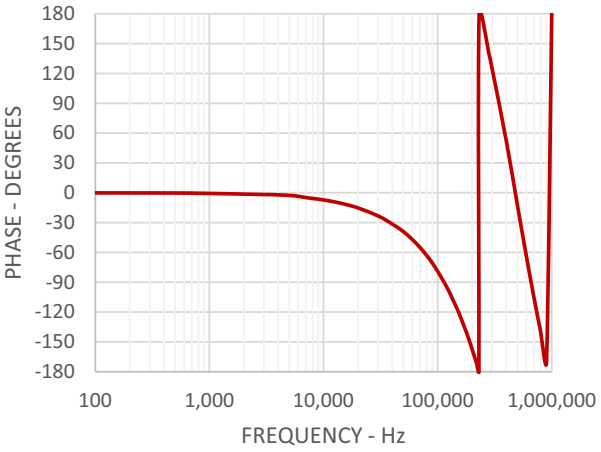


Figure 19: Propagation Delay, Output Rise/Fall Time vs. Temperature

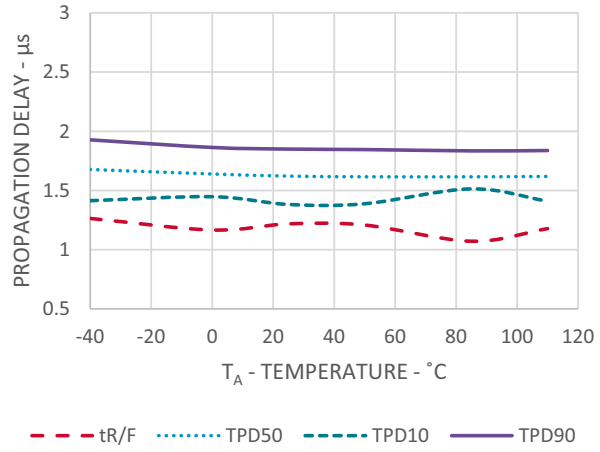
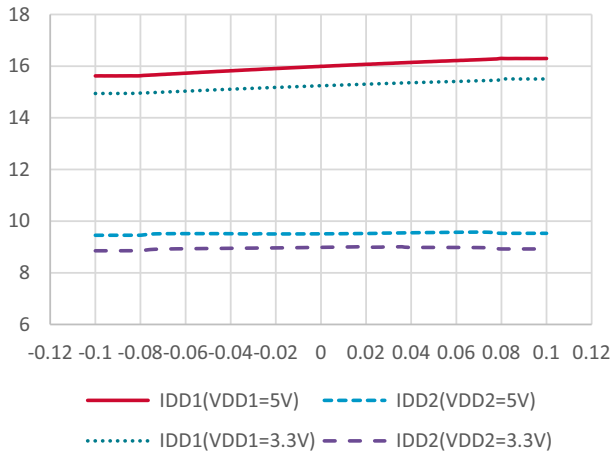


Figure 20: Supply Current vs Input Voltage



Definitions

Gain: The slope of the best-fit line of differential output voltage ($V_{OUT+} – V_{OUT–}$) vs. differential input voltage ($V_{IN+} – V_{IN–}$) over the nominal input range, with offset error adjusted out.

Nonlinearity: Half of the peak-to-peak output deviation from the best-fit gain line, expressed as a percentage of the full-scale differential output voltage.

Input DC Common-Mode Rejection Ratio, $CMRR_{IN}$: The ratio of the differential signal gain (signal applied differentially between pins V_{OUT+} and V_{OUT-}) to the input-side common-mode gain (input pins tied together and the signal applied to both inputs with respect to pin GND1), expressed in dB.

Common-Mode Transient Immunity, CMTI, Also Known as Common-Mode Rejection: CMTI is tested by applying an exponentially rising/falling voltage step on pin 4 (GND1) with respect to pin 5 (GND2). The rise time of the test waveform is set to approximately 50 ns. The amplitude of the step is adjusted until the differential output ($V_{OUT+} – V_{OUT–}$) exhibits more than a 200-mV deviation from the average output voltage for more than 1 µs. The ACPL-C72B/C72A/C720 will continue to function if more than 10-kV/µs common-mode slopes are applied, as long as the breakdown voltage limitations are observed.

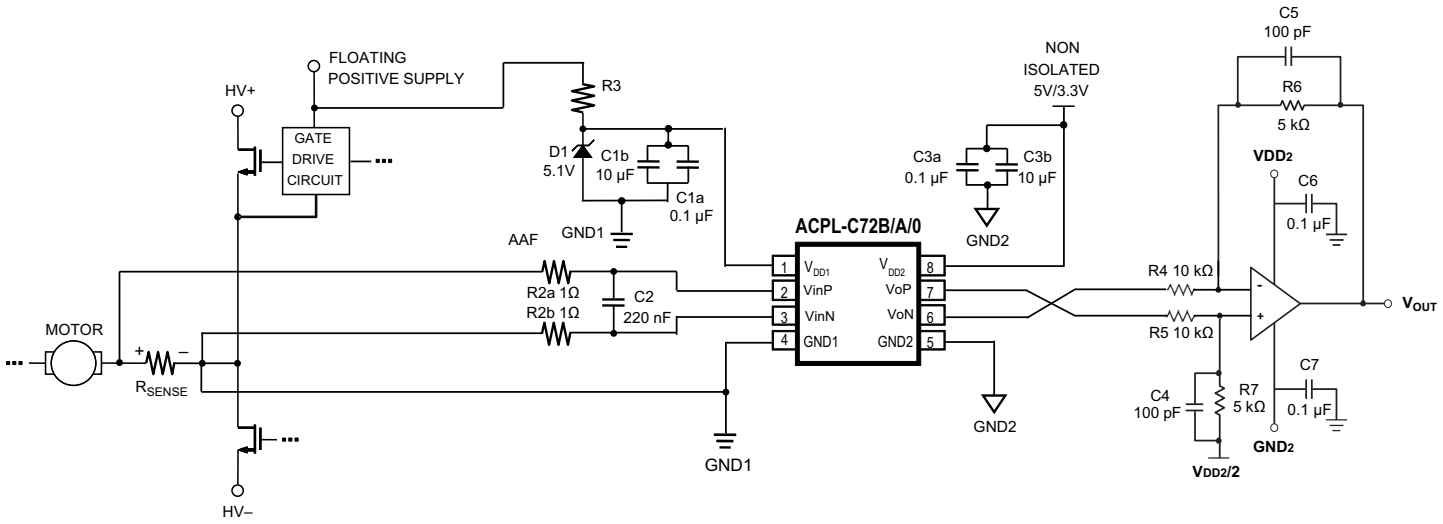
Power Supply Rejection, PSR: The ratio of the differential amplitude of the ripple outputs over the power supply ripple voltage, referred to the input, expressed in dB.

Application Information

Application Circuit

Figure 21 shows the typical application circuit. A floating power supply, which in many applications could be the same supply that is used to drive the high-side power transistor, is regulated to 5V using a simple Zener diode configuration. The voltage from the current sensing resistor, or shunt (R_{SENSE}), is applied to the input of the ACPL-C72B/C72A/C720 through an RC anti-aliasing filter (R2a, C2, R2b). The differential output of the isolation amplifier is converted to a ground-referenced single-ended output voltage with a simple differential amplifier circuit. Although the application circuit is relatively simple, follow these recommendations to ensure optimal performance.

Figure 21: Typical Application Circuit for Motor Phase Current Sensing



Power Supplies and Bypassing

As mentioned previously, an inexpensive Zener diode configuration can be used to reduce the gate-drive power supply voltage to 5V. To help attenuate high-frequency power supply noise or ripple, use a resistor or inductor in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

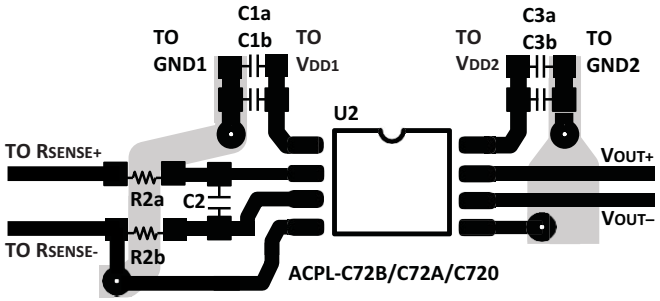
The power supply for the isolation amplifier is most often obtained from the same supply used to power the power transistor gate drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, use some sort of simple isolated supply, such as a line powered transformer or a high-frequency DC-DC converter.

As shown in Figure 21, 10 µF in parallel with 0.1-µF bypass capacitors (C1a, C1b) should be located as close as possible to the pins of the isolation amplifier. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolation amplifier. A 220-nF bypass capacitor (C2) is also recommended at the input pins due to the switched-capacitor nature of the input circuit. The input bypass capacitor also forms part of the anti-aliasing filter, which prevents high-frequency noise from aliasing down to lower frequencies and interfering with the input signal. The input filter also performs an important reliability function, reducing transient spikes from ESD events flowing through the current sensing resistor.

PC Board Layout

Ensure that the design of the printed circuit board (PCB) follows good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, and so on. In addition, the layout of the PCB can also affect the isolation transient immunity (CMTI) of the ACPL-C72B/C72A/C720, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMTI performance, lay out the PC board to minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the ACPL-C72B/C72A/C720. Figure 22 shows an example PCB layout.

Figure 22: Example Printed Circuit Board Layout



NOTE: The drawing is not to scale.

Shunt Resistor Selection

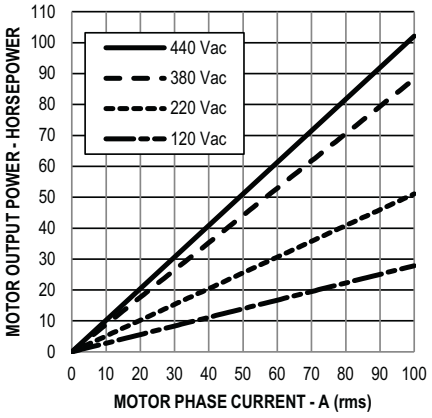
The current sensing resistor should have low resistance to minimize power dissipation, low inductance to minimize di/dt-induced voltage spikes that could adversely affect operation, and reasonable tolerance to maintain overall circuit accuracy. Choosing a particular value for the resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistance decreases power dissipation, whereas larger sense resistance can improve circuit accuracy by utilizing the full input range of the ACPL-C72B/C72A/C720.

The first step in selecting a sense resistor is determining how much current the resistor will be sensing. The graph in Figure 23 shows the RMS current in each phase of a three-phase induction motor as a function of average motor output power (in horsepower, hp) and motor drive supply voltage. The maximum value of the sense resistor is determined by the current being measured and the maximum recommended input voltage of the isolation amplifier. The maximum sense resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the sense resistor should see during normal operation.

Example: If a motor will have a maximum RMS current of 70 A_{rms} and can experience up to 50% overloads during normal operation, then the peak current is $70 \times 1.414 \times 1.5 = 150\ A_{pk}$.

Assuming a maximum input voltage of 50 mV, the maximum value of sense resistance in this case would be about 0.5 mΩ. Under overload conditions, the maximum input voltage will then be 150A × 0.5 mΩ = 75 mV, well within the ±80 mV FSR.

Figure 23: Motor Output Horsepower vs. Motor Phase Current and Supply Voltage



The maximum average power dissipation in the sense resistor can also be easily calculated by multiplying the sense resistance times the square of the maximum RMS current, which is about 2.45W in the previous example.

If the power dissipation in the sense resistor is too high, the resistance can be decreased below the maximum value to decrease power dissipation. The minimum value of the sense resistor is limited by precision and accuracy requirements of the design. As the resistance value is reduced, the output voltage across the resistor is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the sense resistor will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

When sensing currents large enough to cause significant heating of the sense resistor, the temperature coefficient (tempco) of the resistor can introduce nonlinearity due to the signal-dependent temperature rise of the resistor. The effect increases as the resistor-to-ambient thermal resistance increases. Minimize this effect by reducing the thermal resistance of the current sensing resistor or by using a resistor with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the current sensing resistor on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

For a two-terminal current sensing resistor, as the value of resistance decreases, the resistance of the leads becomes a significant percentage of the total resistance. This has two primary effects on resistor accuracy. First, the effective resistance of the sense resistor can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the leads during assembly, issues that will be discussed in more detail shortly. Second, the leads are typically made from a material, such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco overall.

Both of these effects are eliminated when a four-terminal current sensing resistor is used. A four-terminal resistor has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage.

Table 2 shows, as examples, several two-terminal and four-terminal surface-mount type shunt resistors from various suppliers that are suitable for sensing currents in motor drives up to 70 A_{rms} (71 hp or 53 kW).

Table 2: Example of Two-Terminal and Four-Terminal Shunt Resistors for Motor Drives up to 70 A_{rms}

Manufacturer / Shunt Resistor Part Number	Shunt Resistor Type	Shunt Resistance (mΩ)	Maximum RMS Current (A)	Motor Power Range 120 Vac to 440 Vac	
				hp	kW
KOA / CSR Series	Four-Terminal	5	7	1.8 to 6.7	1.4 to 5
Isabellenhütte / BVS Series	Two-Terminal				
Vishay / WSL4026 Series	Four-Terminal	2	17	4 to 17	3 to 13
Isabellenhütte / BVE Series	Two-Terminal				
KOA / PSG4 Series	Four-Terminal	1	35	9 to 36	7 to 27
KOA / PSB Series	Two-Terminal				
Isabellenhütte / BVR Series	Four-Terminal	0.5	70	19 to 72	14 to 54
KOA / PSJ2 Series	Two-Terminal				

When laying out a PC board for the current sensing resistors, a couple of points should be kept in mind. The Kelvin connections to the resistor should be brought together under the body of the resistor and then run very close to each other to the input of the ACPL-C72B/C72A/C720; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields interfering with the measured signal. If the sense resistor is not located on the same PC board as the isolation amplifier circuit, a tightly twisted pair of wires can accomplish the same result.

Also, multiple layers of the PC board can be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the sense resistor to help distribute the current between the layers of the PC board. The PC board should use 2-oz. or 4-oz. copper for the layers, resulting in a current carrying capacity in excess of 100A. Making the current carrying traces on the PC board fairly large can also improve the sense resistor's power dissipation capability by acting as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended.

Shunt Resistor Connections

Figure 21 shows the typical method for connecting the ACPL-C72B/C72A/C720 to the current sensing resistor. V_{IN+} (pin 2) is connected to the positive terminal of the sense resistor, while V_{IN-} (pin 3) is shorted to GND1 (pin 4), with the power-supply return path functioning as the sense line to the negative terminal of the current sense resistor. This allows a single pair of wires or PC board traces to connect the isolation amplifier circuit to the sense resistor. By referencing the input circuit to the negative side of the sense resistor, any load-current-induced noise transients on the resistor are seen as a common-mode signal and will not interfere with the current sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current sensing resistor.

If the same power supply is used for both the gate drive circuit and the current sensing circuit, it is very important that the connection from GND1 of the ACPL-C72B/C72A/C720 to the sense resistor be the *only* return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the ACPL-C72B/C72A/C720 circuit and the gate drive circuit should be the positive power supply line.

Output Side

The op-amp used in the external post-amplifier circuit should be of sufficiently high precision so that it does not contribute a significant amount of offset or offset drift relative to the contribution from the isolation amplifier. Generally, op-amps with bipolar input stages exhibit better offset performance than op-amps with JFET or MOSFET input stages.

In addition, the op-amp should also have enough bandwidth and slew rate so that it does not adversely affect the response speed of the overall circuit. The post-amplifier circuit includes a pair of capacitors (C4 and C5) that form a single-pole low-pass filter; these capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier.

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and adequate gain tolerance for the overall circuit. Resistor networks can be used that have much better ratio tolerances than can be achieved using discrete resistors. A resistor network also reduces the total number of components for the circuit as well as the required board space.