



ACPL-355JC

Wolfspeed FM3 SiC Module Half-Bridge Evaluation Board

**Reference Manual
Version 1.0**

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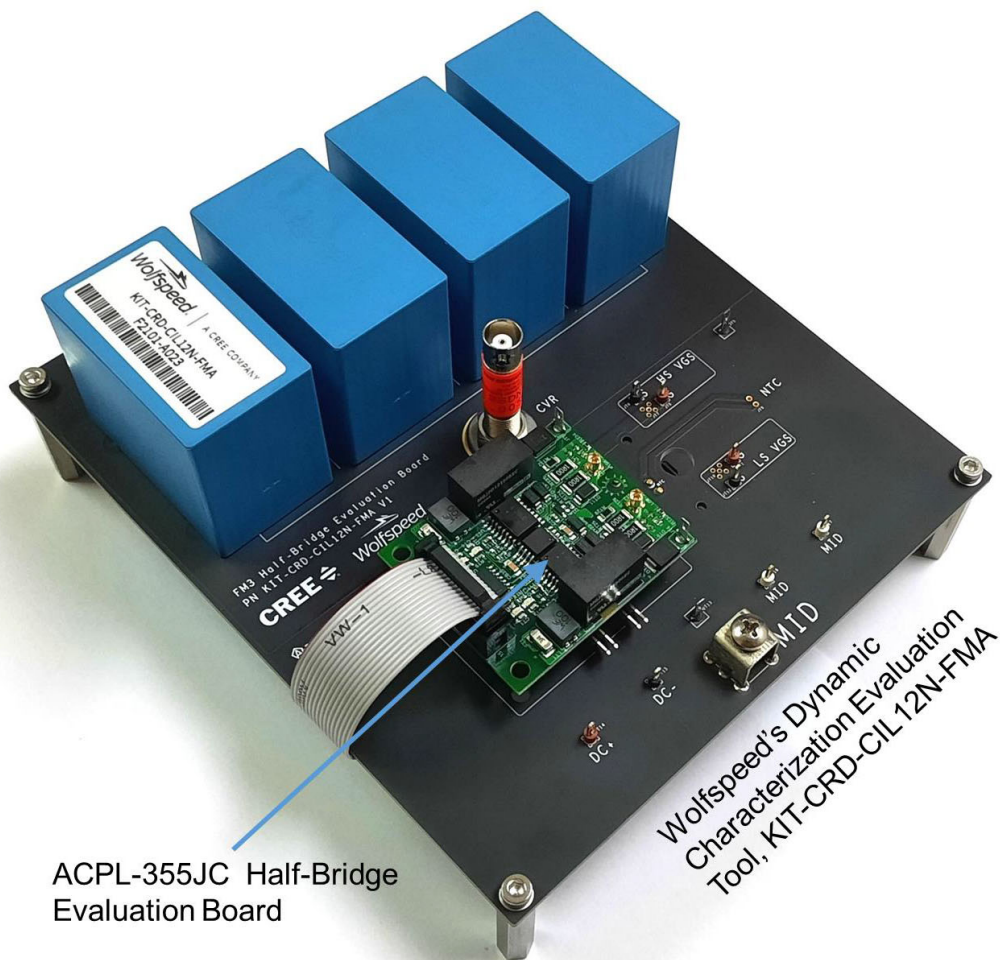
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Wolfspeed FM3 SiC Module Half-Bridge Evaluation Board

1 Introduction

The half-bridge evaluation board features the Broadcom® dual output isolated gate drive optocouplers, ACPL-355JC. The board drives the Wolfspeed SiC MOSFET module in FM3 housing. It also features precision optically isolated amplifiers, ACPL-C87B, used for the module temperature measurements. The evaluation board, shown in [Figure 1](#), is to be used in with Wolfspeed's dynamic characterization evaluation tool, KIT-CRD-CIL12N-FMA. The ACPL-355JC evaluation board and the clamped inductive load (CIL) test circuit with current measurement provide a high-speed, low-inductance test fixture for double pulse and short-circuit testing.

Figure 1: ACPL-355JC Wolfspeed FM3 SiC Module Half-Bridge Evaluation Board



1.1 Design Features

The half-bridge evaluation board has the following features:

- Two ACPL-355JC gate drive optocouplers:
 - 10A peak output current
 - 100 kV/ μ s common mode rejection
 - $V_{IORM} = 2262 V_{PK}$ with CTI > 600V
 - Short-circuit or overcurrent (OC) protection (or DESAT)
 - Soft shutdown during fault
 - Two isolated feedback signals, FAULT (for short circuit) and UVLO
- One ACPL-C87B optically isolated amplifiers for temperature measurement:
 - 0 to 2V nominal input range
 - 100-kHz bandwidth
 - 3 V to 5.5V wide supply range for output side
 - 15 kV/ μ s common-mode transient immunity
- Electrically and mechanically suitable for dynamic characterization evaluation tool, KIT-CRD-CIL12N-FMA
- With adjustment of the OC protection and gate resistors, the evaluation board supports the following FM3 MOSFET modules:
 - CAB011M12FM3
 - CAB016M12FM3

2 Board Description

2.1 Functional Block Diagram

The functional block diagram and disposition of the functional blocks of the half-bridge evaluation board are shown in [Figure 2](#) and [Figure 3](#). The block diagram shows the different functional blocks:

- Power management:
 - +12V VIN power supply connector
 - +15V/–4V derived from isolated DC-DC converter and linear regulator
 - +5V LDO
- High and low side ACPL-355JC gate drivers
- Temperature measurement ACPL-C87B
- User interface connector, JT1
- High and low side gate/source (JB2 and JB3) and short-circuit (JT4 and JT5) connectors to KIT-CRD-CIL12N-FMA

Figure 2: Half-Bridge Evaluation Board Functional Block Diagram

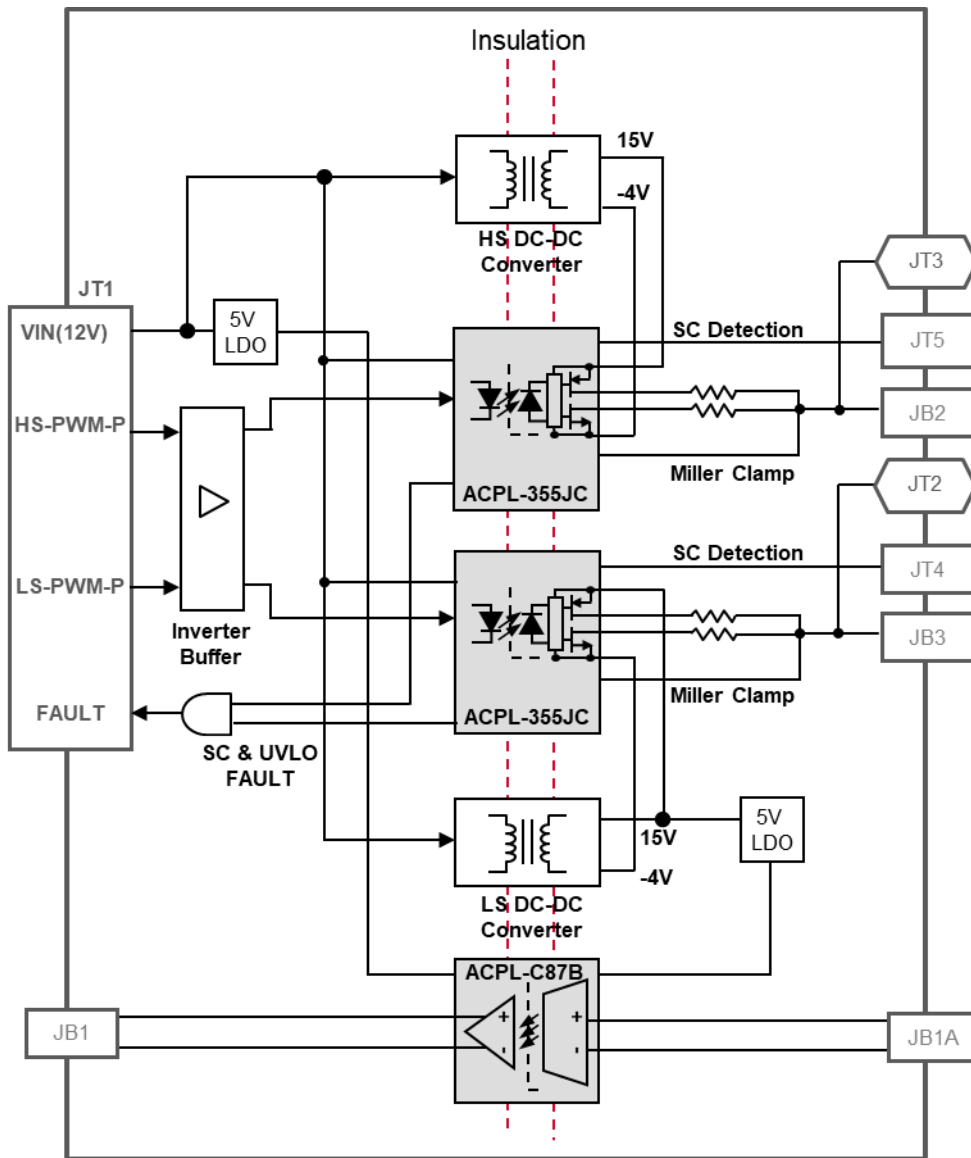
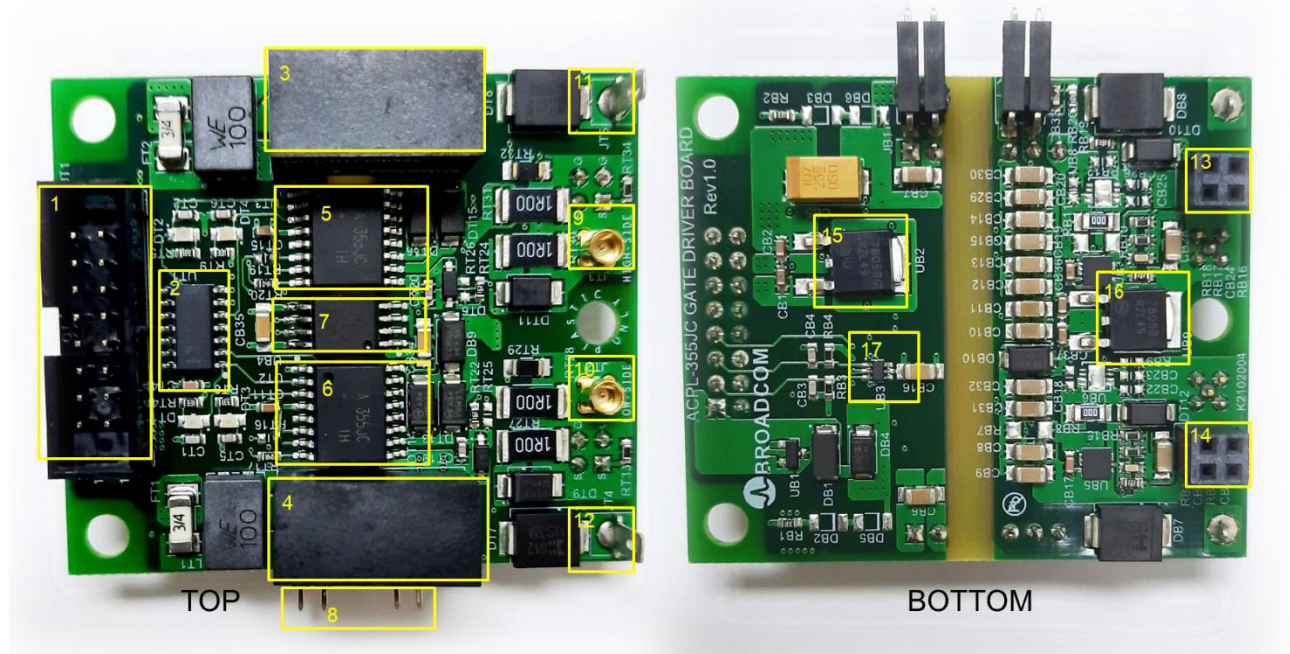


Figure 3: Functional Block Disposition on the Evaluation Board



According to [Figure 3](#), the marked functional blocks are as follows:

1. User interface connector, JT1
2. AND gate for combining the multiple faults to a single FAULT signal
3. High side DC-DC converter
4. Low side DC-DC converter
5. High side SiC driver based on ACPL-355JC
6. Low side SiC driver based on ACPL-355JC
7. Temperature measurement based on ACPL-C87B
8. Temperature measurement input (JB1A) and output (JB1) connectors
9. High side SiC V_{GS} probe test point, JT3
10. Low side SiC V_{GS} probe test point, JT2
11. High side SiC drain connector for short circuit detection, JT5
12. Low side SiC drain connector for short circuit detection, JT4
13. High side SiC V_{GS} to KIT-CRD-CIL12N-FMA connector
14. Low side SiC V_{GS} to KIT-CRD-CIL12N-FMA connector
15. Primary side 5V LDO for ACPL-355JC and ACPL-C87B
16. Secondary side 5V LDO for ACPL-C87B
17. PWM inverter buffering

2.2 Key Specifications

Absolute maximum ratings of the evaluation board are listed in [Table 1](#). Note that this table contains only key parameters. Constraints from ACPL-355JC and ACPL-C87B, as well as specification of other key components, must be considered when the evaluation board is used.

Table 1: Absolute Maximum Ratings

Parameter	Values			Units	Note
	Min.	Typ.	Max.		
VIN Input Voltage	10.8	12	13.2	V	External DC input power supply for digital circuitry and DC-DC converter.
PWM Logic Input Level	0	3.3	5	V	External PWM inputs for gate drivers.
Gate Drivers Peak Output Current	—	—	10	A	The current must be limited by external gate resistors, refer to the ACPL-355JC data sheet.
FAULT Logic Output Level	0	—	5	V	Logic output signal, refer to the ACPL-355JC data sheet.
Temperature Measurement	0	—	5	V	Single-ended analog output signal.

2.3 Pin Assignment

Pin assignments for JT1 connector are shown in [Table 2](#).

Table 2: Pin Assignment of Connector JT1 (User Interface Connector)

Label	Pin	Function	Direction
VIN	1	12V power supply. The 12V is used with the DC-DC converter, MGJ2D121505SC, to provide isolated power supply for the secondary side.	Input
0 (GND)	2, 8, 10, 12, 14, 16	Reference ground for the 12V power supply and primary side.	Input
HS-PWM-P	3	3.3V/5V PWM input signal for the high side driver.	Input
LS-PWM-P	5	3.3V/5V PWM input signal for the low side driver.	Input
FAULT	7	5V single FAULT signal combining secondary side high and low UVLO and short circuit fault signals.	Output
NC	4, 6, 9, 11, 13, 15	No connection.	N/A

Pin assignment for gate drivers and short circuit detection is shown in [Table 3](#).

Table 3: Pin Assignment for Gate Drivers and Short-Circuit Detection

Label	Function	Direction
JB2, JB3	ACPL-355JC gate driver outputs for the gate and source of high and low side SiC MOSFETs.	Output
JT4, JT5	ACPL-355JC OC inputs to be connected to the drain of the SiC MOSFETs. These inputs measure the drain and source voltage of the SiC MOSFETs for short-circuit (SC) detection.	Input
JT2, JT3	MMCX connectors for probing of the high and low side V_{GS} .	Output

Pin assignment for temperature measurement is shown in [Table 4](#).

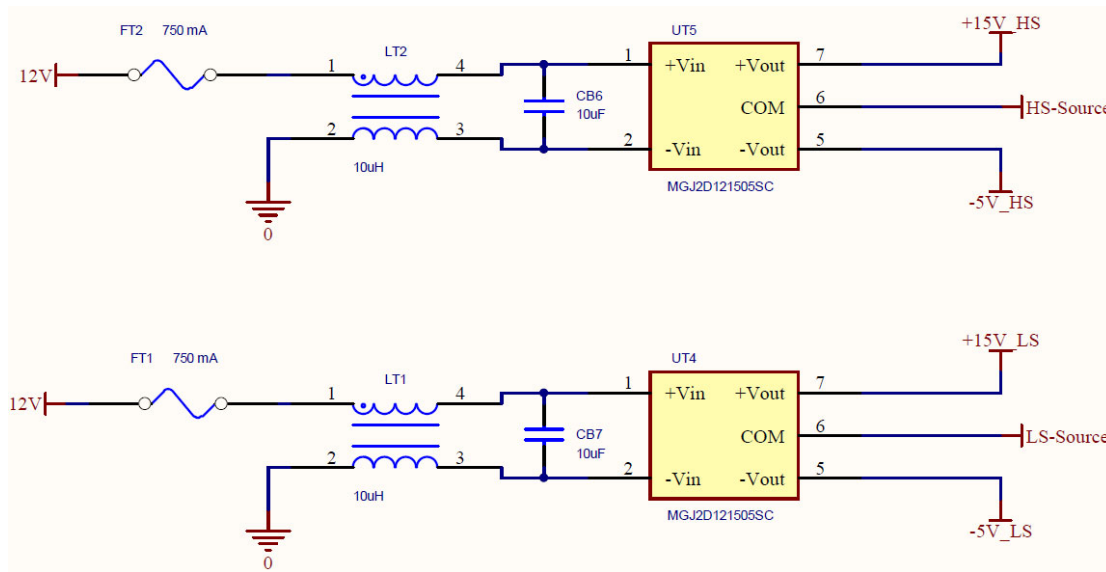
Table 4: Pin Assignment for Temperature Measurement

Label	Function	Direction
JB1A	Connects the NTC terminals of the SiC modules to the isolated voltage sensor ACPL-C87B for temperature measurement.	Input
JB1	Isolated differential outputs from the ACPL-C87B temperature measurement.	Output

3 Circuit Description

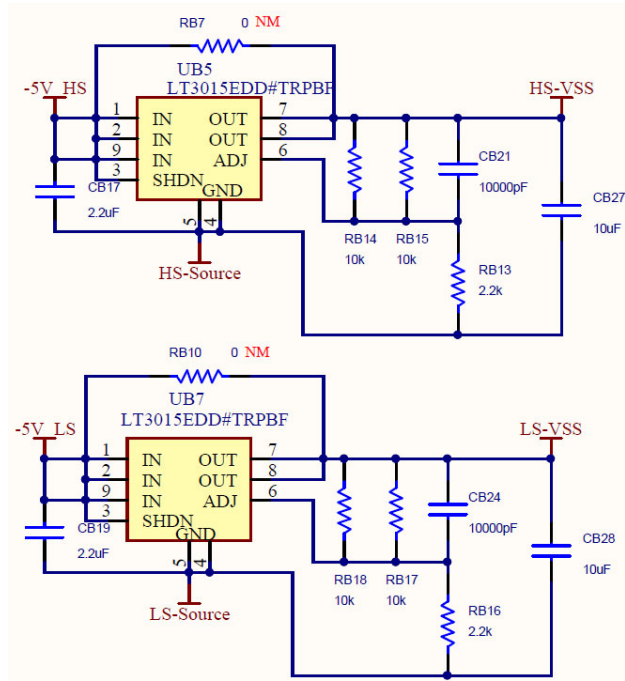
3.1 Power Management

Figure 4: Schematic of the Isolated Power Supplies for the Secondary Side



Two DC-DC converters, MGJ2D121505SC, convert the primary 12V input power supply to isolated secondary supplies for the high and low side. MGJ2D121505SC is a 2W, 5.2 kVDC DC-DC converter that converts the 12V input voltage to +15/-5V for the bidirectional drive of the gate of the SiC.

Figure 5: Schematic of the Negative Gate Voltage Power Supplies

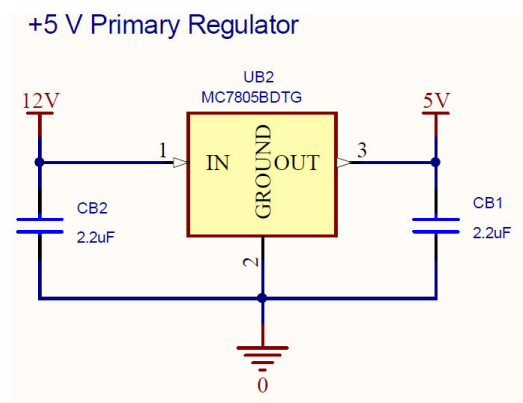


The -5V from the DC-DC converters is further regulated by UB5 and UB7 to achieve -4V gate voltage for switching off of the SiC as recommended by CAB016M12FM3 data sheet.

These negative supply voltages, HS-VSS and LS-VSS, can be derived by the following equation.

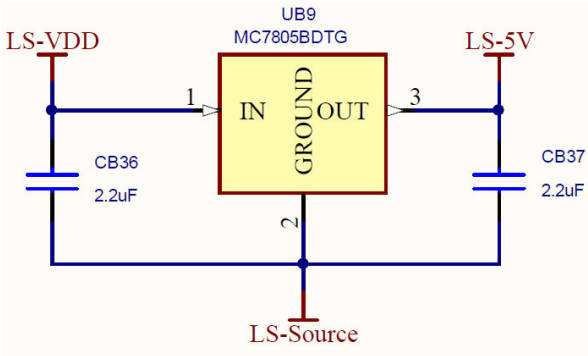
$$\begin{aligned}
 \text{HS-VSS} &= [1 + (\text{RB14} / \text{RB15}) / \text{RB13}] \times -1.22 \\
 &= [1 + 5 / 2.2] \times -1.22 \\
 &= -4\text{V}
 \end{aligned}$$

Figure 6: Schematic of the Primary Side 5V Power Supply



UB2 is a 5V LDO that converts the primary 12V input to 5V output, for the primary side supplies of the gate drivers, ACPL-355JC and ACPL-C87B.

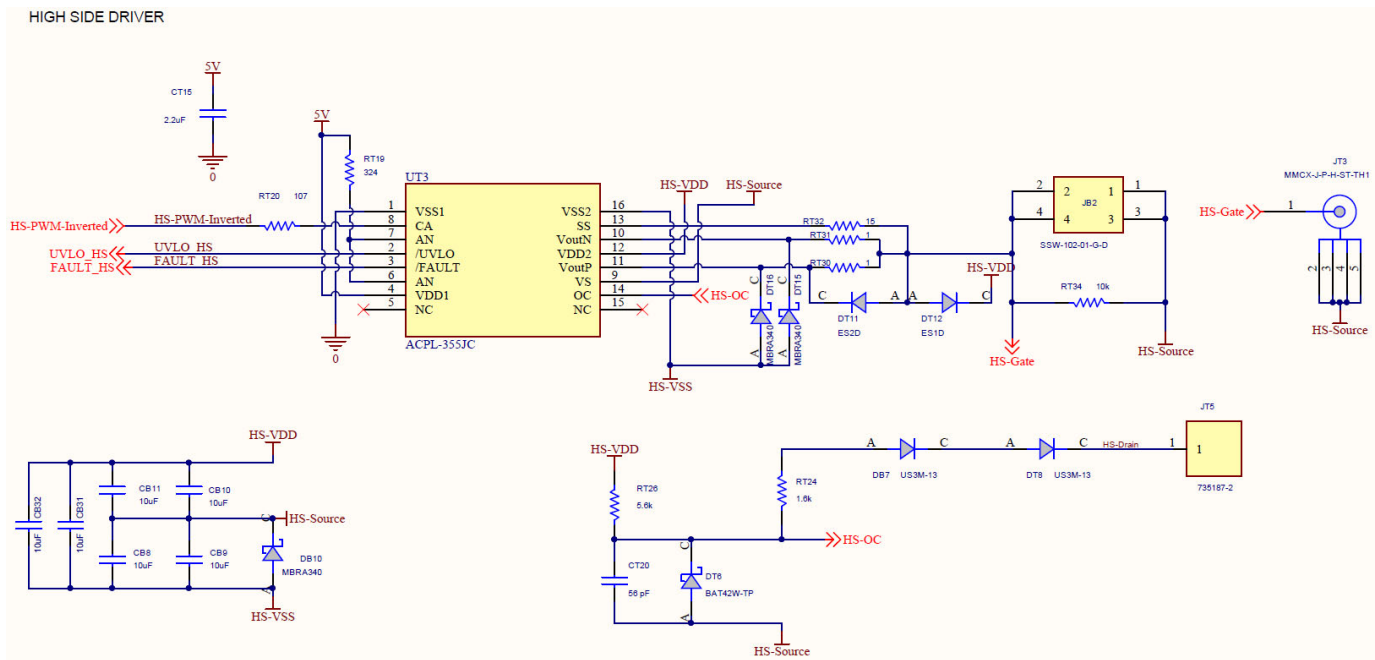
Figure 7: Schematic of the Secondary Side 5V Power Supply



UB9 is a 5V LDO that converts the isolated secondary, low side 15V to 5V, for the secondary side power supply of the ACPL-C87B.

3.2 Gate Driver Circuit

Figure 8: ACPL-355JC Gate Driver Circuitry

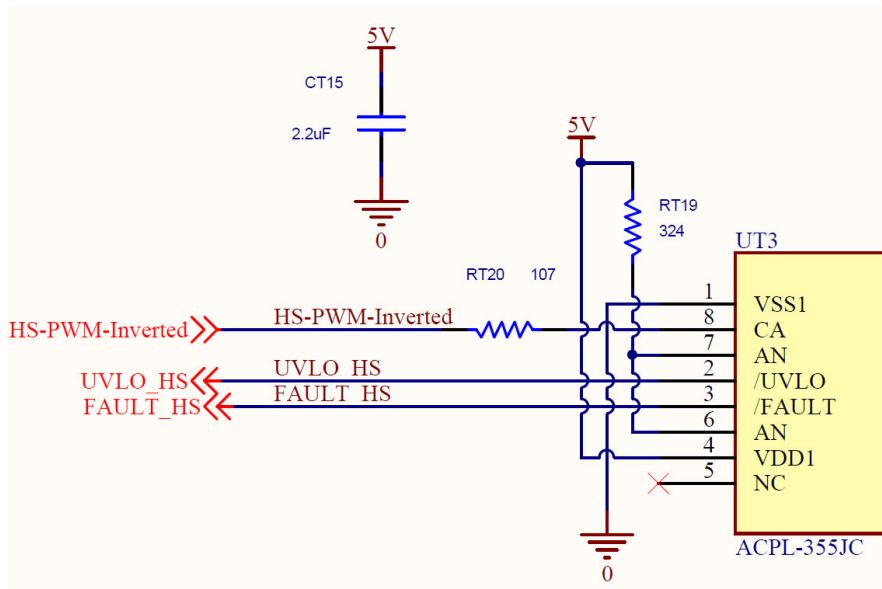


The ACPL-355JC, which has a maximum peak output current of 10A, can drive most of the power IGBT/MOSFET switches directly without an external push-pull stage. This driver contains an LED, electrically isolated and optically coupled to an integrated circuit, on the gate driver high-voltage side, with two power output stages with the CLAMP function to prevent the parasitic turn-on due to the parasitic Miller current during turn-off transient. Other features include undervoltage, short-circuit protection, and as well as soft shut down during short-circuit fault.

The ACPL-355JC has a propagation delay of less than 150 ns. The very high common mode rejection (CMR) of 100 kV/ μ s (minimum) is required to isolate high transient noise during the high-frequency operation from causing erroneous outputs. It is certified by UL1577 for up to V_{ISO} 5000 V_{RMS}/min and IEC 60747-5-5 for working voltage, V_{IORM} up to 2262 V_{PEAK} . It is housed in an SO16 package with molding compound, CTI of more than 600V, which reduces the creepage distance requirement.

3.3 Gate Driver Circuit, Primary Side

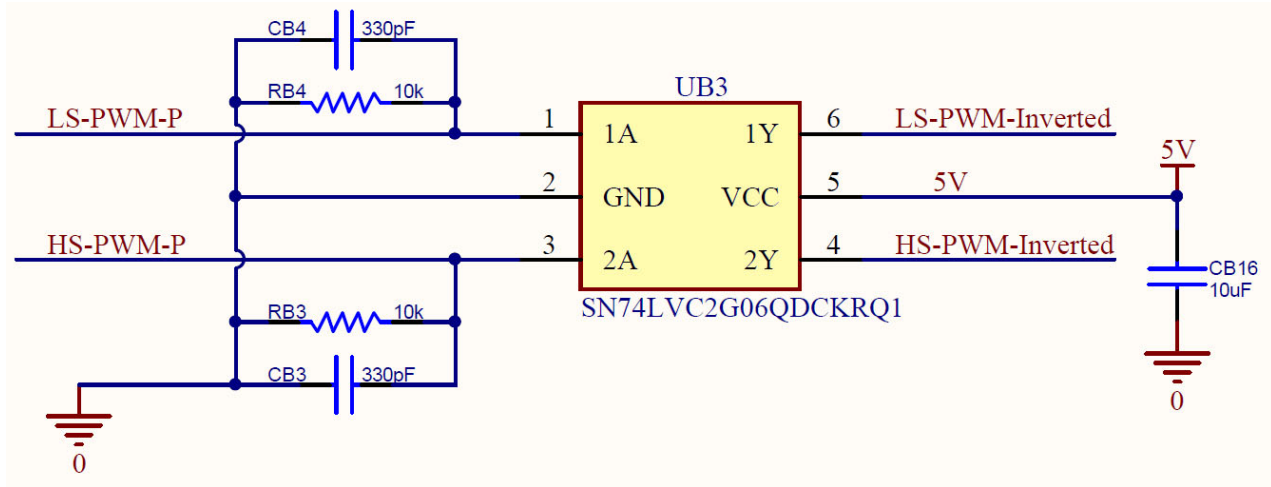
Figure 9: ACPL-355JC Gate Driver Circuitry, Primary Side



Low voltage side of the gate drive circuitry contains the power supply for the ACPL-355JC, the LED anode and cathode, and the safety reporting signals (FAULT and UVLO).

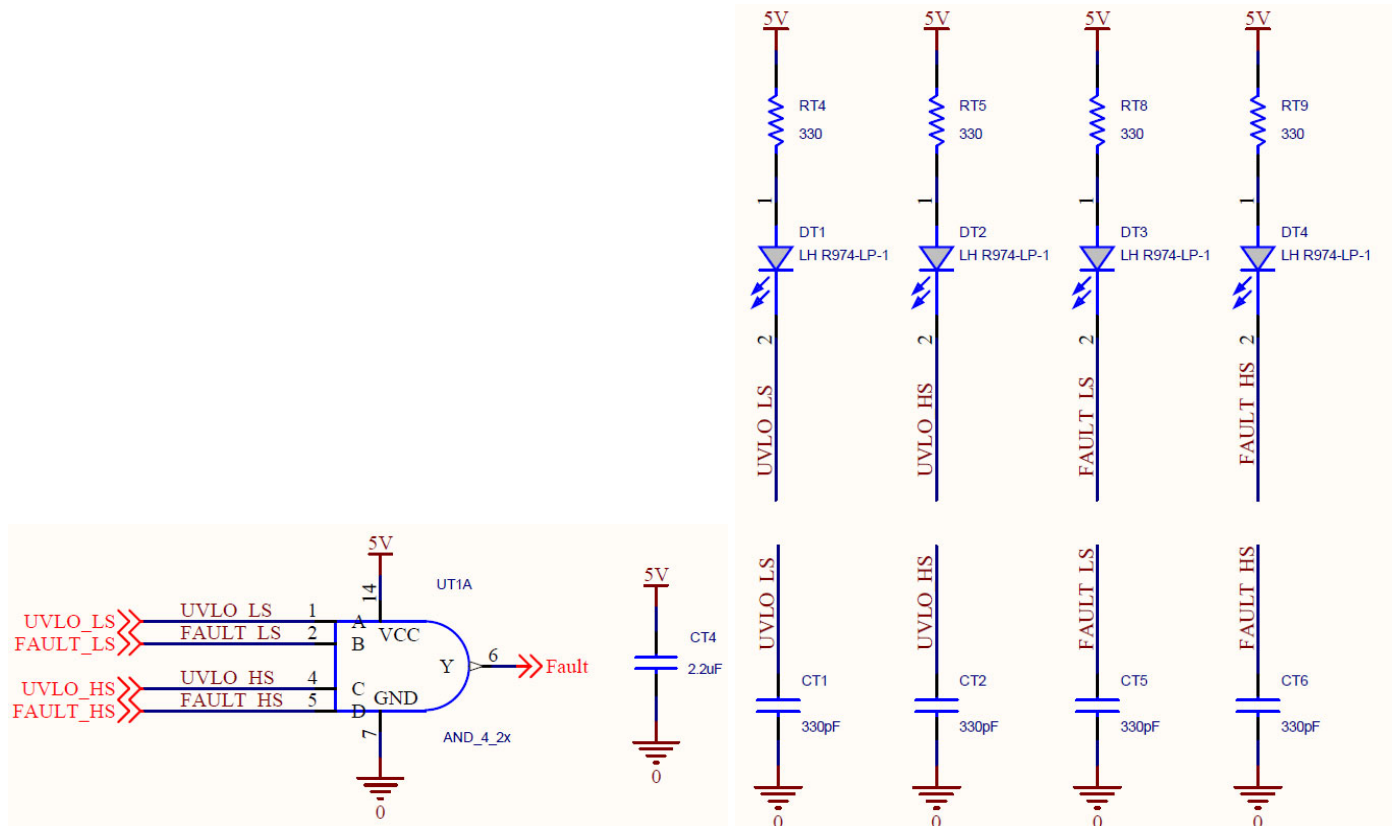
The resistor responsible for the LED forward current setting is split in two. These resistors, RT19 and RT20, are placed at the anode pins 6 and 7 and cathode pin 8 to balance the common mode impedances at the LED's anode and cathode. This helps to equalize the common mode voltage change.

Figure 10: ACPL-355JC Gate Driver Circuitry, PWM Buffer



External PWM signals that propagate through the user interface connector are buffered, as shown above. The buffer features an open drain inverter output, which pulls low when the input of the buffer is high.

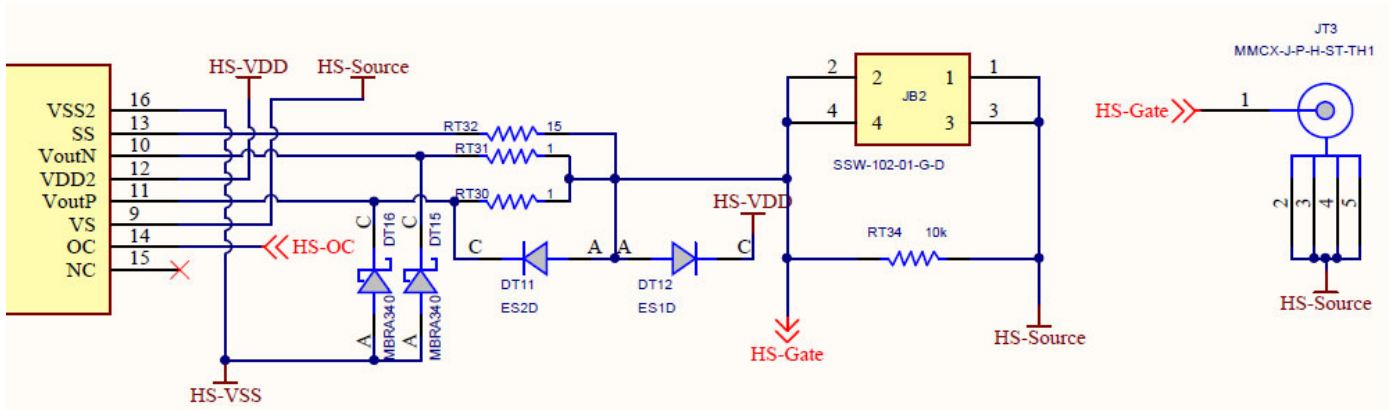
Figure 11: ACPL-355JC Gate Driver Circuitry, FAULT Reporting



The ACPL-355JC has two open drain, UVLO and short-circuit FAULT output signals. Logic for these signals is inverted so they are suitable for wired OR applications. The FAULT signals from both drivers are combined using an AND gate, so the user is notified when either FAULT or UVLO has occurred, from either the high or low side SiC MOSFET.

3.4 Gate Driver Circuit, Secondary Side

Figure 12: ACPL-355JC Gate Driver Circuitry, Secondary Side



When the gate driver input is set to high, the VOUTP becomes high and +15V is supplied to the MOSFET gate through RT30. When the gate driver input is set to low, VOUTN pin becomes active and -4V is supplied to the MOSFET gate through RT31 resistor. These voltages are referred to the source of respective MOSFET. The switching time is determined by gate charging and discharging process. Smaller gate resistors lead to the higher peak gate current, which decreases turn-on and turn-off time, subsequently reducing switching losses. However, too small gate resistors may introduce voltage spikes and current oscillations on MOSFET or can overload the gate driver IC. For the proper selection of the gate resistors, several criteria must be fulfilled.

To limit the gate peak current, MOSFET internal R_{Gint} must be considered when calculating ideal value for gate resistor, and internal minimum turn on resistance of driver R_{VOUTP} . The ACPL-355JC data sheet provides the equation for the gate resistor calculation.

$$R_G \geq \frac{V_{DD2} - V_{SS2}}{I_{O(PEAK)}} - R_{Gint} - R_{VOUTP}$$

The next step in choosing the correct gate resistor is to check the power dissipation of the ACPL-355JC gate driver. If the power dissipation is too high, increase the resistance of the gate resistor. For details for choosing the gate resistor, refer to the ACPL-355JC data sheet.

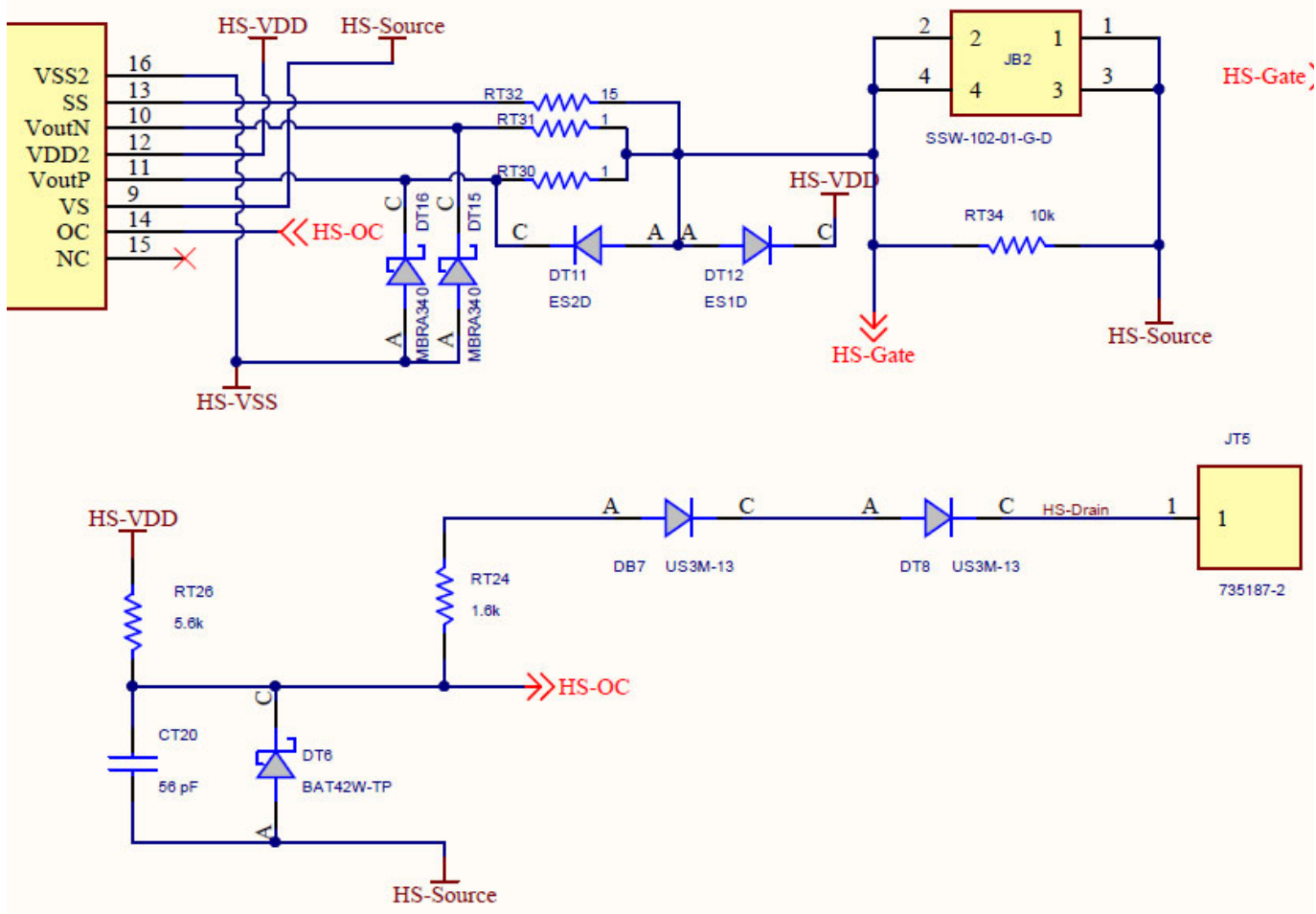
Finally, switching performance, especially turn-off speed, must be measured because the fast-switching transients in combination with parasitic inductances in the switching loop can generate high overvoltages and oscillations.

To ensure the constraints described previously during the worst-case conditions are met, the board comes with 1Ω/1.5W gate resistors for positive and negative gating. Based on CAB016M12FM3's R_{GINT} of 2.4Ω, the ACPL-355JC's R_{VOUTP} of 0.7Ω and external R_G of 1Ω, the peak gate current is estimated to be 4.6A when +15V/-4V supply is applied.

Additionally, diode DT11, placed between gate and VOUTP pin, is used together with CLAMP function to shunt parasitic Miller current during the off cycle.

Schottky diodes, DT15 and DT16, prevent false output if VOUTP and VOUTN are driven more negative than the -4V negative supply during fast-switching transients.

Figure 13: ACPL-355JC Gate Driver Circuitry, Secondary Side Short Circuit Detection

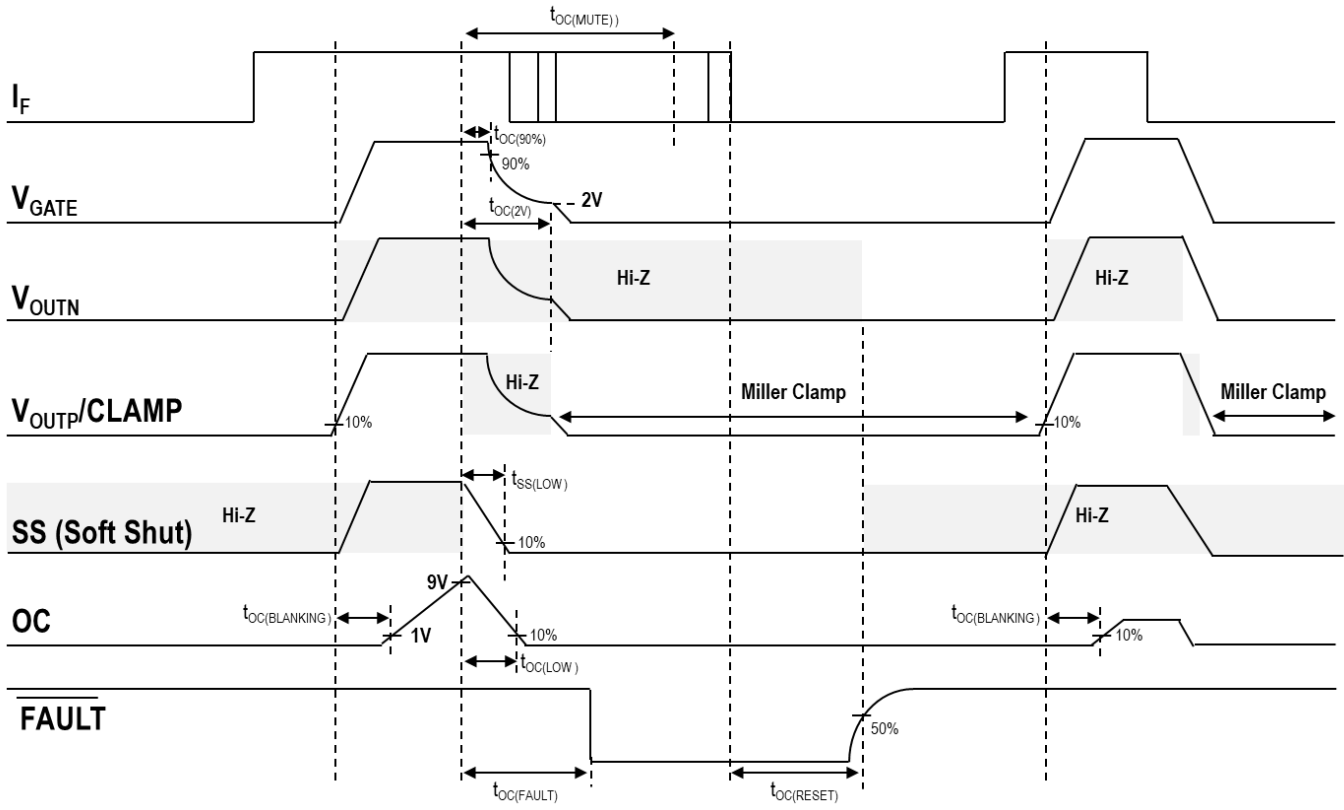


The ACPL-355JC OC pin 14 monitors the MOSFET drain-source voltage. This short-circuit fault-detection circuitry must remain disabled for a short period of time following the turn-on of the MOSFET to allow the drain-source voltage to settle down and fall below the OC threshold. This period, called the blanking time, can be adjusted by the blanking capacitor, CT20 and resistor RT26, which controls the charging time of the blanking capacitor from HS-VDD. The combination of 56 pF and 5.6 kΩ allows the entire short-circuit duration to be a soft shutdown with 1 μs.

When the OC fault is detected and the blanking time has passed, both VOUTP and VOUTN go low and soft shutdown starts. The soft shutdown resistor RT32 controls shutting down the speed of the short-circuit current to prevent high dv/dt spike across the V_{DS} of the SiC.

When OC conditions are met, internal feedback channel is activated, which brings the FAULT output from high to low. When the fault is detected, VOUTP and VOUTN are set to High-Z state for t_{OC(MUTE)} time. After this time, the LED input must be kept low for t_{OC(RESET)} before the fault condition is cleared. The FAULT status returns to high and the LED input must be kept low for another t_{OC(RESET)}.

Figure 14: ACPL-355JC Output Behaviors during Short Circuit Detection and Soft Shutdown



Negative voltage spikes are typically generated by inductive loads, or reverse recovery spikes of the IGBT/MOSFET free-wheeling diodes can bring the OC pin voltage below the reference ground, HS-Source, the threshold thus generating a false fault signal. To prevent this, the Schottky diodes DT6 are placed across the OC and the HS-Source. The Schottky diodes prevent forward biasing of the substrate diode of the gate driver optocoupler.

Figure 16: Waveforms of the Double Pulse Test Performed on the Evaluation Board with CAB016M12FM3

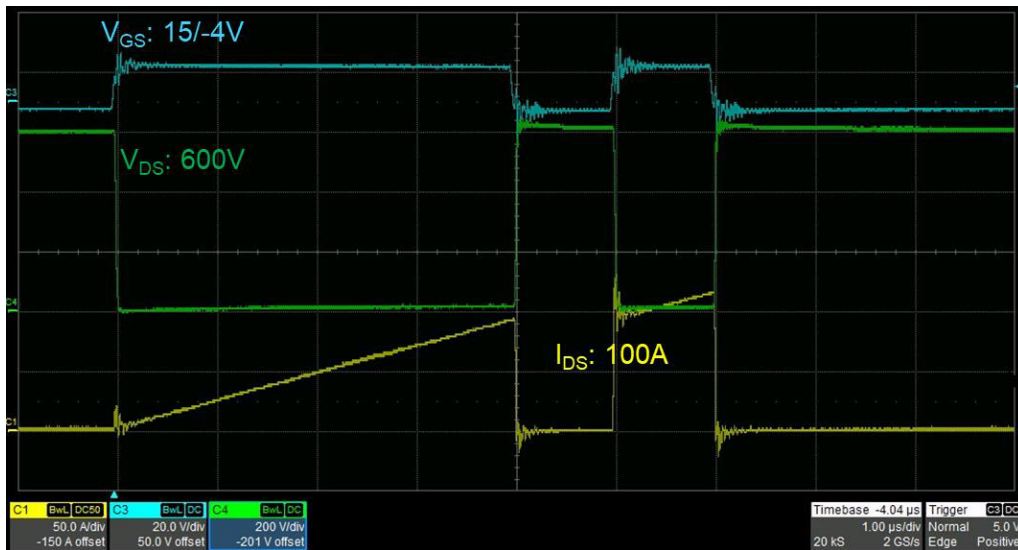
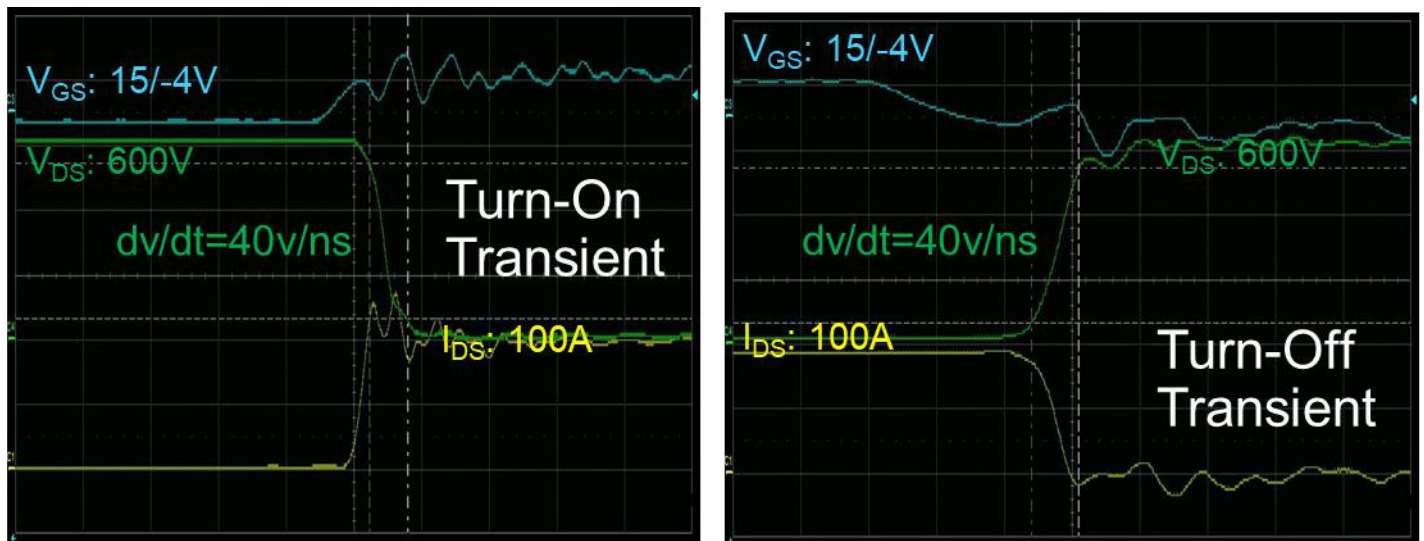


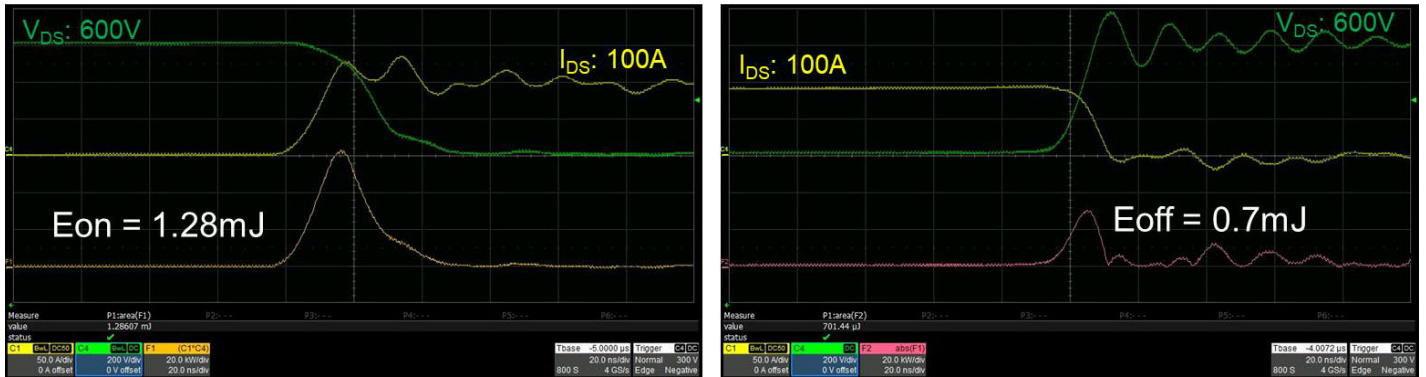
Figure 17: Zoom in of the Double Pulse Turn-On and Turn-Off Switching Transient



4.2 Switching Losses Waveforms

The resulting turn-on switching energy loss, E_{on} , and turn-off switching energy loss, E_{off} , are also measured at 600V V_{DS} and 100A I_{DS} . The measured E_{on} of 1.28 mJ and E_{off} of 0.7 mJ are close to what is specified in the CAB016M12FM3 data sheet.

Figure 18: Waveforms of the Eon and Eoff Switching Losses



4.3 Short-Circuit Waveforms

The short-circuit protection is performed on the SiC module, CAB016M12FM3. Wolfspeed recommends a short-circuit time of 1 μ s. For the safety reasons, gate driver short-circuit protection on this board is set to limit the current at around 500A within 1 μ s. This corresponds to a short-circuit loop inductance of approximately 1 μ H. The short-circuit duration setting is described in Section 3.4, Gate Driver Circuit, Secondary Side, by setting the blanking capacitor CT20 and resistor RT26. The combination of 56 pF and 5.6 k Ω allows the entire short-circuit duration to be soft shutdown with 1 μ s. The soft turn-off function of the ACPL-355JC provides excellent protection from the overvoltage during the turn-off phase after the short-circuit detection. From the voltage waveform, the soft shutdown mechanism results in a minimum VDS overshoot, with sufficient margin from the 1200V absolute maximum voltage of the SiC module.

Figure 19: Waveforms of the Short-Circuit Protection

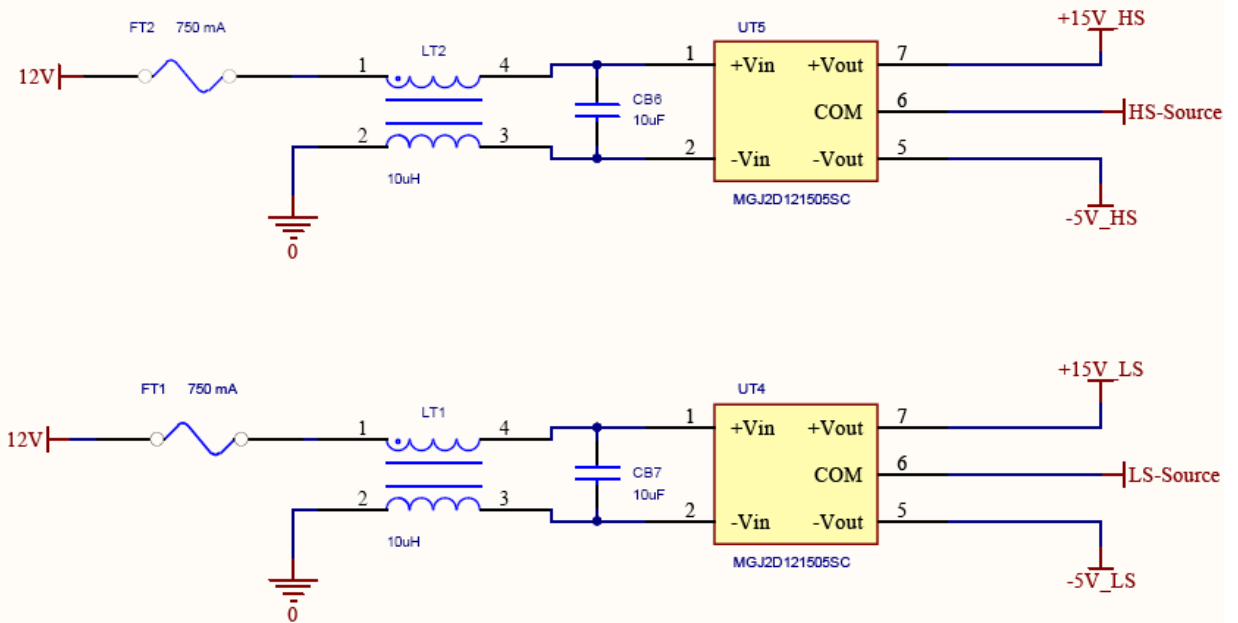


5 Schematics, Layout, and BOM

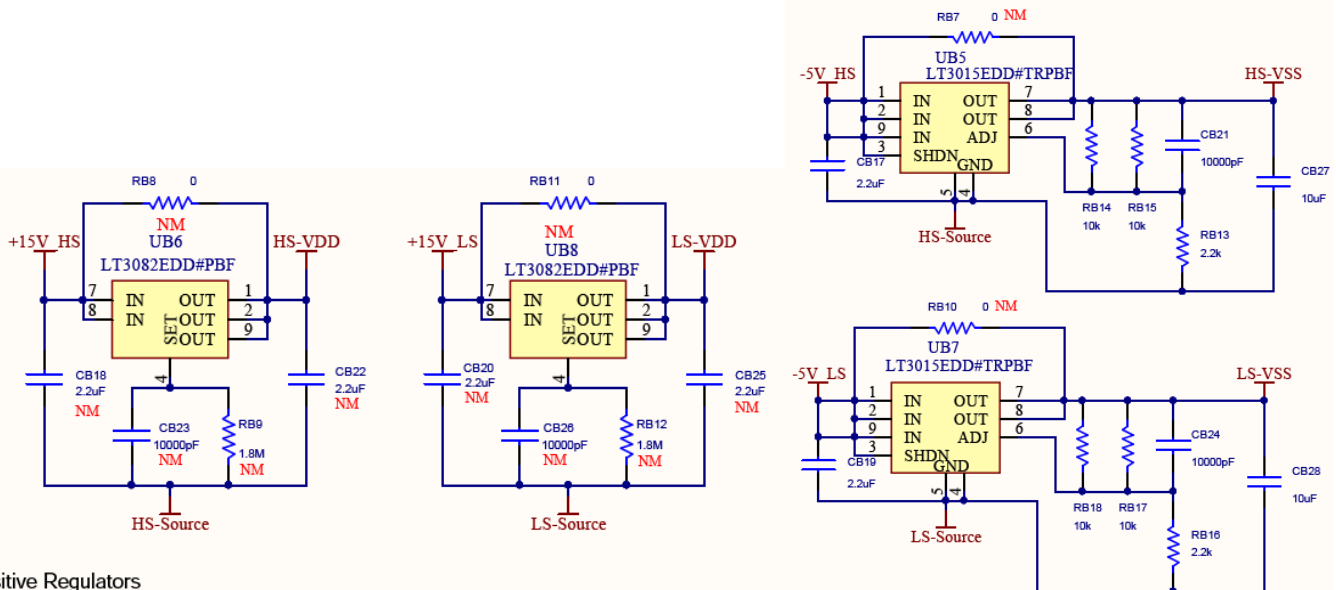
This section gives full schematics, layout, and bill of materials of the half-bridge evaluation board. This information should enable customers to modify the design according to specific requirements.

Figure 20: Schematic of DC-DC Converters and Linear Regulators for +15V/-4V Isolated Power Supply

Isolated DC/DC Converters



Negative Regulators



Positive Regulators

Figure 21: Schematic of IO Interface and Fault Feedback

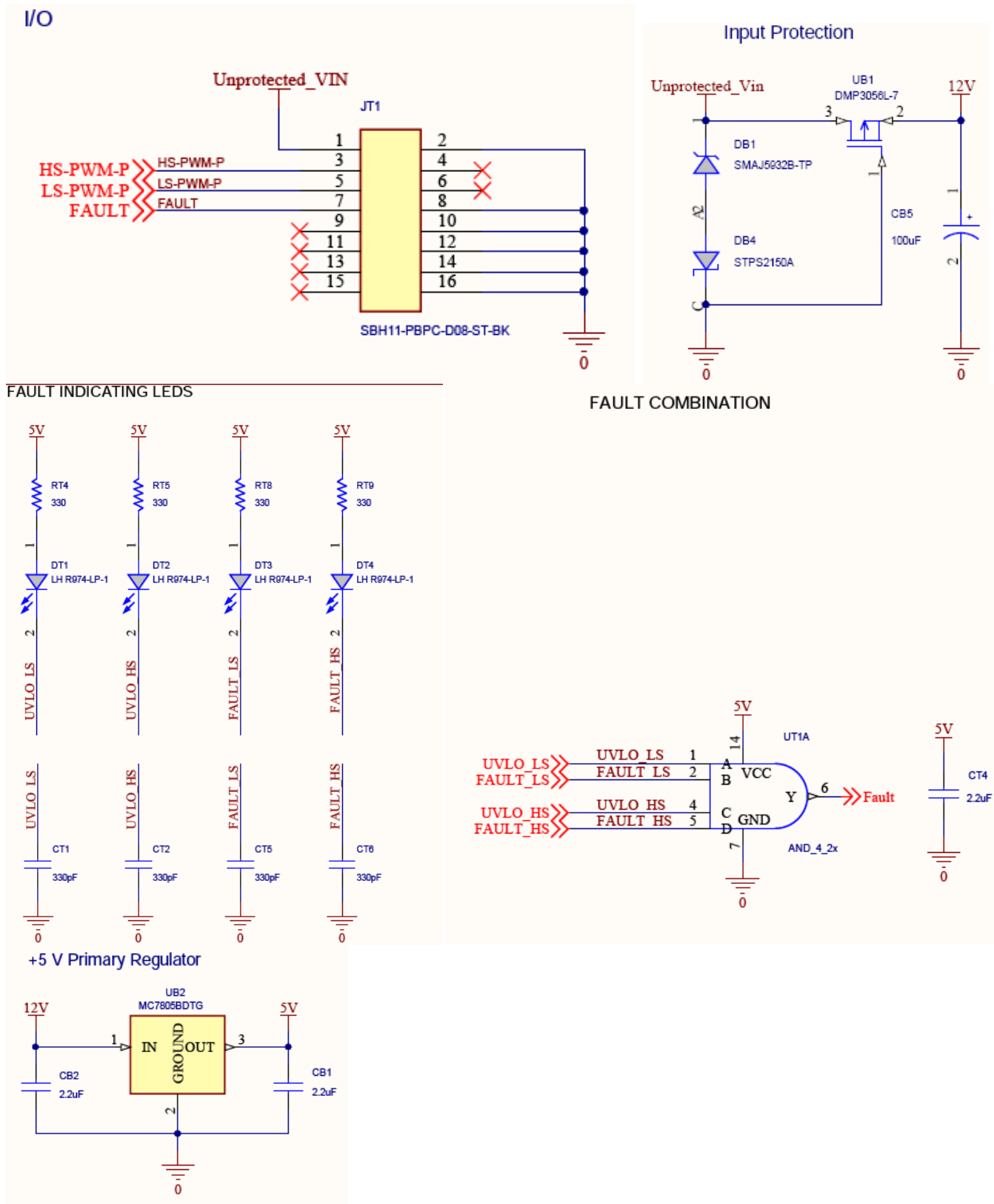


Figure 22: Schematic of High Side Gate Driver and PWM Input Buffer

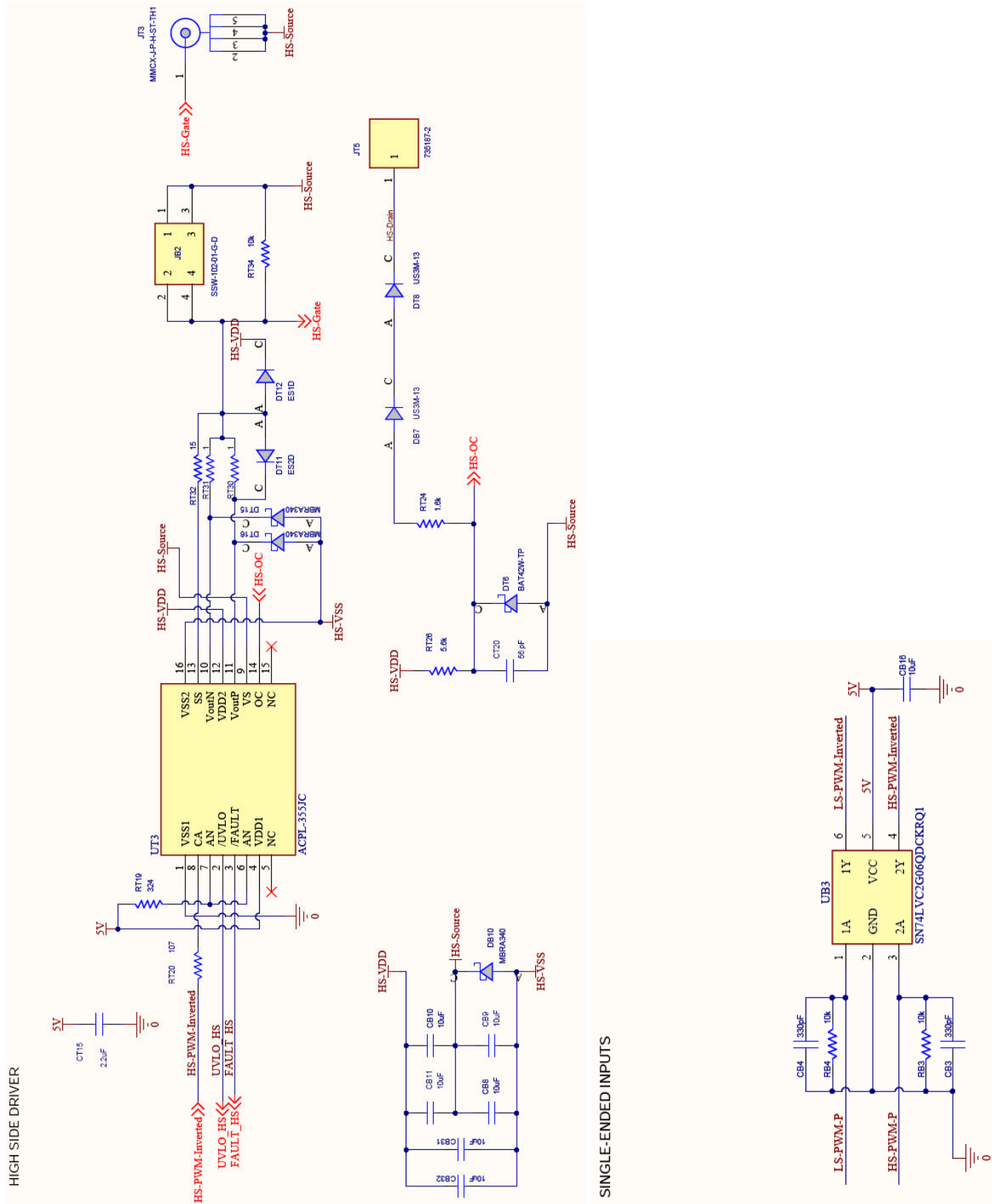


Figure 23: Schematic of Low Side Gate Driver

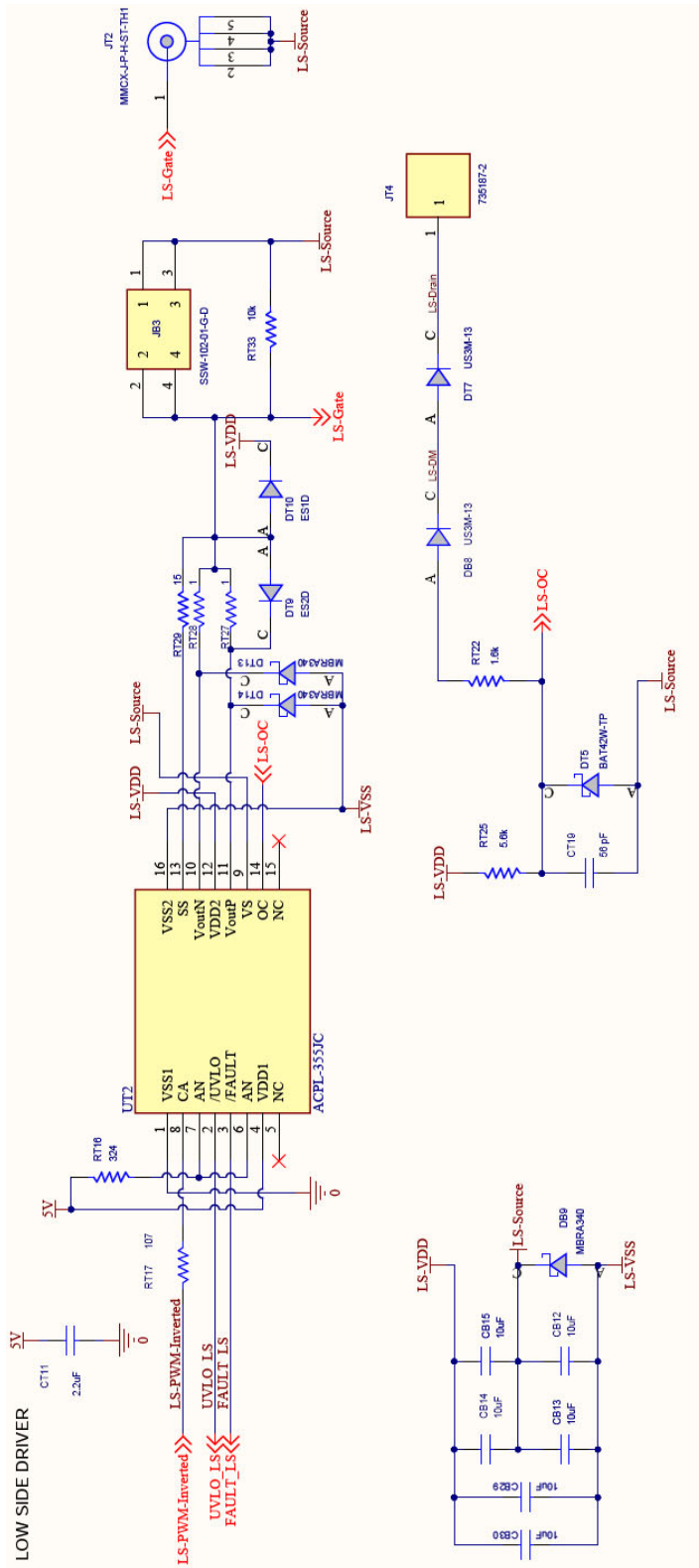


Figure 24: Schematic of Temperature Measurement

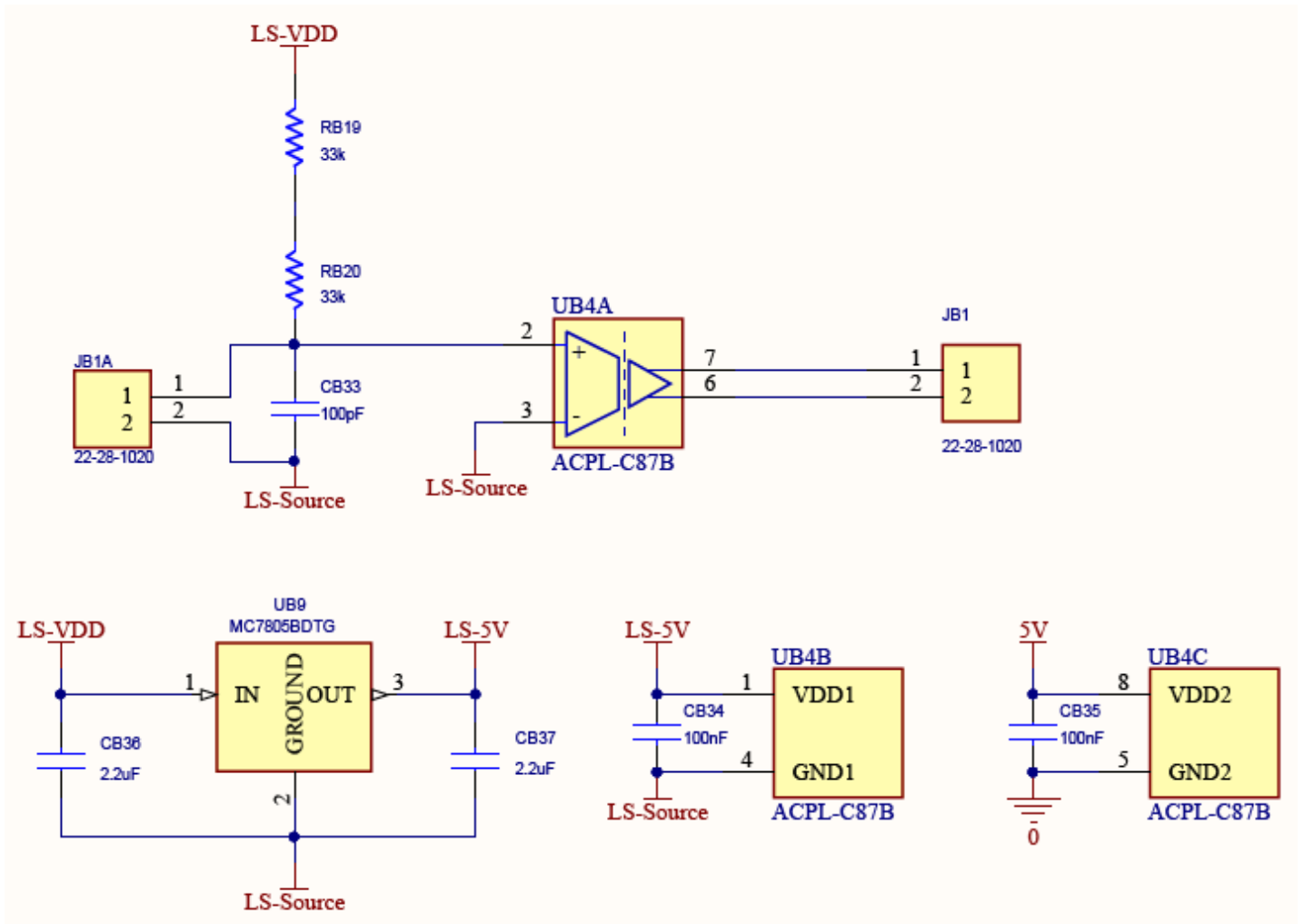


Figure 26: PCB Second Layer

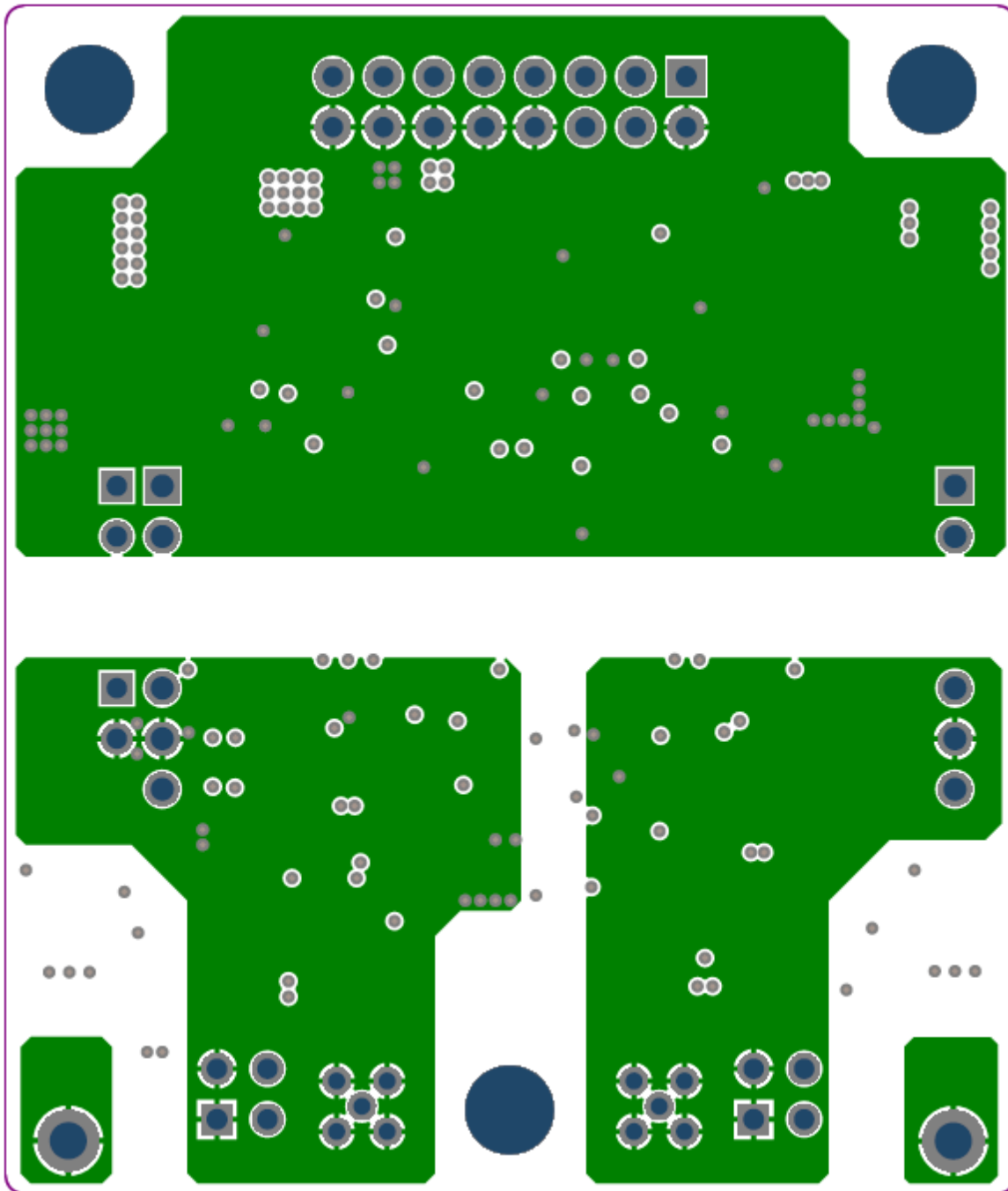


Figure 27: PCB Third Layer

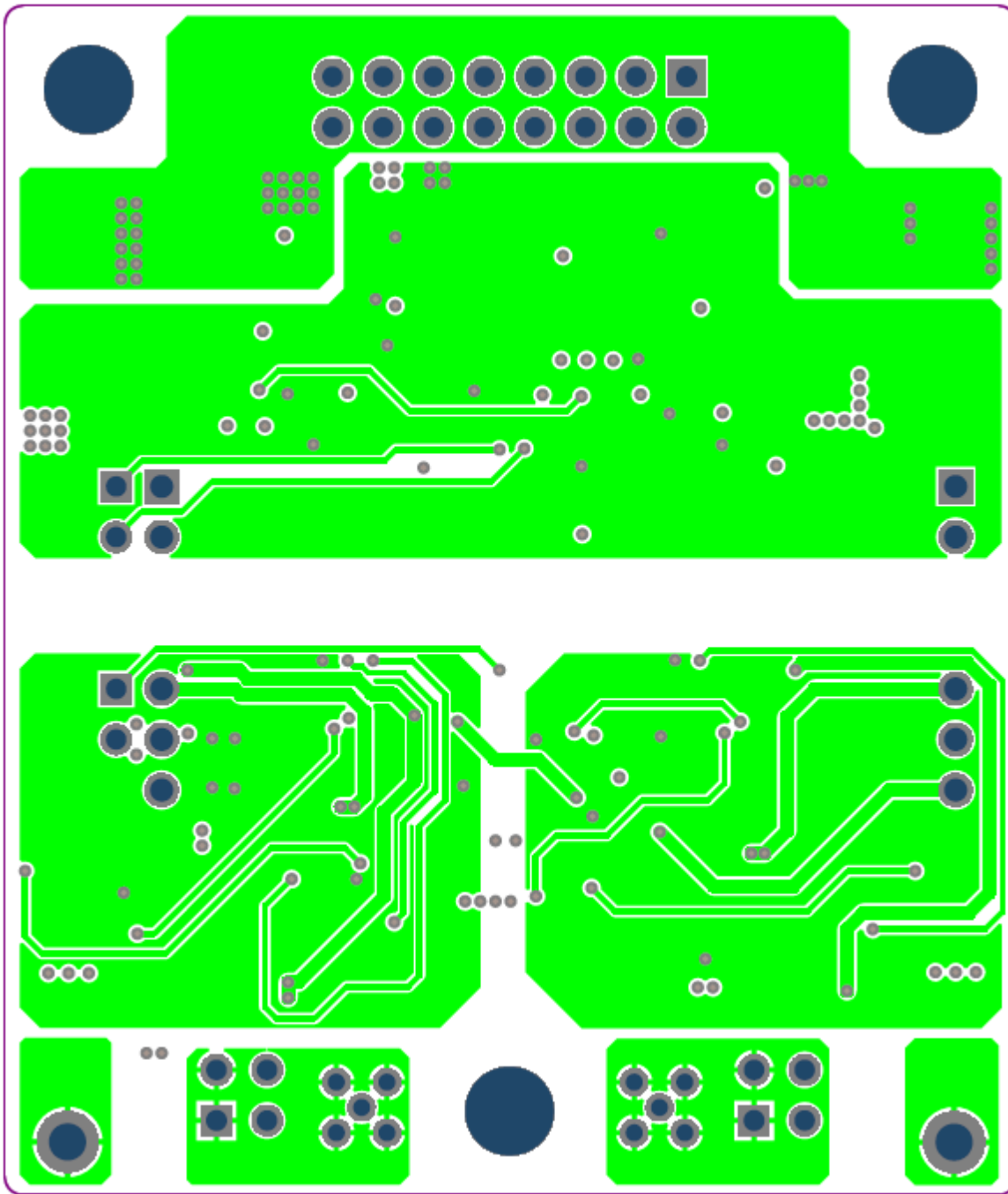


Table 5: Bill of Materials

Item	Ref Designator	Description	Quantity	Manufacturer	Manufacturing Part Number
1	CB33	CAP CER 100PF 50V C0G/NP0 0603	1	Samsung Electro-Mechanics	CL10C101JB8NNNC
2	CT19, CT20	CAP CER 56PF 50V C0G/NP0 0603	2	Samsung Electro-Mechanics	CL10C560JB8NNNC
3	CB3, CB4, CT1, CT2, CT5, CT6,	CAP CER 330PF 50V C0G/NP0 0603	6	Samsung Electro-Mechanics	CL10C331JB8NNNC
4	CB21, CB24	CAP CER 10000PF 50V X7R 0603	2	Samsung Electro-Mechanics	CL10B103KB8NNNC
5	CB34, CB35	CAP CER 0.1UF 50V X7R 1206	2	KEMET	C1206C104K5RAC7800
6	CB1, CB2, CT4, CT11, CT15, CB17, CB19, CB36, CB37	CAP CER 2.2UF 50V X5R 0603	9	Murata Electronics North America	GRT188R61H225ME13D
7	CB6, CB7, CB8, CB9, CB10, CB11, CB12, CB13, CB14, CB15, CB16, CB27, CB28, CB29, CB30, CB31, CB32	CAP CER 10UF 50V X5R 1206	17	Samsung Electro-Mechanics	CL31A106MBHNNNE
8	CB5	CAP TANT 100UF 10% 25V 2917	1	KEMET	T491X107K025AT
9	DB1	DIODE ZENER 20V 1.5W DO214AC	1	Micro Commercial Co	SMAJ5932B-TP
10	DB4	DIODE SCHOTTKY 150V 2A SMA	1	Taiwan Semiconductor Corporation	SK215A R3G
11	DB7, DB8, DT7, DT8	DIODE GEN PURP 1KV 3A SMC	4	Diodes Incorporated	US3M-13
12	DT1, DT2, DT3, DT4	LED RED DIFFUSED 0805 SMD	4	OSRAM Opto Semiconductors Inc.	LH R974-LP-1
13	DT10, DT12	DIODE GEN PURP 200V 1A SMA	2	ON Semiconductor	ES1D
14	DT13, DT14, DT15, DT16, DB9, DB10	DIODE SCHOTTKY 40V 3A SMA	6	ON Semiconductor	MBRA340T3G
15	DT5, DT6	DIODE SCHOTTKY 30V 200MA SOD123	2	Micro Commercial Co	BAT42W-TP
16	DT9, DT11	DIODE GEN PURP 200V 2A DO214AA	2	ON Semiconductor	ES2D
17	FT1, FT2	FUSE BOARD MNT 750MA 125VAC/VDC	2	Bel Fuse Inc.	SSQ 750
18	JB1, JB1A	CONN HEADER R/A 2POS 2.54MM	2	Molex	22281020
19	JB2, JB3	CONN RCPT 4POS 0.1 GOLD PCB	2	Samtec Inc.	SSW-102-01-G-D
20	JT1	CONN HEADER 2.54MM 16POS GOLD	1	Sullins Connector Solutions	SBH11-PBPC-D08-ST-BK
21	JT2, JT3	CONN MMCX JACK STR 50 OHM PCB	2	Samtec Inc.	MMCX-J-P-H-ST-TH1

Table 5: Bill of Materials

Item	Ref Designator	Description	Quantity	Manufacturer	Manufacturing Part Number
22	JT4, JT5	CONN QC TAB 0.110 SOLDER	2	TE Connectivity AMP Connectors	735187-2
23	LT1, LT2	CMC 10UH 1.6A 2LN 920 OHM SMD	2	Würth Elektronik	744226S
24	RT4, RT5, RT8, RT9	RES SMD 330 OHM 5% 1/10W 0603	4	Yageo	RC0603JR-07330RL
25	RB13, RB16	RES SMD 2.2K OHM 1% 1/10W 0603	2	Yageo	RC0603FR-072K2L
26	RB19, RB20	RES SMD 33K OHM 1% 1/10W 0603	2	Yageo	RC0603FR-0733KL
27	RB8, RB11	RES SMD 0 OHM JUMPER 1/4W 1206	2	Panasonic Electronic Components	ERJ-8GEY0R00V
28	RT16, RT19	RES SMD 324 OHM 1% 1/10W 0603	2	Yageo	RC0603FR-07324RL
29	RT17, RT20	RES SMD 107 OHM 1% 1/10W 0603	2	Yageo	RC0603FR-07107RL
30	RT22, RT24	RES SMD 1.6K OHM 1% 1/10W 0603	2	Yageo	RC0603FR-071K6L
31	RT27, RT28, RT30, RT31	RES SMD 1 OHM 1% 1.5W 2512	4	Vishay Dale	CRCW25121R00FKEGH P
32	RT29, RT32	RES SMD 15 OHM 1% 1/4W 1206	2	Vishay Dale	CRCW120615R0FKEBC
33	RT33, RT34, RB3, RB4, RB14, RB15, RB17, RB18	RES SMD 10K OHM 1% 1/10W 0603	8	Panasonic Electronic Components	ERJ-3EKF1002V
34	UB1	MOSFET P-CH 30V 4.3A SOT23	1	Diodes Incorporated	DMP3056L-7
35	UB2, UB9	IC REG LINEAR 5V 1A DPAK	2	ON Semiconductor	MC7805BDTG
36	UB3	IC INVERTER 2CH 2-INP SC70-6	1	Texas Instruments	SN74LVC2G06QDCKRQ 1
37	UB4	IC OPAMP ISOLATION 1 CIRCUIT 8SO	1	Broadcom	ACPL-C87B-000E
38	UB5, UB7	LT3015EDD#TRPBF	2	Analog Devices	LT3015EDD#TRPBF
39	UT1	IC GATE AND 2CH 4-INP 14SOIC	1	Texas Instruments	SN74HC21DR
40	UT2, UT3	10A Gate Driver 16-SOIC	2	Broadcom	ACPL-355JC
41	UT4, UT5	DC DC CONVERTER 15V -5V 2W	2	Murata Power Solutions Inc.	MGJ2D121505SC
42	RT25, RT26	RES SMD 5.6K OHM 1% 1/10W 0603	2		
43	CB18, CB20, CB22, CB25	CAP CER 2.2UF 50V X5R 0603	NM		
44	CB23, CB26	CAP CER 10000PF 50V X5R 0603	NM		
45	RB7, RB10	RES SMD 0 OHM JUMPER 1/4W 1206	NM		

Table 5: Bill of Materials

Item	Ref Designator	Description	Quantity	Manufacturer	Manufacturing Part Number
46	RB9, RB12	RES SMD 1.8M OHM 1% 1/10W 0603	NM		
47	UB6, UB8	LT3082EDD#PBF	NM		

6 Acknowledgment

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Revision History

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- Initial document release.

