BROADCOM®

Data Sheet

ACPL-355JC

10A IGBT and SiC MOSFET Gate Drive Optocoupler with Integrated Overcurrent Sensing, FAULT, and UVLO Status Feedback

Description

The Broadcom® ACPL-355JC is a 10A intelligent gate drive optocoupler. The high peak output current and wide operating voltage range make it ideal for driving IGBT or SiC MOSFET directly in motor control and inverter applications.

The device features fast propagation delay with excellent timing skew performance. It provides IGBT/SiC MOSFET with overcurrent protection and functional safety reporting. This full-featured and easy-to-implement gate drive optocoupler comes in a compact, surface-mountable SO-16 600V CTI package. It provides reinforced insulation certified for safety regulatory IEC/EN/DIN, UL, and cUL.

Features

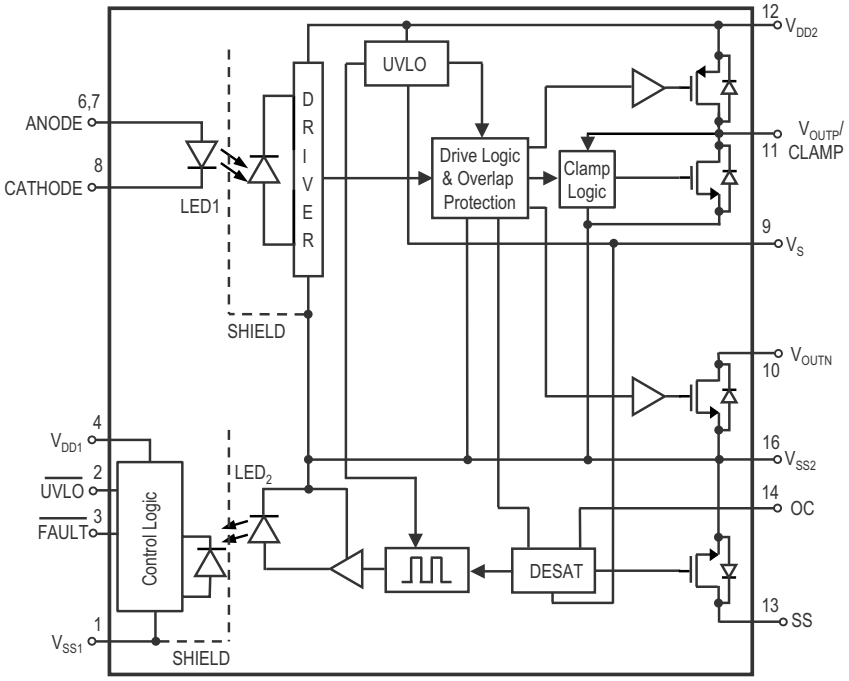
- 10A maximum peak output current
- 140-ns maximum propagation delay
- Dual output drive to control turning on and off time
- Overcurrent detection with configurable soft shutdown
- Functional safety reporting
  - Overcurrent FAULT feedback
  - UVLO status feedback
- Under voltage lockout (UVLO) with hysteresis
- 100-kV/µs minimum common mode rejection (CMR) at V_{CM} = 1500V
- 15V to 30V wide operating V_{DD2} range
- –40°C to 110°C industrial temperature range
- CTI > 600V with 8.3-mm creepage and clearance
- Regulatory approvals:
  - UL/cUL 1577 5000 V_{RMS} for 1 minute
  - IEC 60747-5-5 V_{IORM} = 2262 V_{PEAK}

Applications

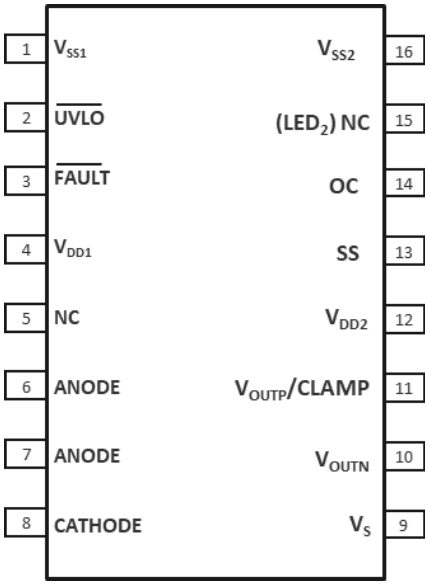
- Mid-voltage motor drives
- 1500V solar inverter and wind inverter
- Static var generator (SVG)/high voltage converter (HVC)

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The component featured in this data sheet is not to be used in military or aerospace applications or environments. The component is also not AEC-Q100 qualified and not recommended for automotive applications.

Functional Diagram



Pin Description



Pin	Symbol	Description
1	V_{SS1}	Input ground
2	UVLO	V_{DD2} under voltage lockout feedback
3	FAULT	Overcurrent fault feedback
4	V_{DD1}	Input power supply
5	NC	No connection
6	ANODE	Input LED anode
7	ANODE	Input LED anode
8	CATHODE	Input LED Cathode
9	V_S	Common (IGBT emitter or MOSFET source) output supply voltage
10	V_{OUTN}	Driver output to turn off IGBT or MOSFET gate
11	V_{OUTP}/CLAMP	Driver output to turn on IGBT or MOSFET gate/miller clamp
12	V_{DD2}	Positive output power supply
13	SS	Soft shutdown
14	OC	Overcurrent input pin. When the voltage on the OC pin exceeds an internal reference voltage of 9V while the IGBT/ MOSFET is on, FAULT output is changed from logic high to low state.
15	(LED_2)NC	No connection
16	V_{SS2}	Negative output power supply

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-355JC	-000E	SO-16	X		X	45 per tube
	-500E		X	X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

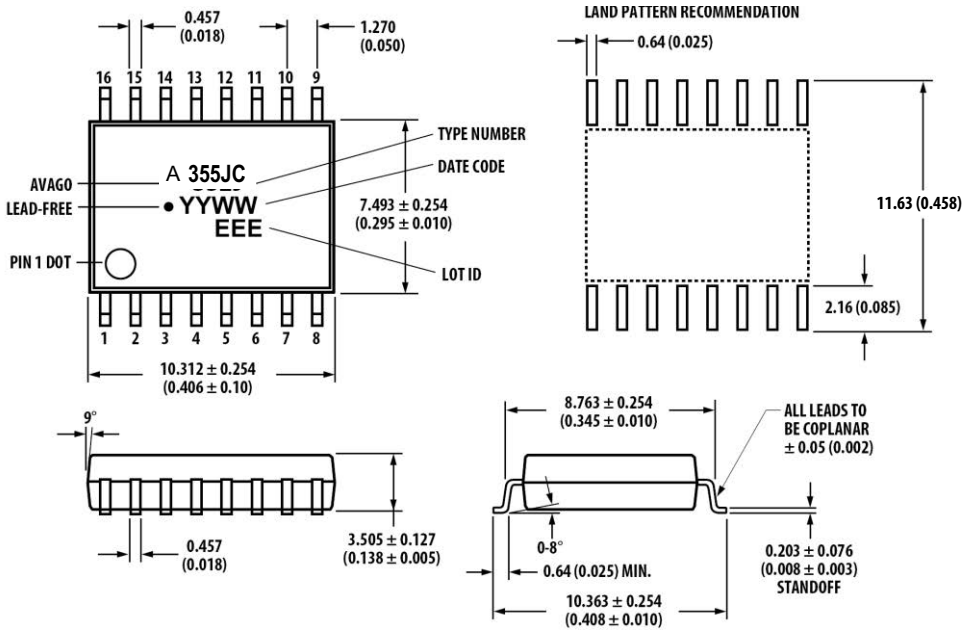
Example 1:

ACPL-355JC-500E to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawing

16-Lead Surface Mount



Dimensions are in inches (millimeters).
Floating lead protrusion is 0.25 mm (10 mils) maximum.

Recommended PB-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Use non-halide flux.

Approvals

The ACPL-355JC is approved by the following organizations.

UL/cUL	UL/cUL 1577, compliance with U.S. and Canadian requirements, component recognition program up to V_{ISO} = 5000 V_{RMS}.
IEC/EN/DIN EN 60747-5-5	IEC 60747-5-5 EN 60747-5-5 DIN EN 60747-5-5

IEC/EN/DIN EN60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic[a]	Unit
Insulation Classification per DIN VDE 0110/1.89, Table 1			
For Rated Mains Voltage ≤ 600Vrms		I - IV	
For Rated Mains Voltage ≤ 1000Vrms		I - IV	
Climatic Classification		40/110/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	2262	V_{PEAK}
Input to Output Test Voltage, Method b[b] V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 seconds, partial discharge < 5 pC	V_{PR}	4242	V_{PEAK}
Input to Output Test Voltage, Method a[b] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, partial discharge < 5 pC	V_{PR}	3619	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 seconds)	V_{IOTM}	8000	V_{PEAK}
Safety-limiting Values – Maximum Values Allowed in the Event of a Failure			
Case Temperature	T_S	175	°C
Input Power	$P_{S,INPUT}$	400	mW
Output Power	$P_{S,OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$	Ω

a. Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.

b. Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the Broadcom Regulatory Guide to Isolation Circuits, AV02-2041EN, for a detailed description of Method a and Method b partial discharge test profiles.

Insulation-Related and Safety-Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		I		Material Group (DIN VDE 0110)

NOTE: All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, when mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended land pattern does not necessarily meet the minimum creepage of the device). Recommended techniques, such as grooves and ribs, may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances also change depending on factors such as pollution degree and insulation level.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	125	°C	
Operating Temperature	T_A	–40	110	°C	
Output IC Junction Temperature	T_J	—	125	°C	
Average Input Current	$I_{F(AVG)}$	—	25	mA	a
Peak Transient Input Current (< 1-µs pulse width, 300pps)	$I_{F(TRAN)}$	—	1.0	A	
Reverse Input Voltage	V_R	—	5	V	
Peak Output Current	$I_{O(PEAK)}$	—	10	A	b
Positive Input Supply Voltage	V_{DD1}	0	7	V	
FAULT Output Current	I_{FAULT}	—	10	mA	
FAULT Pin Voltage	V_{FAULT}	–0.5	V_{DD1}	V	
Total Output Supply Voltage	$(V_{DD2} – V_{SS2})$	–0.5	35	V	
Negative Output Supply Voltage	$(V_S – V_{SS2})$	–0.5	17	V	
Positive Output Supply Voltage	$(V_{DD2} – V_S)$	–0.5	$35 – (V_S – V_{SS2})$	V	
Input Current (Rise/Fall Time)	$t_{r(IN)}/t_{f(IN)}$	—	500	ns	
High Side Pull Up Voltage	V_{OUTP}	$V_{SS2} – 0.5$	$V_{DD2} + 0.5$	V	
Low Side Pull Down Voltage	V_{OUTN}	$V_{SS2} – 0.5$	$V_{DD2} + 0.5$	V	
Overcurrent Pin Voltage	V_{OC}	$V_S – 0.5$	$V_{DD2} + 0.5$	V	
Peak Clamp Sinking Current	I_{CLAMP}	—	4	A	
Miller Clamp Pin Voltage	V_{CLAMP}	$V_{SS2} – 0.5$	$V_{DD2} + 0.5$	V	
Output IC Power Dissipation	P_O	—	600	mW	c
Input LED Power Dissipation	P_I	—	110	mW	d

a. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.

b. Maximum pulse width = 1 µs, maximum duty cycle = 1%. The output must be limited to –10.0A/10.0A of peak current by external resistors and connected to a total load bigger than 2 nF during application or board testing. See the Supply and Ground Planes Layout and Loading Conditions section to prevent output noise at 10A rated current.

c. Derate linearly above 95°C free-air temperature at a rate of 20 mW/°C.

d. Derate linearly above 95°C free-air temperature at a rate of 3.7 mW/°C. The maximum LED junction temperature should not exceed 125°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T_A	–40	110	°C	
Positive Input Supply Voltage	V_{DD1}	4.5	5.5	V	
Total Output Supply Voltage	$(V_{DD2} – V_{SS2})$	15	30	V	
Negative Output Supply Voltage	$(V_S – V_{SS2})$	0	15	V	
Positive Output Supply Voltage	$(V_{DD2} – V_S)$	15	$30 – (V_S – V_{SS2})$	V	
Input Current (ON)	$I_{F(ON)}$	7	11	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	–3.6	0.5	V	

Electrical Specifications (DC)

All typical values at T_A = 25°C, V_{DD1} = 5V, $V_{DD2} – V_S$ = 15 V, $V_S – V_{SS2}$ = 15V; all minimum and maximum specifications are at recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
V_{OUTP} High Level Peak Output Current	I_{OH}	–7.5	–13	—	A	$V_{DD2} – V_{OUTP}$ = 15V	3	a
V_{OUTN} Low Level Peak Output Current	I_{OL}	7.5	14	—	A	$V_{OUTN} – V_{SS2}$ = 15V	4	a
V_{OUTP} Output PMOS $R_{DS(ON)}$	R_{OUTP}	0.4	0.7	1.5	Ω	I_{OP} = –7.5A, I_F = 8 mA	5	a
V_{OUTN} Output NMOS $R_{DS(ON)}$	R_{OUTN}	0.3	0.4	1.2	Ω	I_{ON} = 7.5A, V_F = 0V	6	a
V_{OUTP} Output Voltage	V_{OH}	V_{DD2} – 0.60	V_{DD2} – 0.15	—	V	I_{OP} = –100 mA, I_F = 8 mA	1	b, c
V_{OUTN} Output Voltage	V_{OL}	—	V_{SS2} + 0.04	V_{SS2} + 0.60	V	I_{ON} = 100 mA, V_F = 0V	2	
Clamp Threshold Voltage	V_{TH_CLAMP}	—	V_{SS2} + 2	V_{SS2} + 2.2	V			
Clamp Low Level Sinking Current	I_{CLAMP}	1.7	2.75	—	A	V_{CLAMP} = V_{SS2} + 2.5V	7	
Clamp Low Level Peak Sinking Current	$I_{CLAMPPK}$	2.5A	4.6	—	A	V_{CLAMP} = V_{SS2} + 10V		
Clamp Output Transistor $R_{DS(ON)}$	$R_{DS,CLAMP}$	—	1.1	2	Ω	I_{CLAMP} = 2.5A		
SS Pull Down Current	I_{OSS}	0.5	1	—	A	SS – V_{SS2} < 15V, I_F = 8 mA, OC = Open		
SS R_{DSON}	R_{OUTSS}	—	1.35	—	Ω	I_{SS} = 0.5A, I_F = 8 mA, OC = Open		
High Level Output Supply Current (V_{DD2})	I_{DD2H}	—	6.5	8	mA	I_F = 8 mA, No Load	8	
Low Level Output Supply Current (V_{DD2})	I_{DD2L}	—	5.4	7	mA	V_F = 0V, No Load	8	
High Level Output Supply Current(V_{SS2})	I_{SS2H}	–2.2	–1.7	—	mA	I_F = 8 mA, No Load	9	
Low Level Output Supply Current (V_{SS2})	I_{SS2L}	–1	–0.7	—	mA	V_F = 0V, No Load	9	
Input Threshold Current Low to High	I_{FLH}	0.2	2.5	6.5	mA		10, 11	
Input Threshold Voltage High to Low	V_{FHL}	0.8	—	—	V			
Input Forward Voltage	V_F	1.2	1.4	1.95	V	I_F = 8 mA		
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$		–1.7	—	mV/°C	I_F = 8 mA		
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	I_R = 100 µA		
Input Capacitance	C_{IN}	—	23	—	pF	f = 1 MHz, V_F = 0V		

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
UVLO Threshold, $V_{DD2} - V_S$	V_{UVLO+}	12.2	13.2	13.8	V	I_F = 8 mA, $V_{OUTP} - V_E$ > 5V		b, c, d
	V_{UVLO-}	11.2	12.1	12.7	V	I_F = 8 mA, $V_{OUTP} - V_E$ < 5V		b, c, e
UVLO Hysteresis, $V_{DD2} - V_S$	$V_{UVLO+} - V_{UVLO-}$	0.5	1	—	V			
OC Sensing Voltage Threshold with Reference to V_S	V_{OC}	8.5	9.2	9.8	V	$V_{DD2} - V_S > V_{UVLO+}$	12	c
Blanking Capacitor Charging Current	I_{CHG}	0.95	1	1.05	mA	V_{OC} = 2V	13	c, f
OC Low Voltage when Blanking Capacitor Discharge with Reference to V_S	V_{DSCHG}	—	1.4	2.3	V	I_{DSCHG} = 50 mA		c, f
Input Supply Current (V_{DD1})	I_{DD1}	—	1.6	2.5	mA		14	
V_{CC1} Under Voltage Turn On Threshold	V_{UV1_TH+}	—	4.5	—	V			
V_{CC1} Under Voltage Turn Off Threshold	V_{UV1_TH-}	—	3.8	—	V			
FAULT Logic Low Output Current	I_{FAULTL}	4	8.5	—	mA	V_{FAULT} = 0.4 V, V_{DD1} = 5V		
FAULT Logic High Output Current	I_{FAULTH}	—	—	20	µA	$V_{FAULT} = V_{DD1}$ = 5V		
UVLO Logic Low Output Current	I_{UVLOL}	4	8.5	—	mA	V_{UVLO} = 0.4 V, V_{DD1} = 5V		
UVLO Logic High Output Current	I_{UVLOH}	—	—	20	µA	$V_{UVLO} = V_{DD1}$ = 5V		

a. Output is sourced at –10A /10A with a maximum pulse width = 10 µs.

b. 15V is the recommended minimum operating positive supply voltage ($V_{DD2} - V_S$) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 13.8V. For High Level Output Voltage testing, V_{OUTP} is measured with a 50-µs pulse load current. When driving capacitive loads, V_{OUTP} will approach V_{DD2} as I_{OUTP} approaches zero units.

c. When the system is out of UVLO ($V_{DD2} - V_S$ > VUVLO+), the OC detection feature of the ACPL-355JC will be the primary source of IGBT/MOSFET protection. UVLO must be unlocked to ensure OC is functional. When V_{DD2} exceeds the V_{UVLO+} threshold, OC will remain functional until V_{DD2} is below the V_{UVLO-} threshold. The OC detection and UVLO features of the ACPL-355JC work together to ensure constant IGBT/MOSFET protection.

d. This is the increasing (that is, turn-on or positive-going direction) of $V_{DD2} - V_S$.

e. This is the decreasing (that is, turn-off or negative-going direction) of $V_{DD2} - V_S$.

f. See the OC Fault Detection Blanking Time section for further details

Switching Specifications (AC)

All typical values at T_A = 25°C, V_{DD1} = 5V, $V_{DD2} – V_S$ = 15V, $V_S – V_{SS2}$ = 15V; all minimum and maximum specifications are at recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High V_{OUTP} Output Level	t_{PLH}	40	90	140	ns	R_{GP} = 3Ω, R_{GN} = 3Ω, C_G = 2.2 nF, f = 20 kHz, Duty Cycle = 50%, I_F = 8 mA	15, 16, 21	a
Propagation Delay Time to Low V_{OUTN} Output Level	t_{PHL}	40	100	140	ns		15, 16, 21	b
Pulse Width Distortion	PWD	–50	10	50	ns			c
Propagation Delay Difference Between Any Two Parts	PDD ($t_{PLH} – t_{PHL}$)	–70	—	70	ns			d
Propagation Delay Skew	t_{PSK}	—	—	60	ns			e
10% to 90% Rise Time on V_{OUTP}	t_R	—	35	—	ns	R_{GP} = 3Ω, R_{GN} = 3Ω, C_G = 2.2 nF, f = 20 kHz, Duty Cycle = 50%, I_F = 8 mA		
90% to 10% Fall Time on V_{OUTN}	t_F	—	33	—	ns			
OC Blanking Time	$t_{OC(BLANKING)}$	—	0.6	1	µs	R_{GP} = 3Ω, R_{GN} = 3Ω, C_G = 2.2 nF, f = 2.5kHz, Duty Cycle = 50%, I_F = 8 mA, R_{SS} = 15Ω, C_F = 330 pF, R_F = 10 kΩ	20	f
OC Detection to 90% V_{GATE} Delay	$t_{OC(90\%)}$	0.05	0.13	0.3	µs		20	g
OC Detection to V_{GATE} = 2V Delay	$t_{OC(2V)}$	0.1	0.2	0.5	µs		20	h
OC Detection to OC Pull Low Propagation Delay	$t_{OC(LOW)}$	—	0.3	—	µs		20	i
OC Detection to SS Pull Low Propagation Delay	$t_{SS(LOW)}$	—	0.35	0.8	µs		17, 20	j
OC Detection to Low Level FAULT Signal Delay	$t_{OC(FAULT)}$	—	1.7	5	µs		20	k
Output Mute Time due to Overcurrent	$t_{OC(MUTE)}$	0.13	0.2	0.4	ms		18, 20	l
Time Input Kept Low Before Fault Reset to High	$t_{OC(RESET)}$	0.13	0.2	0.4	ms	C_F = 330 pF, R_F = 10 kΩ	18, 20	m
V_{DD2} to UVLO High Delay	t_{PLH_UVLO}	—	17	25	µs	C_U = 330 pF, R_U = 10 kΩ	22	n
V_{DD2} to UVLO Low Delay	t_{PHL_UVLO}	—	14	30	µs	C_U = 330 pF, R_U = 10 kΩ	22	o
V_{DD2} UVLO to VOUTP High Delay	t_{UVLO_ON}	—	4	—	µs		22	p
V_{DD2} UVLO to VOUTN Low Delay	t_{UVLO_OFF}	—	3.5	—	µs		22	q
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	100	—	—	kV/µs	T_A = 25°C, V_{CM} = 1500V, V_{DD1} = 5V, C_F = 330 pF, R_F = 10 kΩ, I_F = 8 mA		r, s
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	100	—	—	kV/µs	T_A = 25°C, V_{CM} = 1500V, V_{DD1} = 5V, C_F = 330 pF, R_F = 10 kΩ, V_F = 0V		s, t

a. t_{PLH} is defined as propagation delay from 50% of LED input I_F, to 50% of V_{OUTP} high level output.

b. t_{PHL} is defined as propagation delay from 50% of LED input I_F, to 50% of V_{OUTN} low level output.

c. Pulse Width Distortion (PWD) is defined as $|t_{PHL} – t_{PLH}|$ for any given unit.

d. Propagation Delay Difference (PDD) is the difference between tPHL and tPLH between any two units under the same test condition.

e. Propagation Delay Skew (t_{PSK}) is the difference in t_{PHL} or t_{PLH} between any two units under the same test condition.

f. The internal delay time to respond to an OC fault condition without any external blanking capacitor.

g. The amount of time from when OC threshold is exceeded to 90% of V_{GATE} at mentioned test conditions.

h. The amount of time from when OC threshold is exceeded to V_{GATE} at 2V at mentioned test conditions.

i. The amount of time from when OC threshold is exceeded to 10% of OC low voltage.

j. The amount of time from when OC threshold is exceeded to 10% of SS (Soft Shut) low voltage.

k. The amount of time from when OC threshold is exceeded to FAULT output low.

l. The amount of time when OC threshold is exceeded, output is muted to LED input.

m. The amount of time when OC mute time is expired, LED input must be kept low for FAULT status to return to High.

n. The delay time when V_{DD2} exceeds UVLO+ threshold to UVLO high – 50% of UVLO positive-going edge.

o. The delay time when V_{DD2} exceeds UVLO- threshold to UVLO low – 50% of UVLO negative-going edge.

p. The delay time when V_{DD2} exceeds UVLO+ threshold to 50% of V_{OUTP} high level output.

q. The delay time when V_{DD2} exceeds UVLO- threshold to 50% of V_{OUTN} low level output.

r. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (that is, $V_{DD2} – V_{OUTP} < 1.0V$ or FAULT > 2V). V_{DD2} must be higher than V_{UVLO+}.

s. Split resistor network in the ratio 3:1 with 324Ω at the anode and 107Ω at the cathode.

t. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (that is, $V_{OUTN} – V_{SS2} < 1.0V$ or FAULT > 2V). V_{DD2} must be higher than V_{UVLO+}.

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			V_{RMS}	RH < 50%, t = 1 minute, T_A = 25°C	a, b, c
Resistance (Input-Output)	R_{I-O}		109		Ω	V_{I-O} = 500 V_{DC}	c
Capacitance (Input-Output)	C_{I-O}		1.3		pF	f = 1 MHz	
Thermal coefficient between:					°C/W		d
Input IC due to heating of Input IC	R_{11}		42.53				
Input IC due to heating of LED1	R_{12}		17.10				
Input IC due to heating of Output IC	R_{13}		13.01				
Input IC due to heating of LED2	R_{14}		33.06				
Input LED1 due to heating of Input IC	R_{21}		10.91				
Input LED1 due to heating of LED1	R_{22}		88.49				
Input LED1 due to heating of Output IC	R_{23}		17.08				
Input LED1 due to heating of LED2	R_{24}		20.75				
Output IC due to heating of Input IC	R_{31}		13.62				
Output IC due to heating of LED1	R_{32}		29.74				
Output IC due to heating of Output IC	R_{33}		33.90				
Output IC due to heating of LED2	R_{34}		28.67				
Input LED2 due to heating of Input IC	R_{41}		17.56				
Input LED2 due to heating of LED1	R_{42}		19.09				
Input LED2 due to heating of Output IC	R_{43}		16.51				
Input LED2 due to heating of LED2	R_{44}		84.90				

a. In accordance with UL/cUL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 9000 V_{RMS} for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table, if applicable.

b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating.For the continuous voltage rating, refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.

c. The device considered a two-terminal device: Pins 1 to 8 are shorted together, and pins 9 to 16 are shorted together.

d. The device was mounted on a high conductivity test board as per JEDEC 51-7. For further details, see the Thermal Calculation section.

Figure 1: V_{OH} vs. Temperature

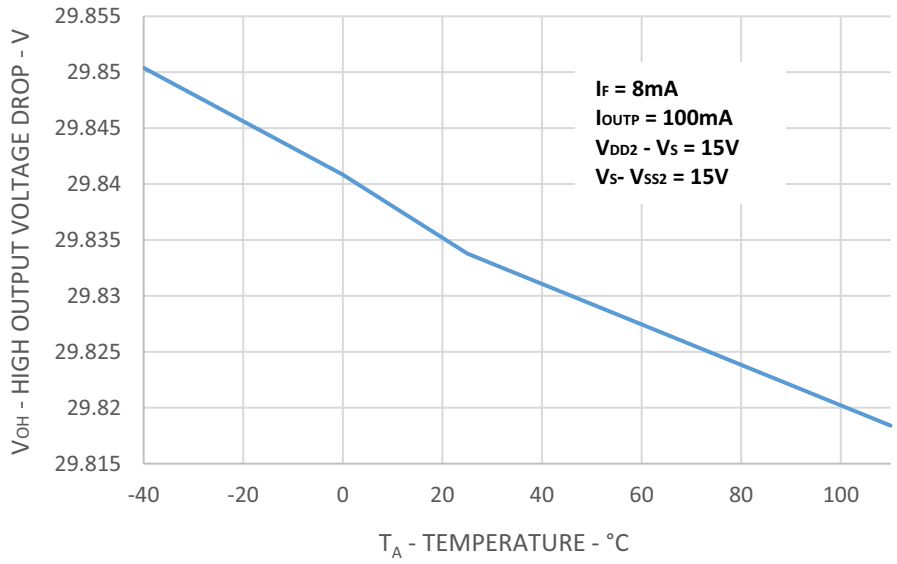


Figure 2: V_{OL} vs. Temperature

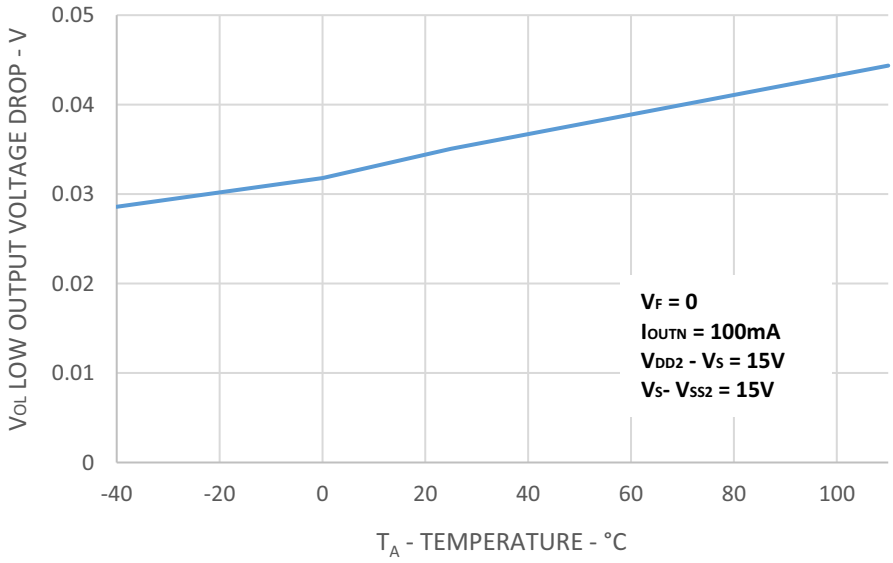


Figure 3: I_{OH} vs. V_{OH}

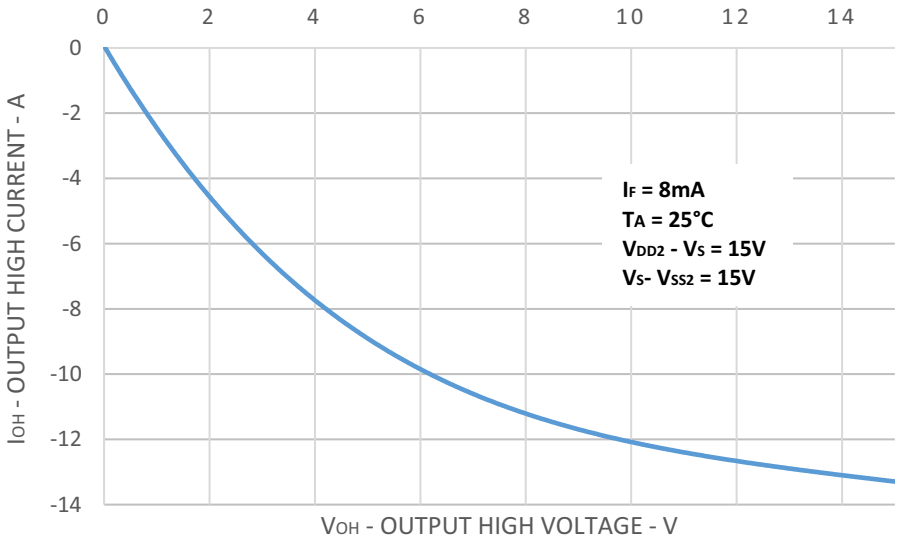


Figure 4: I_{OL} vs. V_{OL}

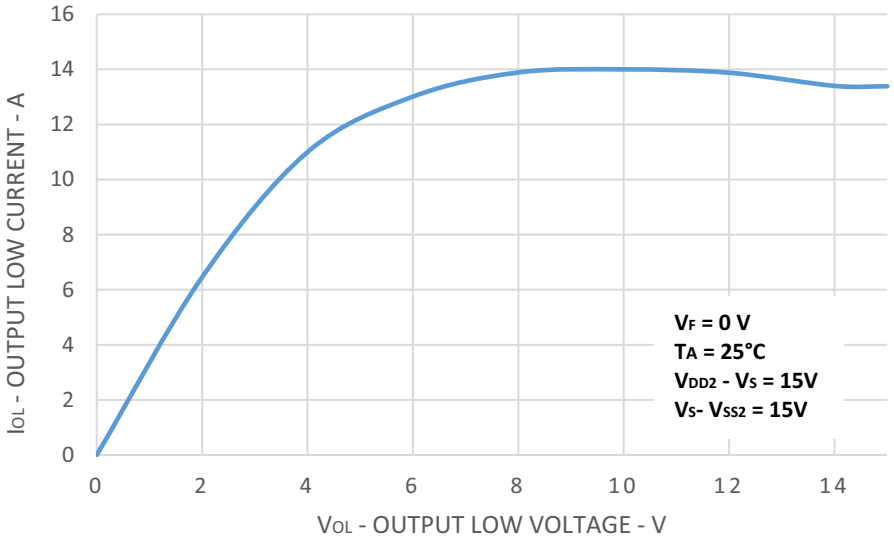


Figure 5: R_{OUTP} vs. Temperature

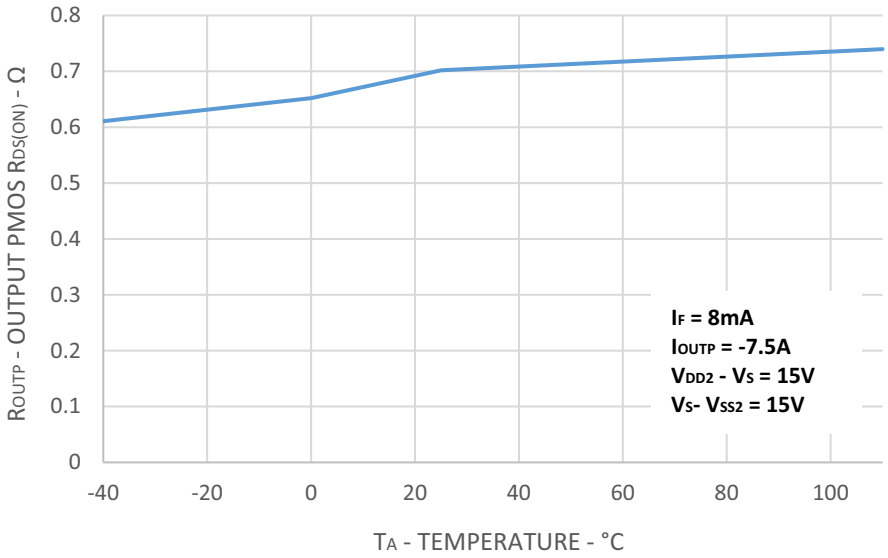


Figure 6: R_{OUTN} vs. Temperature

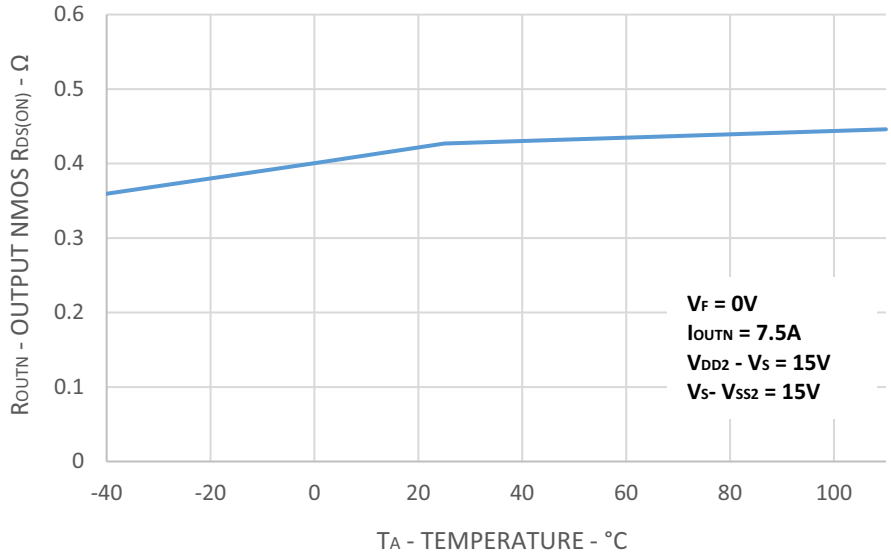


Figure 7: I_{CLAMP} vs. Temperature

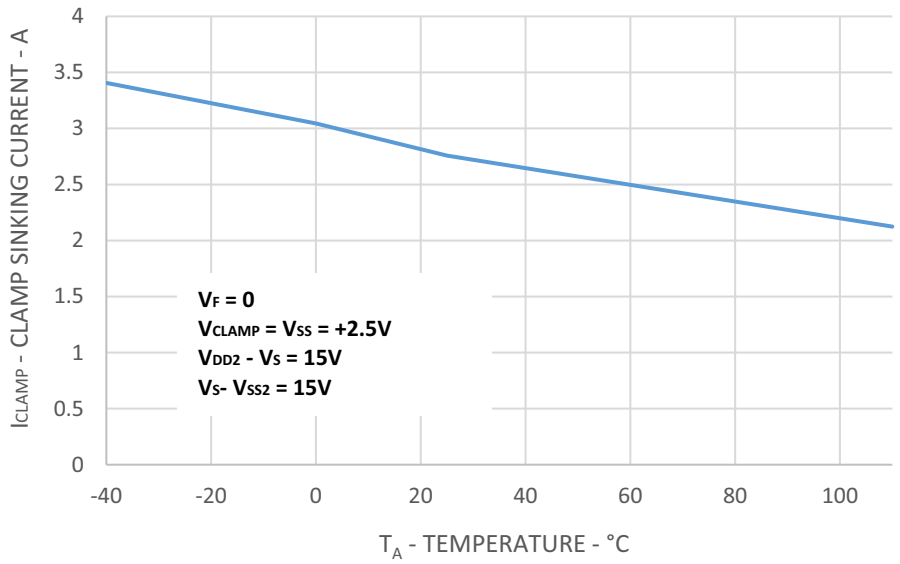


Figure 8: I_{DD2L}/I_{DD2H} vs. Temperature

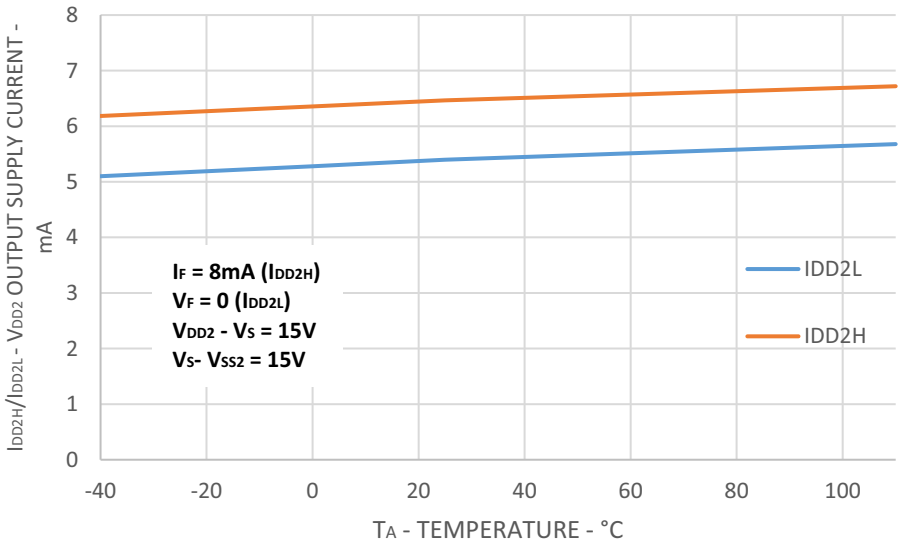


Figure 9: I_{SS2L}/I_{SS2H} vs. Temperature

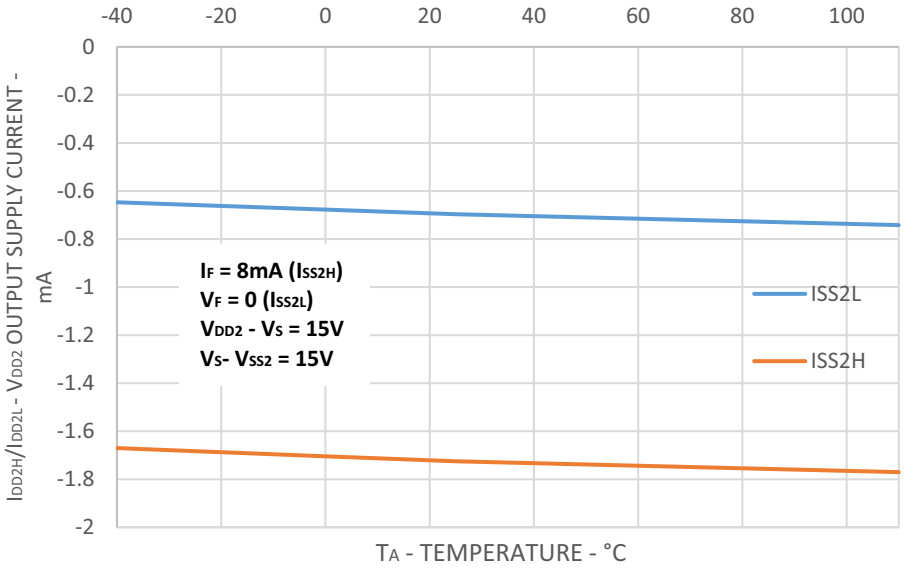


Figure 10: V_{OUTP}/V_{OUTN} vs. I_{FLH}

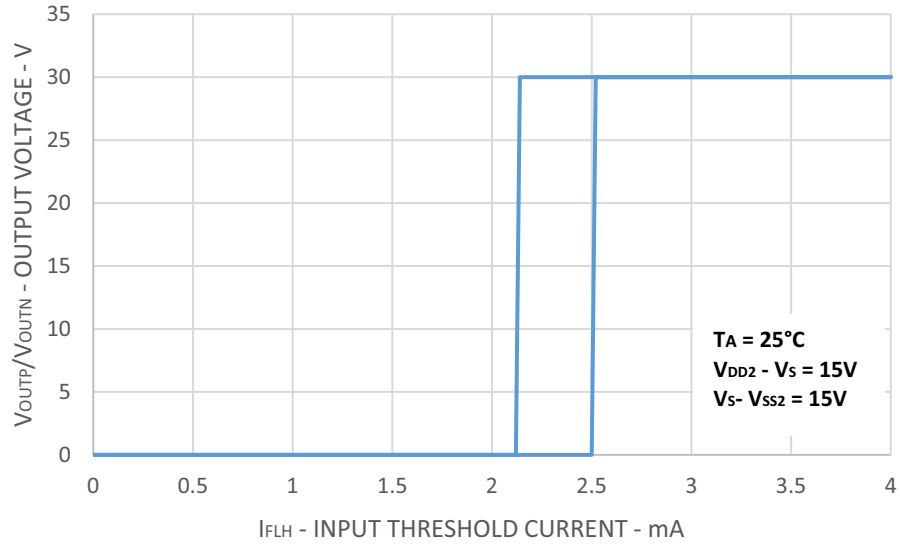


Figure 11: I_{FLH} vs. Temperature

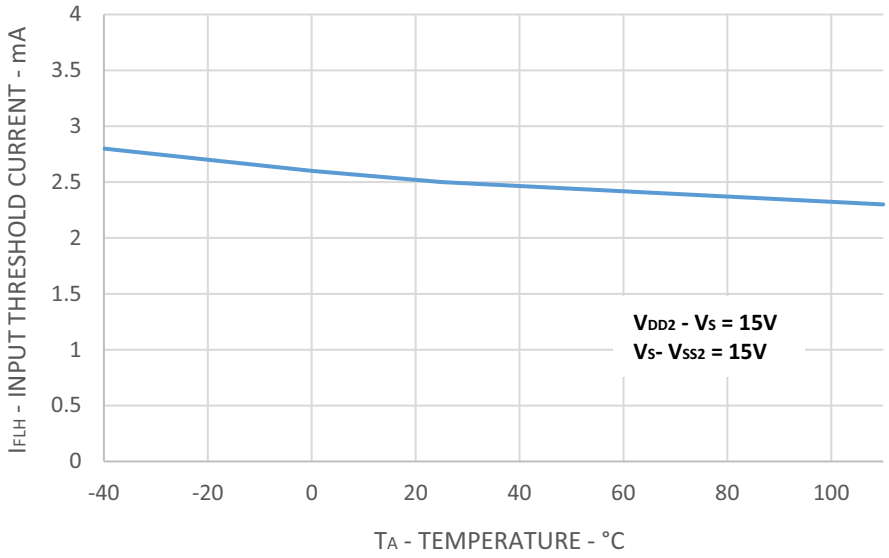


Figure 12: V_{OC} vs. Temperature

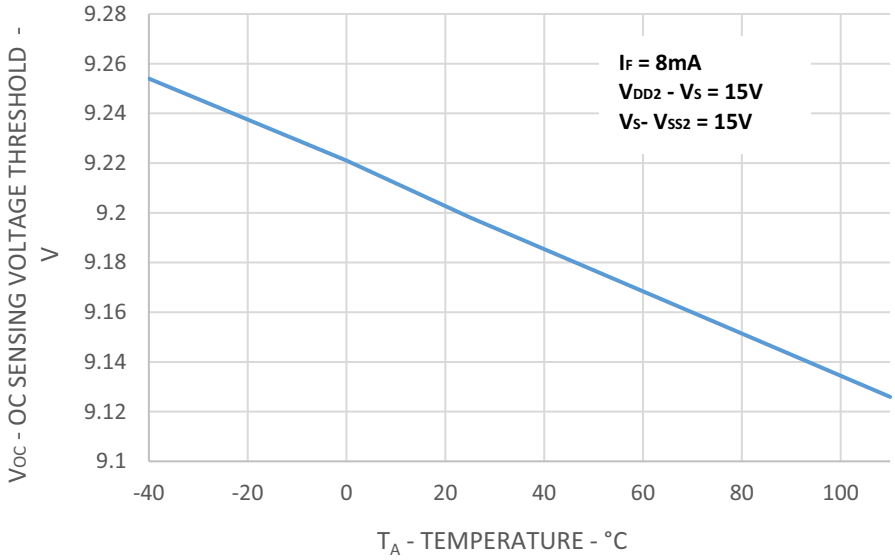


Figure 13: I_{CHG} vs. Temperature

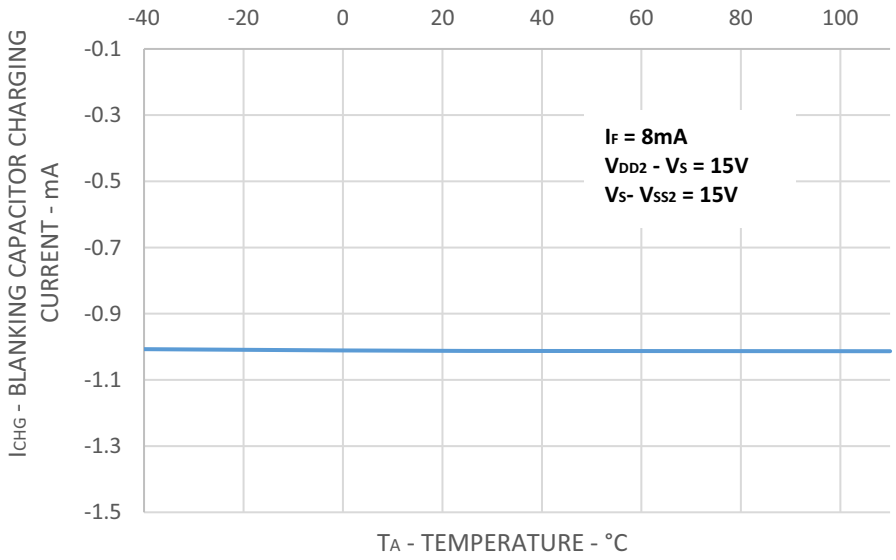


Figure 14: I_{DD1} vs. Temperature

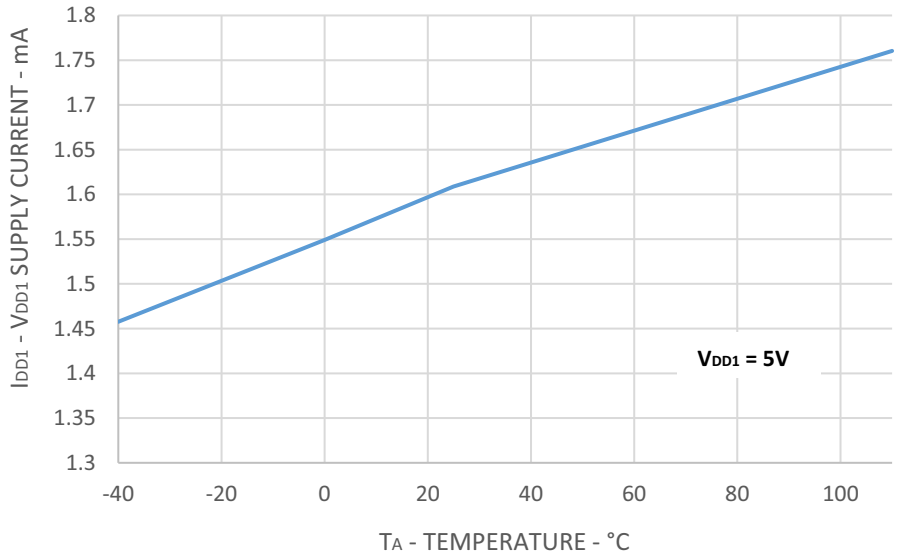


Figure 15: t_{PLH}/t_{PHL} vs. Temperature

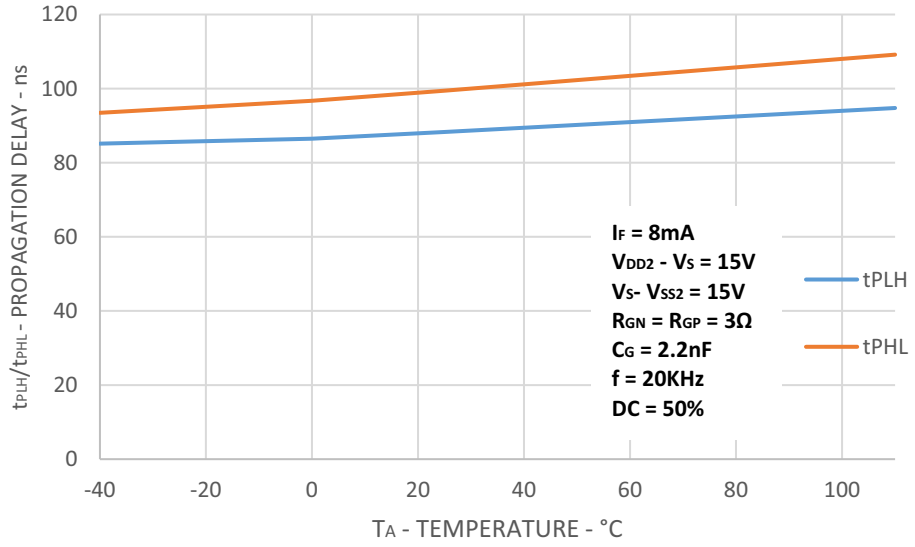


Figure 16: t_{PLH}/t_{PHL} vs. I_F

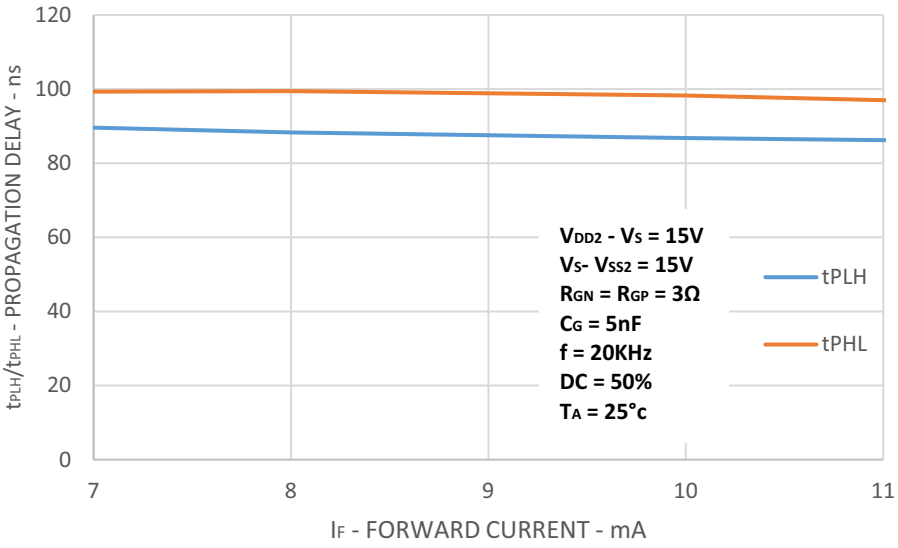


Figure 17: $t_{SS(LOW)}$ vs. Temperature

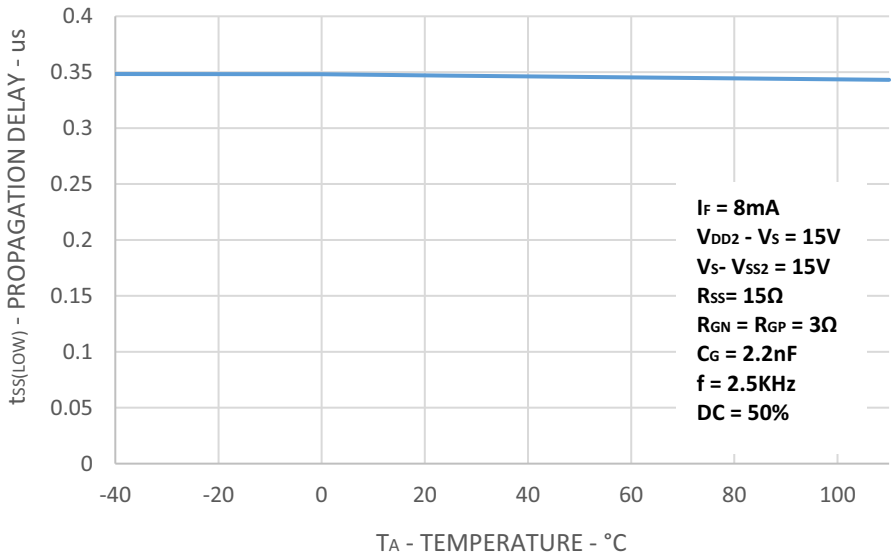
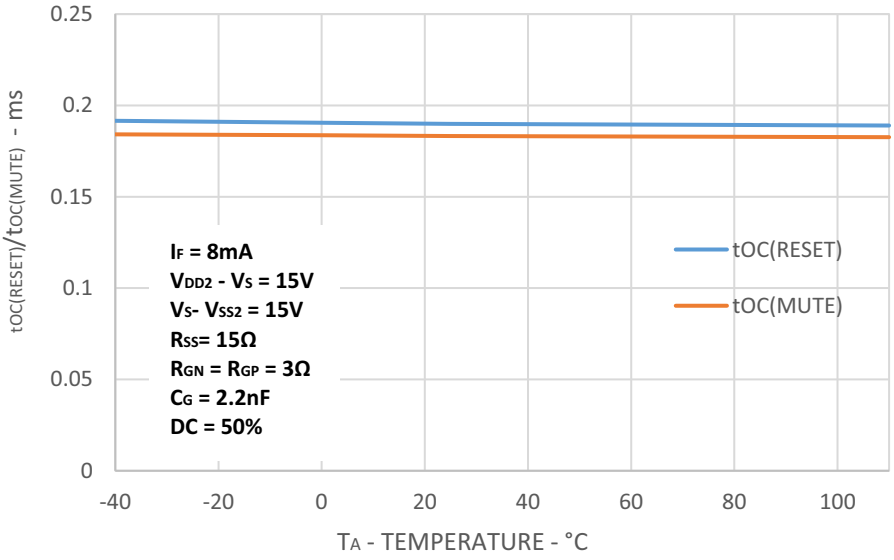


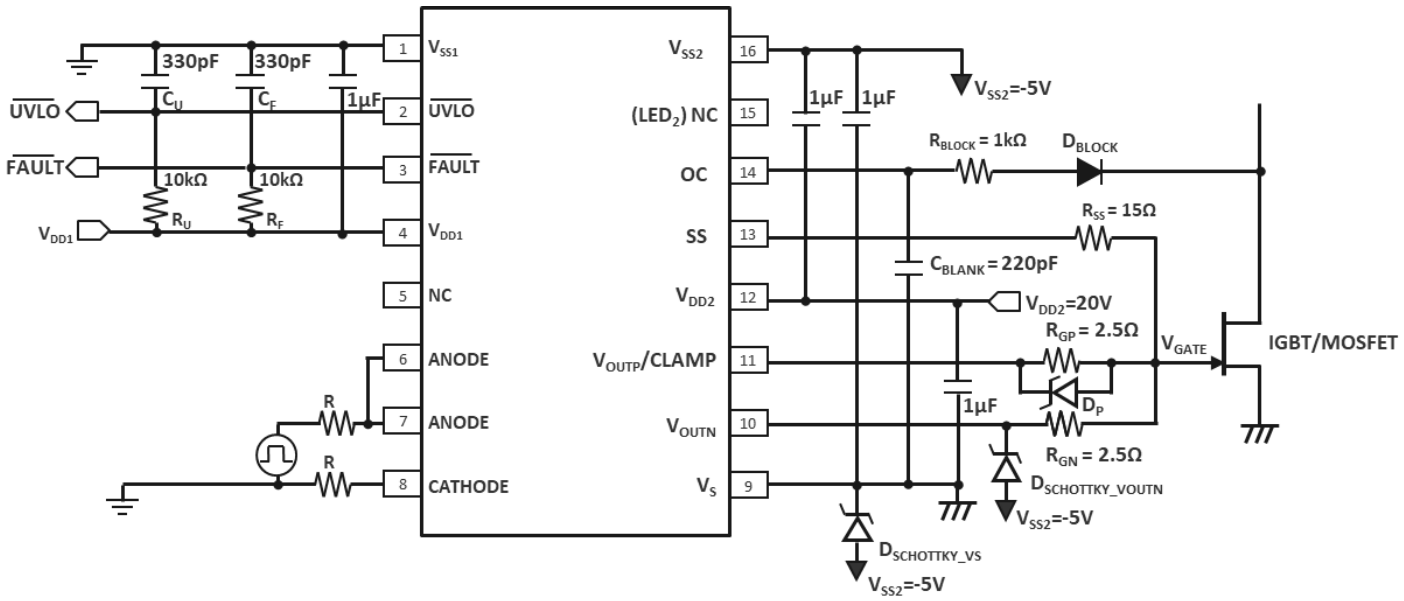
Figure 18: $t_{OC(RESET)}/t_{OC(MUTE)}$ vs. Temperature



Applications Information

Recommended Application Circuit

Figure 19: Recommended Application Circuit for ACPL-355JC



The ACPL-355JC has an LED input control input and two fault reporting mechanisms: namely V_{DD2} under voltage lockout (UVLO) and IGBT/MOSFET overcurrent (FAULT). These open drain FAULT and UVLO GFAULT outputs are connected to 10-kΩ pull-up resistors and 330-pF filtering capacitors and are suitable for wired OR applications. UVLO has the highest fault priority and follows by FAULT. The supplies (V_{DD1} and V_{DD2}) are connected to four 1-µF bypass decoupling capacitors to provide the large transient currents necessary during a switching transition.

The two resistors (R) connected to input LED's anode and cathode are recommended to be split in the ratio of 3:1. They balance the common mode impedances at the LED's anode and cathode, which helps to equalize the common mode voltage changes at the anode and cathode to give high CMR performance.

The HV blocking diode, D_{BLOCK}, R_{BLOCK}, and 220-pF blanking capacitor protect the OC pin and prevent false fault detection. During overcurrent fault condition, the IGBT/MOSFET is soft shutdown through the SS pin, and the rate of shut down can be adjusted by R_{SS}.

The gate resistor (R_{GP} and R_{GN}) limits gate current and indirectly controls the IGBT/MOSFET switching times. Schottky diode, D_P, is used together with the CLAMP function to shunt parasitic IGBT/MOSFET Miller current during the off cycle.

Schottky diodes, $D_{SCHOTTKY\_VOUTN}$ and $D_{SCHOTTKY\_VS}$, prevent V_{OUT} and V_S from going below V_{SS2} due to negative transient caused by parasitic inductance.

Output Control

The secondary output stage (V_{OUT}, CLAMP, OC, and SS) is controlled by the combination of V_{DD2}, LED current (I_F) and overcurrent (OC) conditions. Note that V_{DD1} provides the power supply to the device's fault reporting mechanisms. The secondary output stage (V_{OUT}, CLAMP, OC, and SS) remains operational when there is no V_{DD1} supply. The following table shows the logic truth table for these outputs. The logic level is defined by the respective threshold of each function pin.

	Inputs			Secondary Outputs			Fault Reporting Outputs	
Condition	**V_{DD2}**	**I_F**	**OC**	**V_{OUTN}**	**V_{OUTP}/CLAMP**	**SS**	**UVLO**	**FAULT**
V_{DD2} UVLO	Low	X	Not Active	Low	Low(CLAMP)	High-Z	Low	High
Overcurrent	High	Low	Not Active	Low	Low(CLAMP)	High-Z	High	High
	High	High	Active(OC)	High-Z	Low(CLAMP)	Low	High	Low
Normal Switching	High	Low	Not Active	Low	Low(CLAMP)	High-Z	High	High
	High	High	Active(no OC)	High-Z	High(VOUTP)	High-Z	High	High

Introduction to Overcurrent (or DESAT) Detection and Protection

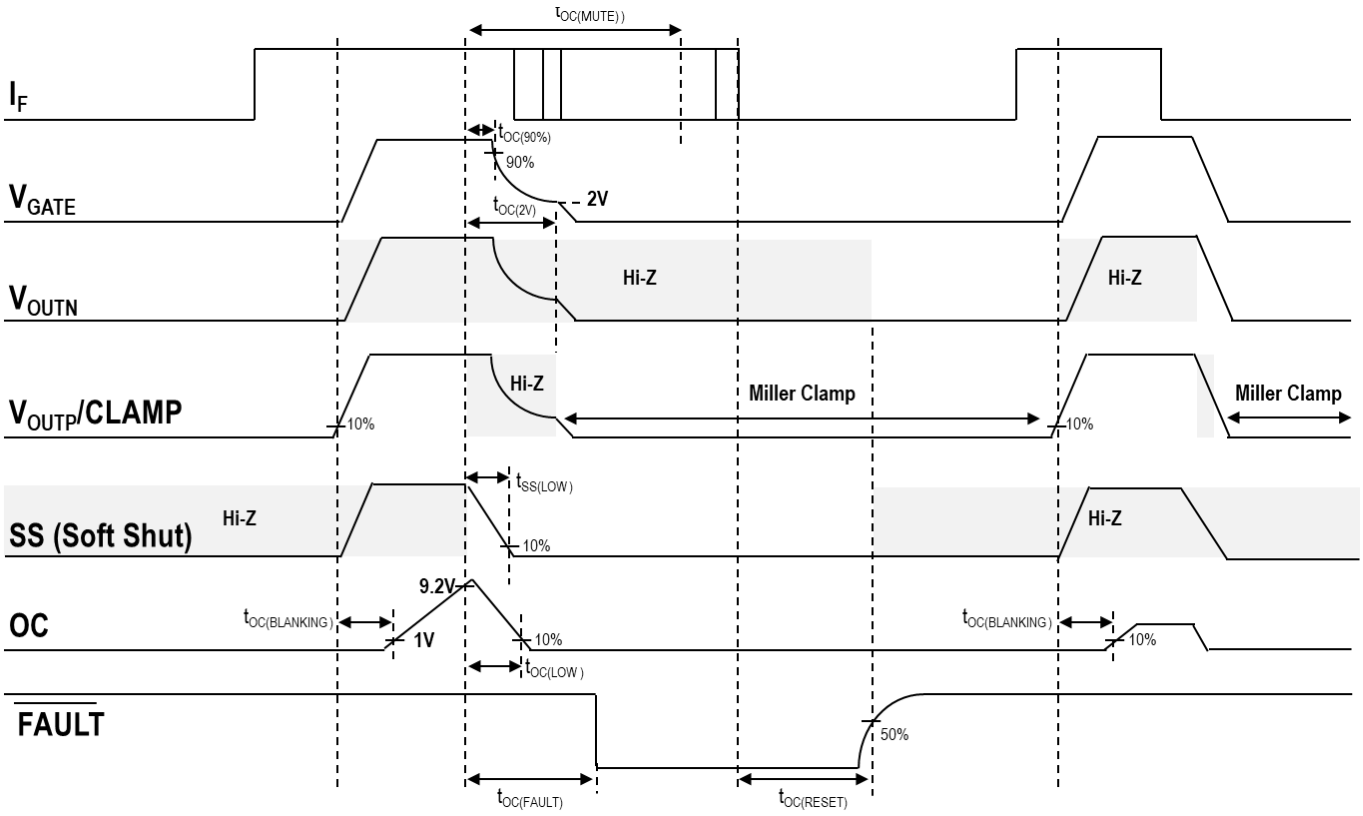
The power stage of a typical three-phase inverter is susceptible to several types of failures, most of which are potentially destructive to the power IGBT/MOSFET. These failure modes can be grouped into four basic categories: phase and/or rail supply short circuits due to user misconnect or bad wiring, control signal failures due to noise or computational errors, overload conditions induced by the load, and component failures in the gate drive circuitry. Under any of these fault conditions, the current through the IGBT/MOSFET can increase rapidly, causing excessive power dissipation and heating. The IGBT/MOSFET becomes damaged when the current load approaches the saturation current of the device, and the collector/drain to emitter/source voltage rises above the saturation voltage level. The drastically increased power dissipation very quickly overheats the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn-off the IGBT/MOSFET during a fault condition.

The ACPL-355JC OC pin monitors the drain/source voltages of the MOSFET or the collector/emitter voltages of the IGBT. When the MOSFET goes into overcurrent or IGBT into desaturation, these voltages exceed the predetermined threshold, V_{OC}. The ACPL-355JC triggers a local fault shutdown sequence and slowly reduces the high overcurrent to prevent damaging the voltage spikes. The fault is reported to controller through the isolated feedback channel of the ACPL-355JC. During the off state (no LED input) of the IGBT, the fault detect circuitry is disabled to prevent false fault signals.

Description of Operation during Overcurrent Condition

1. The OC terminal monitors IGBT's V_{CE} or MOSFET V_{DS} voltage.
2. When the voltage on the OC terminal exceeds 9.2V, the output voltages (V_{OUTP} and V_{OUTN}) go to Hi-Z state, and the SS pulls down the V_{GATE} at a slow rate adjustable using resistor R_{SS}.
3. FAULT output goes low, notifying the microcontroller of the fault condition.
4. The mcrocontroller takes appropriate action.
5. When $t_{OC(MUTES)}$ expires, LED input must be kept low for $t_{OC(RESET)}$ before fault condition is cleared. FAULT status returns to high and SS output returns to the Hi-Z state.
6. In the event LED goes high during $t_{OC(RESET)}$, the $t_{OC(RESET)}$ timing is reset, and the LED input must be kept low for another $t_{OC(RESET)}$ before the fault condition is cleared.
7. V_{GATE} starts to respond to the LED input after the fault condition is cleared.

Figure 20: Circuit Behaviors during Overcurrent Event



OC Fault Detection Blanking Time

The OC fault detection circuitry must remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the OC threshold. This time period, called the total OC blanking time, is controlled by the both internal OC blanking time $t_{OC(BLANKING)}$ (Figure 20) and external blanking time, determined by internal charge current, the OC voltage threshold, and the external blanking capacitor.

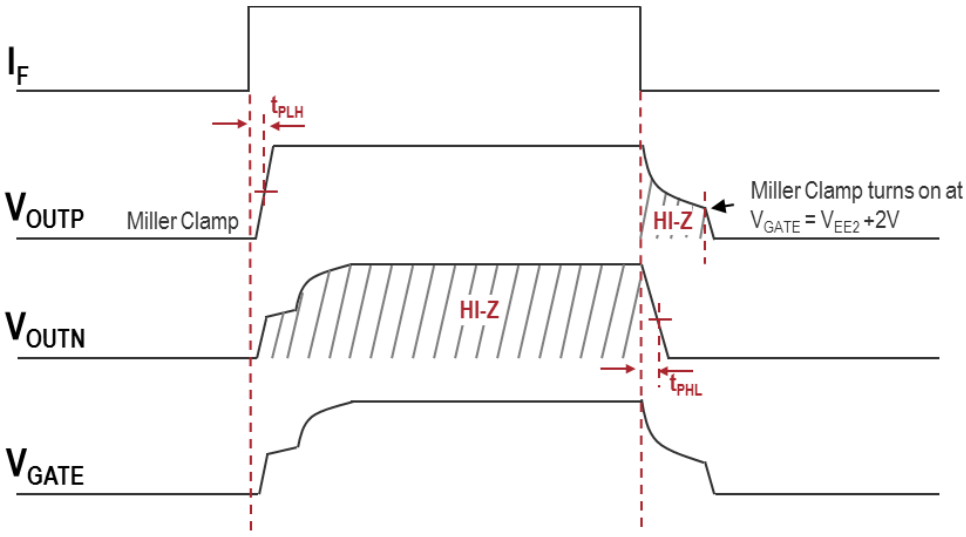
The total blanking time is calculated in terms of internal blanking time ($t_{OC(BLANKING)}$), external capacitance (C_{BLANK}), FAULT threshold voltage (V_{OC}), and blanking capacitor charge current (I_{CHG}) as the following:

$$t_{BLANK} = t_{OC(BLANKING)} + C_{BLANK} \times V_{OC} / I_{CHG}$$

Description of Gate Driver and Miller Clamping

The gate driver is directly controlled by the LED current. When LED current is driven high, the output of the ACPL-355JC is capable of delivering 10A maximum sourcing current to drive the IGBT's/MOSFET's gate. While the LED is switched off, the gate driver can provide 10A maximum sinking current to switch the gate off fast. Additionally, the miller clamping pull-down transistor is activated when output voltage reaches about 2V with respect to V_{SS2} to provide low impedance path to miller current as shown in Figure 21.

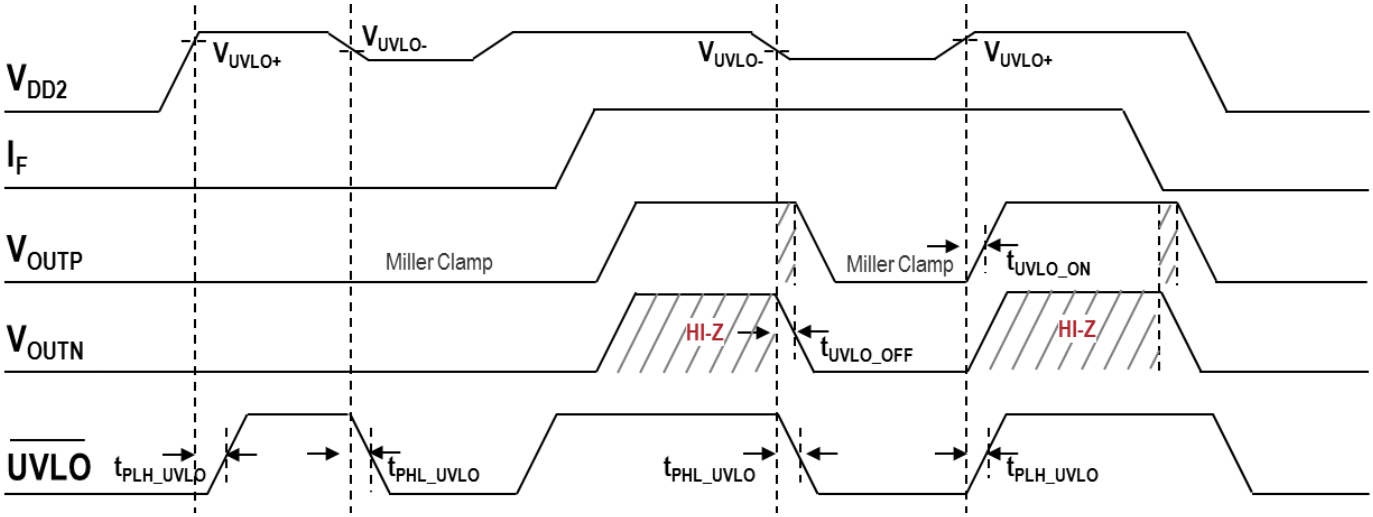
Figure 21: Gate Drive Signal Behavior



Description of Under Voltage Lockout

Insufficient gate voltage to IGBT/MOSFET can increase the turn-on resistance of IGBT/MOSFET, resulting a large power loss and IGBT/MOSFET damage due to high heat dissipation. The ACPL-355JC monitors the output power supply, V_{DD2}, constantly. When output power supply is lower than the under voltage lockout (UVLO), the threshold gate driver output shuts off to protect IGBT/MOSFET from low voltage bias. During power-up, the UVLO feature locks the gate driver output low to prevent unwanted turn on at lower supply voltage.

Figure 22: Circuit Behaviors at Power-Up and Power-Down



Selecting the Gate Resistor (R_G)

Step 1: Calculate R_G minimum from the $I_{O(PEAK)}$ specification. The IGBT/MOSFET and R_G in Figure 19 can be analyzed as a simple RC circuit with a voltage supplied by ACPL-355JC.

$$R_G \geq \frac{V_{DD2}-V_{SS2}}{I_{OPEAK}} - R_{OUTP(MIN)}$$
$$= \frac{20-(-5)V}{10A} - 0.4\Omega$$
$$= 2.1\Omega$$

or

$$R_G \geq \frac{V_{DD2}-V_{SS2}}{I_{OPEAK}} - R_{OUTN(MIN)}$$
$$= \frac{20-(-5)V}{10A} - 0.3\Omega$$
$$= 2.2\Omega$$

The external gate resistor, R_G, and internal minimum turn-on resistance, RDSON, ensure the output current will not exceed the device absolute maximum rating of 10A. In this case, we will use worst case $R_G \geq 2.5\Omega$.

Step 2: Check the ACPL-355JC power dissipation and increase R_G if necessary. The ACPL-355JC total power dissipation (P_T) is equal to the sum of the LED1 power (P_{E1}), input IC power (P_I), output IC power (P_O), and LED2 power (P_{E2}).

$P_T = P_{E1} + P_I + P_O + P_{E2}$

Assuming operation conditions of I_F = 8 mA, R_G = 2.5Ω, Max Duty Cycle = 80%, Q_G = 0.2 µC, f = 150 kHz, and T_A = 85°C.

Calculation of LED1 Power Dissipation

$P_{E1} = I_F \times V_F \times$ Duty Cycle
= 8 mA × 1.95V × 0.8 = 12.5 mW

Calculation of Input IC Power Dissipation

$P_I = I_{DD1}$ (Max) × $V_{DD}1$ (Recommended Max)
= 2.5 mA × 5.5V = 13.75 mW

Calculation of Onput IC Power Dissipation

$P_O = P_{O(BIAS)} + P_{O(SWITCHING)}$
$= I_{DD2} \times (V_{DD2} - V_{SS2}) + P_{HS} + P_{LS}$

$P_{HS} = (V_{DD2} \times Q_G \times f) * R_{OUTP(MAX)} / (R_{OUTP(MAX)} + R_G) / 2$

$P_{LS} = (V_{DD2} \times Q_G \times f) \times R_{OUTN(MAX)} / (R_{OUTN(MAX)} + R_G) / 2$

P_{HS} = (25V × 0.2 µC × 150 kHz) × 1.5Ω / (1.5Ω + 2.5Ω) / 2 = 140.63 mW

P_{LS} = (25V × 0.2 µC × 150 kHz) × 1.2Ω / (1.2Ω + 2.5Ω) / 2 = 121.62 mW

P_O = 8 mA × 25V + 140.63 mW + 121.62 mW
= 462.2 mW < 600 mW ($P_{O(MAX)}$ @ 95°C)

The value of 8 mA for I_{DD2} in the previous equation is the maximum I_{CC2} over the entire operating temperature range.

Because P_O is less than $P_{O(MAX)}$, R_G = 2.5Ω is correct for the power dissipation.

Calculation of LED2 Power Dissipation

$P_{E2} = I_F \times V_F \times$ Duty Cycle

$= 8\ mA \times 1.95V \times 0.1 = 1.56\ mW$

LED2 is designed to be driven by the output IC at 8-mA LED current at 10% duty cycle.

Thermal Calculation

Application and environmental designs for the ACPL-355JC must ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 125°C. The equations that follow are for the purposes of calculating the maximum power dissipation effect on junction temperatures.

LED1 Junction Temperature, T_{E1}

$= R_{21} \times P_{E1} + R_{22} \times P_I + R_{23} \times P_O + R_24 \times P_{E2} + T_A$

$= 10.91°C/W \times 12.5\ mW + 88.49°C/W \times 13.75\ mW + 17.08°C/W \times 462.2\ mW + 20.75°C/W \times 1.56\ mW + 85°C$

$= 94.3°C$

Input IC Junction Temperature, T_I

$= R_{11} \times P_{E1} + R_{12} \times P_I + R_{13} \times P_O + R_{14} \times P_{E2} + T_A$

$= 42.53°C/W * 12.5mW + 17.1°C/W * 13.75mW + 13.01°C/W * 462.2mW + 33.06°C/W * 1.56mW + 85°C$

$= 91.8°C$

Output IC Junction Temperature, T_O

$= R_{31} \times P_{E1} + R_{32} \times P_I + R_{33} \times P_O + R_{34} \times P_{E2} + T_A$

$= 13.62°C/W \times 12.5\ mW + 29.74°C/W \times 13.75\ mW + 33.9°C/W \times 462.2\ mW + 28.67°C/W \times 1.56\ mW + 85°C$

$= 101.3°C$

LED2 Junction Temperature, T_{E2}

$= R_{41} \times P_{E1} + R_{42} \times P_I + R_{43} \times P_O + R_{44} \times P_{E2} + T_A$

$= 17.56°C/W \times 12.5\ mW + 19.09°C/W \times 13.75\ mW + 16.51°C/W \times 462.2\ mW + 84.9°C/W \times 1.56\ mW + 85°C$

$= 93.2°C$

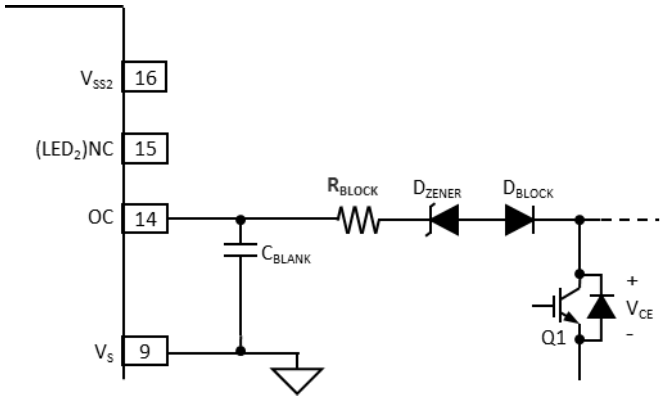
OC (Overcurrent) Blocking Diodes and Threshold

The D_{BLOCK} diode's function is to conduct forward current, allowing sensing of the IGBT's V_{CE} or MOSFET's V_{DS} when it is on and to block high voltages when it is off.

During IGBT/MOSFET switching off and towards the end of the forward conduction of the D_{BLOCK} diode, a reverse current flows for short time. This reverse recovery effect causes the diode to not be able to achieve its blocking capability until the mobile charge in the junction is depleted. During this time, there is commonly a very high dV/dt voltage ramp rate across the IGBT/MOSFET. This results in $I_{CHARGE} = C_{D\text{-}BLOCK} \times dV/dt$ charging current, which charges the blanking capacitor, C_{BLANK}. To minimize this charging current and avoid false overcurrent triggering, it is best to use fast response diodes.

In the application circuit shown in Figure 23, the voltage on pin 14 (OC) is $V_{OC} = (I_{CHG} \times R_{BLOCK}) + V_F + V_{CE}$, (where V_F is the forward ON voltage of D_{BLOCK} and V_{CE} is for example, the IGBT collector-to-emitter voltage). The value of $V_{OC,FAULT(TH)}$, which triggers OC to signal a FAULT condition, is nominally $9V – (I_{CHG} \times R_{BLOCK}) – V_F$. If desired, this threshold voltage can be decreased by using multiple D_{BLOCK} diodes or low voltage Zener diode in series. If *n* is the number of D_{BLOCK} diodes, the nominal threshold value becomes $V_{OC,FAULT(TH)} = 9.2V – (I_{CHG} \times R_{BLOCK}) – (n \times V_F)$. If a Zener diode is used, the nominal threshold value becomes $V_{OC,FAULT(TH)} = 9.2V – (I_{CHG} \times R_{BLOCK}) – V_F – V_Z$. In the case of using two diodes instead of one, diodes with half of the total required maximum reverse-voltage rating may be chosen.

Figure 23: OC (Overcurrent) Blocking Diodes and Threshold



OC Pin Protection Resistor

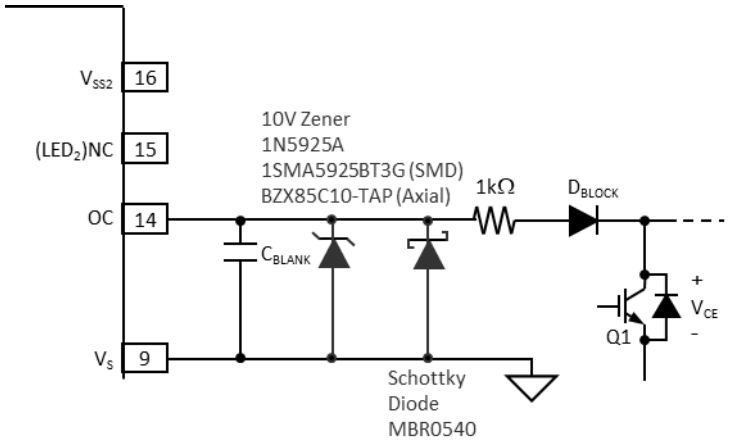
The freewheeling of flyback diodes connected across the IGBT/MOSFET can have large instantaneous forward voltage transients that greatly exceed the nominal forward voltage of the diode. This situation may result in a large negative voltage spike on the OC pin, which draws substantial current out of the driver if protection is not used. To limit this current to levels that do not damage the driver IC, insert a 1-kΩ resistor in series with the D_{BLOCK} diode.

False Fault Prevention Diodes

One of the situations that may cause the driver to generate a false fault signal is if the substrate diode of the driver becomes forward biased. This situation can occur if the reverse recovery spikes coming from the IGBT/MOSFET freewheeling diodes bring the OC pin below ground. Hence, the OC pin voltage is brought above the threshold voltage. These negative-going voltage spikes are typically generated by inductive loads or reverse recovery spikes of the IGBT/MOSFET's free-wheeling diodes. To prevent a false fault signal, connect a Zener diode and Schottky diode across the OC pin and V_S pin

This circuit solution is shown in Figure 24. The Schottky diode prevents the substrate diode of the gate driver optocoupler from being forward-biased while the Zener diode (value around 10V) prevents any positive high-transient voltage to affect the OC pin.

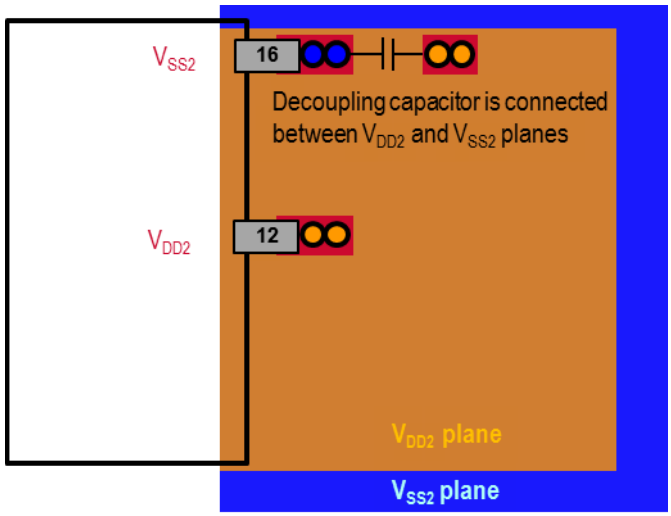
Figure 24: False Fault Prevention Diodes



Supply and Ground Planes Layout and Loading Conditions

At 10A rated high current switching, the decoupling capacitor must be close to the V_{DD} and V_{SS} pins. And due to the fast switching, large V_{DD} and V_{SS} planes should prevent noise by lowering the parasitic inductance. Without the V_{DD} and V_{SS} planes, connect the total load bigger than 2 nF during all applications or board testing to prevent output noise.

Figure 25: Recommended V_{DD2} and V_{SS2}, Supply and Ground Planes Layout



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