BDC-1001-A1

ACPL-355JC Evaluation Board for Half-Bridge SiC Module

Reference Manual

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Chapter 1: Introduction

The BDC-1001-A1 evaluation board features Broadcom® ACPL-355JC dual-output isolated gate drive optocouplers, used to drive half-bridge SiC MOSFET modules in industry-standard F2, 2B, and GM3 packages. It also features precision optically isolated ACPL-C87B amplifiers used for DC bus voltage measurement, and an ACPL-C72B isolation amplifier for SiC module output current measurement. BDC-1001-A1, shown in Figure 1, is developed to support Broadcom customers during their first steps in designing power converter applications with ACPL-355JC drivers.

Components were selected considering lead-free reflow soldering. The design was tested and verified with basic measurements described in this document; it is not qualified for the operation in the whole operating temperature range or lifetime. The board is subjected to functional testing only.

Figure 1: BDC-1001-A1 Evaluation Board

1.1 Design Features

BDC-1001-A1 includes the following features:

- Two isolated ACPL-355JC gate drive optocouplers with the following features:
  - 10A peak output current
  - 100-kV/µs common mode rejection
  - V_{IORM} = 2262, V_{PK} with CTI >600V
  - Short circuit current protection
  - Soft shutdown during fault
  - Two isolated feedback signals: FAULT (for short circuit current) and UVLO
- Two ACPL-C87B optically isolated amplifiers for DC bus voltage and temperature measurement:
  - 0V to 2V nominal input range
  - 100-kHz bandwidth
  - 3V to 5.5V wide supply range for output side
  - 15-kV/µs common-mode transient immunity
- ACPL-C72B isolation amplifier for output current measurement:
  - ±50-mV linear input range
  - ±0.5% high gain accuracy

  - 0.5-mV input offset voltage
  - 65-dB SNR
  - Excellent 0.03% linearity
  - 200-kHz wide bandwidth
  - 25-kV/µs common-mode transient immunity
  - 3V to 5.5V wide supply range
- The evaluation board supports the following half-bridge SiC MOSFET modules in F2/2B/GM3 packages:
  - NXH004P120M3F2PTHG
  - FF6MR12W2M1HP_B11
  - CAB006M12GM3
- DC bus and balancing and discharge resistors
- DC/DC power supply with current limit protection and thermal shutdown
- Isolated SMPS for gate drivers
- Access to FAULT and UVLO output signals for protection and control development purposes
- Access to PWM input signals
- Access to measurement signals (voltage and current)

1.2 Target Applications

Broadcom ACPL-355JC gate drive optocouplers target the following applications:

- Motor drives for industrial automation and robotics
- Power supplies and chargers
- Renewable energy inverters and storage

1.3 Warnings

The board operates at high voltages. Special care must be taken to avoid risk of injury and endangering life. While operating the board, the user must take into consideration following safety precautions:

- If the board is powered up, do not touch the board, especially the exposed metal parts.
- Pay attention to the maximum ratings.
- Use of protection cover made of insulating materials is mandatory.
- If the board is used with a power module to drive continuous load, the power module must be mounted on a heat sink. The board may rise to high temperatures and any contact with the human body must be avoided.
- The board itself does not provide dead-time generation. The recommended minimal dead time is 500 ns.

1.4 Disclaimer

This document contains information that should serve only as a reference for initial evaluation and implementation of Broadcom products. Broadcom does not take responsibility for using and implementing the products in other designs.

Chapter 2: System Description

2.1 Absolute Maximum Ratings

Absolute maximum ratings of the BDC-1001-A1 evaluation board are listed in Table 1. This table contains only key parameters. Constraints from ACPL-355JC, ACPL-C87B, and ACPL-C72B data sheets. Additionally, specifications of other key components must be considered when the BDC-1001-A1 is used.

Table 1: Absolute Maximum Ratings

Parameter	Value			Units	Description
	Min.	Typ.	Max.		
V_DC	—	600	800	V	DC link voltage rating
$I_{D,RMS}$	—	—	150	A	MOSFET half-bridge output current, RMS value
V_{DD}	1.8	5	5.5	V	Digital power supply
V_{DRV}	10	12	15	V	Gate drive power supply
Fault Logic	0	—	5	V	Fault logic level (output signal)
UVLO	0	—	5	V	Undervoltage lockout logic level (output signal)
Voltage	0	—	5	V	Single-ended analog output signal (DC link voltage measurement)
Temperature	0	—	5	V	Single-ended analog output signal (all temperature measurements)
Current	0	—	5	V	Single-ended analog output signal (power current measurement)
t	–20	—	85	°C	Working temperature of the board
t_{amb}	–10	—	60	°C	Ambient temperature

2.2 Functional Block Diagram

Figure 2 shows the BDC-1001-A1 block diagram.

Figure 2: BDC-1001-A1: Block Diagram

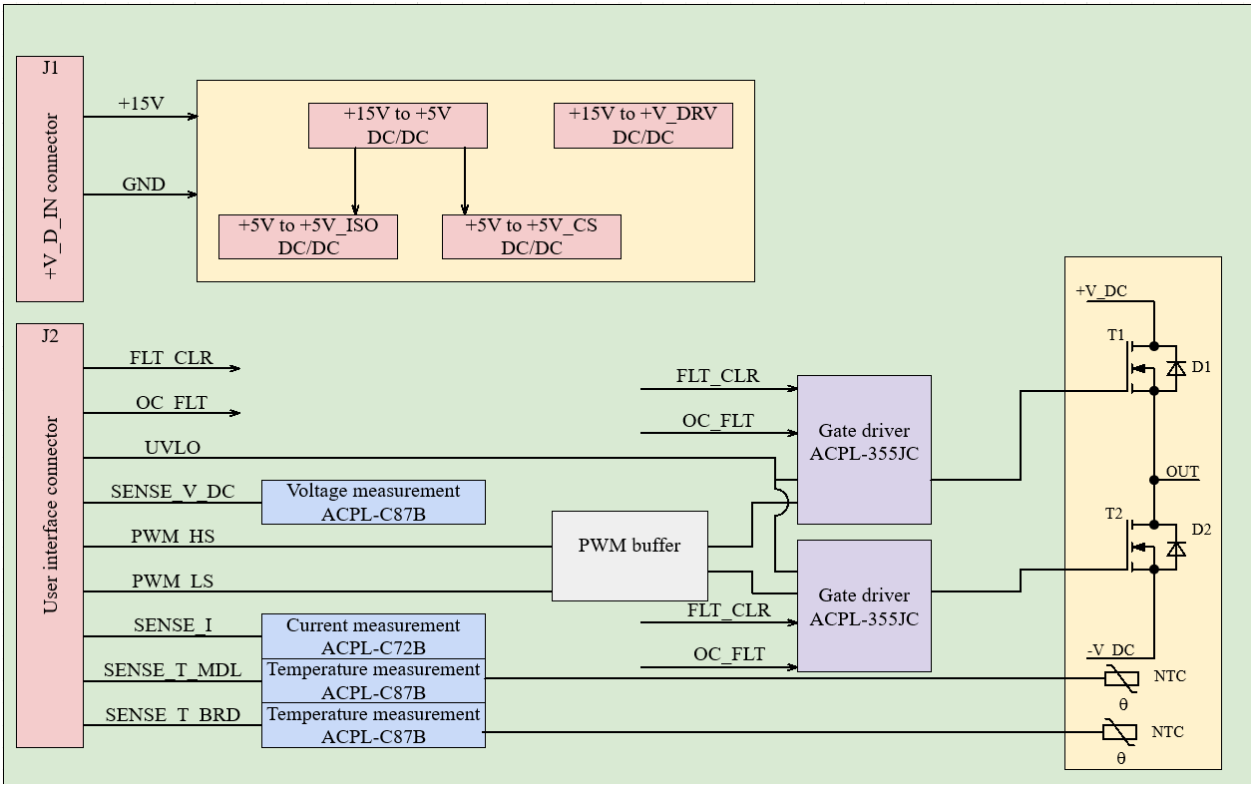
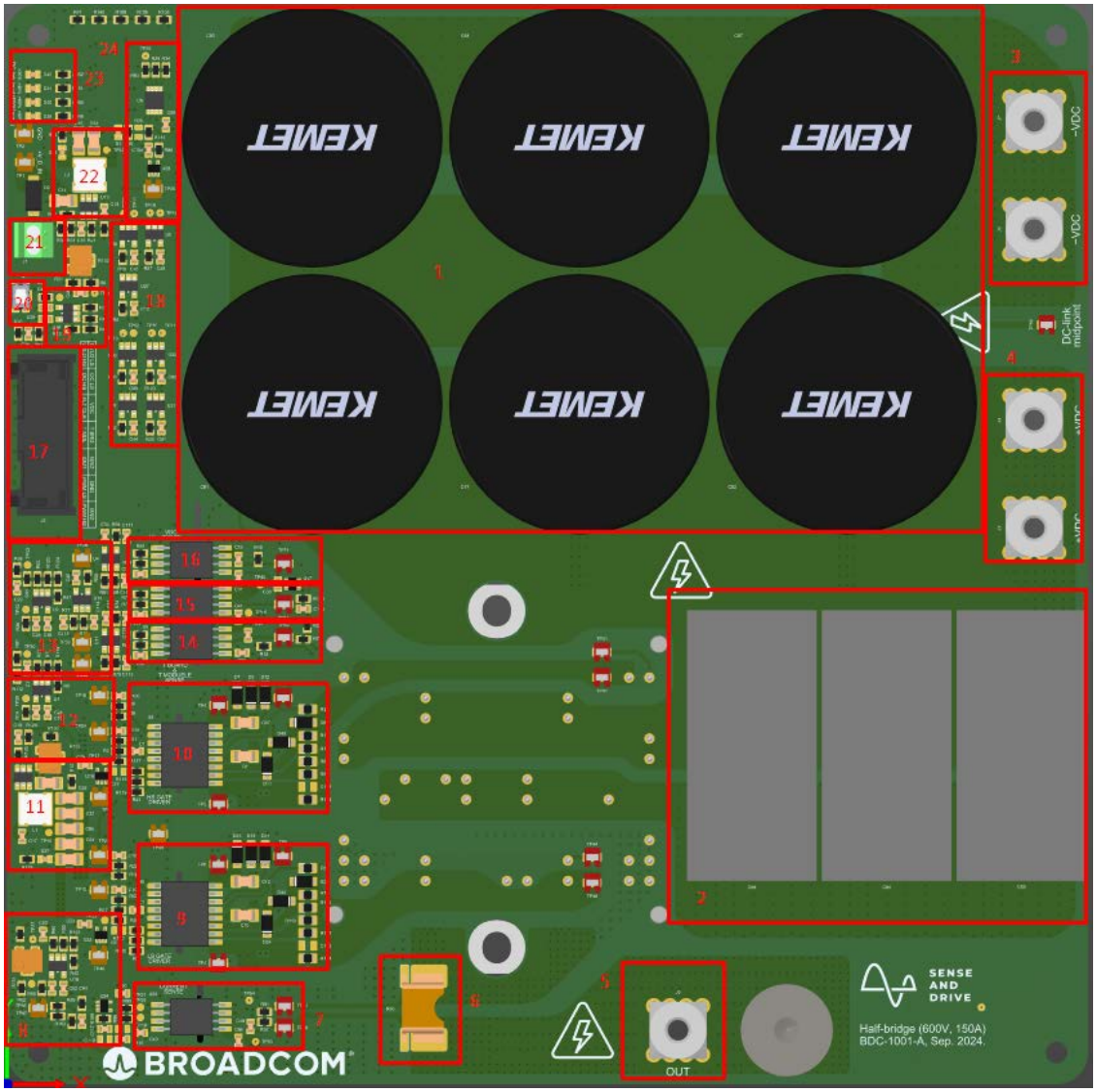


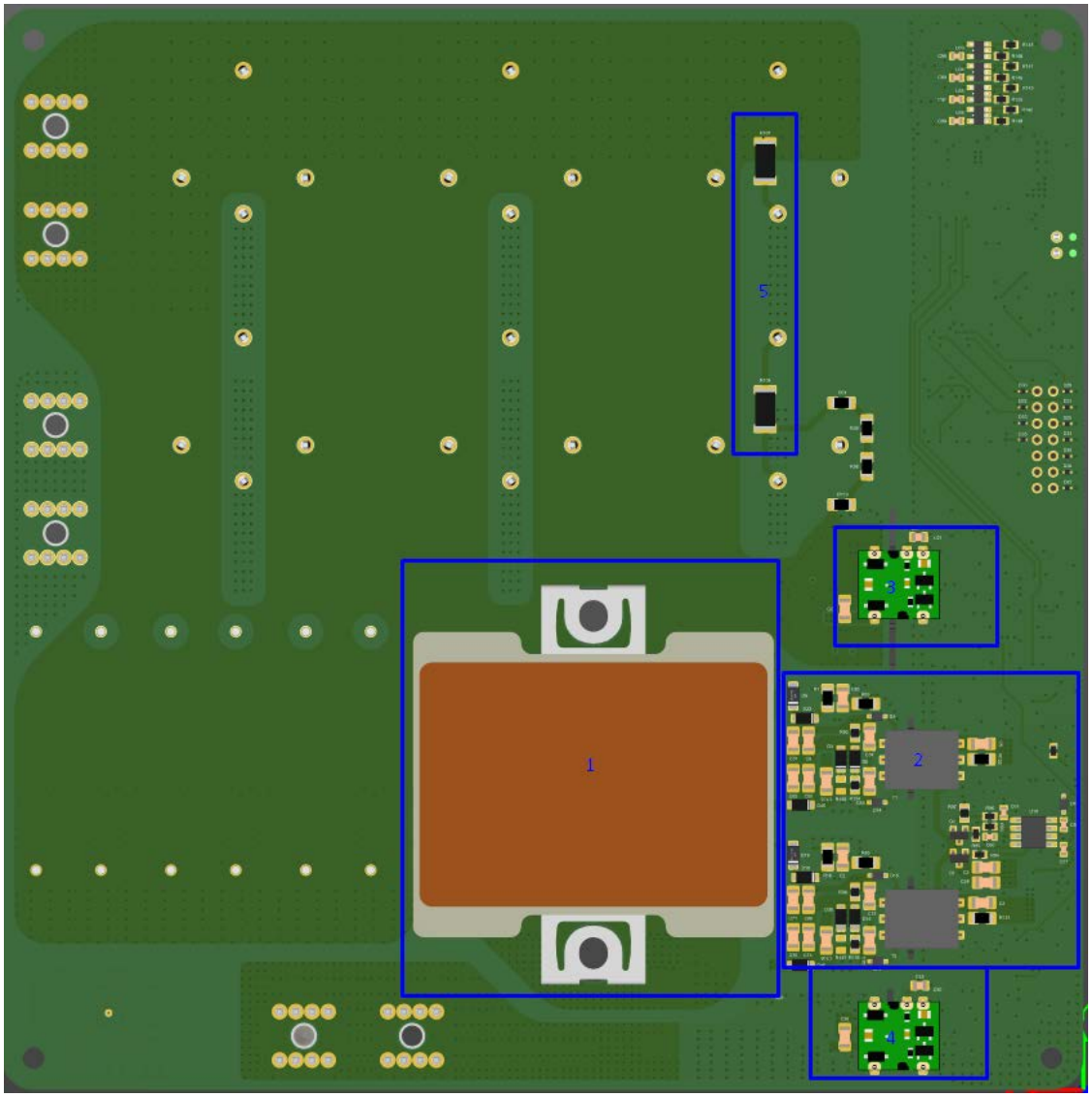
Figure 3: BDC-1001-A1: Overview of the Top of the Board



The numbered components in Figure 3 are as follows:

1 : Electrolytic DC link capacitors
2 : Film DC link capacitors
3 : Negative DC link input
4 : Positive DC link input
5 : Power output
6 : Shunt resistor
7 : Current sense circuit (ACPL-C72B)
8 : Overcurrent comparator
9 : Low-side gate driver
10 : High-side gate driver
11 : DC/DC regulator (15V to +V_DRV)
12 : Over temperature comparator for the NTC temperature
13 : Over temperature comparator for the board temperature
14 : Isolated amplifier (ACPL-C87B) for NTC temperature measurement
15 : Isolated amplifier (ACPL-C87B) for board temperature measurement
16 : Isolated amplifier (ACPL-C87B) for voltage measurement
17 : Signal connector
18 : Protection logic
19 : Overvoltage comparator
20 : Reset (clear) button
21 : Digital power supply connector
22 : DC/DC regulator (15V to 5V)
23 : LEDs for indication of the DC link voltage level
24 : Fault logic

Figure 4: Overview of the Bottom of the Board BDC-1001-A1



The numbered components in Figure 4 are as follows:

1 : MOSFET half-bridge module

2 : Gate driver power supplies

3 : DC/DC regulator (+5V to +5V_ISO)

4 : DC/DC regulator (+5V to +5V_CS)

5 : Balancing resistors of the DC link

2.3 Pin Assignment

The J1 power supply connector supplies all integrated circuits and provides gate driver voltage supply. The pin assignment is shown in Table 2.

Table 2: Power Supply Connector Pin Assignment

Pin	Label	Description
1	+15V	Power supply for low voltage side (digital side)
2	GND	Ground reference

Six screw terminals (J3, J4, J5, J6, J7 and J8) connect the DC bus voltage and the output of the power module (AC output of the MOSFET half-bridge). The pinout is shown in Table 3.

Table 3: Power Terminal Pin Assignment

Pin	Label	Description
J3	+V_DC	DC link power supply, positive terminal
J4	+V_DC	DC link power supply, positive terminal
J5	OUT	Power output
J6	OUT	Power output
J7	–V_DC	DC link power supply, negative terminal
J8	–V_DC	DC link power supply, negative terminal

Table 4 lists pins that are assigned within a signal interface connector (J2).

Table 4: Signal Connector Pin Assignment

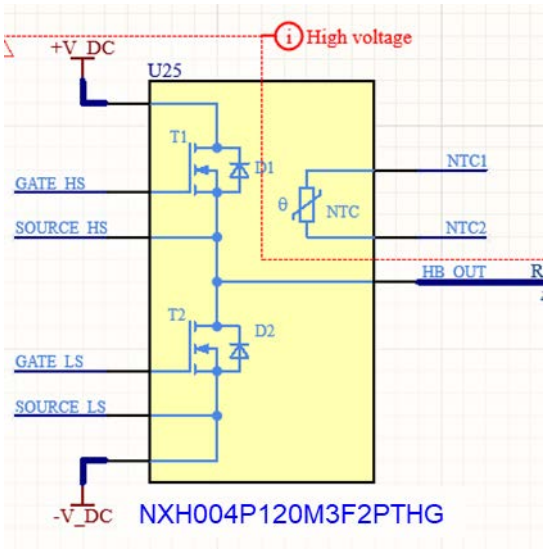
Pin	Label	Description
1	UVLO_HS	Undervoltage lockout from high-side driver (output, active low)
2	UVLO_LS	Undervoltage lockout from low-side driver (output, active low)
3	OC_FLT_HS	Overcurrent from high-side driver (output, active low)
4	OC_FLT_LS	Overcurrent from low-side driver (output, active low)
5	FLT_CLR	Hardware protection fault clear (input)
6	SENSE_V_DC	DC-link voltage measurement (output)
7	SENSE_T_MDL	Module temperature measurement (output)
8	SENSE_T_BRD	Board temperature measurement (output)
9	SENSE_I_OUT	Output current measurement (output)
10	GND	Digital ground reference
11	PWM_LS	PWM for low-side driver switch (input)
12	GND	Digital ground reference
13	PWM_HS	PWM for high-side driver switch (input)
14	GND	Digital ground reference

2.4 Schematic Design and Key Components

2.4.1 SiC MOSFET Module

Figure 5 shows the SiC module.

Figure 5: Onsemi F2 Half-Bridge SiC Module Schematic



The SiC module U25 consists of two Si MOSFETs in half-bridge topology with integrated NTC thermistor. The module is rated for a drain-source voltage of 1200V and a nominal drain current of 200A, with a peak rating of 400A, making it well suited for high-power applications. The circuit also includes NTC thermistors for temperature-dependent monitoring. The values in Table 5 suggest that the NTC resistance varies with temperature, allowing thermal monitoring and protection mechanisms.

The module uses PressFIT connection technology, which ensures secure electrical connections, reduces the need for soldering, and improves mechanical properties. Additionally, the module is designed with integrated mounting clamps and an improved ceramic substrate, ensuring efficient heat dissipation and consistent durability.

Table 5: Characteristics of the NTC Thermistor within the SiC MOSFET Module

Temperature Measured	NTC Resistance
0°C	14 kΩ
50°C	2.086 kΩ
120°C	303.1Ω
140°C	196Ω
150°C	100Ω

2.4.2 Gate Driver Power Supply

This schematic represents an isolated power supply circuit designed for gate drivers, ensuring the right voltage levels and isolation for high-side and low-side switching applications.

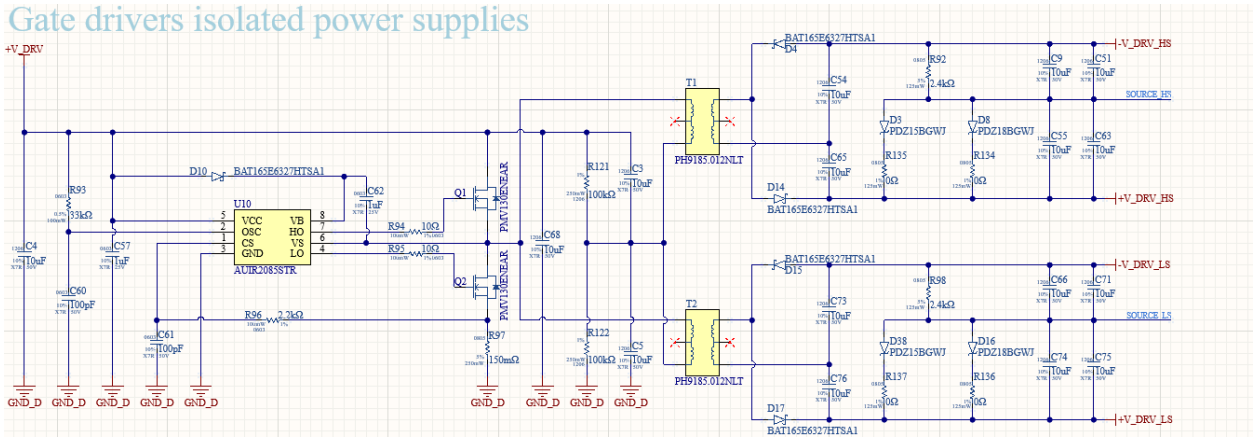
The circuit shown in Figure 6 begins with an AUIR208SSTR gate driver IC labeled U10, which is powered by a voltage source labeled +V_DRV. This integrated circuit has a bootstrap architecture to drive high-side and low-side transistors (Q1 and Q2). BAT1656327HTSA1 diode D10 serves as a fast recovery diode for bootstrap charging.

Q1 and Q2 form a push-pull driver stage, which generates an AC voltage to drive the PH9185.012NLT transformers T1 and T2. These transformers provide galvanic isolation while maintaining the required voltage levels for the high-side and low-side gate drivers. The switching action is controlled by the signals coming from U10.

On the secondary side of the transformers, rectification and filtering occur. BAT1656327HTSA1 diodes rectify the AC signal into DC voltage while PDZ15BGWJ diodes help regulate the output voltage to a stable level. Output capacitors smooth out the rectified DC voltage, providing clean and stable +V_DRV_HS and +V_DRV_LS power rails. The nodes labeled +V_DRV_HS- and +V_DRV_LS- represent the negative rails of the isolated gate driver power supplies for the high-side and low-side switches. These serve as the local ground references for their respective isolated supplies and should not be directly connected to the system ground (GND_D) to maintain isolation.

The high-side driver output is labeled SOURCE_HS, while the low-side output is labeled SOURCE_LS. These points are crucial for ensuring proper gate drive voltages in applications like half-bridge or full-bridge inverters.

Figure 6: Power Supply for Gate Drivers



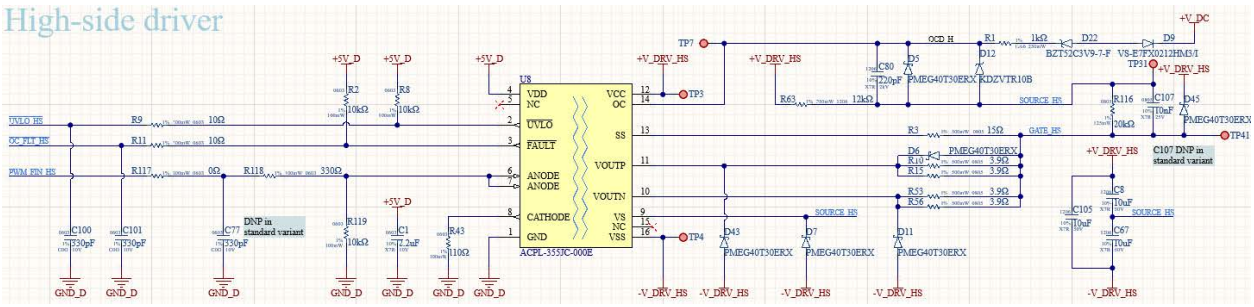
2.4.3 Gate Driver

The high-side gate driver is built around U8 (ACPL-335J-000E) shown in Figure 7, an isolated gate driver with fault detection and under-voltage lockout (UVLO) functionality. The driver is powered by the +V_DRV_HS voltage, which is the isolated gate drive supply generated by the transformer-based power supply circuit.

The PWM_HS input signal comes from the control circuitry and passes through resistors R117 that is 0Ω and can be switched if additional RC filtering is needed (with C77 that is DNP - do not place while assembling) and R118 that is part of the resistor voltage divider with R119, which limits current and voltage and protects the optocoupler input. Capacitors C102 and C103 are used for filtering and signal integrity. The anode and cathode terminals of the driver receive the differential input signals and control the output stage accordingly; the anode signal is coming from the 14-pin connector, while the cathode pin of the driver is grounded via the R43 resistor.

The output section of the driver is connected to a circuit to ensure that the gate drive signals are properly conditioned. The transistors are powered by +V_DRV_HS, and their source terminals are connected to SOURCE_HS, which serves as the switching node. The bootstrap diodes help maintain the necessary voltage levels for driving the high-side transistor effectively. The UVLO and FAULT pins provide protection by shutting down the driver if the supply voltage falls below a safe operating level.

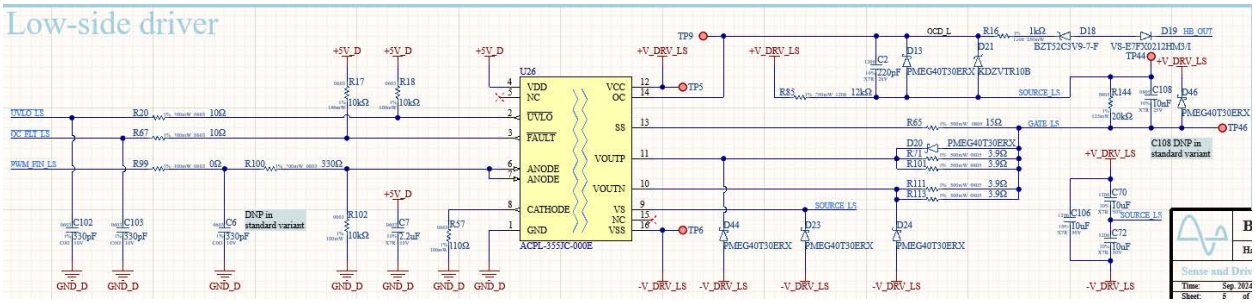
Figure 7: High-Side Driver



The low-side gate driver shown in Figure 8 follows the same design as the high-side driver, using another ACPL-335J-000E (U26). It receives its PWM_LS control signal through R99, C6, R100, and R102, which provide similar signal conditioning.

The output section is powered by +V_DRV_LS, the isolated power rail dedicated to the low-side driver. The gate drive network includes resistors and diodes, which ensure optimal drive conditions for the low-side transistor.

Figure 8: Low-Side Driver



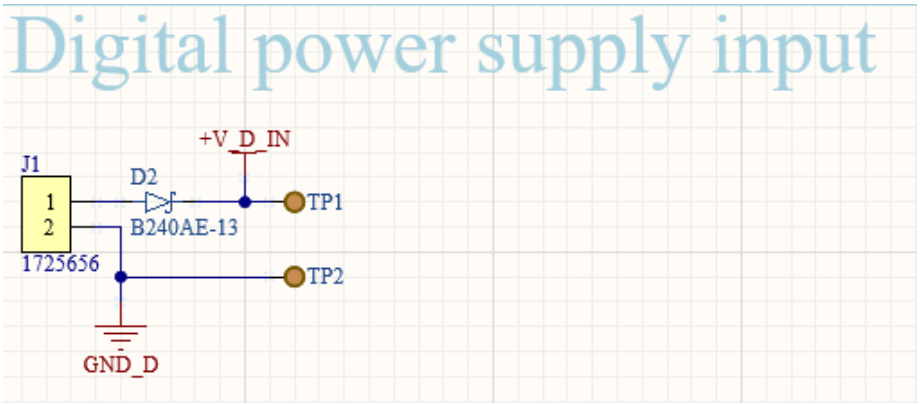
The isolated power supplies ensure that the high-side and low-side transistors operate independently while maintaining proper switching synchronization.

The ACPL-335J driver is capable of directly driving most power MOSFET switches without requiring an external push-pull stage with maximal output current of 10A. It features a CLAMP function that prevents parasitic turn-on due to Miller current during turn-off transitions. Additionally, the driver incorporates over-current (OC) protection, under-voltage lockout (UVLO), and a soft shutdown mechanism during an OC fault.

2.4.4 Digital Power Supply

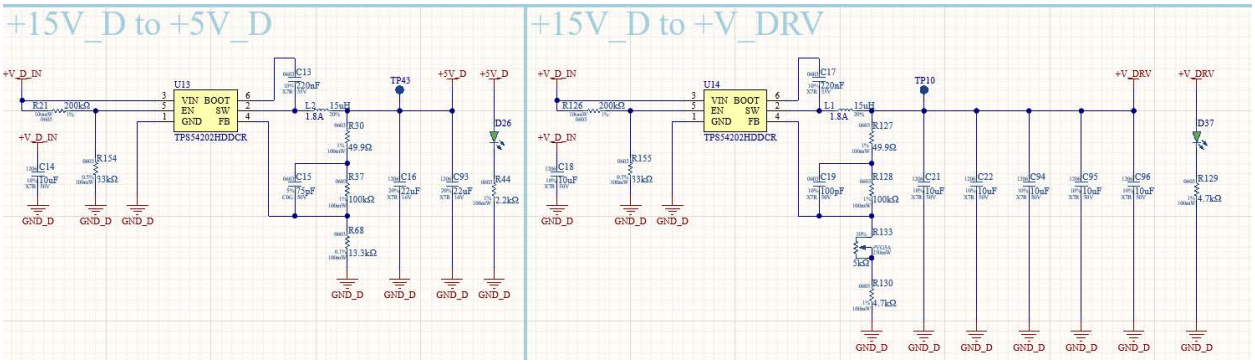
The digital power supply connector is shown in the schematic in Figure 9. The digital power supply section is designed to provide stable voltage rails for the circuit. It features a 1725656 connector with a 2.54-mm pitch, supplying the +V_D_IN voltage, which is protected by a B240AE-13 Schottky diode between pin 1 and the +V_D_IN power rail. The other pin of the connector is ground reference. Both power and ground connections have dedicated test points for monitoring.

Figure 9: Schematic: Digital-Side Power Supply Input Connector



The schematic in Figure 10 shows the voltage rails. From +V_D_IN, two TPS54202HDDCR switching regulators generate the required voltage rails. The first regulator steps down +V_D_IN to +5V_D using a resistor divider of 100 kΩ and 13.3 kΩ, ensuring +5V_D output. To indicate that +5V_D is present, a green LED is included, connected in series with a 2.2-kΩ resistor (R44). The second regulator steps down +V_D_IN to +V_DRV, but the exact output voltage is adjustable. Its resistor divider consists of a 100-kΩ resistor and a combination of a 4.7-kΩ resistor (R130) in series with a trimmer, allowing fine tuning of the +V_DRV voltage level. A green LED with a 4.7-kΩ resistor (R129) is used to indicate the presence of +V_DRV.

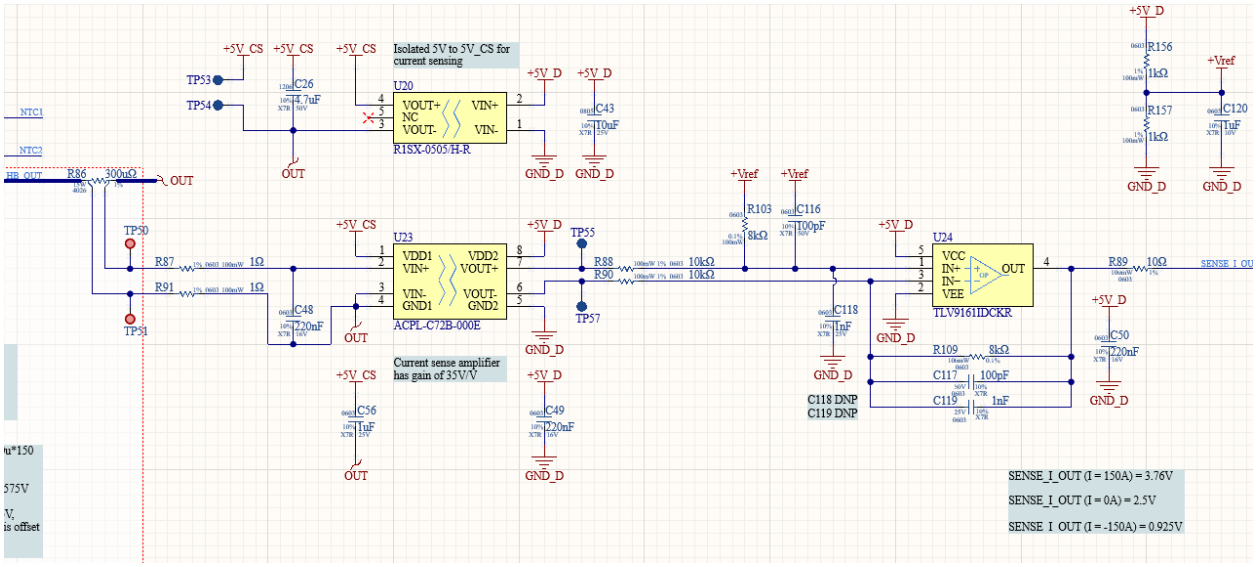
Figure 10: Schematic: Digital Voltage Rails



2.4.5 SiC MOSFET Module Current Measurement

Figure 11 shows the current measurement schematic of the SiC MOSFET module current.

Figure 11: Schematic: Current Measurement Circuit



The current measurement is realized through a shunt resistor with an isolated current sense amplifier.

For a maximum current of 150A, the shunt resistor (R86) is 300 µΩ, which leads to a voltage drop:

V_{R_SENSE} = 300 µΩ × 150A = 45 mV

The power dissipation for a current maximum across this resistor is as follows:

$P_{DISS\_MAX} = V_{R\_SENSE} \times I_{MAX}$ = 45 mV × 150A = 6.75W

The current amplifier output is 1.575V maximum for 150A.

The current sense amplifier ACPL-C72B-000E (U23) has a gain of 35V/V with both differential input and output. Together with a single operational amplifier TLV9161IDCKR (U24) they propagate the SENSE_I_OUT signal that corresponds to the current measured as shown in the formula below, where 0.8 is gain of the opamp and 2.5V is offset of the measurement:

$SENSE\_I\_OUT_{MAX}$ = 1.575V × 0.8V/V + 2.5V = 3.76V

To ensure accurate current measurement while maintaining isolation, R1SX-0505/H-R (U20), a 5V isolated DC/DC converter, provides an isolated 5V supply for the current sensing stage. This isolation is crucial to prevent ground loops and ensure reliable measurement.

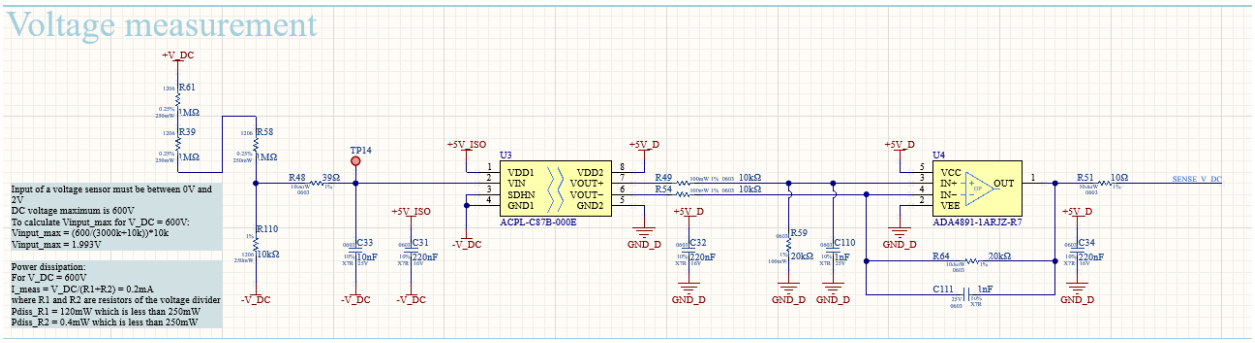
2.4.6 DC Bus Voltage Measurement

The schematic in Figure 12 shows voltage measurement. This voltage measurement circuit is designed to measure a high DC voltage and scale it down to a safe level suitable for a voltage sensor or microcontroller input. The circuit consists of a resistive voltage divider, an ACPL-C87B-000E isolation amplifier (U3), and an AD4891-1ARJZ-R7 operational amplifier (U4) for signal conditioning.

The voltage divider at the input consists of resistors R61, R39, and R58, all rated at 1 MΩ, and resistor R110 at 10 kΩ. This divider scales down the high voltage, ensuring that the input to the isolation amplifier remains within its acceptable range. The calculated maximum input voltage after the divider for a 600V DC input is approximately 1.993V, keeping it safely within the 0V to 2V range required by the isolation amplifier. A test point (TP14) is placed at the output of the voltage divider, allowing for direct measurement of the scaled-down voltage before it enters the isolation amplifier.

The ACPL-C87B-000E isolation amplifier (U3) ensures electrical isolation between the high-voltage side and the low-voltage signal processing circuitry. It takes the voltage from the divider and transfers it across an optical isolation barrier while maintaining signal integrity. The isolated voltage output from U3 is then fed into the AD4891-1ARJZ-R7 operational amplifier. This amplifier is used for signal buffering and conditioning and it ensures that the final output voltage, SENSE V_DC, is a clean and reliable signal.

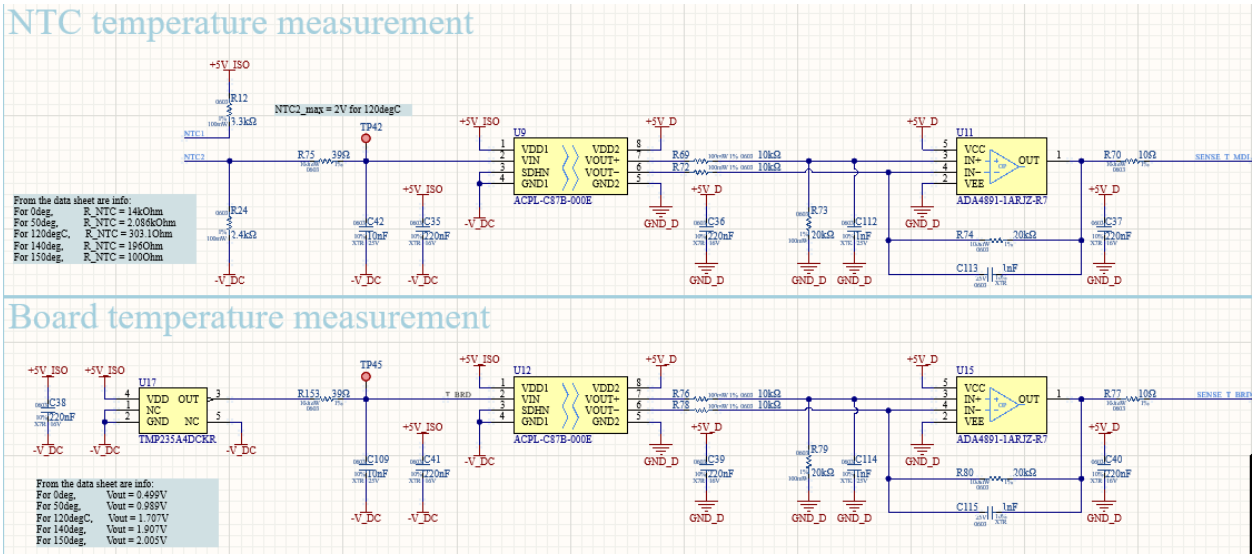
Figure 12: Schematic: Voltage Measurement Circuit



2.4.7 Temperature Measurement

The circuit in Figure 13 consists of two temperature measurement setups: one for an NTC thermistor in the half-bridge module and another for a separate temperature sensor located on the board.

Figure 13: Schematic: Board and Module Temperature Measurement Circuits



In the first temperature measurement setup, the NTC thermistor is used as the sensing element. It forms a voltage divider with a fixed resistors of 3.3 kΩ and 2.4 kΩ, producing a voltage that varies with temperature. The thermistor's resistance decreases as temperature increases, leading to a higher voltage drop across the fixed resistor. This voltage signal passes through an ACPL-C87B-000E optocoupler (U9), which provides galvanic isolation. After isolation, the signal is further conditioned using an ADA4891-1ARJZ-R7 instrumentation amplifier (U11) which amplifies the signal to a level suitable for ADC conversion and makes the signal single-ended.

The second temperature measurement setup involves a TMP235A4DCKR temperature sensor that monitors board temperature and provides a voltage output directly: T_BRD. Unlike the NTC thermistor, this sensor exhibits a more linear response, simplifying signal interpretation. The sensor's output voltage dependence is shown in Table 6.

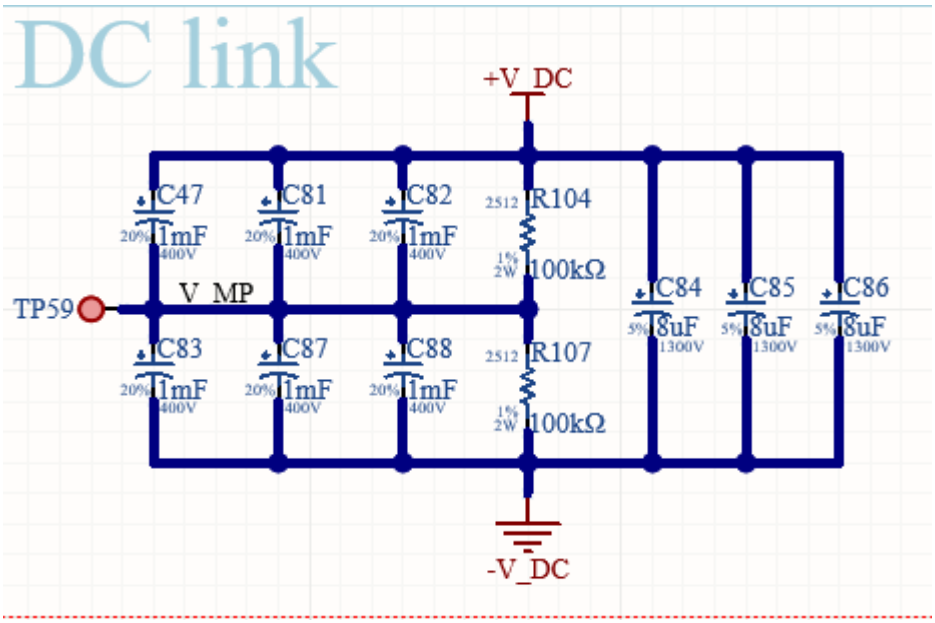
Table 6: TMP235 Temperature Sensor Characteristics

Temperature (°C)	Voltage Output of the Sensor (V)
0	0.499
50	0.989
120	1.707
140	1.907
150	2.005

2.4.8 DC Link BUS Voltage

The DC link circuit shown in the schematic in Figure 14 is important for stabilizing the voltage supply for the power stage of the system. It consists of multiple electrolytic and film capacitors with discharge resistors, which together make a reliable energy storage and voltage balancing.

Figure 14: Schematic: DC Link Capacitor Bank with Resistors for Balancing



The electrolytic capacitors, rated at 1 mF and 400V each, are separated into two sets of three capacitors. One set is connected from the positive DC rail to the midpoint, while the other connects from the midpoint to the negative DC rail. This configuration effectively creates a split DC link. A TP59 test point is placed at the midpoint, allowing direct measurement of the voltage at this node. This can be useful for ensuring the balance in the capacitor bank.

In parallel with the electrolytic capacitors, three film capacitors rated at 8 µF and 1300V are included. Unlike electrolytic capacitors, which are optimized for bulk energy storage, film capacitors are there to handle high-frequency ripples and transient voltage spikes.

In the DC link there are two 100-kΩ resistors, R104 and R107. When the system is turned off, these resistors slowly drain the charge from the capacitors, bringing the voltage to a safe level over time.

2.4.9 Protection Circuits and Comparators

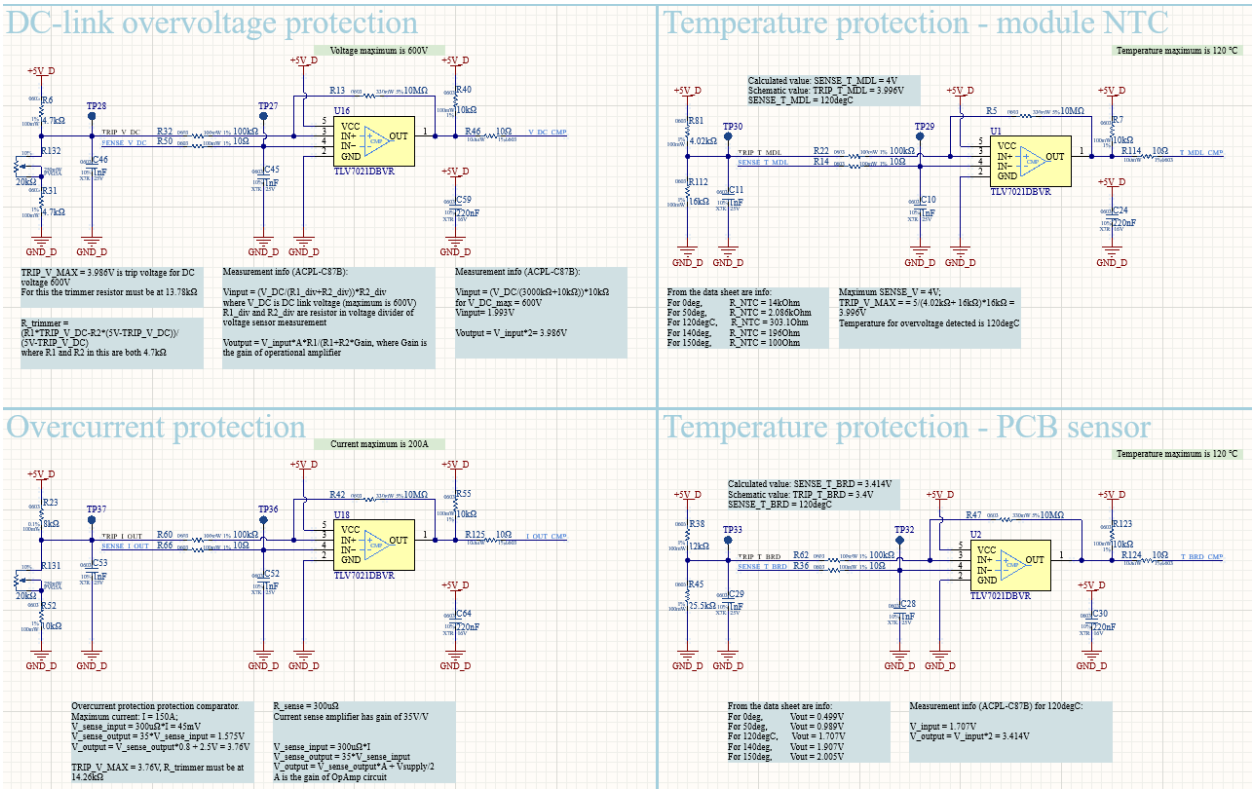
The schematic in Figure 15 consists of four protection circuits designed for different aspects of an electrical system: DC-link overvoltage protection, overcurrent protection, temperature protection of the NTC, and temperature protection on the temperature sensor placed on the PCB. Comparator trip levels for each measurements are as follows:

- If the overvoltage threshold is 600V, this corresponds to 3.986V. This means the TRIP_V_DC (in formula TRIP) needs to be just under 4V. The trimmer must be set to 13.78 kΩ, which corresponds to the following formula:

$$Rtrimmer = \frac{R1 * TRIP - R2 * (5V - TRIP)}{5V - TRIP}$$

- If the overcurrent threshold is 150A, this corresponds to 3.76V. This means the TRIP_I_OUT needs to be 3.76V. The trimmer must be set at 14.26 kΩ, which also corresponds to the formula above.
- The temperature maximum for both temperature sensors is 120°C. This corresponds to the calculated value of SENSE_T_BRD of 3.414V. The value of the TRIP_T_BRD that is set with commonly used resistor values is 3.4V.

Figure 15: Schematic: Protection Comparators

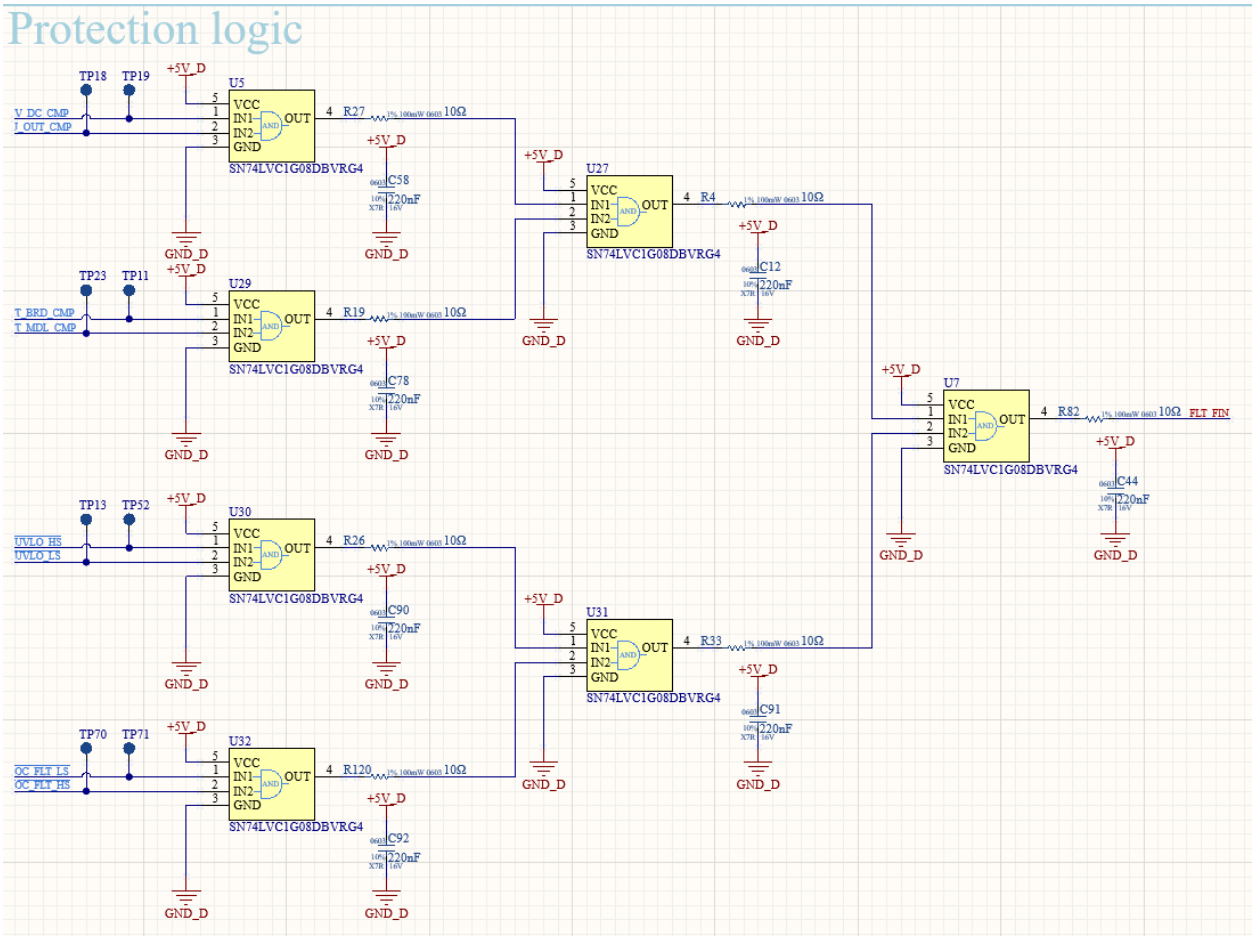


We use the TLV7021DBVR, a high speed comparator with a 1.6V to 5.5V supply range and 260-ns response time, in protection circuits because of its fast response time, ensuring quick fault detection for overvoltage, overcurrent, and overtemperature conditions. Its low power consumption makes it efficient, while the rail-to-rail input range allows it to accurately compare signals across the entire voltage range. The push-pull output simplifies integration with logic circuits, ensuring a reliable trigger for system protection mechanisms.

2.4.10 Protection Circuits Fault Reporting Signals

Figure 16 shows the protection logic circuit, which processes fault signals from different protection mechanisms and unites them into a one final output.

Figure 16: Schematic: Protection Logic



A pair of fault signals (such as overvoltage, overcurrent, or overtemperature) represent inputs for SN74LVC1G08DBVRG4, a dual input AND gate. U5 input signals are for DC overvoltage and output current overshoot and U29 is related to overtemperature of the module and the PCB, while U30 and U32 have as inputs under-voltage lockout and overcurrent fault signals (from high-side and low-side drivers), respectively. The same AND circuits, but with designators U27 and U31, are used for propagating the fault signal to make a united fault final (FLT_FIN) signal. The AND gate integrated circuit is designed for a power supply voltage ranging from 1.65V to 5.5V AND signal table is given in Table 7. The final output from the last AND gate (U7) is important for enabling the board operation.

Table 7: AND Logic for the Protection Comparators

Input		Output
IN1	**IN2**	**OUT**
0	0	0
0	1	0
1	0	0
1	1	1

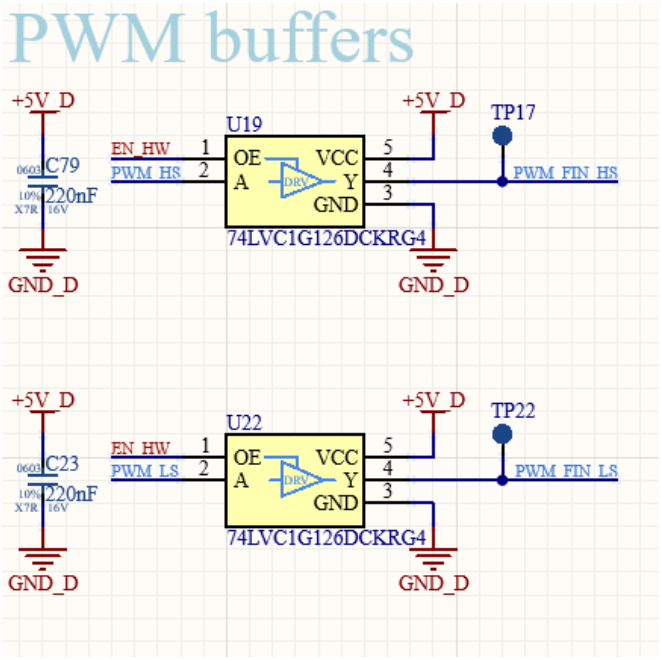
2.4.11 PWM Input Buffer Circuits

The PWM buffer circuits consist of two 74LVC1G126DCKRG4 single-gate buffers, U19 and U22, as shown in Figure 17. These buffers protect the circuit by ensuring that the PWM signals are only active when the system is in a safe state.

The high-side buffer, U19, takes the PWM_HS signal at its A input and outputs the buffered signal as PWM_FIN_HS. Its output is controlled by the EN_HW signal, which originates from the protection logic's AND gate. When EN_HW is high, the buffer allows PWM_HS to pass through. Otherwise, the output remains in a high-impedance state, preventing unintended switching. A test point, TP17, is provided for monitoring the PWM_FIN_HS signal.

The low-side buffer, U22, functions in the same way but handles the PWM_LS signal, outputting it as PWM_FIN_LS. Like the high-side buffer, it is enabled by the shared EN_HW signal. A corresponding test point, TP22, allows for measurement of the low-side PWM output.

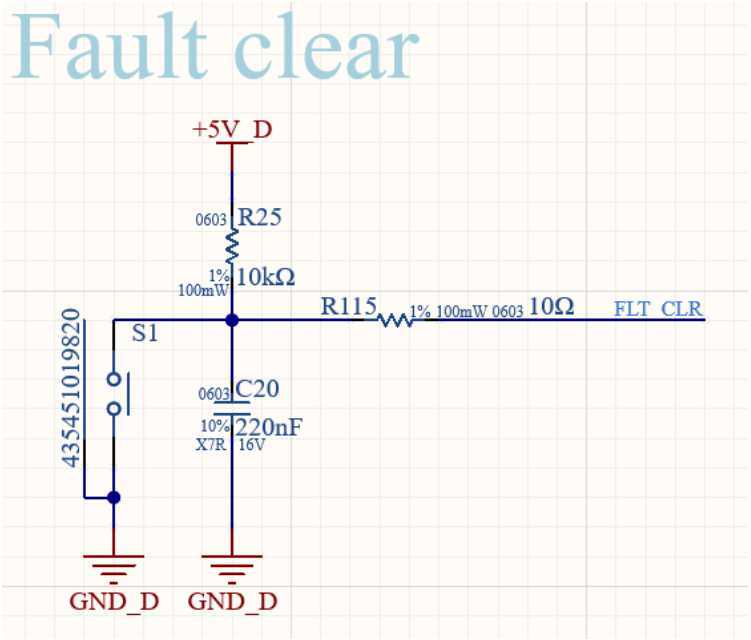
Figure 17: Schematic: PWM Buffers for High-Side and Low-Side Driver



2.4.12 Fault-Clearing Circuit

Figure 18 shows a fault-clearing circuit within a schematic.

Figure 18: Schematic: Fault-Clearing Circuit

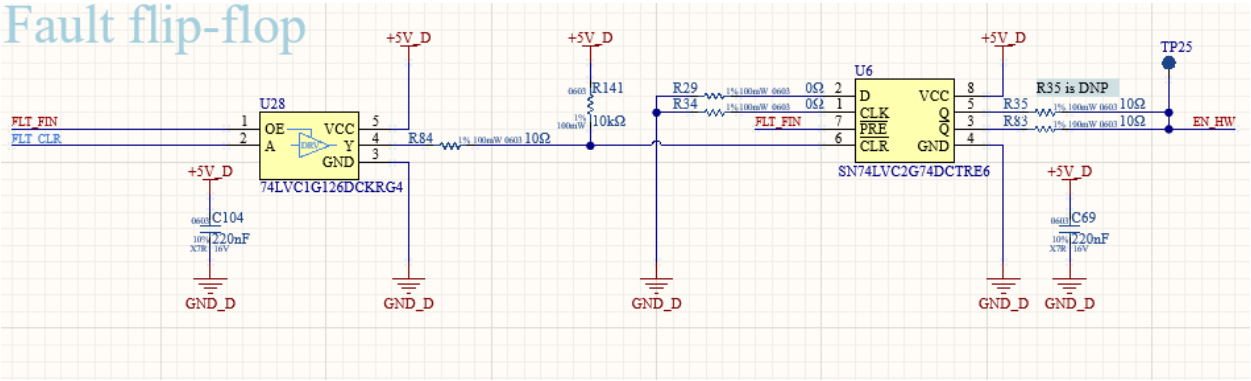


The fault-clearing circuit consists of a tactile switch, a 10-kΩ pull-up resistor, a capacitor, and a series resistor. The tactile switch, part number 435451019820, is a normally open push button that provides a manual way to clear fault conditions. One side of the switch is connected to ground, while the other side is pulled up to 5V through a 10-kΩ resistor. This keeps the FLT_CLR signal high under normal conditions. When the button is pressed, the FLT_CLR signal is pulled low, signaling the system to reset any latched fault conditions. The capacitor helps filter out transient noise, while the resistor limits inrush currents and provides controlled signal shaping.

2.4.13 Fault Circuit for Latching the Fault Signal

The circuit in Figure 19 represents a fault flip-flop system, which latches a fault condition and holds it until it is manually or automatically cleared. It ensures that faults are registered and do not disappear before corrective action is taken. The circuit consists of two main stages: an input stage with a buffer and a flip-flop for latching the fault and generating an output enable signal.

Figure 19: Schematic: Fault Circuit for Latching the Fault Signal

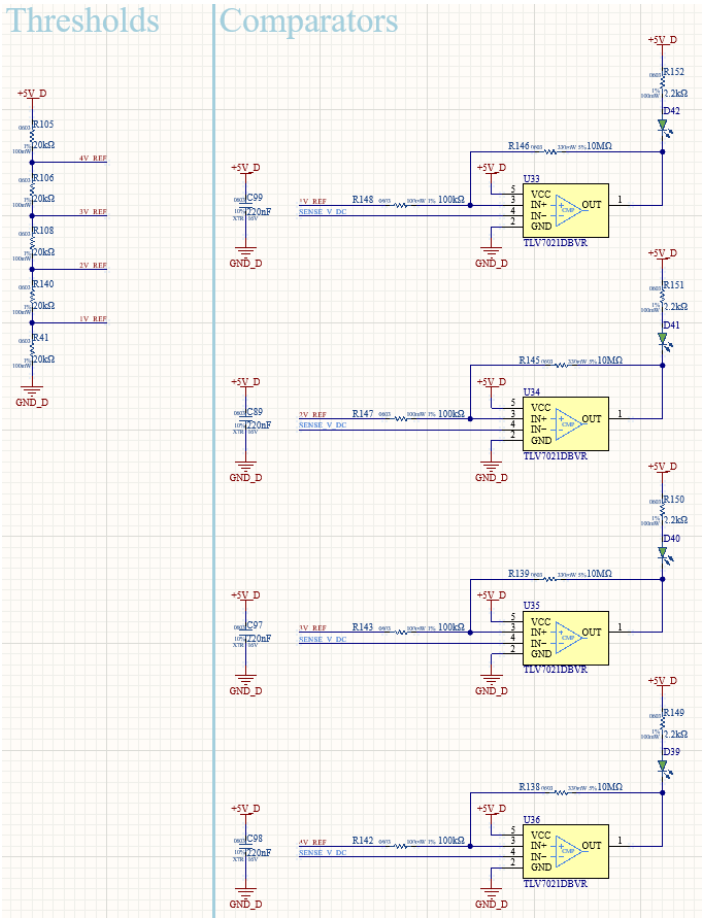


The input stage uses a 74LVC1G126DCKRG4 buffer (U8) to handle two signals: FLT_FIN, which indicates a fault occurrence, and FLT_CLR, which is used to reset the fault state. The buffer's output is conditioned through a network of resistors to minimize noise and interference. The flip-flop stage is built around the SN74LVC2G74DCTRE, a D-type flip-flop with preset and clear functions. The fault input signal is connected to the D input, while a clock signal determines when the fault is registered. Once a fault occurs, the flip-flop latches the fault state, causing its Q output to go high. The fault condition remains active until the clear input is triggered, which resets the flip-flop and clears the fault state. The output signal Q from the flip-flop is the EN_HW signal and test point TP25 is placed. This fault flip-flop system is useful because it ensures that faults are not missed, even if they occur for only a brief moment. The controlled reset mechanism ensures that faults are only cleared when necessary, preventing accidental resets.

2.4.14 DC Voltage Indication

Figure 20 shows DC voltage indication. The circuit incorporates four TLV7021DBVR signal comparators to monitor the DC link voltage and provide visual indication of its level. The trip points are set using a resistive network, defining specific voltage thresholds against which the measured SENSE_V_DC is evaluated. When the voltage crosses a threshold, the corresponding comparator changes state, activating an LED through a pull-up resistor. This setup ensures a clear and reliable indication of different voltage levels.

Figure 20: Schematic: DC Link Voltage Indication Circuit



Chapter 3: Board Testing and Results

Testing was conducted using two NXH004P120M3F2PTHG half-bridge modules in a back-to-back configuration, where the first module operates as a buck converter and the second as a boost converter. In this arrangement, the buck converter steps down the voltage, which represents a controlled DC voltage input to the boost converter, which steps it up. By analyzing voltage, current, and power at different points in the system, this setup enables an overall conversion efficiency. The results obtained from this configuration help in understanding the impact of switching frequency on a system performance and provide insight for optimization converter design.

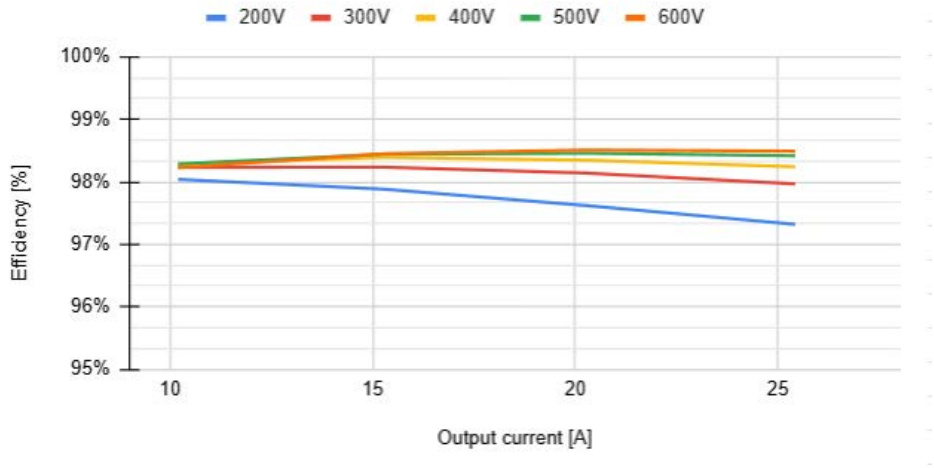
Figure 21 shows the measurement of the back-to-back configuration. The system is configured for a 300V input and 600V output, delivering an output current of 25A at a switching frequency of 60 kHz. The yellow signal is showing the input voltage of the boost converter, while light blue the load voltage is shown. Signal for input current is shown with pink, and the load current is shown in green. The orange signal represents the input power, while the light pink represents the output power. Mean values of each of the signals are shown in the bottom of the figure: C1 = input voltage, C2 = input current, F1 = input power, while C3 = output voltage, C4 = output current, and F2 = output power.

Figure 21: Oscilloscope Overview for Output of 600V and 25A with Switching Frequency of 60 kHz

The efficiency versus output current plots for different voltage levels at different frequencies provide insight into how switching frequency impacts overall system performance. These results highlight the tradeoffs between higher switching frequencies and increased switching losses that are important for optimizing the converter efficiency.

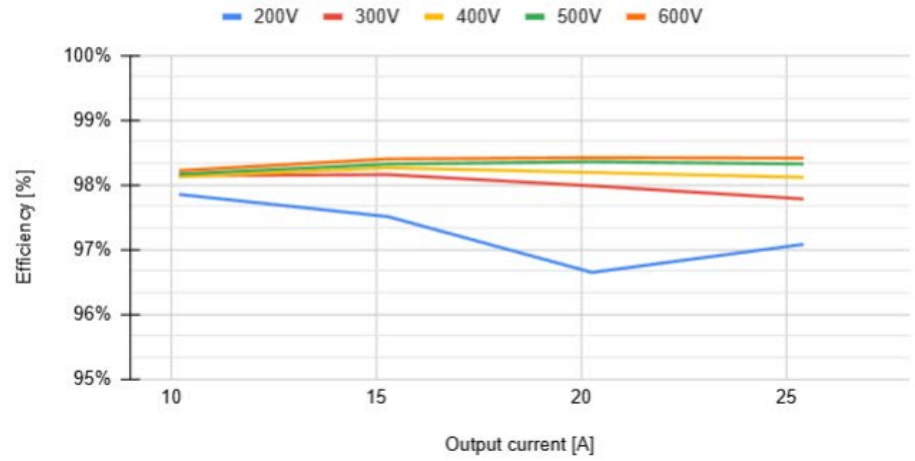
In Figure 22, the efficiency of the setup is shown for different load conditions. The measurements are conducted for various voltage levels with a constant frequency of 60 kHz.

Figure 22: Efficiency vs. Output Current for 60 kHz



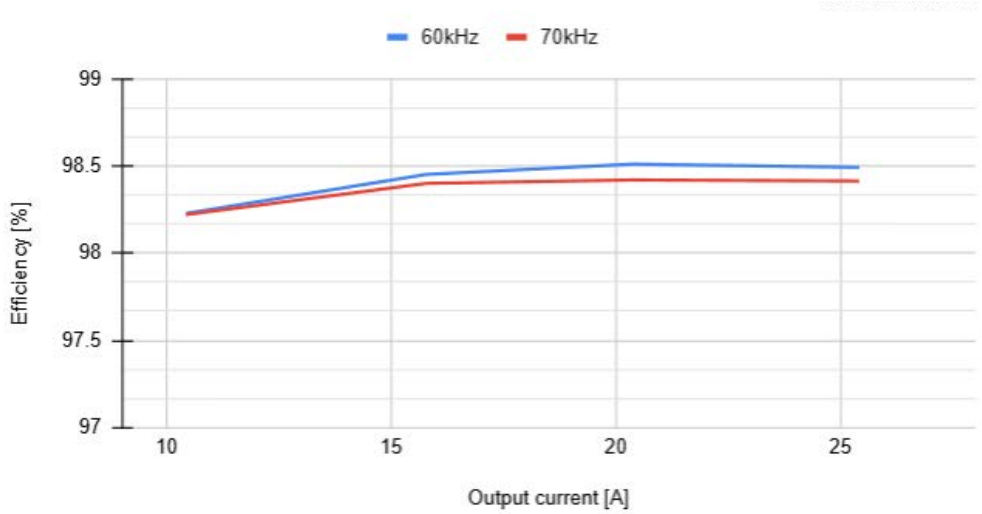
In Figure 23, the efficiency of the setup is shown for different load conditions. The measurements are conducted for various voltage levels with a constant frequency of 70 kHz.

Figure 23: Efficiency vs. Output Current for 70 kHz



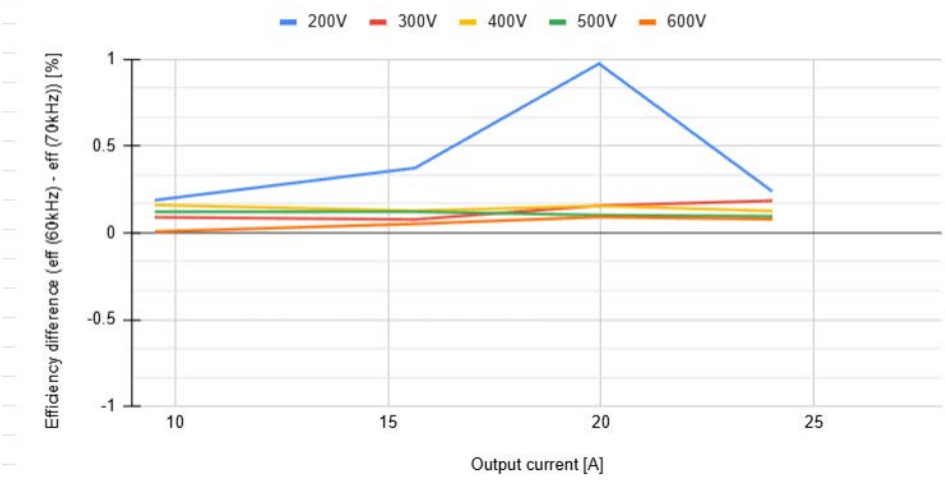
It was important to acknowledge the system efficiency changing with frequency for a fixed voltage value. This shows how the switching losses are partaking in the system losses. The dependency is measured and shown in Figure 24 for two different switching frequencies, 60 kHz and 70 kHz, for a voltage of 600V.

Figure 24: Efficiency vs. Output Current for 600V for Two Different Frequencies: 60 kHz and 70 kHz



In Figure 25, the difference in efficiency between the two switching frequencies (60 kHz and 70 kHz) is plotted against various output currents. The results show that at lower voltages, the efficiency difference varies significantly, whereas at mid-range voltages (400V - yellow plot), the difference remains relatively constant and close to zero. This indicates that frequency-dependent losses are more pronounced at lower voltages, while at mid-range voltages, the system operates with more stable efficiency.

Figure 25: Difference in Efficiencies for 60 kHz and 70 kHz for Different Output Currents



Appendix A: BDC-1001-A1 Bill of Materials and Layout

This section gives the bill of materials and layout of BDC-1001-A1. The intention behind providing this information is to enable customers to modify, copy, and qualify the design for production, according to specific requirements.

A.1 Bill of Materials

Table 8 shows the bill of materials, where all the project components are represented. The part number is manufacturer's name of the component, the designator represents the symbol of the component in the Altium project, and the quantity of each component in the project and detailed description is shown as well.

Table 8: Bill of Materials for BDC-1001-A1

Part Number	Designator	Qty	Description
GRM31CZ71C226ME15L	C16, C93	2	Cap, ceramic, 22 µF, 10%, 16V, X7R, SM 1206, +125°C
RC0805FR-1020KL	R116, R144	2	Res, 20 kΩ, 1%, 125 mW, 100 ppm/°C, thick film, SM 0805, +155°C
RT0603BRE078KL	R23, R103, R109	3	Res, 8 kΩ, 0.1%, 100 mW, 50 ppm/°C, thin film, SM 0603, +155°C
CR0603-F/-1R00ELF	R87, R91	2	Res, 1Ω, 1%, 100 mW, 100 ppm/°C, thick film, 0603, +155°C
ERJ-3EKF39R0V	R48, R75, R153	3	Res, 39Ω, 1%, 100 mW, 100 ppm/°C, thick film, 0603, +155°C
C0603C101K5RACTU	C19, C60, C61, C116, C117	5	Cap, ceramic, 100 pF, 10%, 50V, X7R, SM 0603, +125°C
AC0603FR-07330RL	R100, R118	2	Res, 330Ω, 1%, 100 mW, 100 ppm/°C, thick film, 0603, +155°C
AC0603FR-07110RL	R43, R57	2	Res, 110Ω, 1%, 100 mW, 100 ppm/°C, thick film, 0603, +155°C
ALF70C102EH400	C47, C81, C82, C83, C87, C88	6	Cap, electrolytic, 1 mF, 20%, 400V, custom size, +85°C
5195TR	TP1, TP2, TP8, TP12, TP16, TP20, TP21, TP24, TP26, TP38, TP39, TP47, TP48, TP49	14	SM test point, with plastic spacer (brown)
RC0603FR-0725K5L	R45	1	Res, 25.5 kΩ, 1%, 100 mW, 100 ppm/°C, thick film, SM 0603, +155°C
CRCW08050000Z0EA	R134, R136	2	Res, 0Ω, 1%, 125 mW, 200 ppm/°C, thick film, SM 0805, +155°C
PDZ15BGWJ	D3, D38	2	Diode, Zener, 15V, SM, SOD123-2, +150°C
PVG5A502C03R00	R133	1	Trimmer, 5 kΩ, 10%, 250 mW, 25 ppm/°C, vertical, Cermet, PVG5A, +155°C
KDZVTR10B	D12, D21	2	Diode, Zener, 10V, SM, SOD123-2, +150°C
PMEG40T30ERX	D5, D6, D7, D11, D13, D20, D23, D24, D43, D44, D45, D46	12	Diode, Schottky, 3A, 40V, SM, SOD123-2, +150°C
SDR10EZPF15R0	R3, R65	2	Res, 15Ω, 1%, 500 mW, 100 ppm/°C, thick film, SM 0805, +155°C
SDR10EZPF3R90	R10, R15, R53, R56, R71, R101, R111, R113	8	Res, 3.9Ω, 1%, 500 mW, 200 ppm/°C, thick film, SM 0805, +155°C
ERJ-3EKF1202V	R38	1	Res, 12 kΩ, 1%, 100 mW, 100 ppm/°C, thick film, SM 0603, +155°C
CRCW060310M0JNEA	R5, R13, R42, R47, R138, R139, R145, R146	8	Res, 10 MΩ, 5%, 330 mW, 200 ppm/°C, thick film, 0603, +155°C
CR0603-FX-49R9ELF	R30, R127	2	Res, 49.9Ω, 1%, 100 mW, 100 ppm/°C, thick film, 0603, +155°C
ERJ-3EKF2401V	R24	1	Res, 2.4kΩ, 1%, 100 mW, 100 ppm/°C, thick film, 0603, +155°C

Table 8: Bill of Materials for BDC-1001-A1

Part Number	Designator	Qty	Description
VS-E7FX0212HM3/I	D9, D1	2	Diode, power, 2A, 1200V, SM, SMF (DO-219AB), +175°C
1206GC221KAT2A	C2, C80	2	Cap, ceramic, 220 pF, 10%, 2 kV, X7R, SM 1206, +125°C
AUIR2085STR	U10	1	IC, gate driver, half bridge, SOIC-8, SM, +125°C
CSS4J-4026R-L300F	R86	1	Res, 300 µΩ, 1%, 15W, 50 ppm/°C, current sense, SM, 4026, +170°C
C4AQUBW4800A3FJ	C84, C85, C86	3	Cap, film, 8 µF, 5%, 1300V, custom size, +105°C
PH9185.012NLT	T1, T2	2	Ind, Pulse transformer, 1:2 ratio, 450 uH, custom size,+125°C
RK73G2BTTD1004C	R39, R58, R61	3	Res, 1 MΩ, 0.25%, 250 mW, 50 ppm/°C, thick film, SM, 1206, +155°C
SR2512FK-7W100KL	R104, R107	2	Res, 100 kΩ, 1%, 2W, 200 ppm/°C, thick film, 2512, +155°C
CRCW120612K0FKEAC	R63, R85	2	Res, 12 kΩ, 1%, 250 mW, 100 ppm/°C, thick film, SM, 1206, +155°C
CRCW12061K00FKEAC	R1, R16	2	Res, 1 kΩ, 1%, 250 mW, 100 ppm/°C, thick film, SM, 1206, +155°C
ERJ-U6SJR15V	R97	1	Res, 150 mΩ, 5%, 250 mW, 150 ppm/°C, thick film, SM 0805, +155°C
ERJ-6GEYJ242V	R92, R98	2	Res, 2.4 kΩ, 5%, 125 mW, 200 ppm/°C, thick film, SM 0805, +155°C
1725656	J1	1	Connector, 1725656, 2 positions, 2.54 mm
5190TR	TP3, TP4, TP5, TP6, TP7, TP9, TP14, TP31, TP41, TP42, TP44, TP45, TP46, TP50, TP51, TP59	16	SM test point, with plastic spacer (red)
BAT165E6327HTSA1	D4, D10, D14, D15, D17	5	Diode, Schottky, 0.75A, 40V, SM, SOD323-2, +150°C
PDZ18BGWJ	D8, D16	2	Diode, Zener, 18V, SM, SOD123-2, +150°C
BZT52C3V9-7-F	D18, D22	2	Diode, Zener, 3.9V, SM, SOD123-2, +150°C
B240AE-13	D2	1	Diode, Schottky, 2A, 40V, SM, DO-214AC (SMA), +150°C
FF6MR12W2M1HB70BPSA1	U25	1	Module, N-channel MOSFET with NTC, dual configuration, custom size, TH, +175°C
ADA4891-1ARJZ-R7	U4, U11, U15	3	IC, operational amplifier, 1 channel, rail-to-rail, SOT23-5, +125°C
PMV130ENEAR	Q1, Q2	2	Transistor, MOSFET, N-channel, 40V, 2.1A, SOT23-3, SM, +150°C
R1SX-0505/H-R	U20, U21	2	IC, DC/DC converter, isolated, 1W, SM, R1SX, +100°C
ACPL-C72B-000E	U23	1	IC, isolated current amplifier, SSO-8, SM, 110°C
ACPL-C87B-000E	U3, U9, U12	3	IC, isolated voltage sensor, SSO-8, SM, 105°C
ACPL-355JC-000E	U8, U26	2	IC, gate driver, 30V, 10A, SO-16, SM, 110°C
885012206076	C56, C57, C62	3	Cap, ceramic, 1 µF, 10%, 25V, X7R, SM 0603, +125°C
435451019820	S1	1	Switch, tactile, SM
SN74LVC2G74DCTRE6	U6	1	IC, flip flop, D type, SM-8 (SOT-505), SM, +125°C
ESD9L5.0ST5G	D25, D27, D28, D29, D30, D31, D32, D33, D34, D35, D36	11	IC, TVS diodes, 1 channel, SOD-923-2, SM, +125°C
CL21B106KAYQNNE	C27, C43	2	Cap, ceramic, 10 µF, 10%, 25V, X7R, SM 0805, +125°C
PVG5A203C03R00	R131, R132	2	Trimmer, 20 kΩ, 10%, 250 mW, 25 ppm/°C, vertical, Cermet, PVG5A, +155°C
C1608X7R1V224K080AB	C13, C17	2	Cap, ceramic, 220 nF, 10%, 35V, X7R, SM 0603, +125°C
C0603C103K3RAC	C33, C42, C109	3	Cap, ceramic, 10 nF, 10%, 25V, X7R, 0603, +125°C
AC1206FR-07100KL	R121, R122	2	Res, 100 kΩ, 1%, 250 mW, 100 ppm/°C, thick film, SM 1206, +155°C
RT0603FRE074K7L	R6, R31, R129, R130	4	Res, 4.7 kΩ, 1%, 100 mW, 50 ppm/°C, thin film, 0603, +155°C
CRCW120610K0FKEA	R110	1	Res, 10 kΩ, 1%, 250 mW, 100 ppm/°C, thick film, SM, 1206, +155°C
TLV9161IDCKR	U24	1	IC, operational amplifier, 1 channel, rail-to-rail, SC70-5, +125°C

Table 8: Bill of Materials for BDC-1001-A1

Part Number	Designator	Qty	Description
ERA-3ARB1332V	R68	1	Res, 13.3 kΩ, 0.1%, 100 mW, 10 ppm/°C, thin film, 0603, +155°C
06035A750JAT2A	C15	1	Cap, ceramic, 75 pF, 5%, 35V, C0G, 0603, +125°C
CRCW0603200KFKEBC	R21, R126	2	Res, 200 kΩ, 1%, 100 mW, 100 ppm/°C, thick film, 0603, +155°C
RT0603DRE0733KL	R93, R154, R155	3	Res, 33 kΩ, 0.5%, 100 mW, 50 ppm/°C, thin film, 0603, +155°C
885012206059	C10, C11, C28, C29, C45, C46, C52, C53, C110, C111, C112, C113, C114, C115	14	Cap, ceramic, 1 nF, 10%, 25V, X7R, 0603, +125°C
ERJ-3EKF10R0V	R4, R9, R11, R14, R19, R20, R26, R27, R33, R36, R46, R50, R51, R66, R67, R70, R77, R82, R83, R84, R89, R94, R95, R114, R115, R120, R124, R125	28	Res, 10Ω, 1%, 100 mW, 100 ppm/°C, thick film, 0603, +155°C
TLV7021DBVR	U1, U2, U16, U18, U33, U34, U35, U36	8	IC, analog comparator, single, SOT23-5, SM, +125°C
SN74LVC1G08DBVRG4	U5, U7, U27, U29, U30, U31, U32	7	IC, AND gates, double input, single gate, SOT23-5, SM, +125°C
TMP235A4DCKR	U17	1	IC, temperature sensor, 1°C accuracy, SC70-5, SM, +150°C
RC0603FR-070RL	R29, R34, R99, R117	4	Res, 0Ω, 1%, 100 mW, 200 ppm/°C, thick film, 0603, +155°C
AC0603FR-1020KL	R41, R59, R64, R73, R74, R79, R80, R105, R106, R108, R140	11	Res, 20 kΩ, 1%, 100 mW, 100 ppm/°C, thick film, SM 0603, +155°C
AC0603FR-074K02L	R81	1	Res, 4.02 kΩ, 1%, 0.1W, 100 ppm/°C, thick film, SM 0603, +155°C
74LVC1G126DCKRG4	U19, U22, U28	3	IC, buffer, non-inverting, with enable, SC70-5, SM, +125°C
RT0603FRE072K2L	R28, R44, R96, R149, R150, R151, R152	7	Res, 2.2 kΩ, 1%, 100 mW, 50 ppm/°C, thin film, 0603, +155°C
RT0603FRE0716KL	R112	1	Res, 16 kΩ, 1%, 100 mW, 50 ppm/°C, thin film, 0603, +155°C
RT0603FRE073K3L	R12	1	Res, 3.3 kΩ, 1%, 100 mW, 50 ppm/°C, thin film, 0603, +155°C
SRN5040-150M	L1, L2	2	Ind, power, 15 µH, 20%, 1.8A, SM, SRN5040, semi-shielded, +125°C
VJ0603A331FXQPW1BC	C100, C101, C102, C103	4	Cap, ceramic, 330 pF, 1%, 10V, C0G, SM 0603, +125°C
885012208094	C25, C26	2	Cap, ceramic, 4.7 µF, 10%, 50V, X7R, SM 1206, +125°C
CL31B106KBHNNNE	C3, C4, C5, C8, C9, C14, C18, C21, C22, C51, C54, C55, C63, C65, C66, C67, C68, C70, C71, C72, C73, C74, C75, C76, C94, C95, C96, C105, C106	29	Cap, ceramic, 10 µF, 10%, 50V, X7R, SM 1206, +125°C
885012206026	C120	1	Cap, ceramic, 1 µF, 10%, 10V, X7R, SM 0603, +125°C
885012206027	C1, C7	2	Cap, ceramic, 2.2 µF, 10%, 10V, X7R, SM 0603, +125°C
AC0603FR-07100KL	R22, R32, R37, R60, R62, R128, R142, R143, R147, R148	10	Res, 100 kΩ, 1%, 100 mW, 100 ppm/°C, thick film, SM 0603, +155°C

Table 8: Bill of Materials for BDC-1001-A1

Part Number	Designator	Qty	Description
AC0603FR-0710KL	R2, R7, R8, R17, R18, R25, R40, R49, R52, R54, R55, R69, R72, R76, R78, R88, R90, R102, R119, R123, R141	21	Res, 10 kΩ, 1%, 100 mW, 100 ppm/°C, thick film, SM 0603, +155°C
AC0603FR-071KL	R156, R157	2	Res, 1 kΩ, 1%, 100 mW, 100 ppm/°C, thick film, SM 0603, +155°C
TPS54202HDDCR	U13, U14	2	IC, DC/DC Buck converter, SOT-23-Thin-6, SM, +125°C
150060VS55040	D1, D26, D37, D39, D40, D41, D42	7	Diode, LED green, 20 mA, 2V, SM 0603, +115°C
885012206048	C12, C20, C23, C24, C30, C31, C32, C34, C35, C36, C37, C38, C39, C40, C41, C44, C48, C49, C50, C58, C59, C64, C69, C78, C79, C89, C90, C91, C92, C97, C98, C99, C104	33	Cap, ceramic, 220 nF, 10%, 16V, X7R, SM 0603, +125°C
7460307	J3, J4, J5, J6, J7, J8	6	Conn, power terminal, M4, TH, RedCube

3.0.1 PCB and Layout

The PCB is designed with eight copper layers because of the current rating of the board. In total there are 437 components, 334 of which are placed on the top and 103 on the bottom. The layer stack-up follows standard specifications, with 2-oz copper in the outer layers and 4-oz copper in the inner layers. Material is FR-4-HT (high temperature) and the color is green with total thickness of 3.2308 mm that corresponds to 3.2 mm ±10% (this is a rounded value from the layer stack manager shown in Figure with the tolerance of 10%).

Figure 26 shows the TOP, layer 1.

Figure 26: Top Layer of the PCB BDC-1001-A1

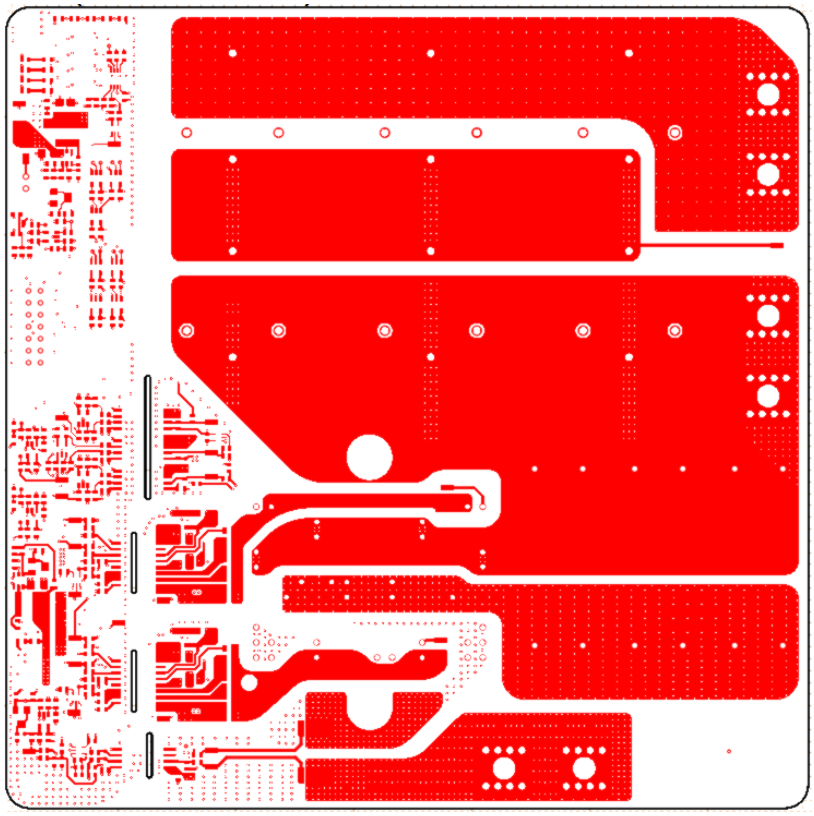


Figure 27 shows S1, layer 2. This is a GND polygon of the board.

Figure 27: S1 Layer of the PCB BDC-1001-A1

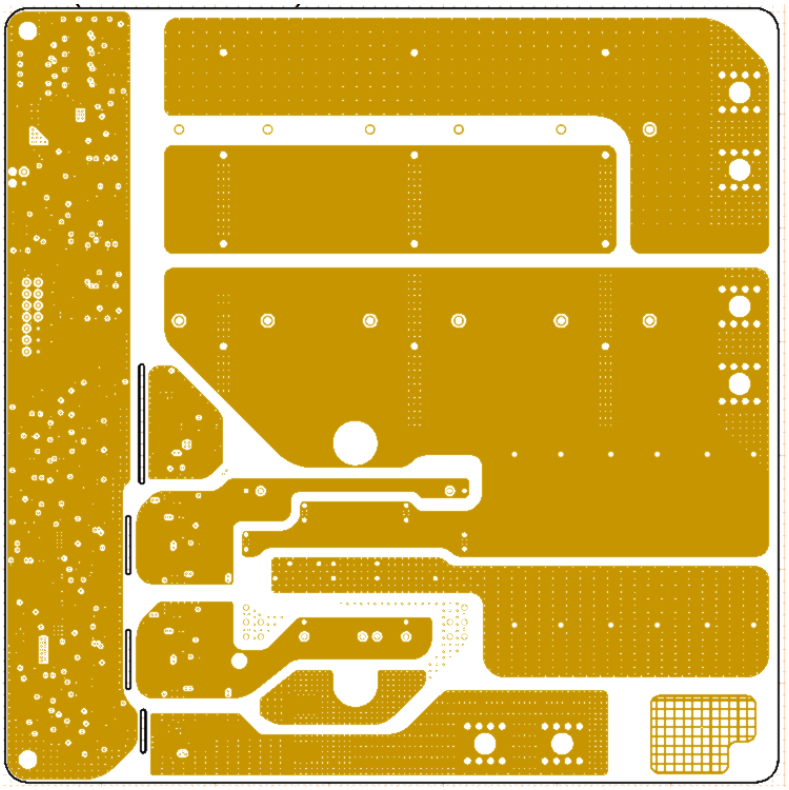


Figure 28 shows S2, layer 3.

Figure 28: S2 Layer of the PCB BDC-1001-A1

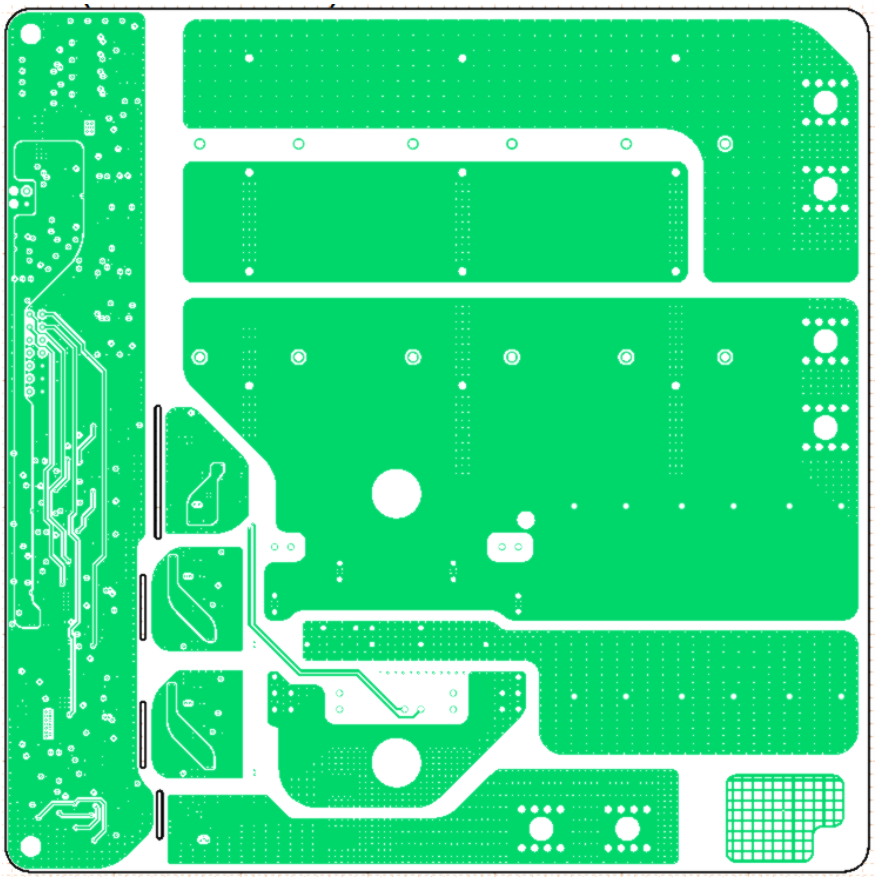


Figure 29 shows S3, layer 4.

Figure 29: S3 Layer of the PCB BDC-1001-A1

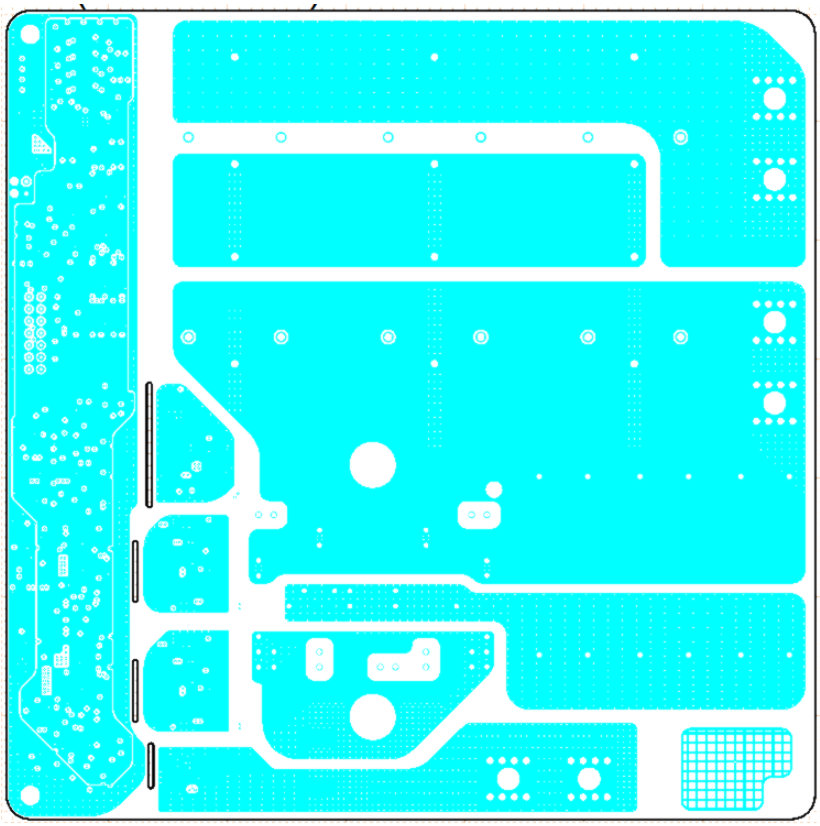


Figure 30 shows S4, layer 5.

Figure 30: S4 Layer of the PCB BDC-1001-A1

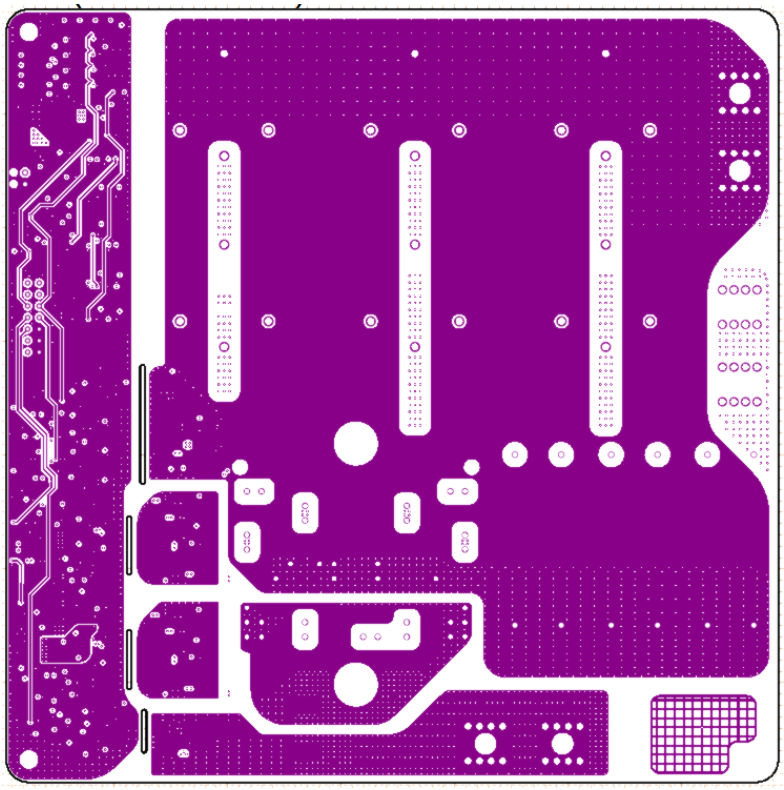


Figure 31 shows S5, layer 6.

Figure 31: S5 Layer of the PCB BDC-1001-A1

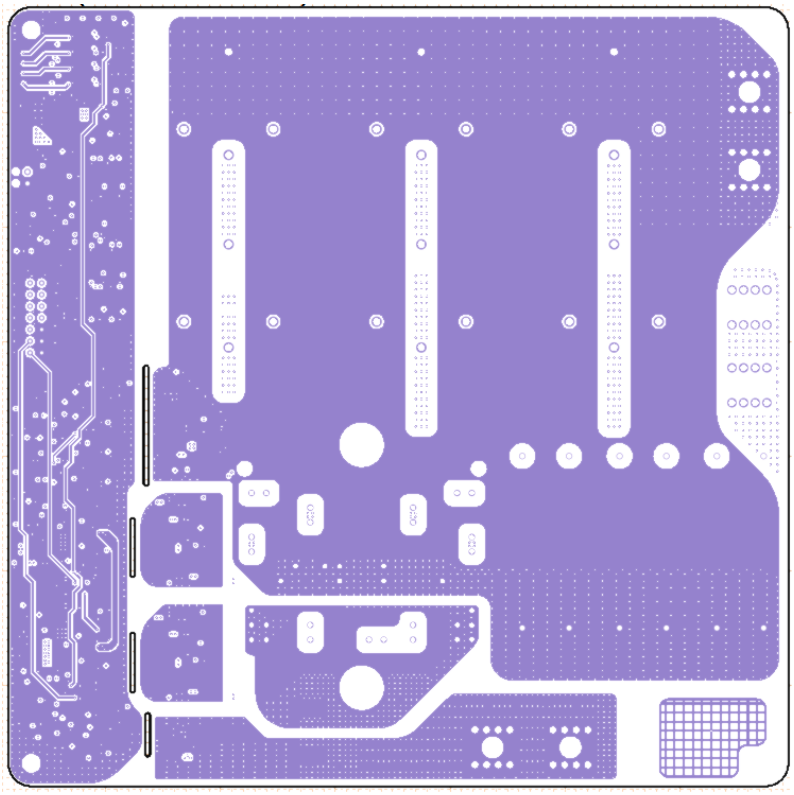


Figure 32 shows S6, layer 7.

Figure 32: S6 Layer of the PCB BDC-1001-A1

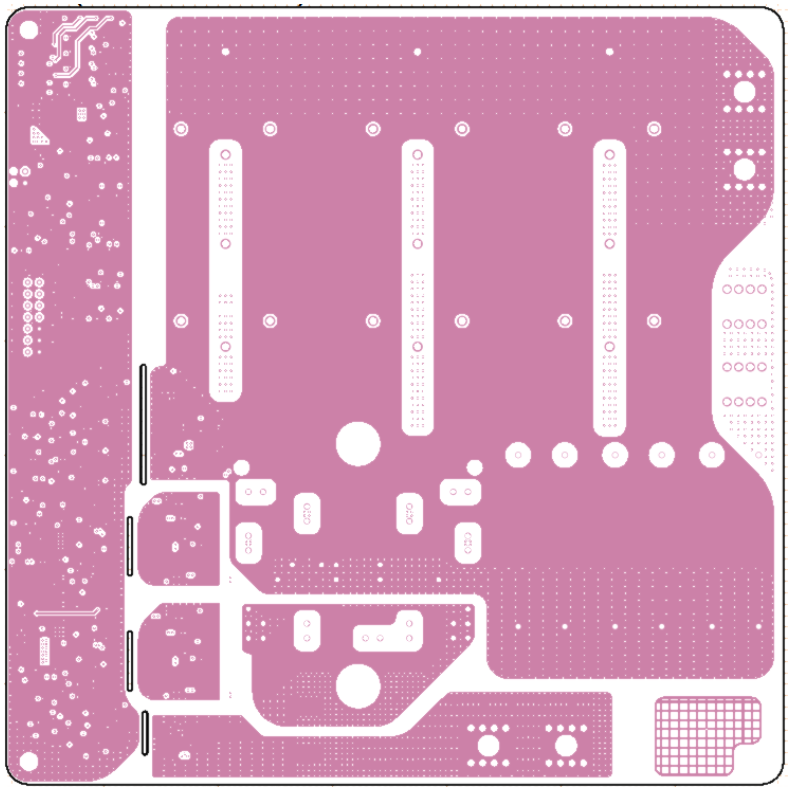
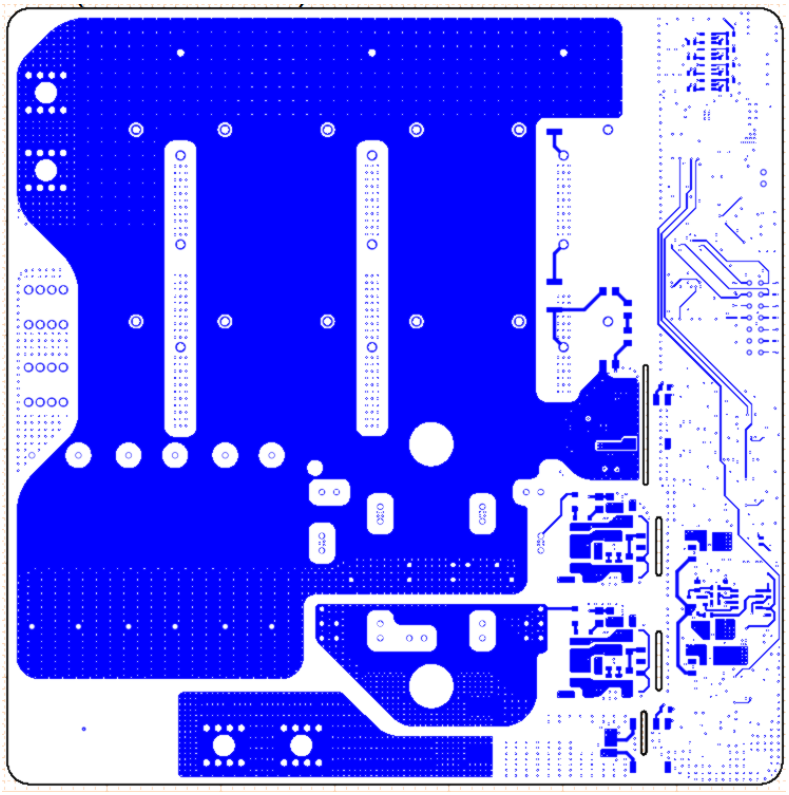


Figure 33 shows BOTTOM, layer 8.

Figure 33: Bottom Layer of the PCB BDC-1001-A1



Revision History

ACPL-355JC-F2GM32B-RM100; June 23, 2025

Initial release.