ACPL-355JC

DUAL 1B SiC Module EB1200-355JC Evaluation Board

Reference Manual
Version 1.1

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ACPL-355JC: DUAL 1B SiC Module EB1200-355JC Evaluation Board

1 Introduction

The EB1200-355JC evaluation board features the Broadcom® dual-output isolated gate drive optocouplers ACPL-355JC, used to drive SiC MOSFET module in DUAL 1B housing, precision optically isolated amplifiers ACPL-C87B used for DC Bus voltage and temperature measurements, and optically isolated sigma delta modulator ACPL-736J used for output current measurement. In addition, the board features an integrated capacitor DC bus with optimized layout that minimizes the commutation loop inductance. EB1200-355JC, shown in Figure 1, is developed to support Broadcom customers during their first steps in designing power converter applications with ACPL-355JC drivers. Properties of the board are described in the following sections of this document.

Components were selected considering lead-free reflow soldering. The design was tested and verified with basic measurements described in this document, but it is not qualified for the operation in the whole operating temperature range or lifetime. The board is subjected to functional testing only.

Figure 1: Evaluation Gate Driver Board EB120-355JC

The EB1200-355JC is originally designed to be used with the DUAL 1B SiC MOSFET module FF11MR12W1M1. With adequate adjustments regarding overcurrent (OC) protection and gate resistors, the EB1200-355JC supports modules from different manufacturers in the same packaging, rated up to 1200V and having the same pin assignment.

1.1 Design Features

The EB1200-355JC includes the following main features:

- Two isolated ACPL-355JC gate drive optocouplers with following features:
  - 10A peak output current
  - 100-kV/µs common mode rejection
  - V_{IORM} = 2262 V_{PK} with CTI > 600V
  - Overcurrent protection (or DESAT)
  - Soft shutdown during fault
  - Two isolated feedback signals, FAULT (for over current) and UVLO
- Two ACPL-C87B optically isolated amplifiers for DC bus voltage and temperature measurement:
  - 0 to 2V nominal input range
  - 100-kHz bandwidth
  - 3V to 5.5V wide supply range for output side
  - 15 kV/µs common mode transient immunity.
- ACPL-736J optically isolated sigma-delta modulator for output current measurement:
  - ±50 mV linear range
  - 10 to 20 MHz external CLK
  - CMOS clock and data interface
  - 1-bit, second-order sigma delta modulator
  - 16 bits resolution no missing codes
  - 80dB typ SNR, 78dB typ. SNDR
- Electrically and mechanically suitable for DUAL 1B module FF11MR12W1M1
- With adjustment of the OC protection and gate resistors, the evaluation board supports the following DUAL 1B SiC MOSFET modules:
  - FF11MR12W1M1
  - FF23MR12W1M1
  - CAB011M12FM3
  - CAB016M12FM3
- DC bus and balancing and discharge resistors
- DC/DC power supply with current limit protection and thermal shutdown
- Isolated SMPS for gate drivers
- Access to FAULT and UVLO output signals for protection and control development purposes
- Access to PWM input signals
- Access to measurement signals (voltage and current)

1.2 Target Applications

Broadcom ACPL-355JC gate drive optocouplers target the following applications:

- Motor drive for industrial automation and robotics
- Power supply and charger
- Renewable energy inverter and storage

1.3 Warnings

The board operates at high voltages. Take special care to avoid risk of injury and life endangering. While operating the board, take the following safety precautions into considerations:

- If the board is powered up, do not touch the board, especially exposed metal parts.
- Pay attention to the maximum ratings.
- Use of a protection cover made of insulating materials is mandatory.
- If the board is used with power module to drive continuous load, the power module must be mounted on a heat sink. The board may rise to high temperatures, and any contact with the human body must be avoided.
- Whenever a change in the test setup is performed (for example, changing the probe position), turn off the power supply and ensure that the DC bus is fully discharged to avoid injuries and the destruction of the board.
- The board itself does not provide dead-time generation. The minimal dead time is 500 ns.

2 System Description

This section gives essential electrical and mechanical specifications of the EB1200-355JC evaluation board.

2.1 Key Specifications

Absolute maximum ratings of the EB1200-355JC evaluation board are listed in Table 1. This table contains only key parameters. Constraints from ACPL-355JC, ACPL-C87B, and ACPL-736J data sheets, as well as specification of other key components, must be considered when the EB1200-355JC is used.

Table 1: Absolute Maximum Ratings

Parameter	Values			Units	Note
	Min.	Typ.	Max.		
DC Bus Supply Voltage	—	600	800	V	Limited by the DC bus capacitors' voltage rating
MOSFET Half-Bridge Output Current (RMS)	-	15	30	A	Limited by the PCB copper traces
Vcc Input Voltage	11	12	14	V	External DC input power supply for digital circuitry. Limited by SMPS range for gate drivers.
PWM Logic Input Level	0	3.3	5	V	External PWM inputs for gate drivers.
Fault Logic Output Level	0	—	5	V	Logic output signal; refer to the ACPL-355JC data sheet.
UVLO Output Logic Level	0	—	5	V	Logic output signal; refer to the ACPL-355JC data sheet.
CLK and DATA Output Logic Level	0	—	5	V	Clock and data logic output signals for current measurement; refer to the ACPL-736J date sheet
Voltage Measurement	0	—	5	V	Single-ended analog output signal
Temperature Measurement	0	—	5	V	Single-ended analog output signal

2.2 Functional Block Diagram

The functional block diagram and disposition of the functional blocks of the EB1200-355JC gate driver evaluation board are shown in Figure 2 and Figure 3. The block diagram shows several different functional blocks:

- Power management:
  - +12V/+5V DC/DC regulator
  - Two +5V/+5V isolated DC/DC regulators
  - +5V to +3.3V LDO
- +12V/(+18V, –3.4V) isolated SMPS with two outputs (one for high side driver and one for low side driver)
- High and low side ACPL-355JC gate drivers with circuitry
- Voltage and temperature measurements with two ACPL-C87Bs
- Current measurement with ACPL-736J
- DC bus and resistors for the voltage symmetry
- DC bus supply terminals
- User interface connector
- +12V Vcc power supply connector
- Power terminals

Figure 2: Functional Block Diagram of EB1200-355JC

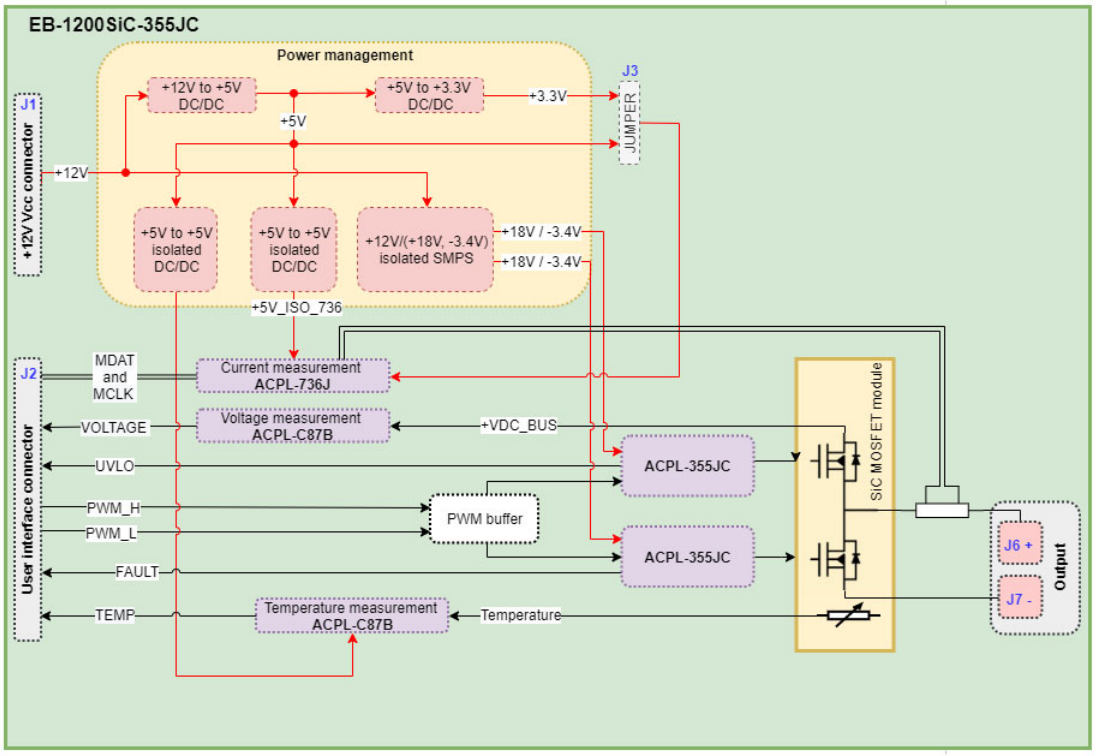
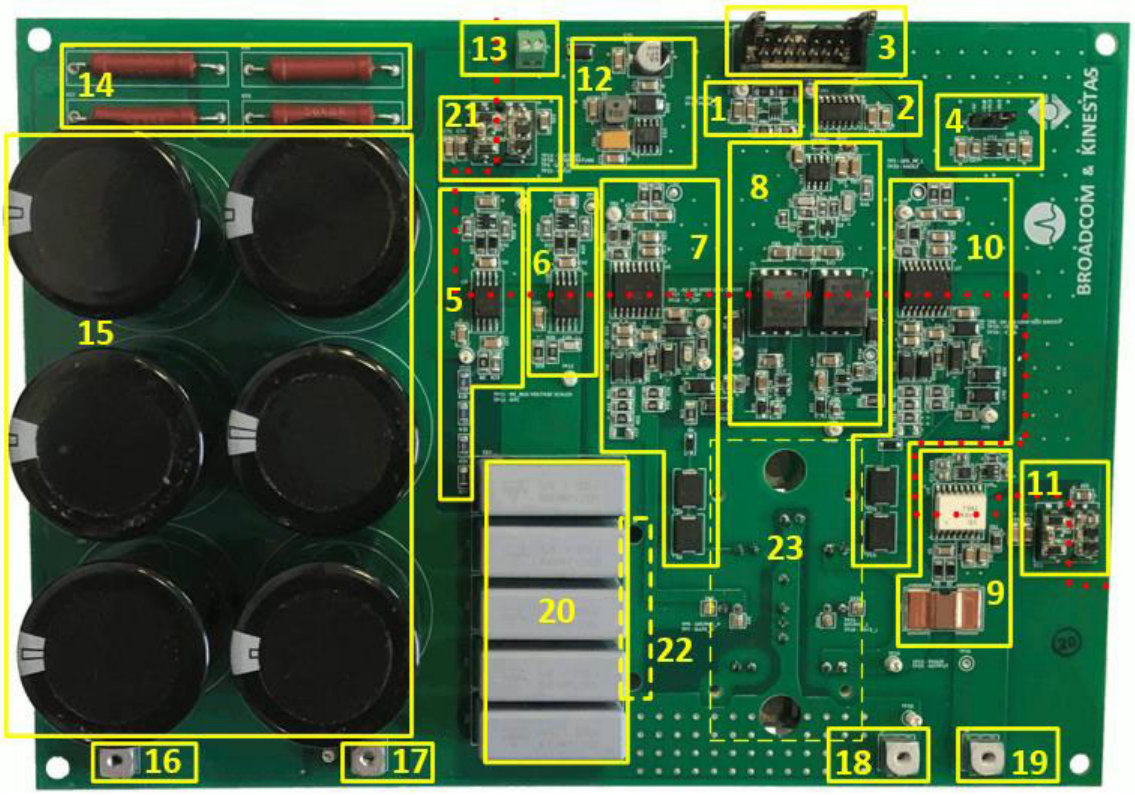


Figure 3: Functional Blocks Disposition of the EB1200-355JC. Isolation border is marked with red dots.



According to Figure 3, marked functional blocks are as follows:

1. PWM buffering
2. MCLK and MDATA buffering
3. J2 – Signal connector
4. J3 – Voltage level selector 3.3V/5V to interface from current sense measurement
5. Temperature measurement based on ACPL-C87B
6. DC bus voltage measurement based on ACPL-C87B
7. High side SiC driver based on ACPL-355JC
8. Isolated SMPS for gate drivers
9. Shunt current measurement based on ACPL-736J
10. Low side SiC driver based on ACPL-355JC
11. Isolated 5V/5V
12. Switched power supply 12V/5V
13. J1 – Auxiliary connector input 12V
14. Balancing resistors
15. DC bus – Electrolytic capacitors

16. J5 – Power connector –DC_bus
17. J4 – Power connector +DC_bus
18. J7 – Power connector –DC_bus
19. J6 – Power connector – AC half bridge output
20. DC bus filtering – Film capacitors
21. Isolated 5V/5V
22. Holes for Rogowski probe
23. SiC half bridge module in DUAL 1B package

2.3 Pin Assignment

Pin assignment for all connectors on the EB1200-355JC are listed in the following paragraphs.

2.3.1 Power Interface

The J1 power supply connector supplies all ICs and provides gate driver voltage supply, and its pin assignment is shown in Table 2. Four screw terminals (J4, J5, J6, J7) connect the DC bus voltage and the output of the power module (AC output of the MOSFET half-bridge). Table 3 lists the functions for each of the mentioned connectors.

Table 2: Pin Assignment of Connector J1 (Power Supply Connector)

Pin	Label	Function
1	+V_SUPPLY	Power supply for low voltage side
2	GND	Ground

Table 3: Power Connectors J4, J5, J6, J7

Designator	Label	Function
J4	DC+	DC Bus power supply - positive terminal
J5	DC-	DC Bus power supply - negative terminal
J6	OUTPUT	AC Output of the half-bridge MOSFET module (switching node).
J7	DC-	DC Bus negative power supply.

2.3.2 Signal Interface

The pin assignments of connectors J2 and J3 are listed in Table 4 and Table 5.

Table 4: Pin Assignment of Connector J2 (User Interface Connector)

Pin	Label	Function	Direction
1	GND	Ground	Bidirectional
2	GND	Ground	Bidirectional
3	MDAT	Data signal for sigma-delta current measurement	Output
4	UVLO	UVLO fault signal for both drivers	Output
5	GND	Ground	Bidirectional

Table 4: Pin Assignment of Connector J2 (User Interface Connector) (Continued)

Pin	Label	Function	Direction
6	FAULT	Fault signal for overcurrent protection of both drivers	Output
7	MCLK	Clock signal for sigma-delta current measurement	Output
8	GND	Ground	Bidirectional
9	GND	Ground	Bidirectional
10	PWM_L	PWM signal for low side driver	Input
11	TEMP	Single ended temperature measurement signal	Output
12	PWM_H	PWM signal for high side driver	Input
13	VOLTAGE	Single ended DC Bus voltage measurement signal	Output
14	GND	Ground	Bidirectional

Table 5: Pin Assignment of Jumper J3 (Power Supply Selection Jumper for Current Measurement)

Pin	Label	Function	Direction
1	+5V	Jumper position 1; +5V interface with current measurement	Output
2	+5V/+3V3	Jumper common point for current measurement power supply	Bidirectional
3	+3V3	Jumper position 2; +3.3V interface with current measurement	Output

2.4 Mechanical Data

Table 6 lists the basic mechanical data of the evaluation board.

Table 6: Mechanical Characteristics of the EB1200-355JC Evaluation Board

Description	Value
Number of Layers	4
PCB Copper Thickness	70 µm to all layers
PCB Insulating Material	FR4
Board Length	219.4 mm
Board Wdth	161.3 mm
Board Height	60.6 mm
PCB Thickness	1.6 mm

3 Circuit Description

This section provides an in-depth insight of the EB1200-355JC gate driver evaluation board features.

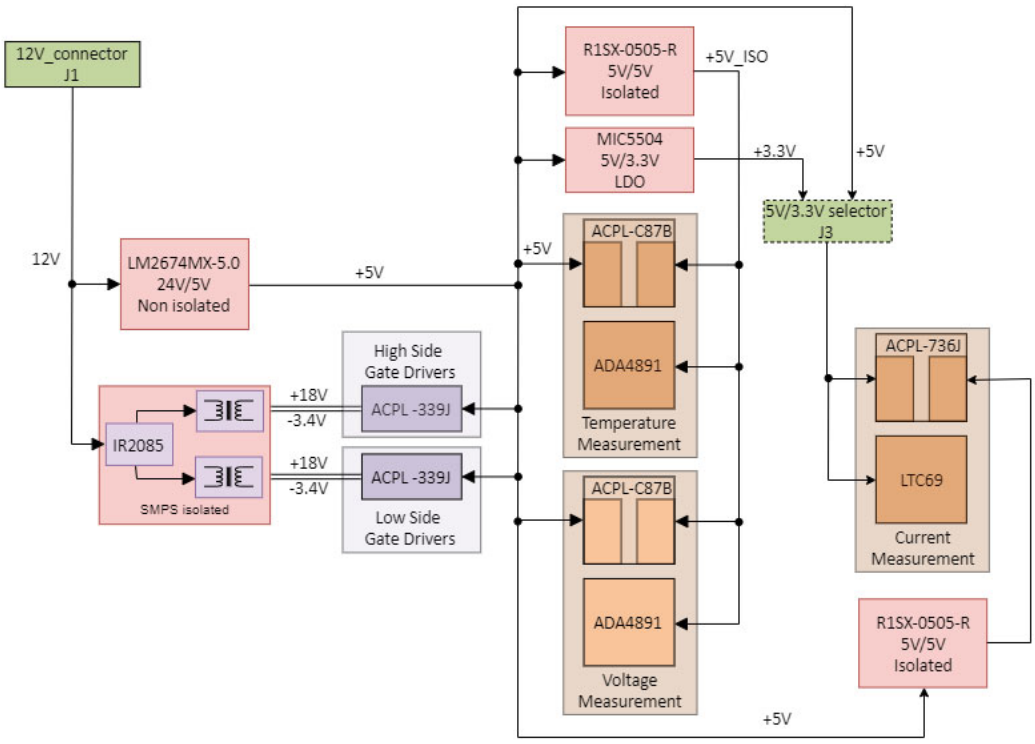
3.1 Power Management

Auxiliary power management block diagram of the EB1200-355JC is shown in Figure 4. The evaluation board, by default, is supplied from an external +12V source.

The EB1200-355JC is equipped with switch mode power supply (SMPS) that provides two isolated dual outputs of +18V and –3.4V for each gate driver high-voltage side. This circuitry is shown in Figure 5. SMPS is based on IR2085 self-oscillating half bridge gate driver and two transformers with 1:2 ratio.

In case of a need for evaluation of the semiconductor switching characteristics with other positive/negative gate voltage levels, the external auxiliary power supply could go down to 11V; in which case, the output of the SMPS provides +15V, –4V. To ensure a positive voltage level of +15V, change the Zener diodes in output stage of the SMPS (D20 and D25) with the Zenner diodes that clamp voltage equal to 15V. These enable in depth evaluation of switching characteristics or benchmarking SiC modules in the DUAL 1B package from different semiconductor manufacturers.

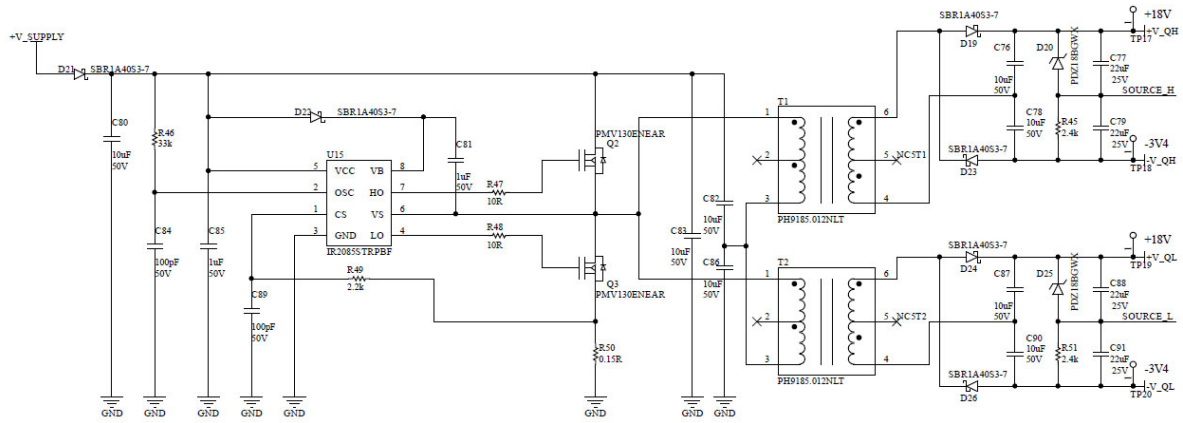
Figure 4: Power Management Block Diagram



The main 12V/5V power supply is realized with an LM2674 DC-DC switching regulator, as shown in Figure 6. The +5V output supplies the low voltage side of the ACPL-355JC gate drivers and two ACPL-C87B voltage sensors. The +5V power supply is capable of driving 500mA load and supplies all ICs on the board.

There are two isolated 5V/5V voltage regulators R1SX-0505-R; one provides isolated 5V for ACPL-C87B ICs, and the other provides isolated 5V for ACPL-736J sigma-delta modulator, as shown in Figure 7.

Figure 5: Isolated SMPS for Gate Driver Output Stage



The output current measurement is based on Broadcom's isolated sigma delta modulator ACPL-736J. Because the low voltage side of the ACPL-736J supports a power supply of either 5V or 3.3V, the EB1200-355JC enables voltage level selection using a jumper on the J3 connector. For this purpose, the EB1200-355JC features the high performance LDO 5V/3.3V in case 3.3V digital logic is to be used, as shown in Figure 8.

Figure 6: +12V/+5V DC/DC Switching Regulator Circuit

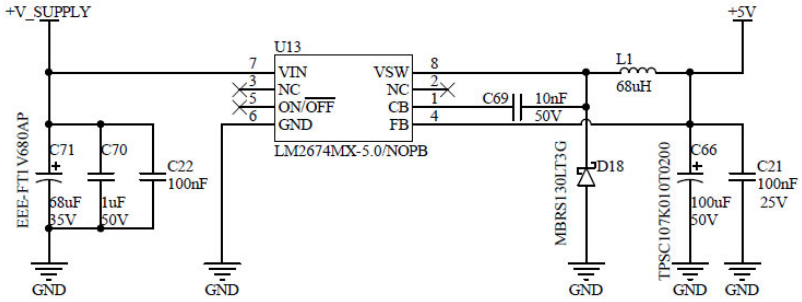


Figure 7: +5V to +5V_ISO Unregulated Isolated DC/DC Converter

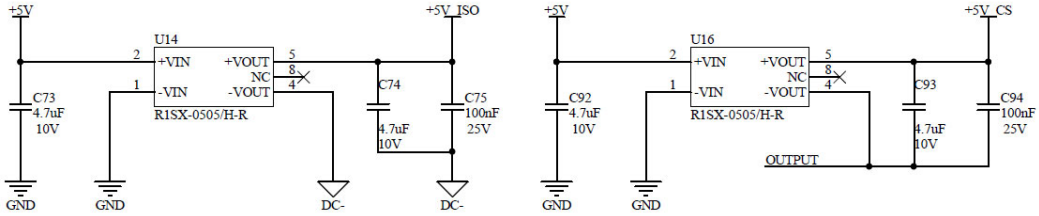
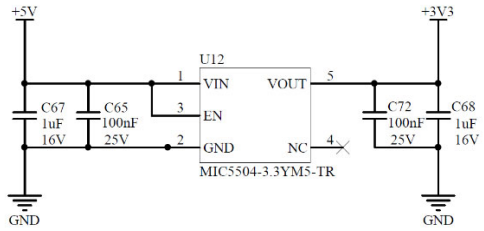


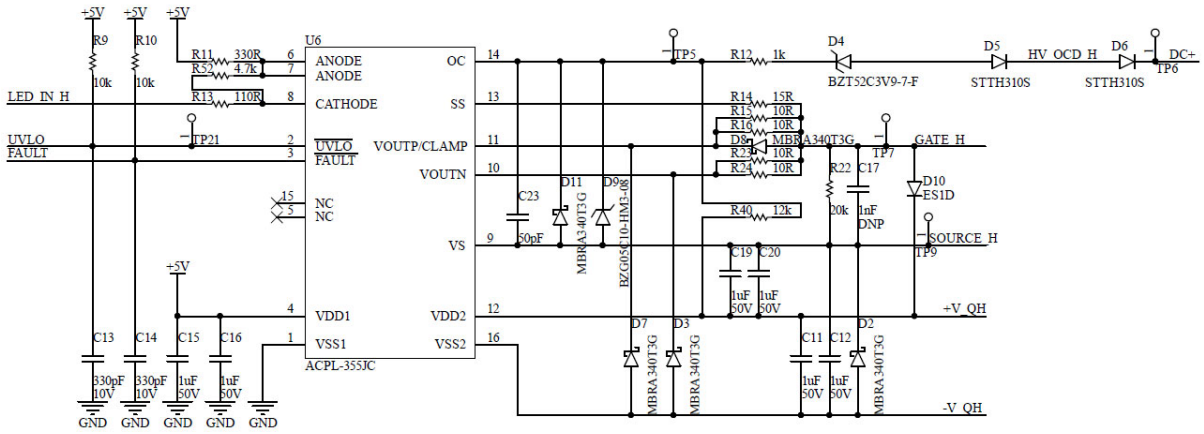
Figure 8: +5V/+3V3 LDO



3.2 Gate Driver Circuit

This section describes the gate driver circuitry on the EB1200-355JC. The related features and functionalities are described in the following paragraphs. The gate drive circuitry is shown on Figure 9.

Figure 9: ACPL-355JC Gate Driver Circuitry



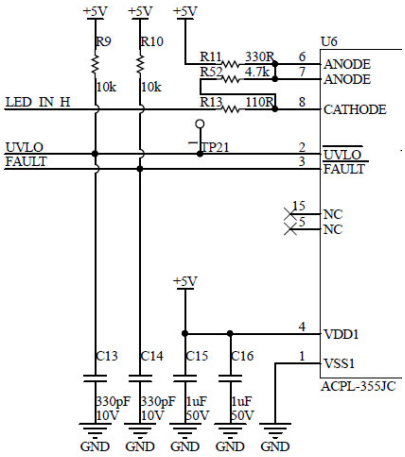
With a maximum peak output current of 10A, the ACPL-355JC can drive most of the power IGBT/MOSFET switches directly without an external push-pull stage. This driver contains an LED, electrically isolated and optically coupled to an integrated circuit, on the gate driver high-voltage side, with two power output stages with CLAMP function to prevent the parasitic turn-on due to the parasitic Miller current during turn-off transient. Other features encompass under-voltage and overcurrent protection features, as well as soft shut down at fault.

3.2.1 Gate Driver Circuit: Low-Voltage Side

The low-voltage side of the gate drive circuitry, shown in Figure 10, contains the power supply for the ACPL-355JC, an LED anode and cathode, and safety reporting signals (FAULT and UVLO).

The resistor responsible for the LED forward current setting is split in two, and those resistors are placed on anode pins 6 and 7 and cathode pin 8 to balance the common mode impedances at the LED's anode and cathode. This helps to equalize the common mode voltage change. Resistor values are selected as referred to in the data sheet of the gate driver.

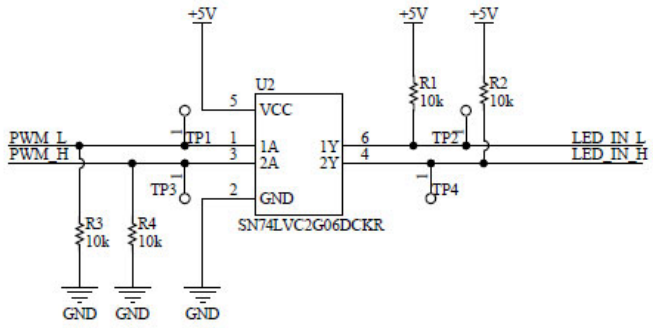
Figure 10: Gate Driver Circuit: Low-Voltage Side



While the input LED is directly polarized and there is no fault, the turn-on command is transferred to the high-voltage side, and the VOUTP pin of the ACPL-355JC is set high. The ANODE pin is pulled high using resistor R11. The input signal LED_IN_L is connected to the CATHODE pin. When the input LED_IN_L signal is low, the LED is directly polarized, and MOSFET is turned on. In case the input signal LED_IN_L is high, voltage across the LED and the two resistors is low; therefore, LED is not conducting and the MOSFET is in the off state.

External PWM signals, which propagate through user interface connector, are buffered, as it is shown on Figure 11. As buffer features an open drain output, inputs of the buffer are pulled down while outputs of the buffer are pulled high, to ensure that MOSFET module is off in case that the input PWM signals are in high impedance states.

Figure 11: PWM Buffer

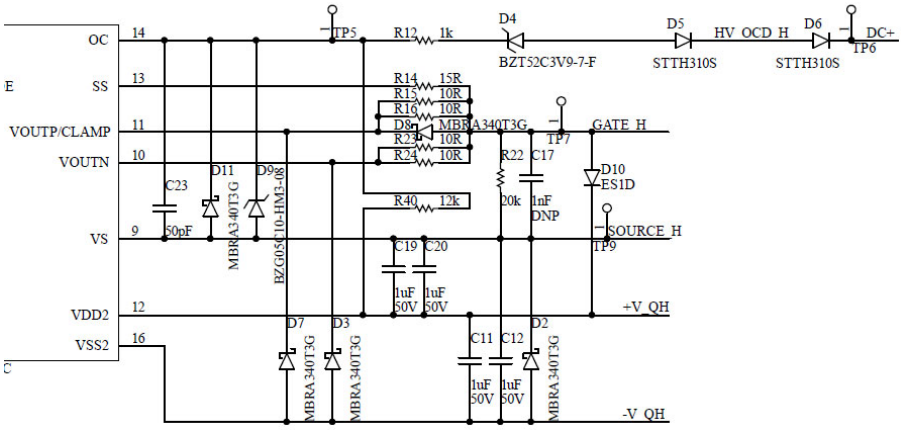


UVLO and FAULT signals are open drain, so they are pulled-up with 10-kΩ resistors, and have 330-pF filtering capacitors. Logic for these signals is inverted, so they are suitable for wired OR applications. In this case, FAULT signals from both drivers are connected in parallel, and the same is done with UVLO signals, so that the user is notified if FAULT or UVLO has occurred regardless on which MOSFET. UVLO has the highest fault priority followed by FAULT.

3.2.2 Gate Driver Circuit: High-Voltage Side

The secondary side of the gate drive circuitry, shown on Figure 12, includes OC and UVLO protection-related circuits and soft shut down in case of fault.

Figure 12: Gate Driver Circuit: High-Voltage Side



When the gate driver input is set to high, VOUTP becomes high and +18V is supplied to the MOSFET gate using two 10Ω (default value) parallel resistors. When the gate driver input is set to low, VOUTN pin becomes active and –3.4V is supplied to the MOSFET gate using two 10Ω (default value) parallel resistors, and when VOUTN is low, –3.4V is connected to the MOSFET gate. These voltages are referred to the source of the respective MOSFET. The switching time is determined by the gate charging and discharging process. Smaller gate resistors lead to the higher peak gate current that decreases turn-on and turn-off times, subsequently reducing switching losses. However, two small gate resistors may introduce voltage spikes and current oscillations on MOSFET or can overload the gate driver IC. For the proper selection of the gate resistors, several criteria must be fulfilled.

First is the limit of the gate peak current. Consider the MOSFET internal R_{Gint} when calculating ideal value for gate resistor, and internal minimum turn-on resistance of driver R_{VOUTP}. The equation for the gate resistor calculation is provided in the ACPL-355JC data sheet.

$$R_G \geq \frac{V_{DD2}-V_{SS2}}{I_{O(PEAK)}} - R_{Gint} - R_{VOUTP}$$

The next step in choosing the right gate resistor is checking the power dissipation of the ACPL-355JC gate driver. If the power dissipation is too high, increase the resistance of the gate resistor. For instructions on choosing the gate resistor, refer to the ACPL-355JC data sheet.

Finally, switching performance, especially turn-off speed, must be measured because the fast-switching transients in combination with parasitic inductances in the switching loop can generate high over voltages and oscillations.

To assure the constraints described previously during the worst-case conditions, the EB1200-355JC comes with 5Ω gate resistors for positive and 5Ω for negative gating. Both resistances are realized with two parallel resistors to increase the power dissipation capacity of the gate circuit. In addition, the evaluation board is designed to enable Broadcom customers to evaluate switching characteristics of the semiconductors by changing or combining turn-on and turn-off resistors.

Additionally, a Schottky diode D8, placed between gate and VOUTP pin, is used together with CLAMP function to shunt parasitic Miller current during the off cycle.

3.2.3 Protection Features

VOUTP and VOUTN will remain functional until OC or UVLO protection features are activated.

3.2.3.1 OC

The OC-pin monitors the MOSFET drain-source voltage. OC fault detection circuitry must remain disabled for a short period of time following the turn-on of the MOSFET to allow the drain-source voltage to settle down and fall below the OC threshold. This period, called the OC blanking time, is determined by the blanking capacitor and the internal current source provided in the gate driver IC. The total blanking time is calculated in terms of internal blanking time ($t_{OC(BLANKING)}$), external capacitance (C_{BLANK}), FAULT threshold voltage (V_{OC}), and blanking capacitor charge current (I_{CHG}) as follows.

Equation

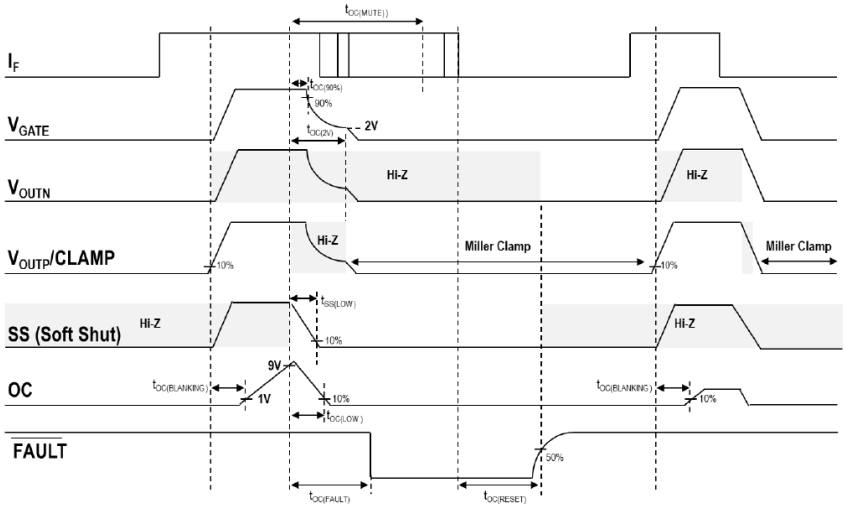
$$t_{BLANK} = t_{OC(BLANKING)} + \frac{C_{BLANK} \cdot V_{OC}}{I_{CHG}}$$

C_{BLANK} corresponds to capacitance C23 (C36 for the low-side driver) in Figure 12, V_{OC} fault threshold voltage is nominally 9V, and I_{CHG} OC charge current is 1 mA. Nominal blanking time also represents the longest time it will take for the driver to respond to an OC fault condition. The blanking time can also be shortened by adjusting the R40, 12-kΩ resistor, which also charges the blanking capacitor using VDD2. When the OC fault is detected and blanking time has passed, both VOUTP and VOUTN go low and soft shutdown starts. The soft shutdown resistor R14 (R53) should be small enough to speed up the shutdown of MOSFET to prevent overheating.

When OC conditions are met, internal feedback channel is activated which brings the FAULT output from high to low. When the fault is detected, VOUTP and VOUTN are set to High-Z state for $t_{OC(MUTE)}$ time. After this time, the LED input needs to be kept low for $t_{OC(RESET)}$ before the fault condition is cleared. The FAULT status returns to high and the SS output returns to the High-Z state. If the LED goes high during $t_{OC(RESET)}$, the $t_{OC(RESET)}$ timing resets, and the LED input must be kept low for another $t_{OC(RESET)}$. Figure 133 shows the circuit behavior during an overcurrent event.

The total voltage measured at the OC pin is the sum of the drain-source voltage across MOSFET switch and total voltage drop on following components: R12 (R20), D5 (D13), D6 (D14), D4 (D12). The drain-source voltage threshold value for OC triggering is equal to $9V – (I_{CHG} \times R_{R12}) – V_{D5} – V_{D6} – V_{D4}$, where V_{D5} and V_{D6} are forward voltage drops of diodes D5 and D6, respectively, and V_{D4} is the blocking voltage of the Zener diode D4. The high-voltage diodes D5 (D13) and D6 (D14) conduct the current from the OC pin through the MOSFET when it is in on state, allowing for drain-source voltage sensing, and to block high voltages when MOSFET is in the off state. Proper adjustment of the OC detection level can be performed by choosing the correct voltage rating of the Zener diode D4.

Figure 13: Driver Behaviors during an Overcurrent Event



In the current design, the threshold voltage is set to be 3.2V. This means that the OC protection reacts after MOSFET drain current reaches approximately 300A for the selected MOSFET at 25°C ambient temperature.

The freewheeling of the antiparallel diodes connected across the MOSFET can have large instantaneous forward voltage transients. This may result in a large negative voltage spike on OC pin which will draw substantial current from the driver if protection is not used. Limiting this current is done using a 1-kΩ resistor placed in series with OC diodes.

Negative voltage spikes typically generated by inductive loads, or reverse recovery spikes of the IGBT/MOSFET free-wheeling diodes can bring OC pin voltage above the threshold, thus generating false fault signal. To prevent this, Zener and Schottky diodes are placed across the OC and VS pins. Zener diode protects OC pin from positive high transient voltage and Schottky prevents forward biasing of the substrate diode of the gate driver optocoupler.

Because MOSFETs are more sensitive to overcurrent than IGBT, the OC protection must be faster. That can be done by tweaking OC blanking time, thus one additional resistor (R40) is added between the OC pin and VDD2. This allows an additional blanking capacitor charging current component from the secondary driver power supply, so that blanking time can be shorter and can be adjusted using resistor R40.

3.2.3.2 UVLO

Insufficient gate voltage on the MOSFET during the turn-on phase can increase the voltage drop across the MOSFET. This results in a large power loss and MOSFET damage due to high heat dissipation. The ACPL-355JC monitors the output power supply constantly. If the power supply voltage is lower than the UVLO threshold, the driver output turns off to protect the MOSFET from low-voltage bias. UVLO protection precedes OC protection.

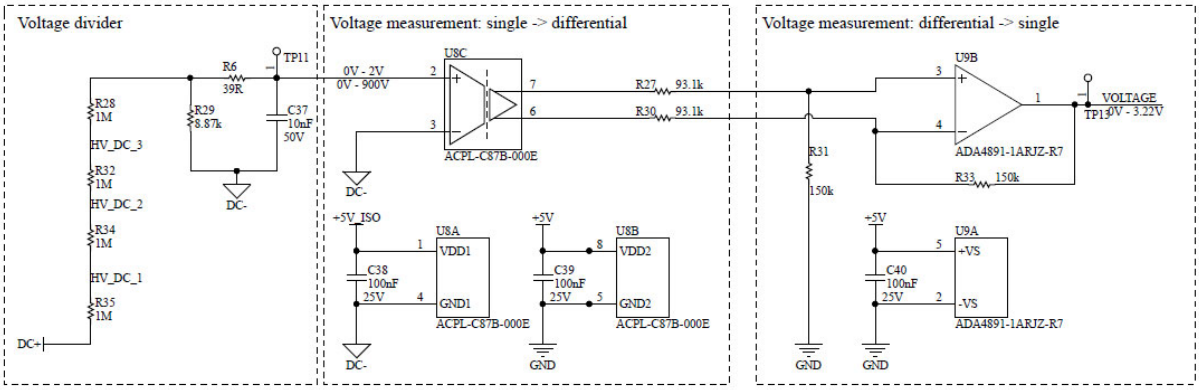
3.3 Measurements

The EB1200-355JC features DC bus voltage measurements, MOSFET module temperature measurement, and output current measurement. Available measurements are described in the following sections.

3.3.1 Isolated DC Bus Voltage Measurement

The isolated DC bus voltage measurement is obtained by using the ACPL-C87B optically isolated high-precision voltage sensor. Figure 14 shows voltage measurement circuitry.

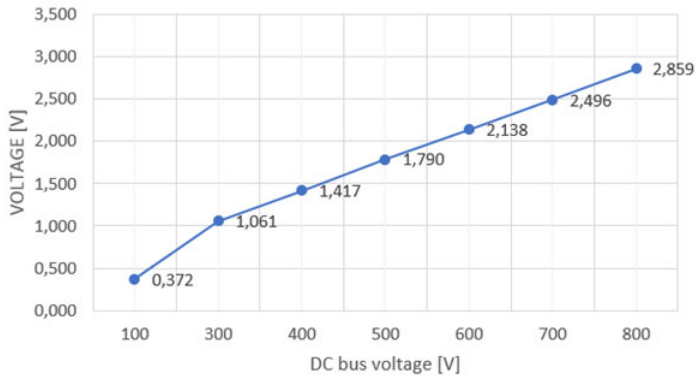
Figure 14: Isolated DC Bus Voltage Measurement



DC bus voltage is brought to voltage divider, which scales 900V to 2V. In this design, four 1-MΩ (R28, R32, R34, R35) resistors and one 8.87-kΩ resistor (R29) are used to form the voltage divider. These resistors must have low tolerance due to required precision. Resistor R6 and capacitor C37 are added for antialiasing.

The obtained signal is then transformed in differential signal on the secondary side of the ACPL-C87B. To make the measurement more user-friendly, this differential signal is transformed back to single-ended signal using ADA4891 low-cost high-speed amplifier. Output of the circuitry is 0V to 3.2V analog signal which is a linear representation of DC bus voltage ranging from 0V to 900V. The typical DC bus voltage response of the measurement circuit is shown in Figure 15.

Figure 15: Typical Voltage Measurement Characteristic



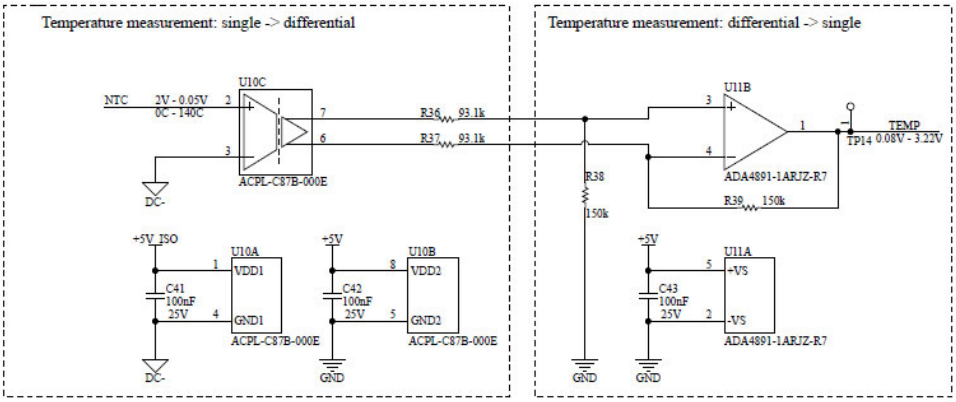
In case of using the proposed single-ended configuration for the end-user application design, add an additional filter (capacitor parallel to the R33) across the operational amplifier to attenuate high-frequency spikes.

3.3.2 Isolated Module Temperature Measurement

Isolated temperature measurement is designed using the same isolated ACPL-C87B voltage sensor as in DC bus voltage measurement circuit and can be seen in Figure 16. A similar circuit configuration is used for the temperature measurement.

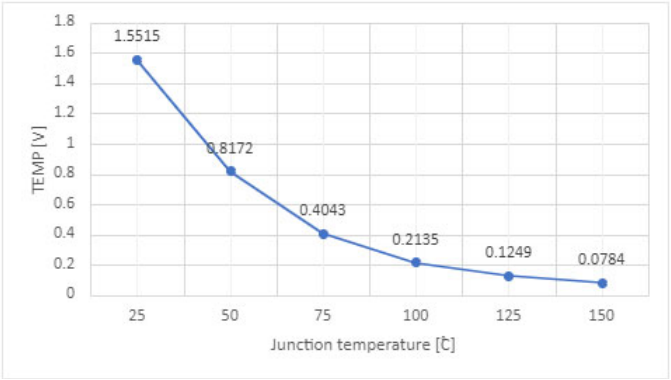
The DUAL 1B module has an internal NTC thermistor mounted on the DCB ceramic. Isolated 5V is supplied to the series connection of the NTC thermistor and two 10-kΩ resistors (R25 and R26), as presented on the Figure 33. This forms a voltage divider, and the measured temperature range from 0°C to 140°C is represented with voltages, at the output of the circuit, from 2V down to 0.05V. The rest of the temperature measurement circuitry is the same as in DC bus voltage measurement.

Figure 16: Isolated Temperature Measurement



The typical response of the temperature measurement circuit is shown in Figure 17. The output voltage range can be adjusted by changing the value of resistors R36, R37, R38, and R39 in the amplifier circuit.

Figure 17: Typical Temperature Measurement Characteristic



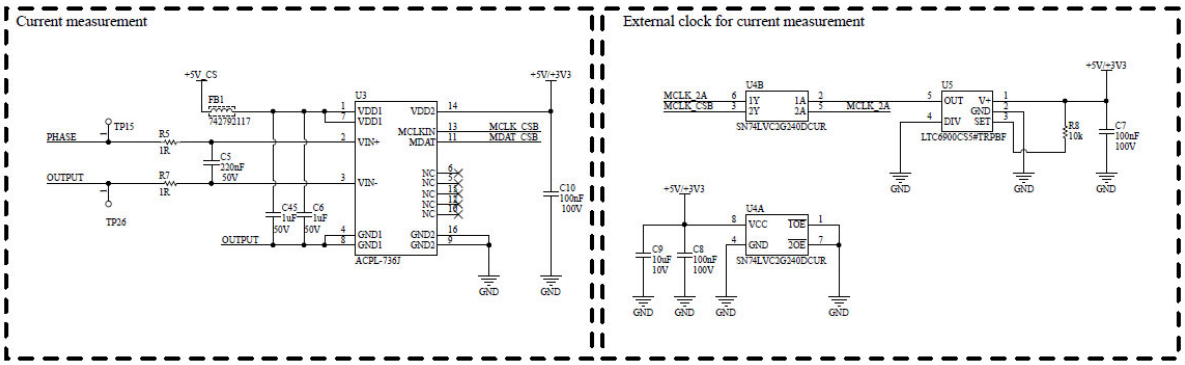
Output Current Measurement

The MOSFET half-bridge output current measurement is realized using the ACPL-736J current sensor and 300-µΩ shunt resistor (R63). The ACPL-736J features a linear range of ±50 mV, thus using the suggested shunt resistor currents provides current measurement range of ±160A (absolute peak value). The thermal limits of the MOSFET half-bridge and PCB copper traces limit the output current of the evaluation board.

The ACPL-736J is a 1-bit, second-order sigma-delta modulator, with galvanic isolation based on the optical coupling technology, that converts an analog input signal into a high-speed datastream. The ACPL-736J operates with the power supply range of 3.3V or 5V, which enables flexibility regarding the user microcontroller power supply.

The ACPL-736J is driven by the external clock coupled across the isolation barrier, which allows synchronous operation with any digital controller. Figure 18 shows the output current measurement circuit with external clock circuit. The signal information is contained in the modulator data as a density of 1s with data rate up to 20 MHz, and the data are encoded and transmitted across the isolation boundary where they are recovered and decoded into high-speed data stream of digital 1s and 0s. The original signal information can be reconstructed with a digital filter.

Figure 18: Current Measurement Circuit with External Clock



Combined with superior optical coupling technology, the modulator delivers high noise margins and excellent immunity against isolation-mode transients. With 0.5-mm minimum distance through insulation (DTI), the ACPL-736J provides reliable double protection and high working insulation voltage, which are suitable for fail-safe designs.

3.3.3 Switch Current Measurement

The EB1200-355JC features holes dedicated to enable user to measure the high-side switch transient current with the high frequency mini Rogowski probe (Figure 19) and evaluate switching characteristics of the SiC MOSFET.

Figure 19: High-Side Switch Current Measurement with a Rogowski Probe

3.4 Connectors

Connectors of EB1200-355JC are described in the following sections.

3.4.1 Power Connectors for the High-Voltage Side

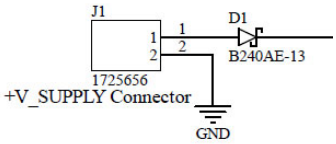
The board is supplied with the power connectors realized with screw (M3 screw) terminals. The following power connectors are available on the board:

- J4 for the DC+.
- J5 and J7 for the DC–.
- J6 for the half-bridge output.

3.4.2 Vcc +12V Connector

Auxiliary power supply connector +12V is a standard two-pin PCB terminal block. This connector supports the wire cross section of maximum 0.5mm^2. Figure 20 shows the connector schematic.

Figure 20: +12V Power Supply Connector

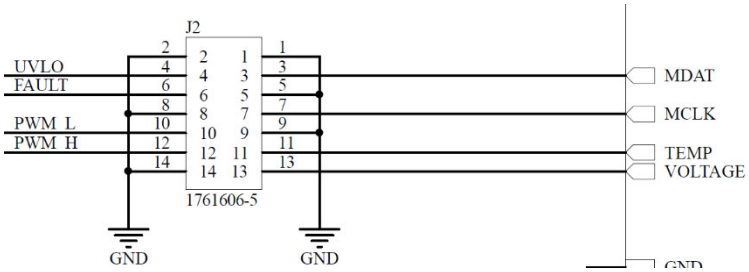


For reversed voltage protection, the Schottky diode is placed in series with the main power supply.

3.4.3 User Interface Connector

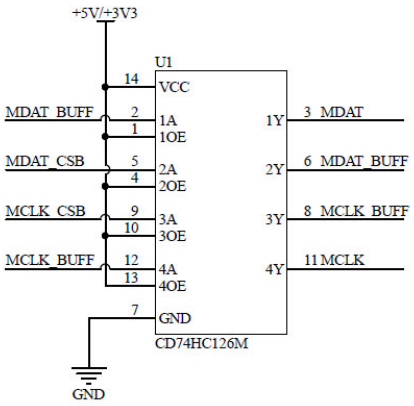
The user interface header connector serves as an interface between the microcontroller or PWM signal source and the EB1200-355JC evaluation board. Figure 21 shows the disposition of signals across this connector.

Figure 21: User Interface Connector



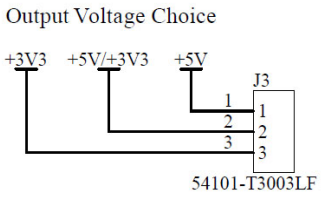
Besides providing input for the PWM signals, user interface connector J2 provides output for the fault signals, DC bus voltage, and module DCB ceramic temperature measurements, as well as buffered CLK and DATA signals for current measurement. In Figure 22, the buffer configuration for CLK and DATA signals is shown. Note that these signal routes must be the same length; therefore, apply length matching in the layout design.

Figure 22: CLK and DATA Double Buffer Configuration



EB1200-355JC gives the user a possibility to select voltage reference to be used for powering the ACPL-736J (output current measurement). Available voltage levels are 5V and 3.3V can be chosen by adjusting jumper J3, which is shown in Figure 23.

Figure 23: Connector J3



4 Setup in Use

WARNING! The EB1200-355JC gate driver evaluation board works with voltages up to 800V and requires that all safety precautions and national accident prevention rules to be undertaken. Reserve installation and use of the board for the skilled technical personnel. A danger of serious injury and damage of property exist if the board is not properly used or installed. Equip the system that is to supply the evaluation board with control and protection devices, in agreement with applicable safety standards.

ATTENTION: Signals dedicated for the high-side driver and the low-side driver must have proper dead time. The board itself does not provide dead time generation. The recommended minimal dead time value is 500 ns.

4.1 Installation of EB1200-355JC

Before starting with the evaluation of the board, consider and observe the following installation steps:

1. Before any installation, visually inspect the board to make sure it contains all components assembled except the module. See Section 6.3, Bill of Materials, for the list of components. The EB1200-355JC, by default, does not contain an assembled module to avoid damage to the module and the evaluation board during transport, as well as to provide the customer an option to use other modules with the same footprint.
2. Assemble the DUAL 1B module. The footprint for the power module (PCB holes) supports both pin type versions, solder and press-fit pins. In both cases, solder the module pins.

3. Ensure that the overcurrent protection feature is well adjusted. Depending on the MOSFET module assembled, consider a readjustment of the OC Zener diode D12 (D4 for the high-side MOSFET), as well as an adjustment of the blanking time for additional resistor R58 (R40 for the high-side MOSFET) (see Section 3.2.3, Protection Features).
4. With the available jumper, select the desired voltage reference for current measurement. Available references are 5V and 3.3V.
5. Connect the user interface connector. Connect the PWM signals as well as the ACPL-355JC output fault signals to the control board with 5V logic.
6. Connect the 12V external power supply. The EB1200-355JC requests a 12V external power supply to enable 5V and 3.3V digital operations and +18V and -3.4V gate driver high voltage-side power supply. Although the polarity is marked, the board is reverse-protected at the Vcc terminal of +12V external supply.
7. Connect the DC bus power supply and the load to the board.

4.2 Evaluation of EB1200-355JC

The EB1200-355JC enables users to evaluate the following items:

- ACPL-355JC driver features
- ACPL-C87B precision voltage sensor features
- ACPL-736J sigma delta modulator features
- Switching characteristics of the SiC power semiconductors in DUAL 1B package
- Half-bridge inverter basic features
- Buck-boost basic features

For the power semiconductor switching characteristics evaluation, with the EB1200-355JC, perform a double pulse test, and measure the switching transients related to the semiconductor and the ACPL-355JC gate driver circuit.

5 Typical Switching and Over Current Protection Characteristics

5.1 Typical Switching Waveforms

Switching waveforms during hard switching of the semiconductors are measured with an oscilloscope using the standard double pulse test procedure. The SiC MOSFET module used for testing is FF11MR12W1M1_B11. Figure 24 shows the turn-on switching transient, while in the Figure 25, the turn-off switching transient is depicted, at the different drain current levels. The switching performance measurements were done with the default gate resistor values, 5Ω for both on and off resistors, and +18V/–3.4V gate power supply. Although the nominal positive gate voltage of the FF11MR12W1M1_B11 is +15V, +18V was selected for the efficiency improvement since higher on state gate voltage reduces effective Rds-on of the MOSFET. This approach is common practice in industry, and, for this reason, short-circuit characterization was also done for this voltage level because it represents the worst case, as the device will have a higher short-circuit current in case it is driven with the higher voltage.

Figure 24: Characteristic Waveforms during the Turn-on Switching Transients at Different Load Currents

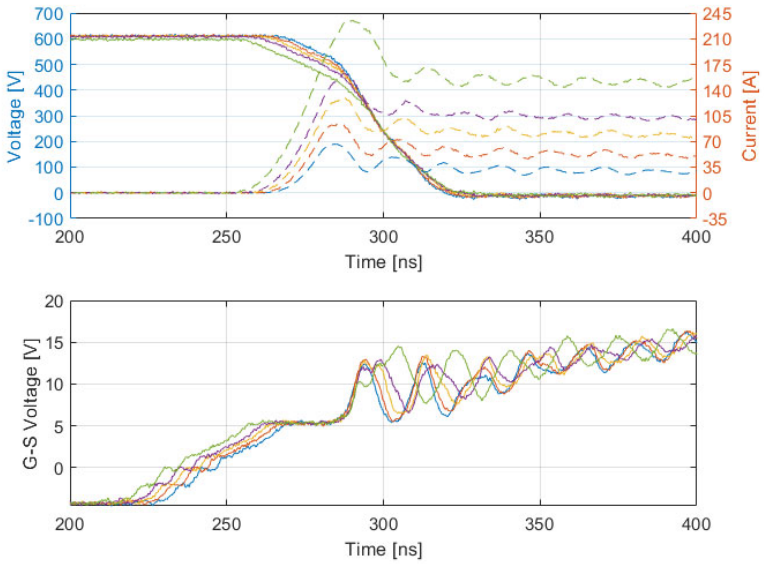
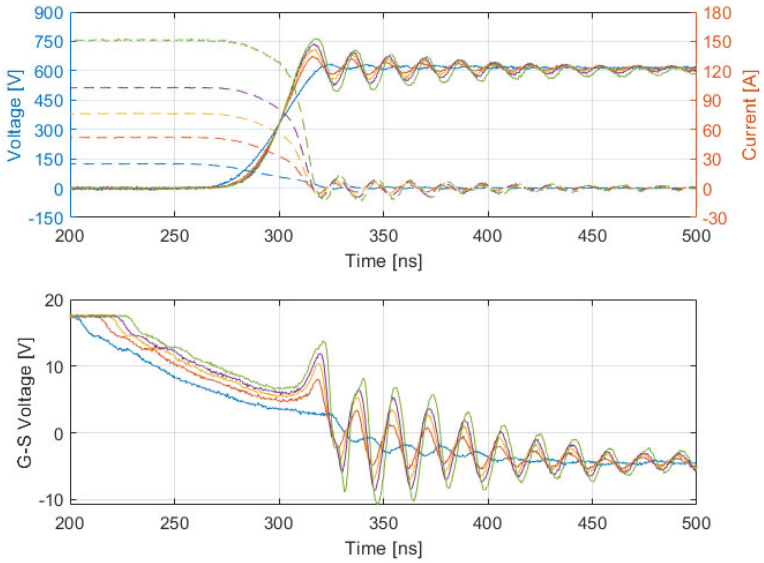


Figure 25: Characteristic Waveforms during the Turn-Off Switching Transients at Different Load Currents



5.2 Typical Switching Losses

In Figure 26, instantaneous power during switching and resulting turn-on switching energy loss is shown for DC voltage of 600V, while in Figure 27 the same waveforms are shown for the case of turn-off transient.

Figure 26: Turn-On Switching Energy Loss at 600V DC Bus

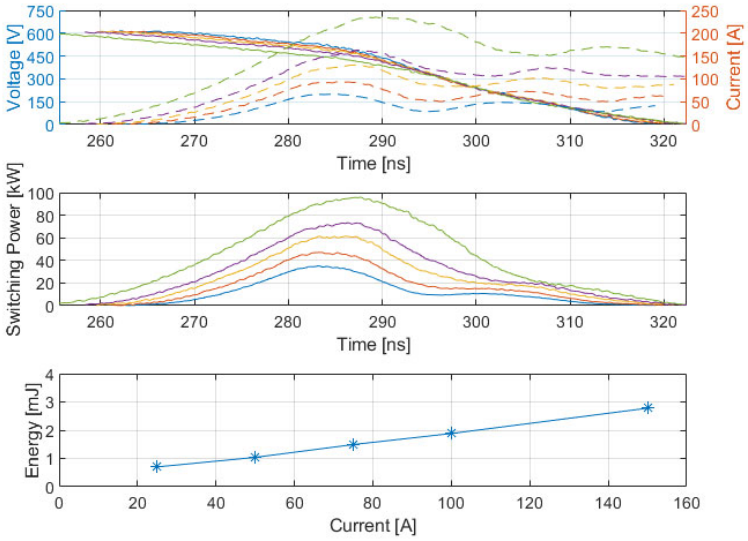
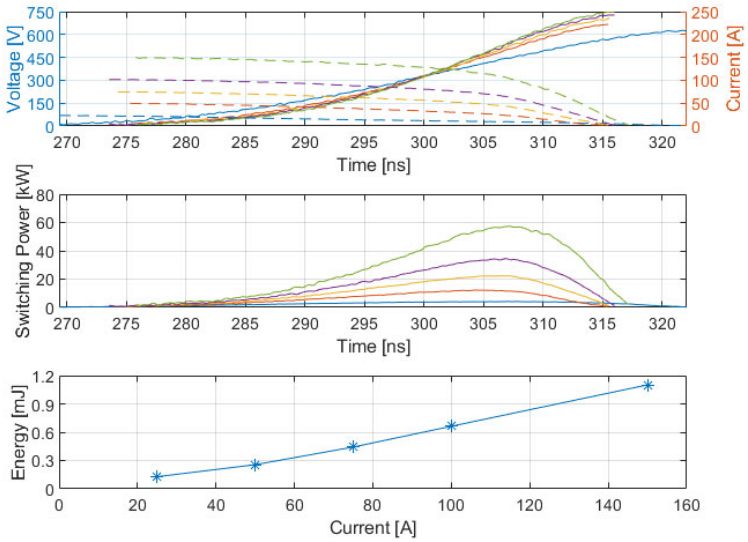


Figure 27: Turn-Off Switching Energy Loss at 600V DC Bus

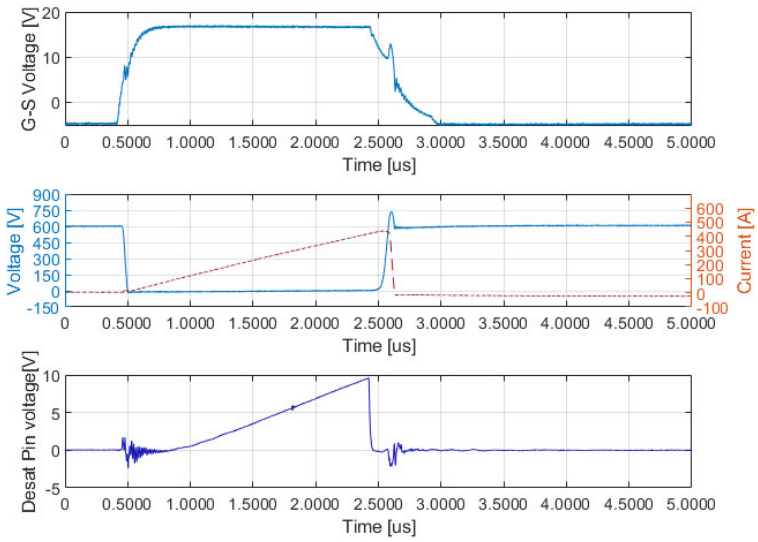


5.3 Typical Overcurrent Protection Performance

The overcurrent protection function is obtained by performing the soft short circuit to the output of the power module FF11MR12W1M1. Figure 28 shows the measurement results. The FF11MR12W1M1 data sheet specifies short-circuit time of 2 µs and maximal short circuit current of 820A (at 150°C chip temperature). For the safety reasons, gate driver overcurrent protection on this board is set to limit the current at around 500A within 2 µs, as described in Section 3.2.3, Protection Features. This corresponds to a short-circuit loop inductance of approximately 2.5 µH. Use this board with the minimal short-circuit limiting inductance of approximately 2 µH. Because SiC MOSFET turns on much faster than a typical IGBT, direct short circuit (simultaneous turn-on of both top and bottom switch) may result in extreme current values within very

short time, much shorter than the SC time specified by the module manufacturers. Note that some manufacturers do not specify the short-circuit robustness; therefore, avoid short-circuit stress in such a module. The soft turn/off function of the ACPL-355JC provides excellent protection from the overvoltage during turn-off phase after the short-circuit detection, which can be observed on the voltage waveform on Figure 28.

Figure 28: Measurement Results from Overcurrent Detection, Soft Short Circuit at Vdc = 600V and Short Circuit Inductance of L ≈ 2.5 µH .



6 Appendix

This section provides full schematics, layout, and bill of materials of the EB1200-355JC. The information enables customers to modify, copy, and qualify the design for production, according to specific requirements.

6.1 Schematics

Figure 29: EB1200-355JC – Top-Level Sheet

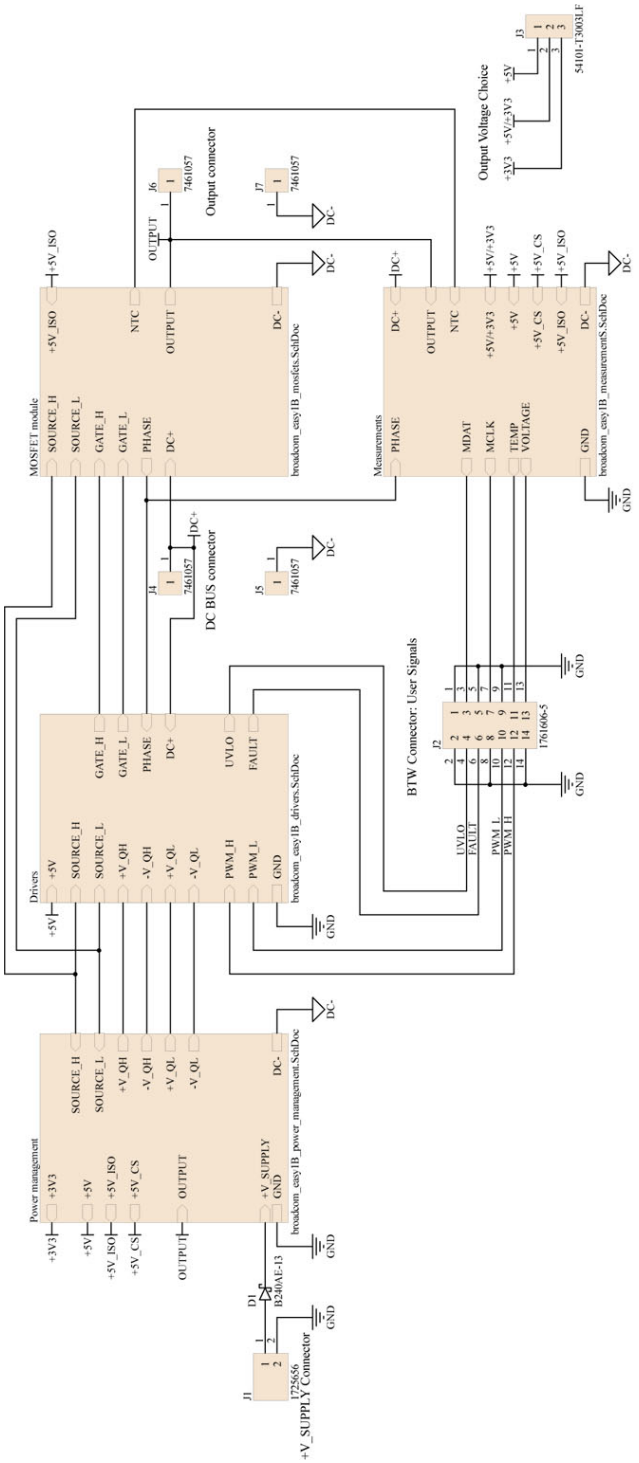


Figure 30: EB1200-355JC – Sheet 1 – Gate Drivers and Buffer

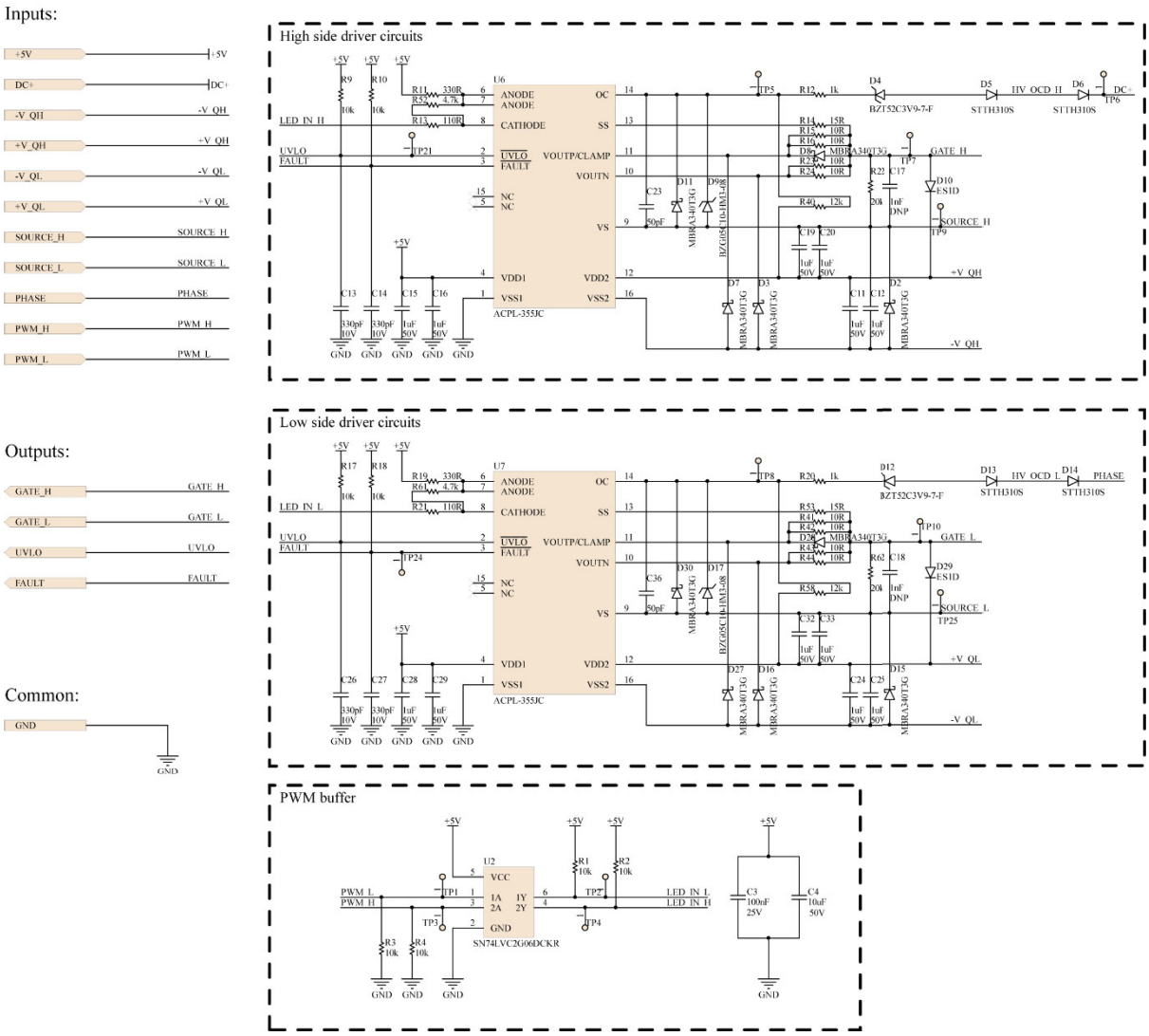


Figure 31: EB1200-355JC – Sheet 2 – Power Management

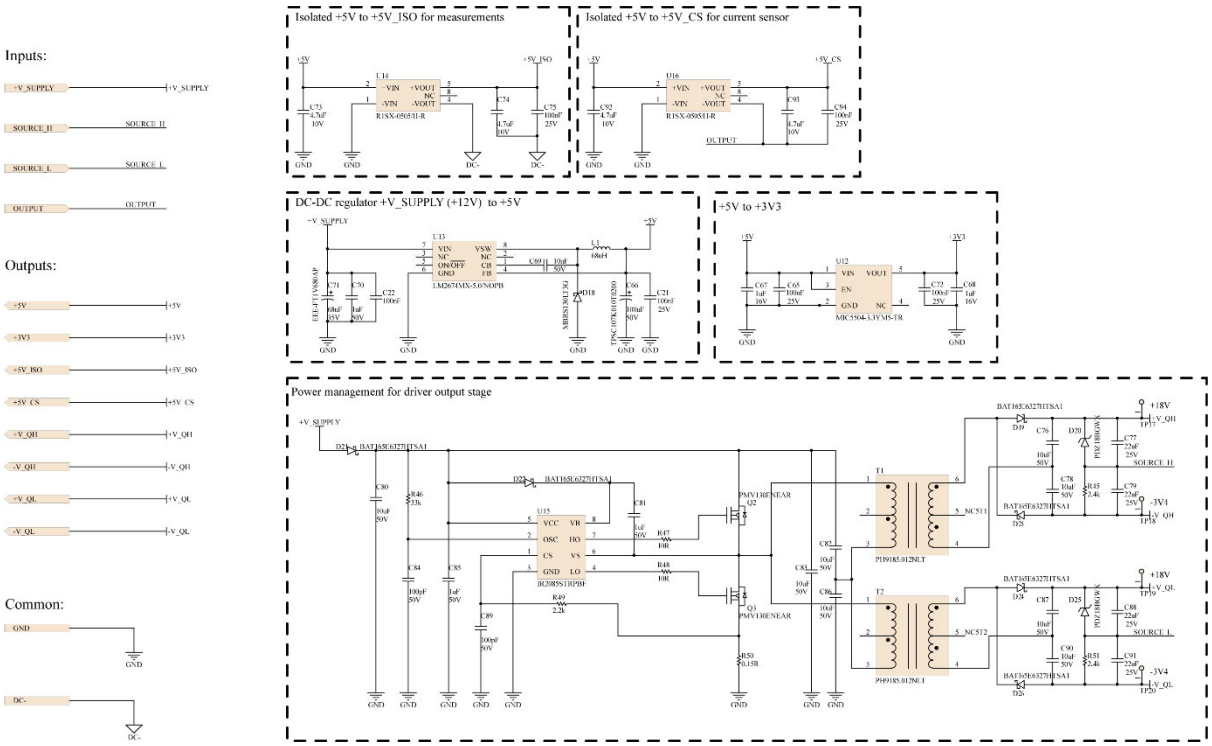


Figure 32: EB1200-355JC – Sheet 3 – Measurements

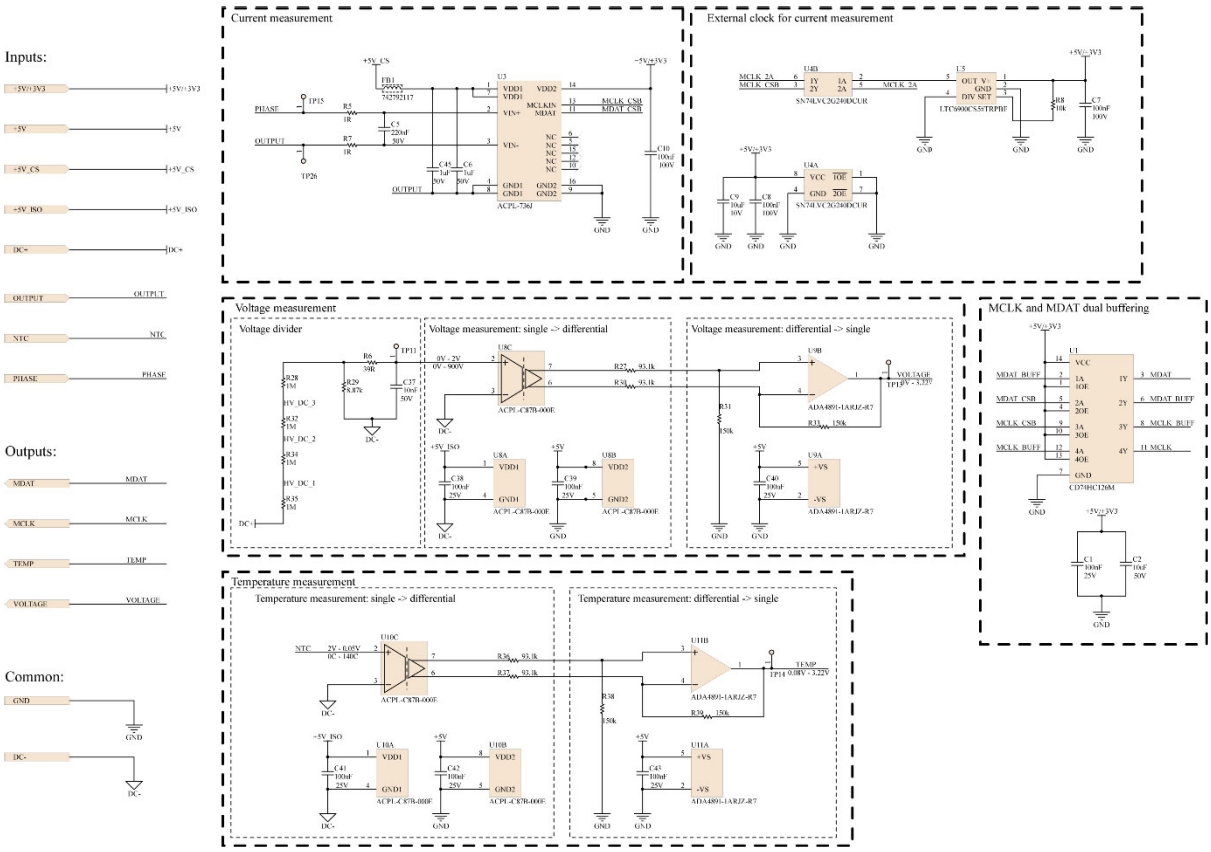
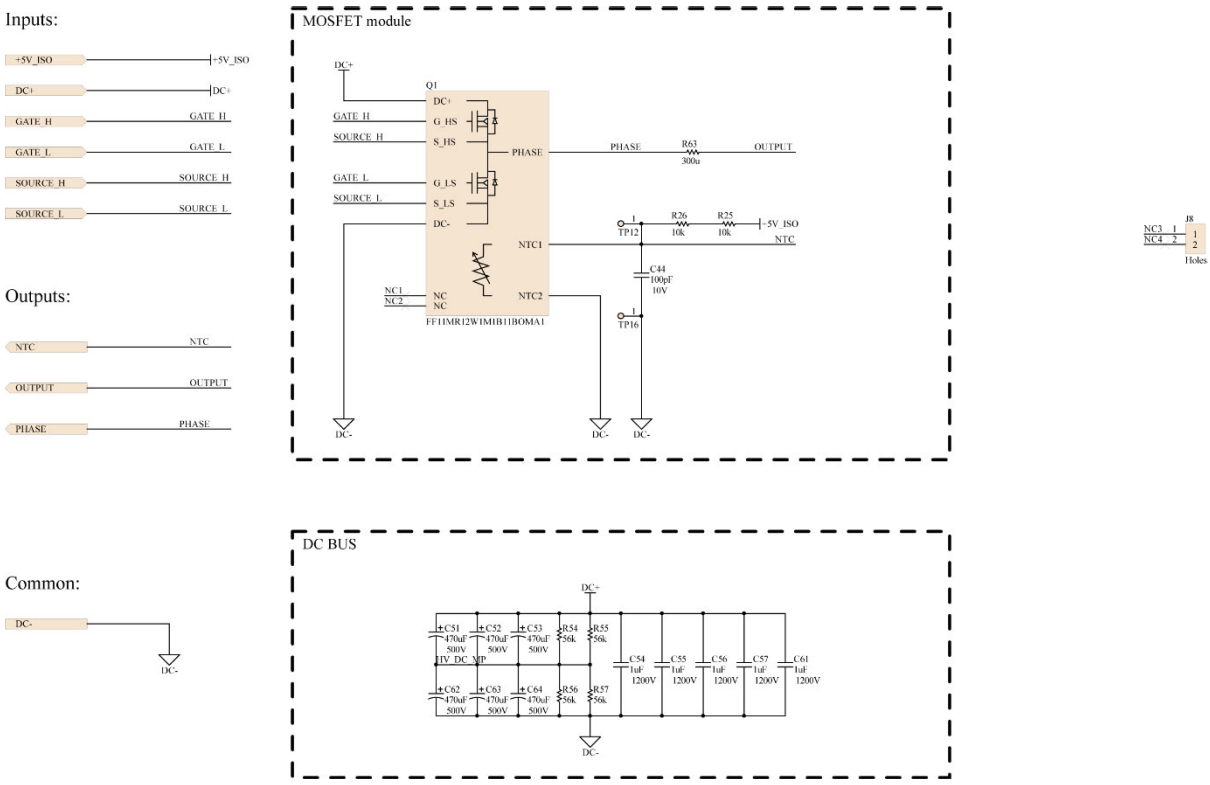


Figure 33: EB1200-355JC – Sheet 4 – MOSFET Module and DC Bus



6.2 Layout

Figure 34: EB1200-355JC – Assembly Drawing

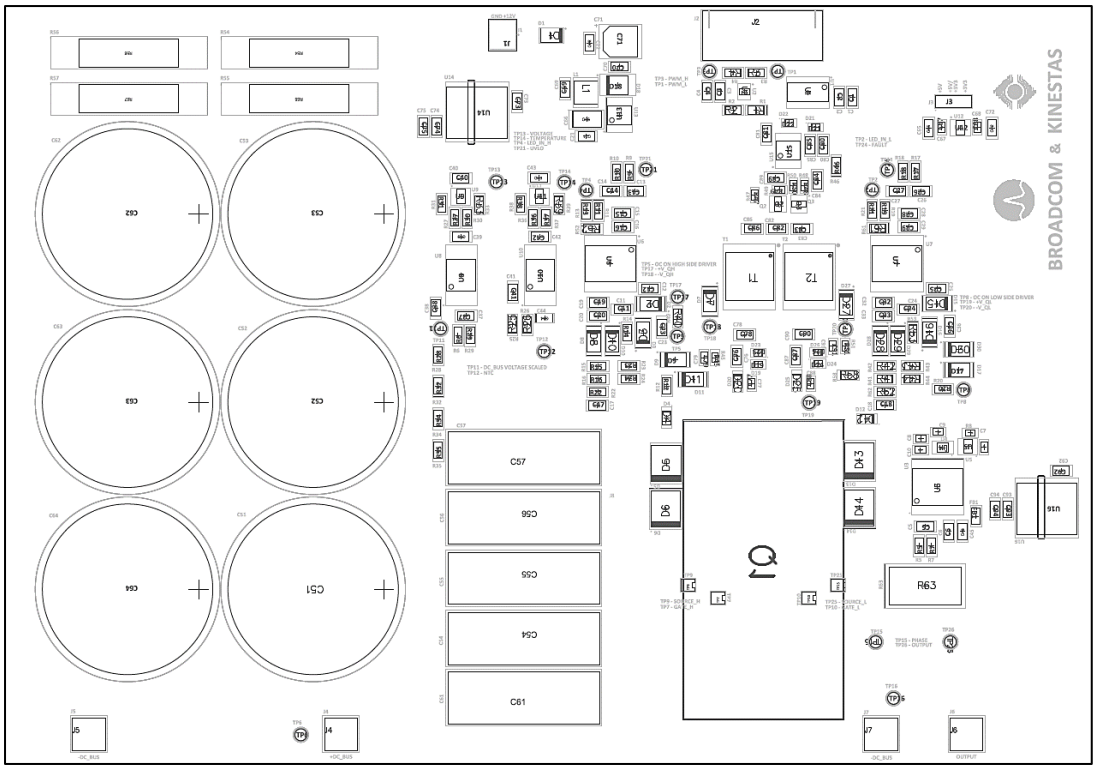


Figure 35: EB1200-355JC – Top Layer

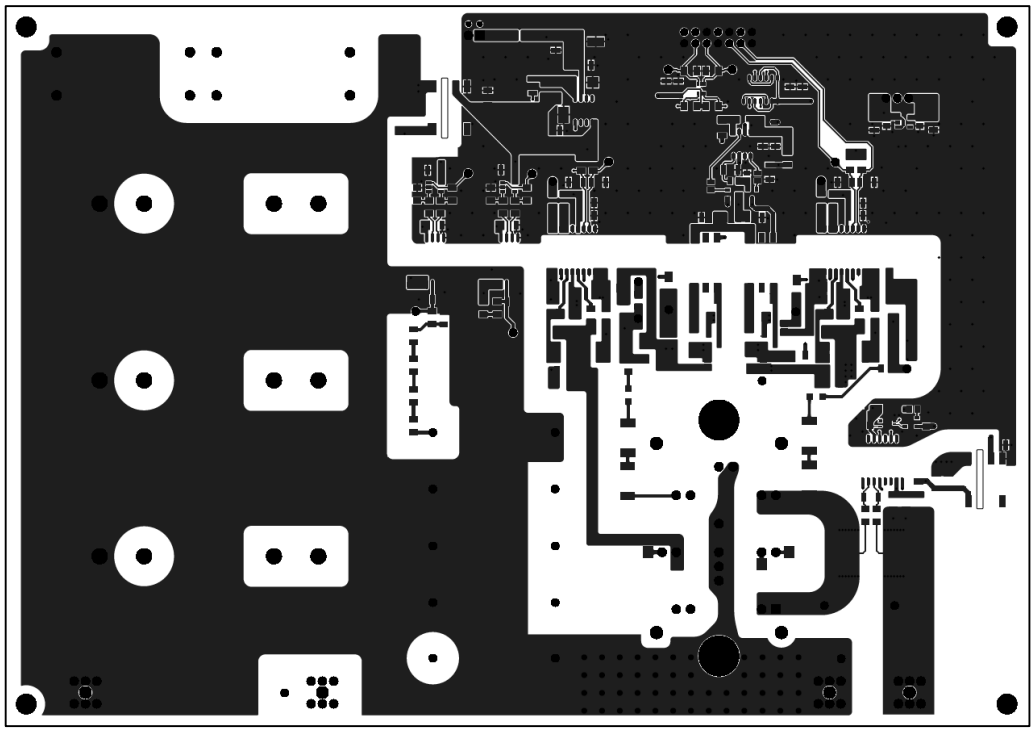


Figure 36: EB1200-355JC – Signal Layer 1

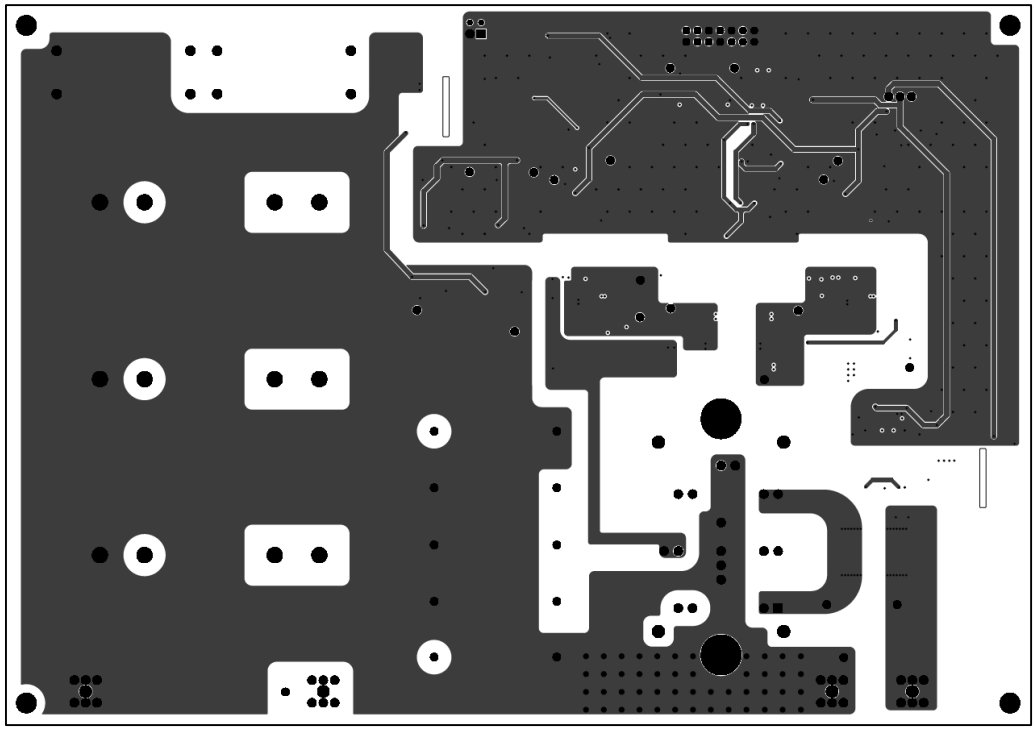


Figure 37: EB1200-355JC – Signal Layer 2

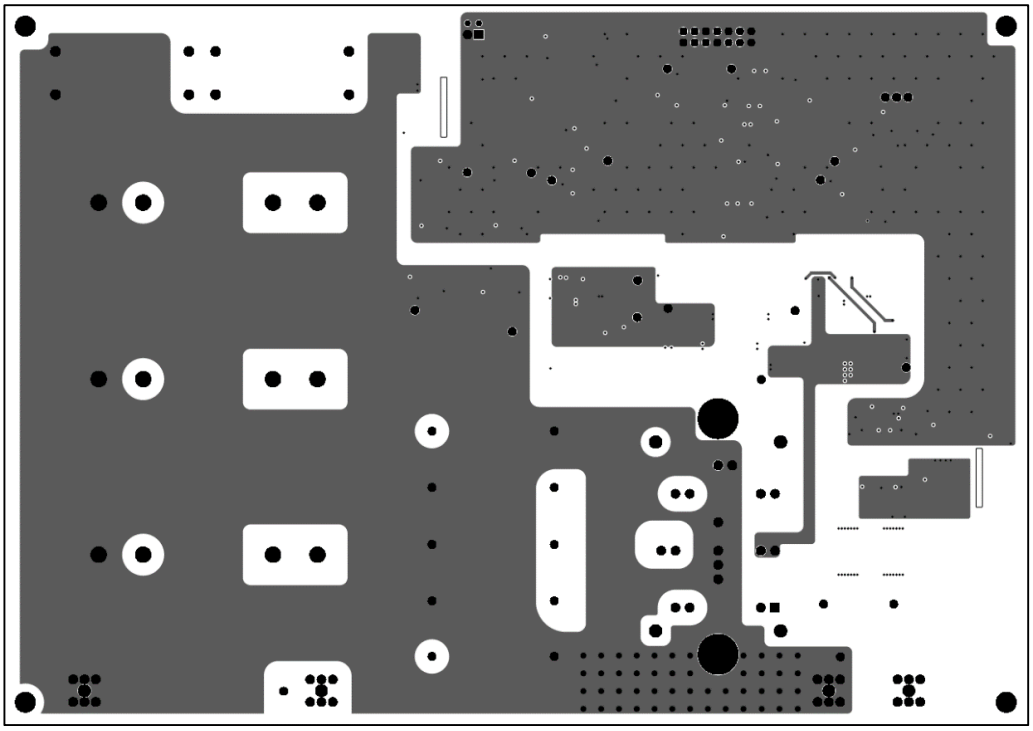
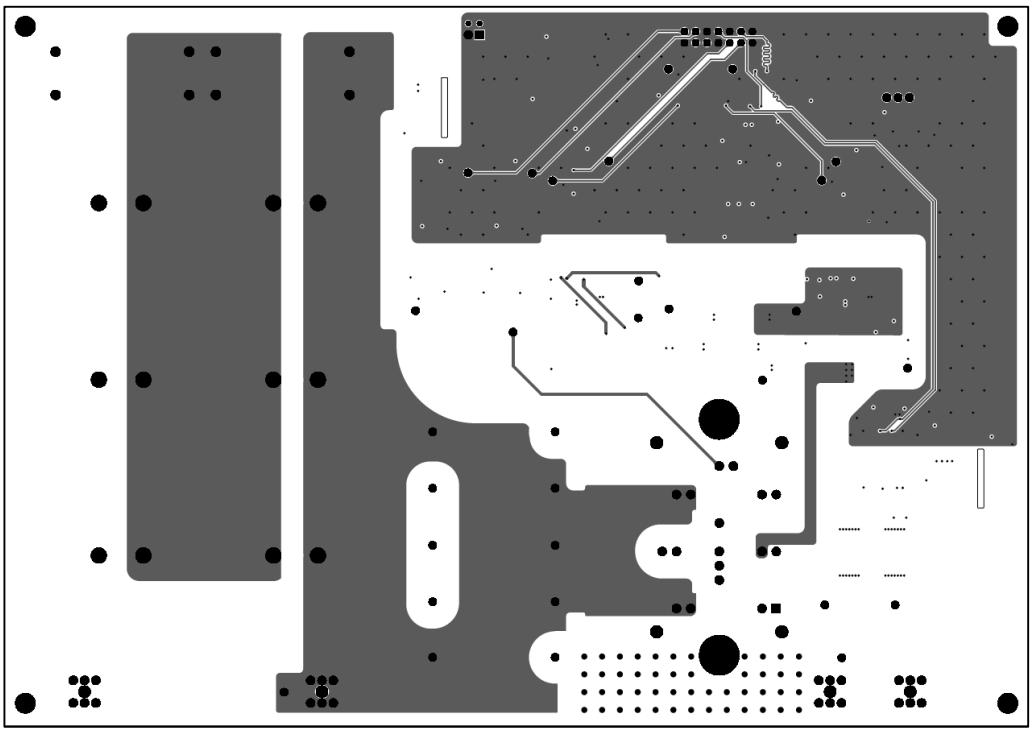


Figure 38: EB1200-355JC – Bottom Layer



6.3 Bill of Materials

The bill of materials of EB1200-355JC is listed in Table 7.

Table 7: Bill of Materials for the EB1200-355JC Evaluation Board

EB1200-355JC, BOM	
Designator	**Manufacturer Part Number**
R50	ERJ-U6SJR15V
R12, R20	CRCW12061K00FKEAC
R28, R32, R34, R35	RK73G2BTTD1004C
R5, R7	CRCW12061R00FKEA
C67, C68	885382207001
C6, C11, C12, C15, C16, C19, C20, C24, C25, C28, C29, C32, C33, C45, C70, C81, C85	SH31B105K500CT
C54, C55, C56, C57, C61	MKP1848C51012JK2
R49	RT0805FRE072K2L
R52, R61	CRCW12064K70FKEBC
R45, R51	RT0805FRE074K7L
C73, C74, C92, C93	885012208017
R29	ERJ-8ENF8871V
R1, R2, R3, R4, R9, R10, R17, R18, R25, R26	RC1206JR-0710KL
R8	RT0805FRE0710KL
C37, C69	VJ1206Y103JXAMC
R15, R16, R41, R42, R23, R24, R43, R44	CRCW120610R0FKEAC
R47, R48	CRCW080510R0FKEAC
C9	885012107010
C2, C4, C76, C78, C80, C82, C83, C86, C87, C90	GRT31CR61H106ME01L
R40, R58	CR1206-JW-153ELF
R14, R53	CRCW120615R0FKEAC
R22, R62	CRCW120620K0FKEAC
C77, C79, C88, C91	GRM21BR61E226ME44L
R46	ERJ-8ENF3302V
R6	AC1206JR-0739RL
C17, C18 - DNP	885012208075
R54, R55, R56, R57	HPC2C563K
L1	VLS5045EX-680M
R27, R30, R36, R37	CRCW120693K1FKEA
C1, C3, C21, C22, C38, C39, C40, C41, C42, C43, C65, C72, C75, C94	885012208058
C7, C8, C10	885012207128
C44	885012008004
C84, C89	885012008043
C66	TPSC107K010T0200
C71	EEE-FT1V101AP
R13, R21	CR1206-JW-111ELF
R31, R33, R38, R39	ERJ-8ENF1503V
C5	C1206C224K5RAC

Table 7: Bill of Materials for the EB1200-355JC Evaluation Board (Continued)

EB1200-355JC, BOM	
Designator	**Manufacturer Part Number**
C23, C36	885012208071
R63	WSLP5931L3000FEB
C13, C14, C26, C27	885012208004
R11, R19	CRCW1206330RFKEA
C51, C52, C53, C62, C63, C64	ALA7DA471DE500
TP1, TP2, TP3, TP4, TP5, TP6, TP8, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP24, TP26	5002
TP7, TP9, TP10, TP25	5190TR
J3	54101-T3003LF
J1	1725656
J2	1761606-5
J4, J5, J6, J7	7461057
FB1	742792117
U6, U7	ACPL-355JC
U3	ACPL-736J
U8, U10	ACPL-C87B-000E
U9, U11	ADA4891-1ARJZ-R7
D1	B240AE-13
D19, D21, D22, D23, D24, D26	SBR1A40S3-7
D9, D17	BZG05C10-HM3-08
D4, D12	BZT52C3V9-7-F
U1	CD74HC126M
D10, D29	ES1D
Q1	FF23MR12W1M1B11BOMA1
U15	IR2085STRPBF
U13	LM2674MX-5.0/NOPB
U5	LTC6900CS5#TRPBF
D2, D3, D7, D8, D11, D15, D16, D27, D28, D30	MBRA340T3G
D18	MBRS130LT3G
U12	MIC5504-3.3YM5-TR
D20, D25	PDZ18BGWX
T1, T2	PH9185.012NLT
Q2, Q3	PMV130ENEAR
U14, U16	R1SX-0505/H-R
U2	SN74LVC2G06DCKR
U4	SN74LVC2G240DCUR
D5, D6, D13, D14	STTH310S

6.4 Test Points

Available test points of EB1200-355JC are listed in Table 8.

Table 8: Available Test Points for the Evaluation Board EB1200-355JC

Test Point Designator	Signal
TP1	PWM_L (before buffer)
TP2	LED_IN.L (after buffer)
TP3	PWM_H (before buffer)
TP4	LED_IN.H (after buffer)
TP5	OC pin on high side driver
TP6	DC+
TP7	SOURCE_H
TP8	OC pin on low side driver
TP9	GATE_H
TP10	SOURCE_L
TP11	Signal from voltage divider on DC+
TP12	NTC
TP13	Voltage measurement
TP14	Temperature measurement
TP15	PHASE
TP16	DC-
TP17	18V for high side driver
TP18	-3.4V for high side driver
TP19	18V for low side driver
TP20	-3.4V for low side driver
TP21	UVLO.H
TP22	FAULT.H
TP23	UVLO.L
TP24	FAULT.L
TP25	GATE_L

7 Disclaimer

This reference manual contains information that should serve only as a reference for initial evaluation and implementation of the Broadcom products. Broadcom does not take responsibility for using and implementing the products in other designs.

Revision History

Version 1.1, November 11, 2021

- Changed Easy 1B to DUAL 1B throughout the document.

Version 1.0, November 10, 2021

- Initial document release.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