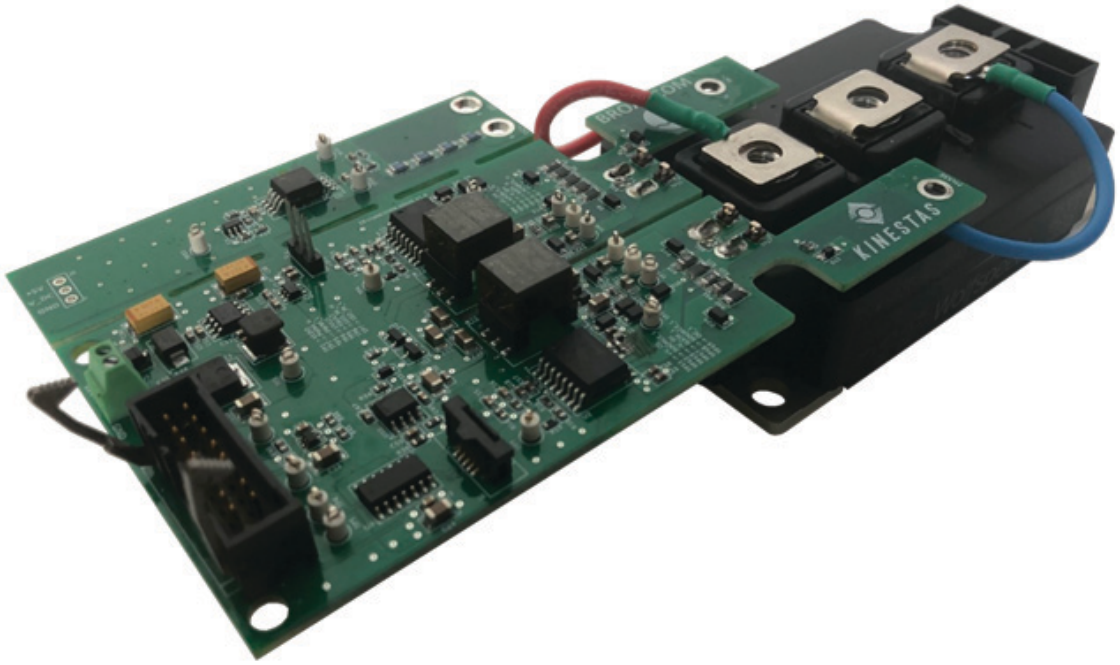
ACPL-355JC

62-mm SiC Module EB1200M62-355JC Evaluation Board

Reference Manual
Version 1.0



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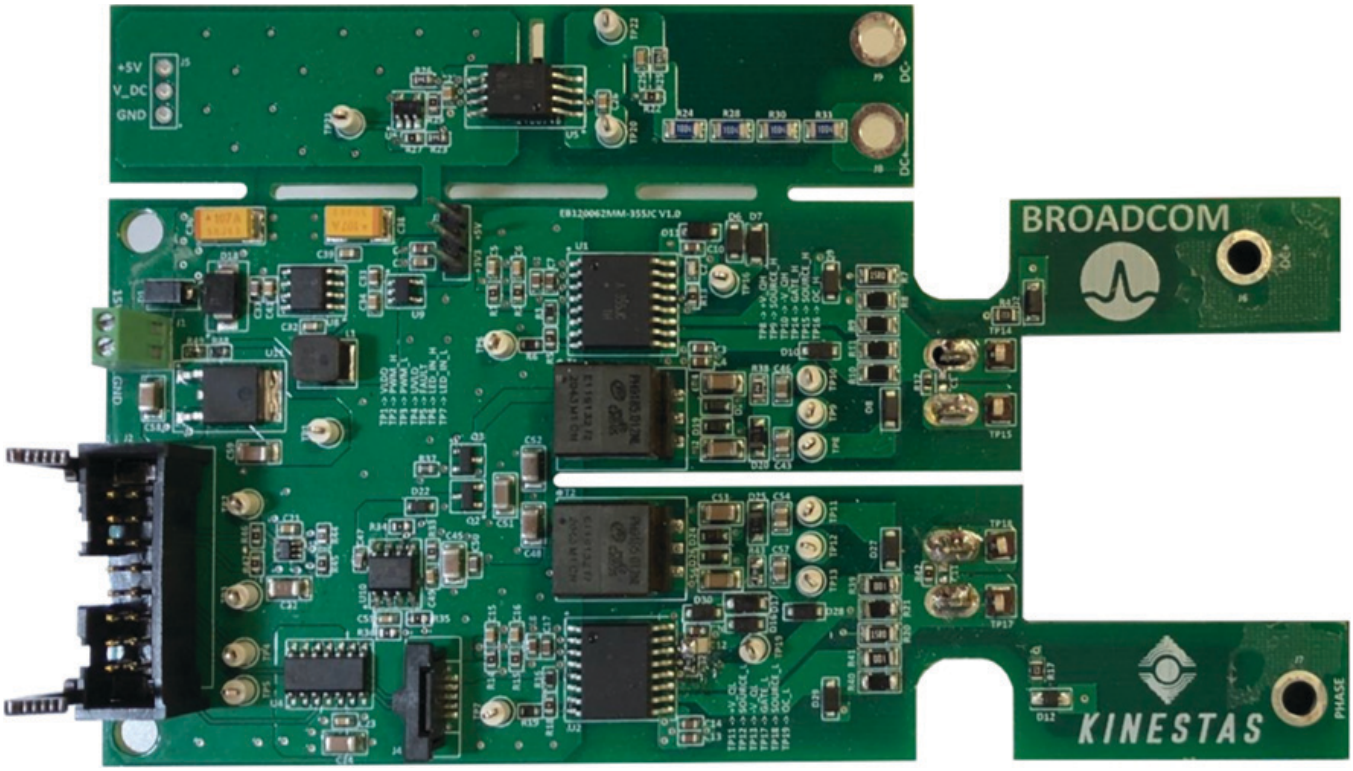
Chapter 1: Introduction

The evaluation board EB1200M62-355JC features Broadcom's dual-output isolated gate drive optocouplers ACPL-355JC, which are used to drive the SiC MOSFET module in an industry-standard 62-mm package. It also features precision optically isolated amplifiers ACPL-C87B, which are used for DC bus voltage measurement, and a user interface/buffering circuit for accommodating external output current measurement signals coming from the optically isolated sigma-delta modulator ACPL-736J. EB1200M62-355JC, shown in Figure 1, has been developed to support Broadcom customers during their first steps in designing power converter applications with ACPL-355JC drivers. Properties of the board are described in the following chapters of this document.

Components were selected considering lead-free reflow soldering. The design was tested and verified with basic measurements described in this document, but the evaluation board is not qualified for the operation in the whole operating temperature range or lifetime. The board was subjected to functional testing only.

Figure 1: Evaluation Gate Driver Board EB1200M62-355JC



EB1200M62-355JC was originally designed to be used with the SiC MOSFET half-bridge module FF6MR12KM1 and WAB300M12BM3, in a 62-mm package. With adequate adjustments for over-current (OC) protection and gate resistors, the EB1200M62-355JC can support modules from different manufacturers in the same packaging, rated up to 1200V and having the same pin assignment.

1.1 Design Features

The EB1200M62-355JC includes the following main features:

- Two isolated ACPL-355JC gate drive optocouplers with the following features:
  - 10A peak output current
  - 100-kV/µs common mode rejection
  - V_{IORM} = 2262V_{PK} with CTI > 600V
  - Over-current protection (or DESAT)
  - Soft shutdown during fault
  - Two isolated feedback signals, FAULT (for over-current) and UVLO
- A single ACPL-C87B optically isolated amplifier for DC bus voltage measurement:
  - 0 to 2V nominal input range
  - 100-kHz bandwidth
  - 3 to 5.5V wide supply range for the output side
  - 15-kV/µs common-mode transient immunity
- Electrically and mechanically suitable for 62-mm module FF6MR12KM1 and WAB300M12BM3.
- With adjustment of the OC protection and gate resistors, the evaluation board supports the following 62-mm SiC MOSFET modules:
  - FF6MR12KM1
  - FF3MR12KM1
  - FF2MR12KM1
  - WAB300M12BM3
  - WAB400M12BM3
- DC/DC power supply with current-limit protection and thermal shutdown.
- Isolated SMPS for gate drivers.
- Access to FAULT and UVLO output signals for protection and control development purposes.
- Access to PWM input signals.
- Access to current measurements via the ACPL-736J sigma-delta current sensing module:
  - ±50-mV linear range (±80-mV full scale)
  - 10- to 20-MHz external clock input range
  - 1-bit, second-order sigma-delta modulator
  - 16-bit resolution, no missing codes
  - 80-dB typical SNR, 78-dB typical SNDR
  - Sensing range of up to 1000A current together with a 0.05-mΩ shunt

1.2 Target Applications

Broadcom ACPL-355JC gate drive optocouplers target the following applications:

- Motor drive for industrial automation and robotics
- Power supply and battery charger
- Renewable energy inverter and storage

1.3 Warnings

The board operates at high voltages. Special care must be taken to avoid injury or endanger life. While operating the board, the user must take into consideration following safety precautions:

- If the board is powered up, do not touch the board, especially exposed metal parts.
- Pay attention to the maximum ratings.
- Use of a protection cover made of insulating materials is mandatory.
- If the board is used with a power module to drive continuous load, the power module must be mounted on a heatsink. The board may rise to high temperatures, and any contact with the human body must be avoided.
- The board itself does not provide dead-time generation. The recommended minimal dead time is 500 ns.

Chapter 2: System Description

This chapter gives essential electrical and mechanical specifications for the EB1200M62-355JC evaluation board.

2.1 Key Specifications

Table 1 lists the absolute maximum ratings of the EB1200M62-355JC evaluation board. Note that this table contains only key parameters. Constraints from the ACPL-355JC, ACPL-C87B, and ACPL-736J data sheets, as well as specification of other key components, must be considered when the EB1200M62-355JC is used.

Table 1: Absolute Maximum Ratings

Parameter	Values			Unit	Note
	Min.	Typ.	Max.		
DC bus supply voltage	—	600	800	V	Limited by the DC bus capacitor voltage rating.
MOSFET half-bridge output current (RMS)	—	270	382	A	Limited by the module thermal.
V_{cc} input voltage	14	15	16	V	External DC input power supply for digital circuitry. Limited by the SMPS range for gate drivers.
PWM logic input level	0	3.3	5	V	External PWM inputs for gate drivers.
Fault logic output level	0	—	5	V	Logic output signal; refer to the ACPL-355JC data sheet.
UVLO output logic level	0	—	5	V	Logic output signal; refer to the ACPL-355JC data sheet.
CLK and DATA output logic level	0	—	5	V	Clock and data logic output signals for current measurement; refer to the ACPL-736J data sheet.
Voltage measurement	0	—	5	V	Single-ended analog output signal.

2.2 Functional Block Diagram

Figure 2 and Figure 3 show the functional block diagram and the disposition of the functional blocks of the EB1200M62-355JC gate driver evaluation board. The block diagram shows several different functional blocks:

- Power management:
  - +15V/+5V DC/DC regulator
  - +15V/+10 (adjustable +10 to +12)
  - +5V/+5V isolated DC/DC regulator
  - +5V to +3.3V LDO
- +10V/(+14V, –4V) isolated SMPS with two outputs (one for the high-side driver and one for the low-side driver)
- High-side and low-side ACPL-355JC gate drivers with circuitry
- Voltage measurements with ACPL-C87B
- DC bus supply terminals
- User interface connector
- 5V V_{cc} power supply connector
- ACPL-736J current sensing module interface connector
- Power terminals

Figure 2: Functional Block Diagram of EB1200M62-355JC

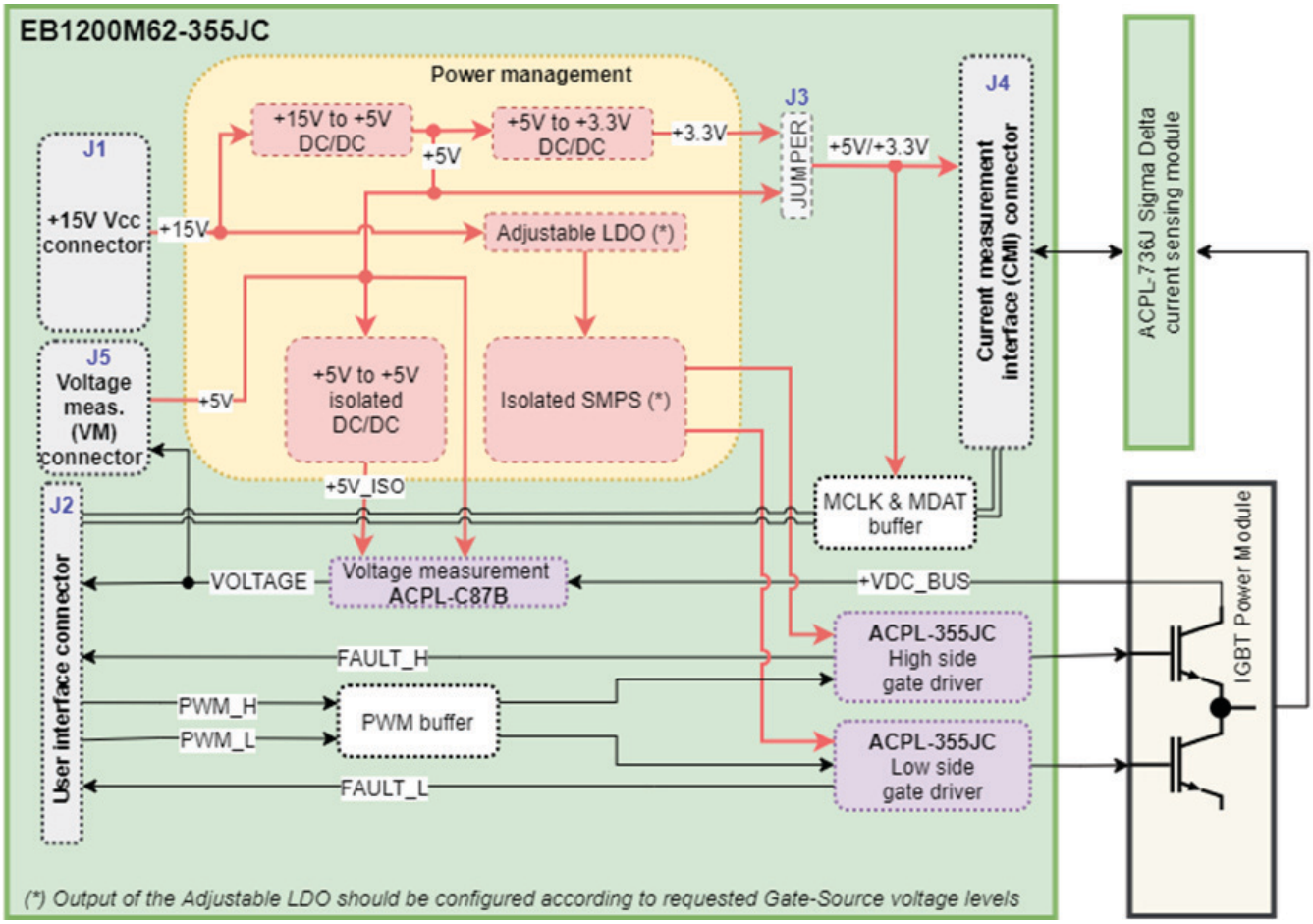
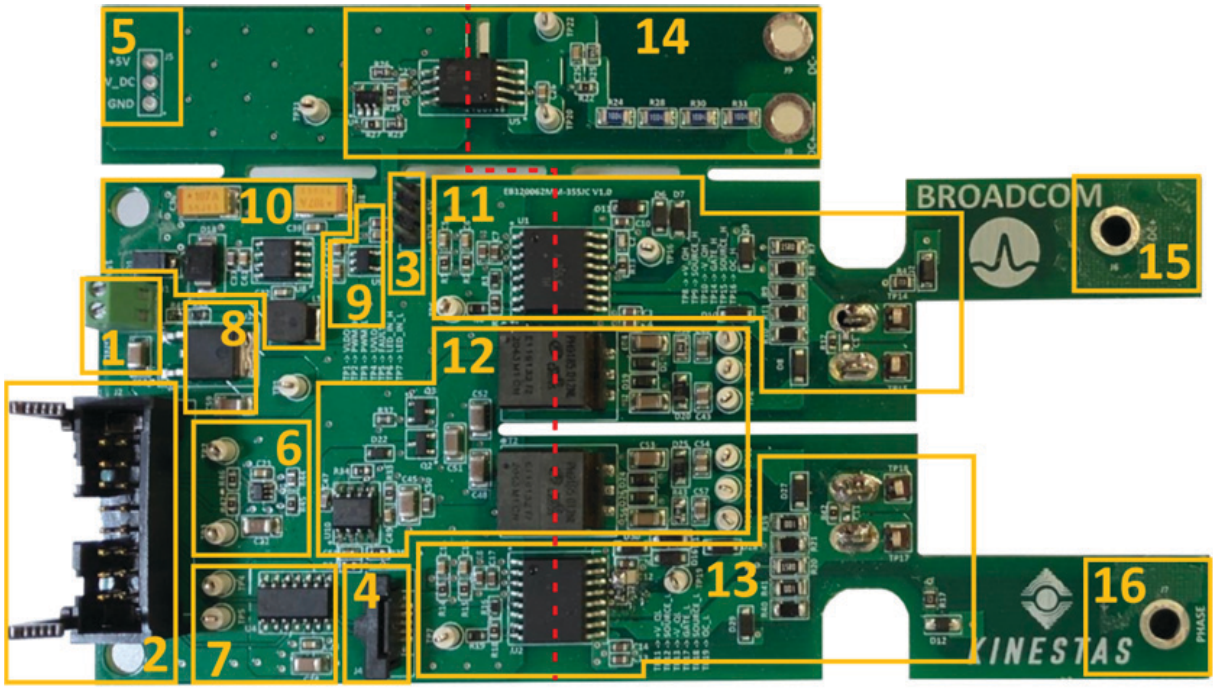


Figure 3: Disposition of the EB1200M62-355JC Functional Blocks. The Isolation Border Is Marked in Red.



According to Figure 3, the marked functional blocks are as follows:

1. J1 – Auxiliary connector input 15V
2. J2 – Signal connector
3. J3 – Voltage level selector 3.3V/5V for current measurement interface
4. J4 – Current measurement interface
5. J5 – Voltage measurement stand-alone supply
6. PWM buffering
7. MCLK and MDATA buffering for ACPL-736J current sensing module
8. Adjustable LDO
9. Switched power supply 5V/3V3
10. Switched power supply 15V/5V
11. High-side SiC driver based on ACPL-355J
12. Isolated SMPS for gate drivers
13. Low-side SiC driver based on ACPL-355J
14. DC bus voltage measurement based on ACPL-C87B. J8/J9 – Terminal to positive/negative DC bus rail for voltage measurement
15. J6 – Terminal to high-side switch drain connection for OC detection
16. J7 – Terminal to low-side switch drain connection for OC detection

2.3 Pin Assignment

Pin assignment for all connectors on the EB1200M62-355JC is listed in the following sections.

2.3.1 Power Interface

The J1 power supply connector is used to supply all ICs and supply gate driver voltage, and Table 2 shows its pin assignment. There are four screw terminals (J6, J7, J8, J9). Terminals J6 and J7 are used for connecting the drain terminals of the half bridge switches to the OC pin of the gate driver, and terminals J8 and J9 are used for connecting to the high-voltage DC rails (DC+, DC-) for voltage measurement. Table 3 lists the functions for each of these connectors.

Table 2: Pin Assignment of Connector J1 (Power Supply Connector)

Pin	Label	Function
1	+V_SUPPLY	Power supply for low-voltage side.
2	GND	Ground.

Table 3: Power Connectors J4, J5, J6, and J7

Designator	Label	Function
J6	DC+	Terminal to the high-side switch drain connection for OC detection.
J7	PHASE	Terminal to the low-side switch drain connection for OC detection.
J8	DC+	Terminal to the positive DC bus rail for voltage measurement.
J9	DC-	Terminal to the negative DC bus rail for voltage measurement.

2.3.2 Signal Interface

Table 4 to Table 7 list the pin assignments of connectors J2, J3, J4, and J5.

Table 4: Pin Assignment of Connector J2 (User Interface Connector)

Pin	Label	Function	Direction
1	VOLTAGE	Single-ended DC bus voltage measurement signal.	Output
2	GND	Ground.	Bidirectional
3	GND	Ground.	Bidirectional
4	MDAT	Data signal for sigma-delta current measurement.	Output
5	GND	Ground.	Bidirectional
6	MCLK	Clock signal for sigma-delta current measurement.	Output
7	GND	Ground.	Bidirectional
8	GND	Ground.	Bidirectional
9	FAULT	Fault signal for over-current protection of both drivers.	Output
10	UVLO	UVLO fault signal for both drivers.	Output
11	GND	Ground.	Bidirectional
12	PWM_L	PWM signal for low-side driver.	Input
13	PWM_H	PWM signal for high-side driver.	Input
14	GND	Ground.	Bidirectional

Table 5: Pin Assignment of Jumper J3 (Power Supply Selection Jumper for Current Measurement)

Pin	Label	Function	Direction
1	+5V	Jumper position 1; +5V interface with current measurement.	Output
2	+5V/+3V3	Jumper common point for current measurement power supply.	Bidirectional
3	+3V3	Jumper position 2; +3.3V interface with current measurement.	Output

Table 6: Pin Assignment of Connector J4 (Interface to the ACPL-736J Current Sensing Module)

Pin	Label	Function	Direction
1	+5V	+5V power supply fed directly to current measurement.	Output
2	+5V/+3V3	Either +5V or +3.3V chosen by setting the jumper on J4.	Output
3	MCLK_CSB	Clock signal for current measurement.	Input
4	MDAT_CSB	Data signal for current measurement.	Input
5	GND	Ground.	Bidirectional

Table 7: Pin Assignment of Jumper J5 (External Supply and Output of the Voltage Measurement Circuit)

Pin	Label	Function	Direction
1	GND	Ground.	Bidirectional
2	VOLTAGE	Single-ended DC bus voltage measurement signal.	Output
3	+5V	+5V external power supply.	Bidirectional

2.4 Mechanical Data

Table 8 lists the basic mechanical data of the evaluation board.

Table 8: Mechanical Characteristics of the EB1200M62-355JC Evaluation Board

Description	Value
Number of layers	4
PCB copper thickness	70 µm to all layers
PCB insulating material	FR4
Board length	134.5 mm
Board width	82.6 mm
Board height	29.4 mm
PCB thickness	1.6 mm

Chapter 3: Circuit Description

This chapter provides in-depth insight into the EB1200M62-355JC gate driver evaluation board features.

3.1 Power Management

Figure 4 shows the auxiliary power management block diagram of the EB1200M62-355JC. By default, the evaluation board is supplied from an external +15V source.

Figure 4: Power Management Block Diagram

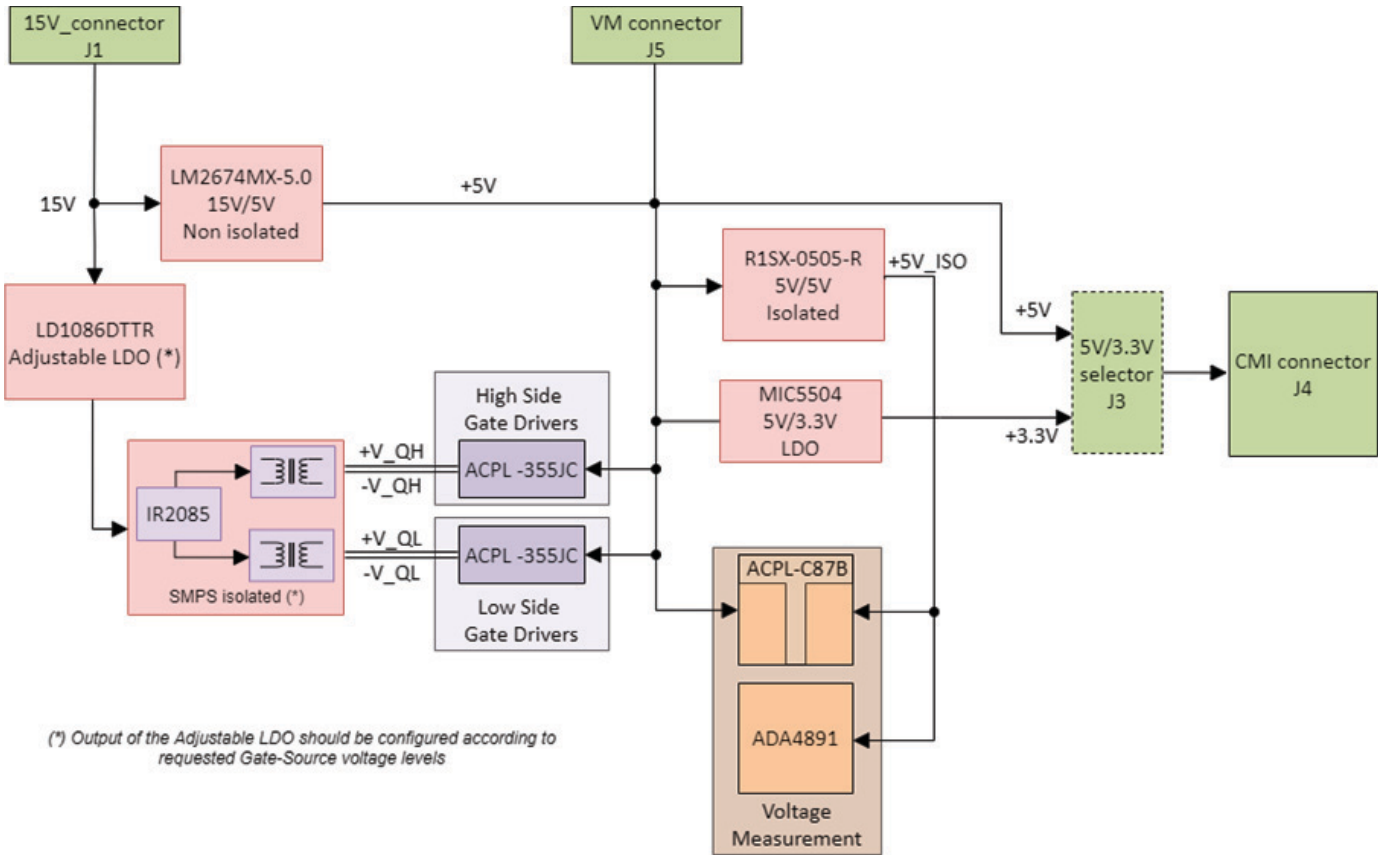
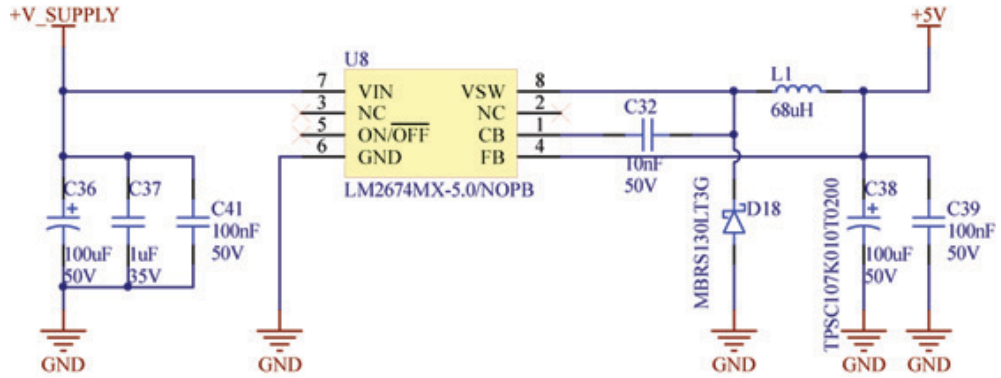


Figure 5: +15V/+5V DC/DC Switching Regulator Circuit



EB1200M62-355JC is equipped with a nonisolated switch mode power supply (SMPS), which provides 5V for the ICs on the low-voltage side. The +15V/+5V power supply is realized with an LM2674 DC-DC switching regulator, as shown in Figure 5. The +5V output is used to supply the low-voltage side of ACPL-355JC gate drivers and the isolated SMPS controller IC. The +5V power supply is capable of driving a 500-mA load and supplying all ICs on the board.

The power for the high-voltage side of the gate drivers is realized with the isolated SMPS, which provides two dual outputs of +14V and –4V.

Since SiC MOSFETs from various manufacturers have different recommended gate voltage levels, the power supply for the gate driver high-voltage side is designed to be configurable. There are two adjustments that must be done before the board can be used on a MOSFET with a different part number.

- The first parameter to be configured is the input voltage of the isolated SMPS. This is achieved by adjusting the feedback resistor R49 of the adjustable LDO voltage regulator, shown in Figure 6. The output of the adjustable LDO LD1086 is calculated as follows:

$$V_o = 1.25V \cdot \left(1 + \frac{R_{49}}{120}\right)$$

  The minimum value for V_o is limited by the isolated SMPS to 10V. Do not adjust V_o below 10V to avoid unexpected board behavior.
- The second parameter is the Zener diodes D20 and D25 placed in the output stage of the SMPS, which define the positive gate driver voltage, shown in Figure 7. A diode with a Zener voltage equal to the positive gate voltage level recommended by the power module manufacturer should be used.

The presented adjustable circuitry enables in-depth evaluation of switching characteristics or benchmarking of SiC modules in a 62-mm package from different semiconductor manufactures.

Figure 6: Adjustable LDO +15V/(+10V ... 12V)

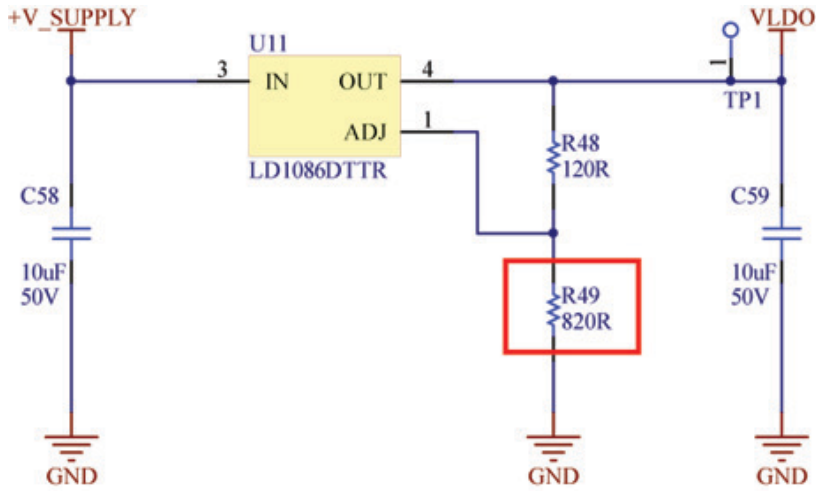


Figure 7: Output Stage of the Isolated SMPS

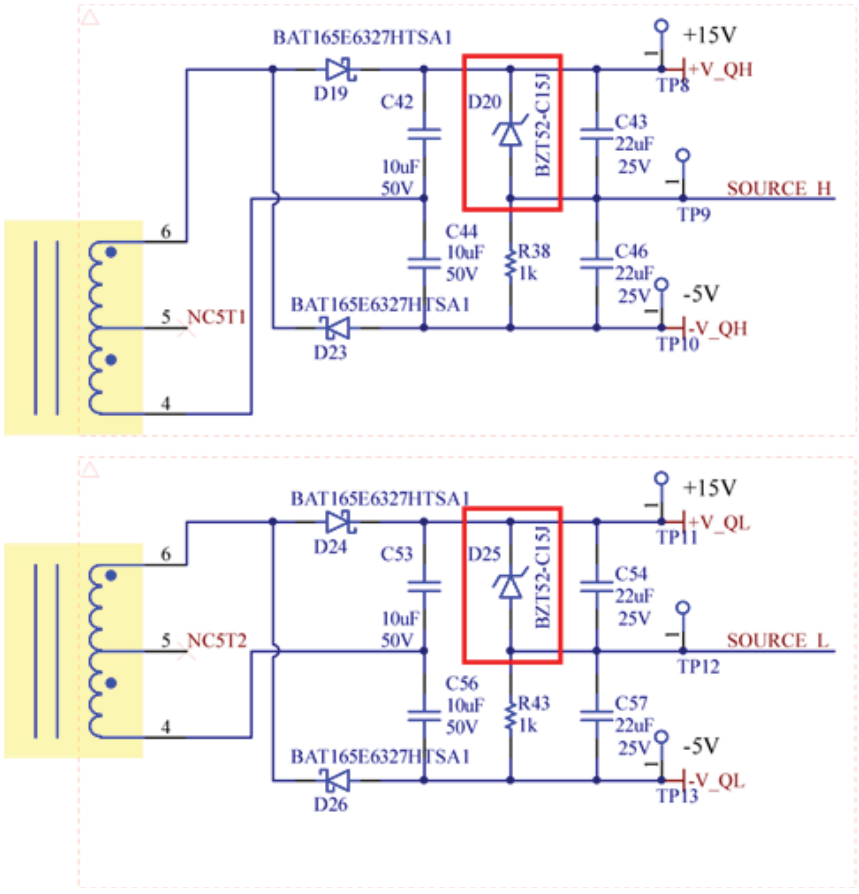


Figure 8: Isolated SMPS for the Gate Driver Output Stage

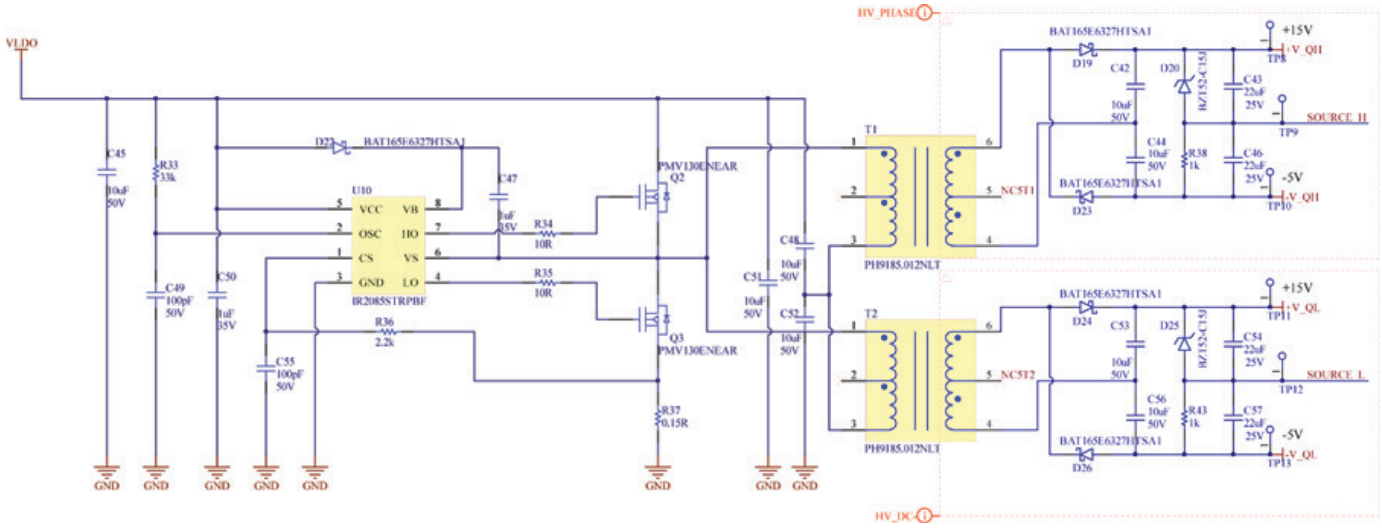


Figure 8 shows the isolated SMPS circuitry. The SMPS is based on the IR2085 self-oscillating half-bridge gate driver and two transformers with a 1:2 ratio. Table 9 shows the recommended power supply configurations for the WAB300M12BM3 and FF6MR12KM1 MOSFET modules. Based on the values shown in table, it is recommended to use the resistor and Zener diode values that were used in the circuit with the FF6MR12KM1 and WAB300M12BM3 modules, due to small voltage drops related to switching.

Table 9: Power Supply Configurations

Device	+V_Q	–V_Q	R49	D20 and D25
WAB300M12BM3	+14V	–4V	820R	16V Zener diode
FF6MR12KM1	+15V	–5V	953R	16V Zener diode

An isolated 5V/5V voltage regulator R1SX-0505-R provides isolated 5V for ACPL-C87B IC, as shown in Figure 9.

The EB1200M62-355JC can be connected to a current sensing module through the FPC 5-pin J4 connector. The J4 connector is provided for the external output current measurement board, which is based on Broadcom's isolated sigma-delta modulator ACPL-736J, but different current measurement boards with an equivalent pinout can be used. Because the low-voltage side of the ACPL-736J supports a power supply of either 5V or 3.3V, the EB1200M62-355JC enables voltage level selection via jumper J3. For this purpose, the EB1200M62-355JC features the high-performance LDO 5V/3.3V, shown in Figure 10, which enables alternative powering of the ACPL-736J current sensing module with 3.3V.

Figure 9: +5V to +5V_ISO Unregulated Isolated DC/DC Converter

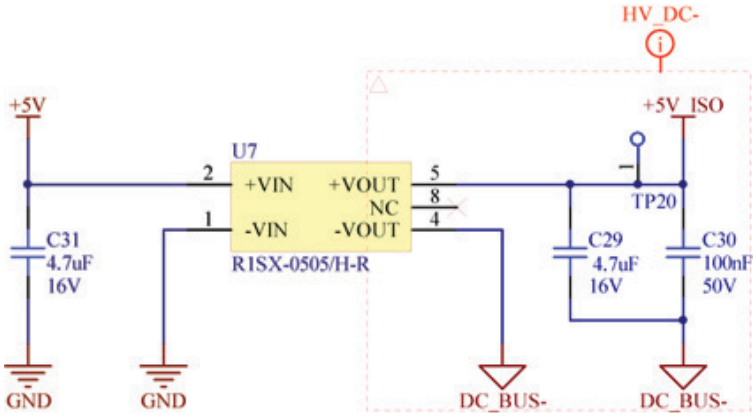
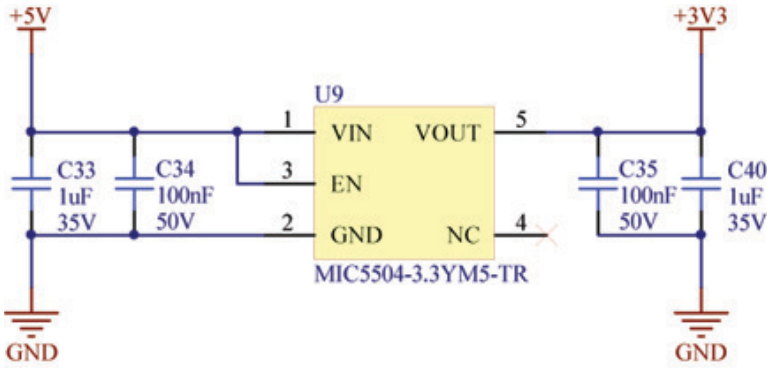


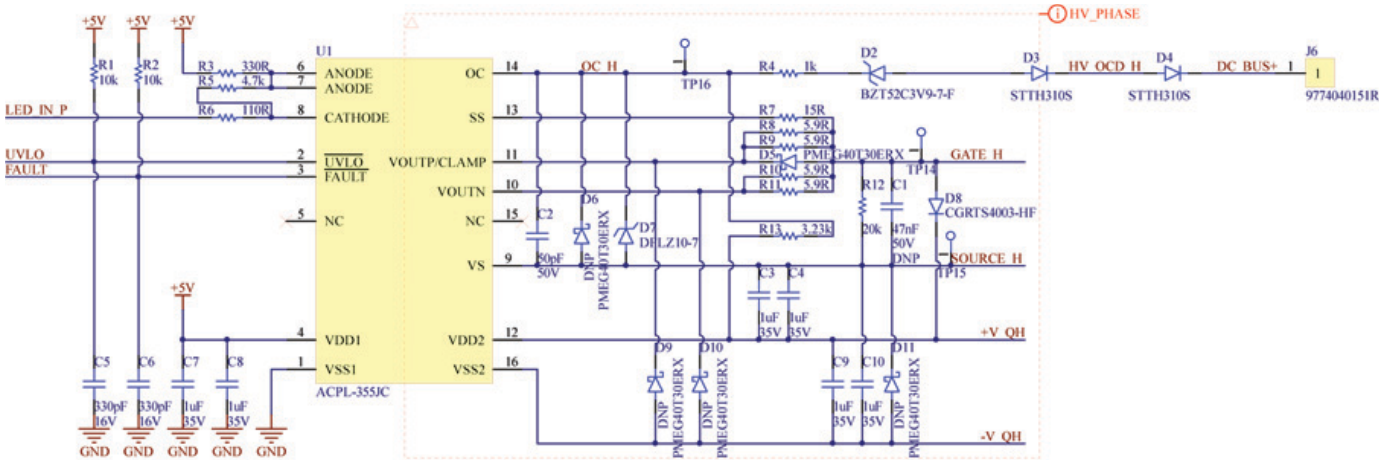
Figure 10: +5V/+3V3 LDO



3.2 Gate Driver Circuit

This section deals with the gate driver circuitry on the EB1200M62-355JC. A description of related features and functionalities is presented in the following subsections. Figure 11 shows the gate drive circuitry.

Figure 11: ACPL-355JC Gate Driver Circuitry



With a maximum peak output current of 10A, the ACPL-355JC can drive most of the power IGBT/MOSFET switches directly without an external push-pull stage. This driver contains an LED that is electrically isolated and optically coupled to an integrated circuit on the gate driver high-voltage side with two power output stages and a CLAMP function for preventing the parasitic turn-on due to the parasitic Miller current during turn-off transient. Other features encompass under-voltage lockout (UVLO) and over-current (OC) protection as well as a soft shutdown during an OC fault.

Table 10 provides the recommended gate turn-on/turn-off resistor values for the WAB300M12BM3 and FF6MR12KM1 MOSFET modules.

Table 10: Recommended Values for Gate Turn-On/Turn-Off Resistors

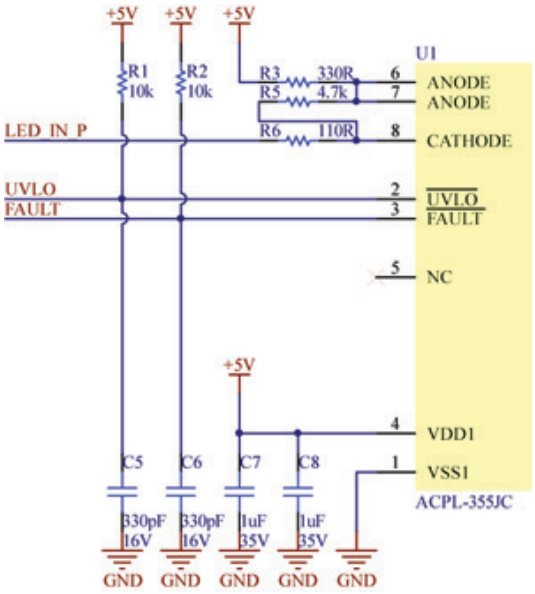
Device	R_{g_on}	R_{g_off}
WAB300M12BM3	2.95Ω (2x parallel 5.9Ω)	2.95Ω (2x parallel 5.9Ω)
FF6MR12KM1	4.03Ω (2x parallel 8.06Ω)	4.03Ω (2x parallel 8.06Ω)

3.2.1 Gate Driver Circuit: Low-Voltage Side

Figure 12 shows the low-voltage side of the gate drive circuitry, which contains the power supply for ACPL-355JC, the LED anode and cathode, and safety reporting signals (FAULT and UVLO).

The resistor responsible for the LED forward current setting is split in two, and those resistors are placed on anode pins 6 and 7 and cathode pin 8 to balance the common mode impedances at the LED's anode and cathode. This helps to equalize the common mode voltage change. Resistor values are selected because it was recommended in the device data sheet.

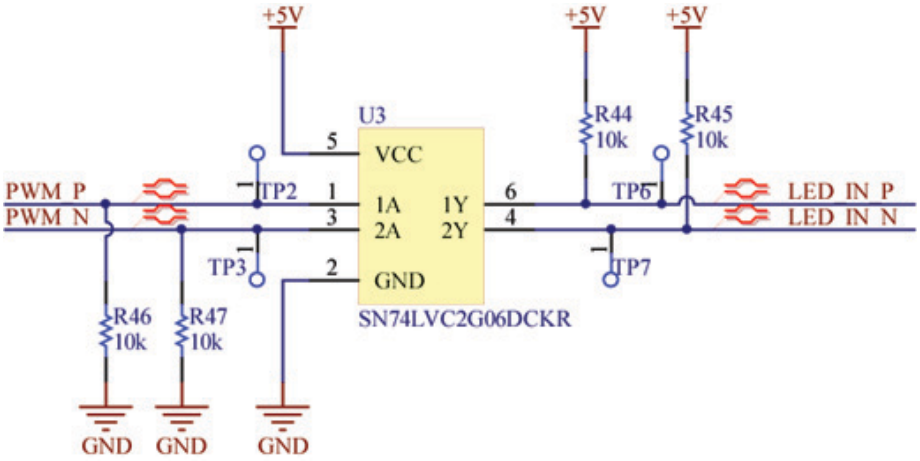
Figure 12: Gate Driver Circuit – Low-Voltage Side



While the input LED is directly polarized, and there is no fault, the turn-on command will be transferred to the high-voltage side and the ACPL-355JC V_{OUTP} pin will go high. The ANODE pin is pulled high via resistor R3. The input signal LED_IN_P is connected to the CATHODE pin. When the input LED_IN_P signal is low, the LED is directly polarized and the MOSFET is turned on. If the input signal LED_IN_P is high, the voltage across the LED and the two resistors is low; therefore the LED is not conducting and the MOSFET is in off state.

External PWM signals that propagate through the user interface connector are buffered, as shown in Figure 13. Because the buffer features an open drain output, inputs of the buffer are pulled down while outputs of the buffer are pulled high, to ensure that the MOSFET module is off in case the input PWM signals are in high impedance states.

Figure 13: PWM Buffer

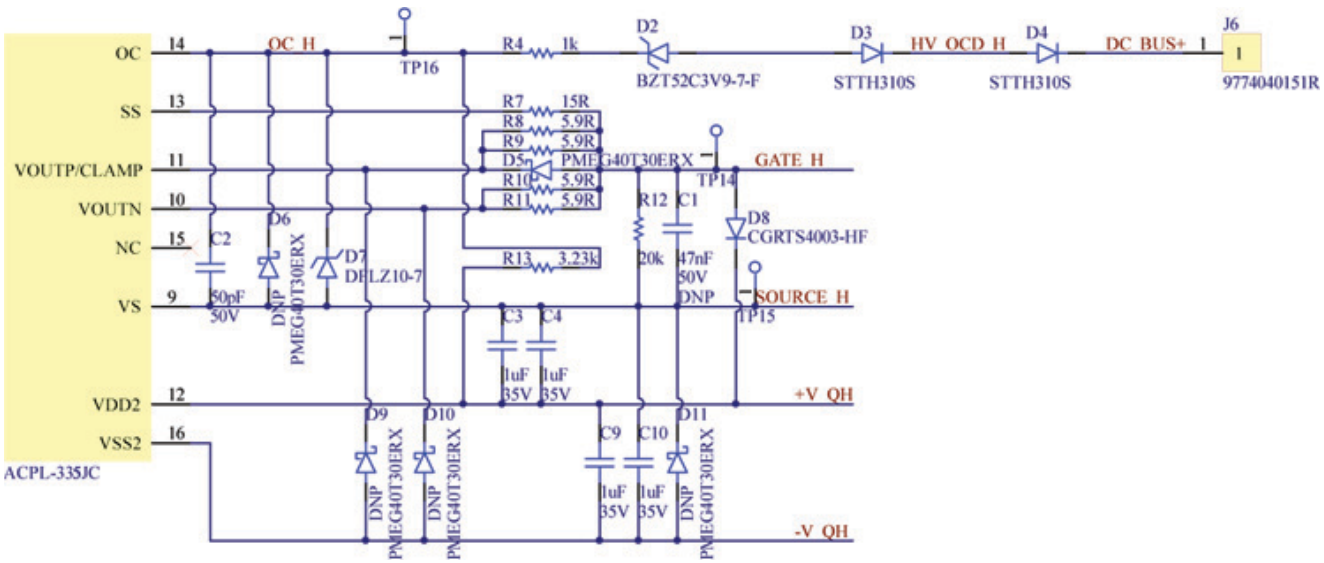


UVLO and FAULT signals are open drain, so they are pulled up with 10-kΩ resistors and have 330-pF filtering capacitors. The logic for these signals is inverted, so they are suitable for wired 'OR' applications. In this case, FAULT signals from both drivers are connected in parallel, and the same is done with UVLO signals, so the user is notified if a FAULT or UVLO has occurred regardless of which MOSFET it has occurred on. UVLO has the highest fault priority followed by FAULT.

3.2.2 Gate Driver Circuit: High-Voltage Side

The secondary side of the gate drive circuitry, shown in Figure 14, includes circuits related to OC and UVLO protection and a soft shutdown in case of fault.

Figure 14: Gate Driver Circuit – High-Voltage Side



Based on FF6MR12KM1, when the gate driver input is set to high, V_{OUTP} becomes high and +15.5V is supplied to the MOSFET gate via two 8.06Ω (default value) parallel resistors. When the gate driver input is set to low, the V_{OUTN} pin becomes active and –5V is supplied to the MOSFET gate via two 8.06Ω (default value) parallel resistors; and when V_{OUTN} is low, –5V is connected to the MOSFET gate. These voltages are referred to the source of the respective MOSFET. The switching time is determined by the gate charging and discharging process. Smaller gate resistors lead to higher peak gate current, which subsequently decreases turn-on and turn-off time, reducing switching losses. However, gate resistors that are too small may introduce voltage spikes and current oscillations on the MOSFET or can overload the gate driver IC. For the proper selection of the gate resistors, several criteria must be fulfilled.

First is the limit of the gate peak current. MOSFET internal R_{Gint} must be considered when calculating the ideal value for the gate resistor and the internal minimum turn-on resistance of driver R_{VOUTP}. The equation for the gate resistor calculation is given in the ACPL-355JC data sheet.

$$R_G \geq \frac{V_{DD2} - V_{SS2}}{I_{O(PEAK)}} - R_{Gint} - R_{VOUTP}$$

The next step in choosing the right gate resistor is checking the power dissipation of the ACPL-355JC gate driver. If the power dissipation is too high, the resistance of the gate resistor should be increased. For detailed instructions on choosing the gate resistor, refer to the ACPL-355JC data sheet.

Finally, switching performance, especially the turn-off speed, must be measured since the fast-switching transients in combination with parasitic inductances in the switching loop can generate high over-voltages and oscillations.

To ensure the constraints described above during the worst-case conditions, based on FF6MR12KM1, the EB1200M62-355JC comes with 4.03Ω gate resistors for positive and 4.03Ω for negative gating. Both resistances are realized with two parallel resistors to increase the power dissipation capacity of the gate circuit. In addition, the evaluation board is designed to enable Broadcom customers to evaluate switching characteristics of the semiconductors by changing or combining the turn-on/off resistors.

Additionally, Schottky diode D5, placed between the gate and the V_{OUTP} pin, is used together with the CLAMP function to shunt parasitic Miller current during the off cycle.

3.2.3 Protection Features

V_{OUTP} and V_{OUTN} will remain functional until OC or UVLO protection features are activated.

3.2.3.1 OC

The OC pin monitors the MOSFET drain-source voltage. OC fault detection circuitry must remain disabled for a short period of time following the turn-on of the MOSFET to allow the drain-source voltage to settle down and fall below the OC threshold. This period, called the OC blanking time, is determined by the blanking capacitor and the internal current source provided in the gate driver IC. The total blanking time is calculated in terms of the internal blanking time ($t_{OC(BLANKING)}$), the external capacitance (C_{BLANK}), the FAULT threshold voltage (V_{OC}), and the blanking capacitor charge current (I_{CHG}) as follows:

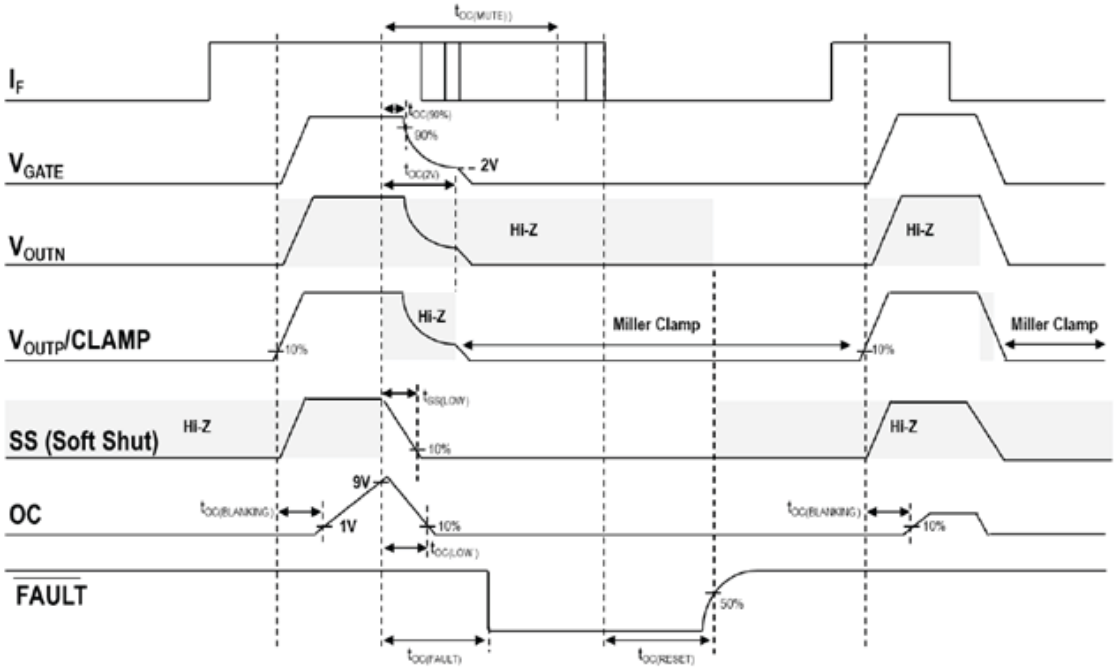
$$t_{BLANK} = t_{OC(BLANKING)} + \frac{C_{BLANK} \cdot V_{OC}}{I_{CHG}}$$

C_{BLANK} corresponds to capacitance C2 (C12 for the low-side driver) in Figure 14, the V_{OC} fault threshold voltage is nominally 9V, and the I_{CHG} OC charge current is 1 mA. The nominal blanking time also represents the longest time it takes for the driver to respond to the OC fault condition. Once the OC fault is detected and the blanking time has passed, both V_{OUTP} and V_{OUTN} will go low and a soft shutdown will start. The soft shutdown resistor R7 (R20) should be small enough to speed up the shutdown of the MOSFET to prevent overheating.

When the OC conditions are met, an internal feedback channel is activated, which brings the FAULT output from high to low. Once the fault is detected, V_{OUTP} and V_{OUTN} are set to the High-Z state for the $t_{OC(MUTE)}$ time. After this time, the LED input must be kept low for $t_{OC(RESET)}$ before the fault condition is cleared. The FAULT status will return to high, and the SS output will return to the High-Z state. If the LED goes high during $t_{OC(RESET)}$, the $t_{OC(RESET)}$ timing will reset, and the LED input will need to be kept low for another $t_{OC(RESET)}$. Figure 15 depicts the circuit behavior during the over-current event.

The total voltage measured at the OC pin is the sum of the drain-source voltage across the MOSFET switch and the total voltage drop on following components: R4 (R17), D3 (D13), D4 (D14), D2 (D12). The drain-source voltage threshold value for OC triggering is equal to 9V – (I_{CHG} x R4) – V_{D3} – V_{D4} – V_{D2}, where V_{D3} and V_{D4} are the forward voltage drops of diodes D3 and D4, and V_{D2} is the blocking voltage of Zener diode D2. The function of the high-voltage diodes D3 (D13) and D4 (D14) is to conduct the current from the OC pin through the MOSFET when it is in the on state, allowing for drain-source voltage sensing, and to block high voltages when the MOSFET is in the off state. Proper adjustment of the OC detection level can be performed by choosing the correct voltage rating of Zener diode D2.

Figure 15: Driver Behaviors during an Over-Current Event



In the current design, the threshold voltage is set to 2.5V. This means that the OC protection will react after the MOSFET drain current reaches approximately 600A for the selected MOSFET at an ambient temperature of 25°C.

The freewheeling of the antiparallel diodes connected across the MOSFET can have large instantaneous forward voltage transients. This may result in a large negative voltage spike on the OC pin, which will draw substantial current from the driver if protection is not used. Limiting this current is done via a 1-kΩ resistor placed in series with the OC diodes.

Negative voltage spikes typically generated by inductive loads or reverse recovery spikes of the IGBT/MOSFET freewheeling diodes can bring the OC pin voltage above the threshold, thus generating a false fault signal. To prevent this, Zener and Schottky diodes are placed across the OC and V_S pins. The Zener diode protects the OC pin from positive high transient voltage, and the Schottky diode prevents forward biasing of the substrate diode of the gate driver optocoupler. Table 11 provides the recommended Zener diode voltage values for the WAB300M12BM3 and FF6MR12KM1 MOSFET modules.

Table 11: Recommended Values for Zener Diode Cutoff Voltage

Device	D2, D12
WAB300M12BM3	3.9V
FF6MR12KM1	1.8V

Because MOSFETs are more sensitive to over-current than IGBT, the OC protection must be faster. That can be done by tweaking the OC blanking time; thus one additional resistor R13 (R32) is added between the OC pin and V_{DD2}. This allows an additional blanking capacitor charging current component from the secondary driver power supply, so that blanking time can be shorter and can be adjusted via resistor R13 (R32).

3.2.3.2 UVLO

Insufficient gate voltage on the MOSFET during the turn-on phase can increase the voltage drop across the MOSFET. This results in a large power loss and MOSFET damage due to high heat dissipation. ACPL-355JC constantly monitors the output power supply. If the power supply voltage is lower than the UVLO threshold, the driver output will turn off to protect the MOSFET from low-voltage bias. UVLO protection precedes OC protection.

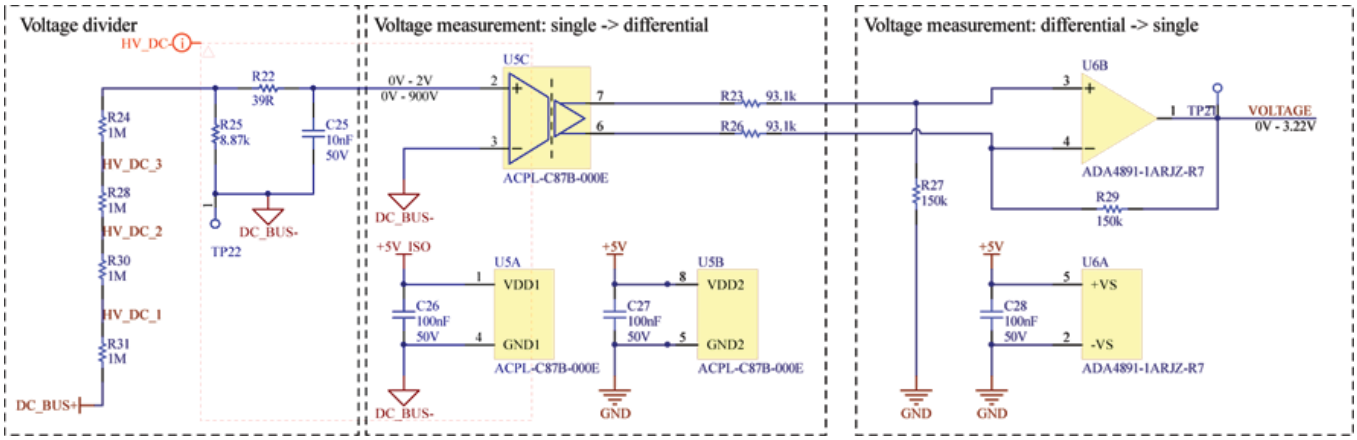
3.3 Measurements

The EB1200M62-355JC features DC bus voltage measurement and an interface for the output (phase) current measurement realized with the external shunt and isolated sigma-delta converter. The external shunt and PCB with the sigma-delta IC are not part of this evaluation board and can be ordered separately.

3.3.1 Isolated DC Bus Voltage Measurement (Detachable)

The isolated DC bus voltage measurement is realized using the ACPL-C87B optically isolated high-precision voltage sensor. Figure 16 shows the voltage measurement circuitry.

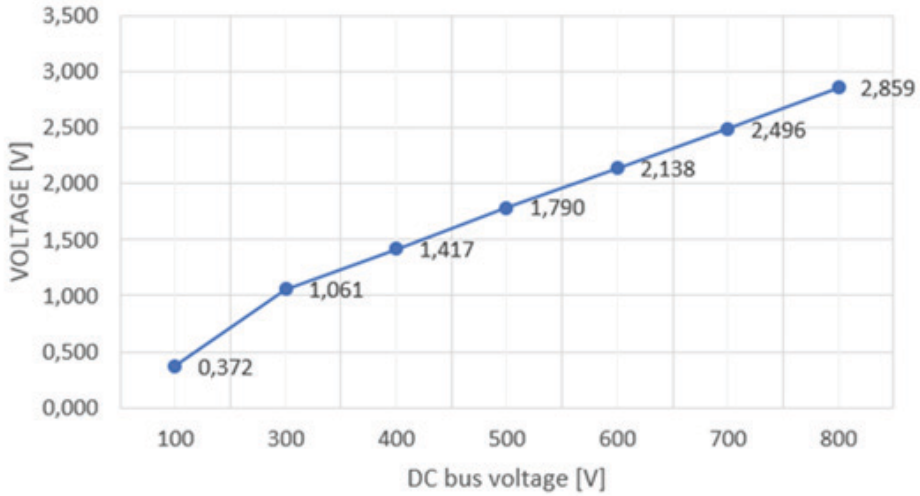
Figure 16: Isolated DC Bus Voltage Measurement



The maximal DC bus voltage that can be measured is 900V. The DC bus voltage is brought to a voltage divider, which scales from 900V to 2V. In this design, four 1-MΩ resistors (R24, R28, R30, R31) and one 8.87-kΩ resistor (R25) are placed in series to form the voltage divider. Note that these resistors must have a low tolerance due to the required precision. Resistor R22 and capacitor C25 are added for anti-aliasing.

The obtained signal is then transformed into a differential signal on the secondary side of the ACPL-C87B. To make the measurement more user friendly, this differential signal is transformed back to a single-ended signal using the ADA4891 high-speed amplifier. On the output of the circuitry, an analog signal, in the range from 0V to 3.2V, is generated as the linear representation of the DC bus voltage ranging from 0V to 900V. Figure 17 shows the typical DC bus voltage response of the measurement circuit.

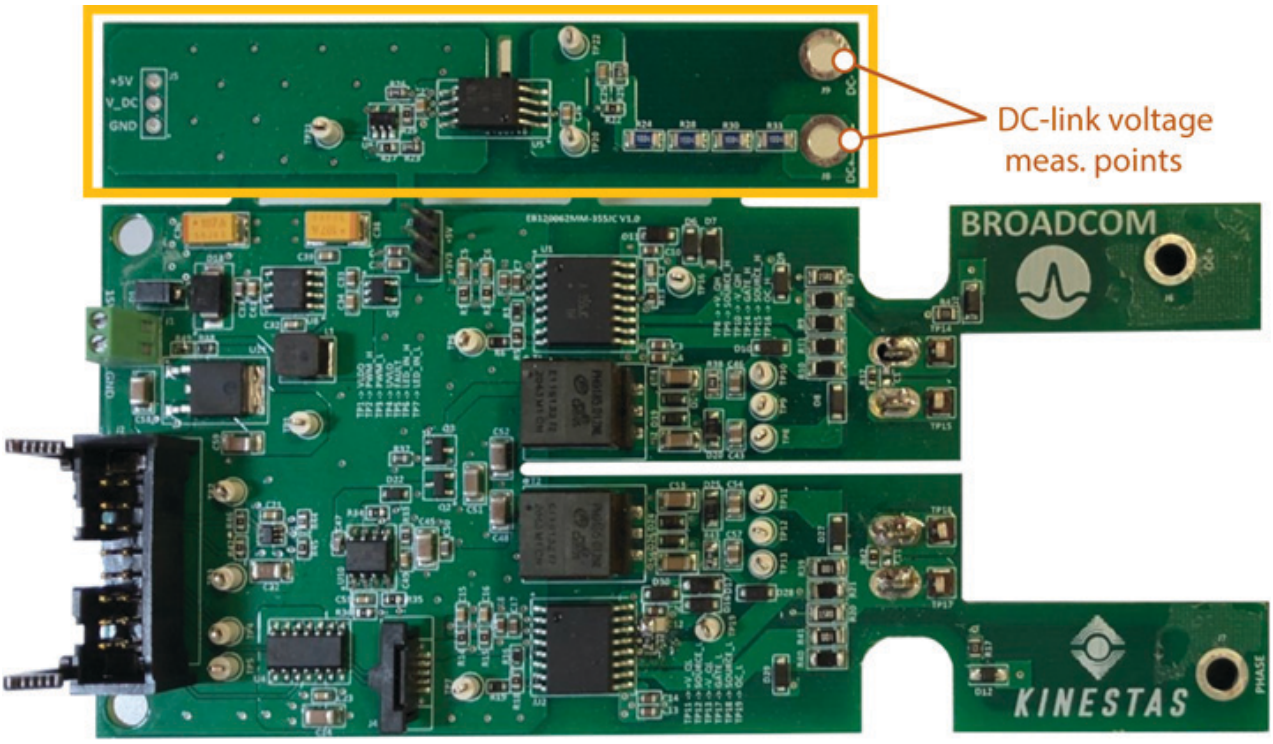
Figure 17: Typical Voltage Measurement Characteristic



If using the proposed single-ended configuration for the end-user application, it is strongly recommended to add a capacitor parallel to resistor R29 (compare with Figure 16) in the final design to attenuate high-frequency spikes. The DC bus voltage measurement circuit is presented in Figure 18 outlined in yellow. The DC bus voltage must be connected to the dedicated pads on the PCB (marked with the amber color in Figure 18).

The DC bus voltage measurement circuit is placed on the detachable part of the PCB and can serve as the stand-alone isolated DC voltage measurement board. If the DC bus voltage board is used as the stand-alone unit, the board must be supplied with the 5V external power supply. The power supply input and measurement signal can be accessed via dedicated pads (J5) on the PCB.

Figure 18: Detachable DC Bus Voltage Measurement Circuit Outlined in Yellow

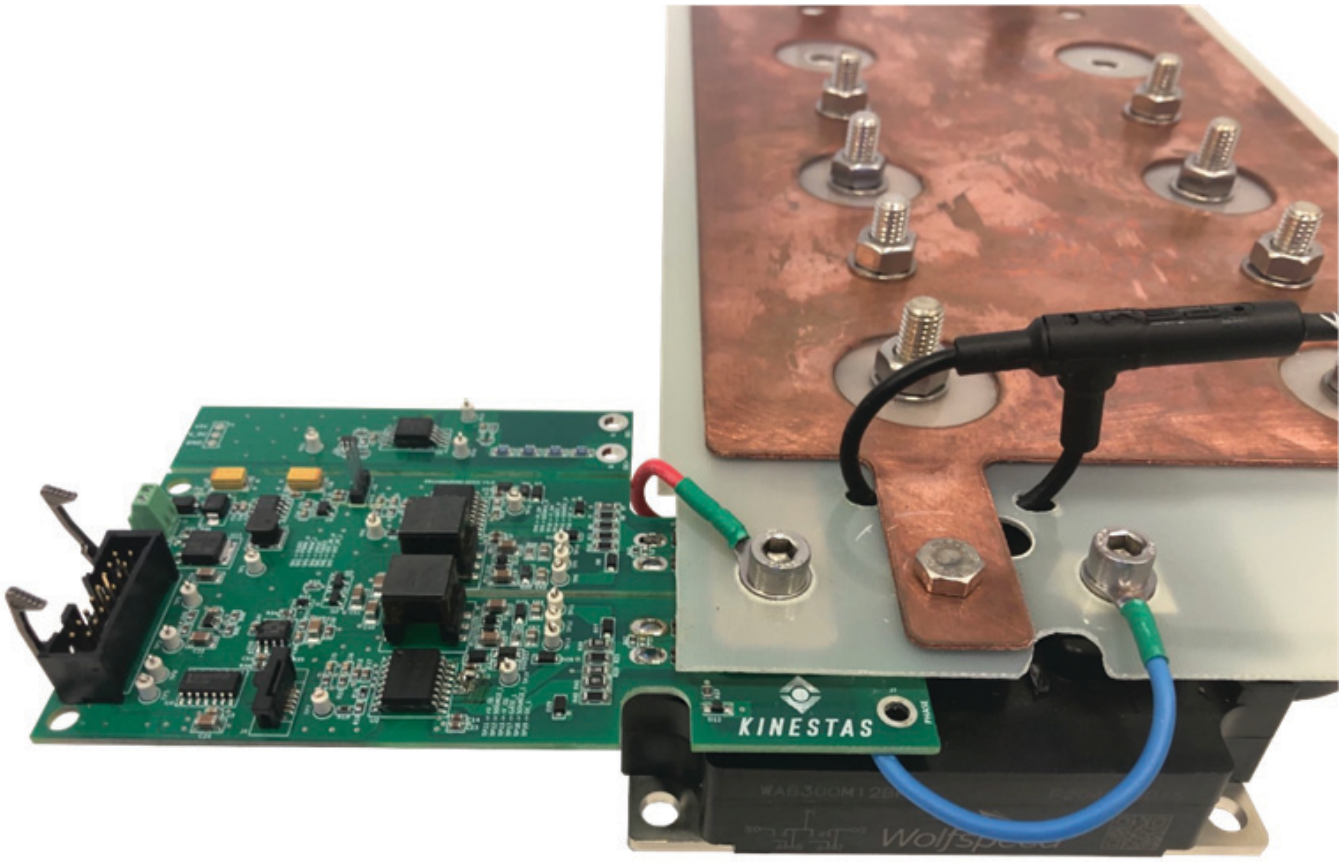


NOTE: Please take care with the polarity of the DC bus voltage connected to the measurement circuit!

3.3.2 Example Test Setup for Switching Current Measurement

For measuring the switching current with a Rogowski coil, provisions can be made when designing the DC-link circuit for testing/application. One such example, used for performing tests presented in this document, is shown in Figure 19.

Figure 19: Test Setup Example for Measuring Module Switching Currents with a Custom Designed DC-Link



3.4 Connectors

EB1200M62-355JC connectors are described in the following sections.

3.4.1 Power Connectors for the High-Voltage Side

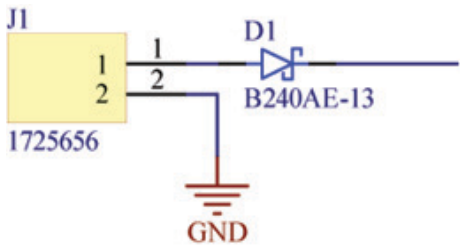
The board is supplied with the high-voltage connectors realized with the M3 screw terminals. The following power connectors are available on the board:

- J6 – DC+ for the high-side switch OC protection.
- J7 – PHASE for the low-side switch OC protection.
- J8 – DC+ for the voltage measurement circuitry.
- J9 – DC- for the voltage measurement circuitry.

3.4.2 V_{CC} +15V Connector

The auxiliary power supply connector +15V is a standard 2-pin PCB terminal block. This connector supports a maximum wire cross-section of 0.5 mm². Figure 20 shows the connector schematic.

Figure 20: +15V Power Supply Connector

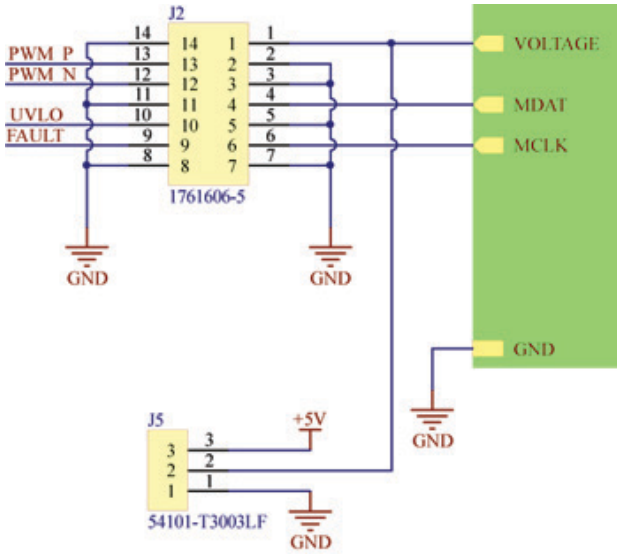


For reversed voltage protection, the Schottky diode is placed in series with the main power supply.

3.4.3 User Interface Connector

The user interface header connector (J2) serves as an interface between the microcontroller or PWM signal source and the EB1200M62-355JC evaluation board. Figure 21 shows the disposition of signals across this connector. In addition to connector J2, an additional user interface header connector (J5) is placed in the part of the board with voltage measurement circuitry. Over this connector, an external +5V supply can be used to supply the voltage measurement board when it is detached from the main board. In addition to supply pins, a VOLTAGE pin is provided to read the scaled and buffered DC link voltage measurement.

Figure 21: User Interface Connector



3.4.4 Current Measurement Interface Connector

The EB1200M62-355JC evaluation board integrates double-buffered MCLK and MDAT input, which serves as the interface to the external current measurement board. The two signals from the ACPL-736J current sensing module are brought to the EB1200M62-355JC using an FPC connector. They are then routed to the buffer and subsequently to the user via user interface connector. Note that these signal routes must have the same length; therefore length matching must be applied in the layout. Figure 22 shows the buffer configuration, and Figure 23 current measurement interface connector.

Besides providing input for the PWM signals, the user interface connector J2 provides output for the fault signals, DC bus voltage, and buffered CLK and DATA signals for current measurement. Figure 22 shows the buffer configuration for the CLK and DATA signals. Note that these signal routes must have the same length; therefore length matching must be applied in the layout design.

Figure 22: CLK and DATA Double-Buffer Configuration

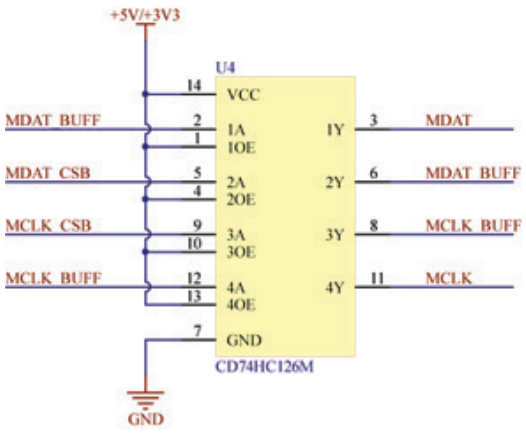
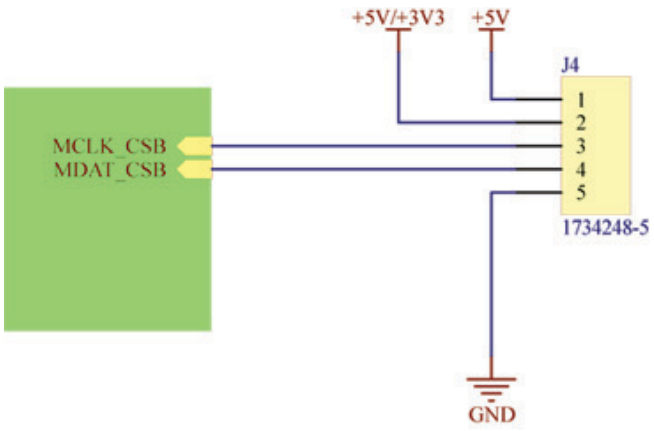
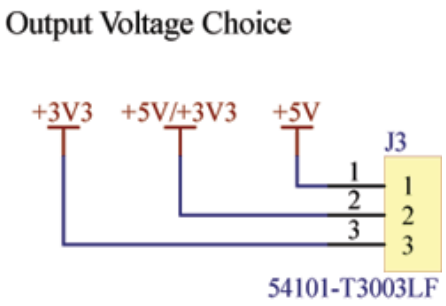


Figure 23: Current Measurement Interface Connector



The EB1200M62-355JC allows the user to select the voltage reference to be used for powering the ACPL-736J (external output current measurement). Available voltage levels are 5V and 3.3V, which can be chosen by correctly adjusting the J3 jumper, which is shown in Figure 24.

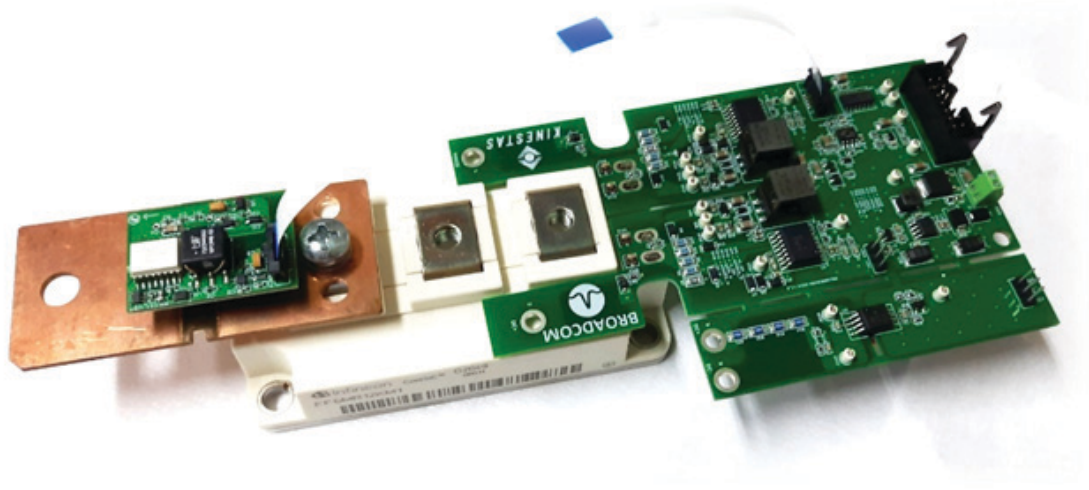
Figure 24: Connector J3



3.4.5 ACPL-736J Sigma-Delta Current Sensing Module

The ACPL-736J sigma-delta current sensing module is a separate board that is not integrated onto the EB1200M62-355JC evaluation board. The current sensing module's H1 connector is connected to the EB1200M62-355JC's J4 connector using a 5-pole FPC cable. The shunt resistor is connected to the current sensing board via S1 and S2 terminals with M3 screws. The current from the 62-mm module OUT terminal is then measured using the 0.05-mΩ shunt resistor (KOA HS-50U-2) as shown in Figure 25. Depending on the module's ratings, the output current will range from 250A to 500A. This will give a sense voltage of 12.5 mV to 25 mV, which is within the ±50-mV linear range of the ACPL-736J.

Figure 25: Current Sensing Module – EB1200M62-355JC and 62-mm Connection



The current sensing module's H1 connector is connected to the EB1200-339J's J1 connector using a 5-pole FPC cable. The EB1200-339J provides 5 VCC and VDD2 to power up the board and the ACPL-736J respectively. The U2 (pSemi PE33100) transformer driver will switch transformer T1 (Wurth 750344162) to provide isolated supply to VDD1 of the ACPL-736J. U3 provides a 20-MHz external CLK to ACPL-736J, and the CLK frequency can be adjusted by changing the value of resistor R4.

Figure 26: Functional Blocks Disposition of the ACPL-736J Current Sensing Module

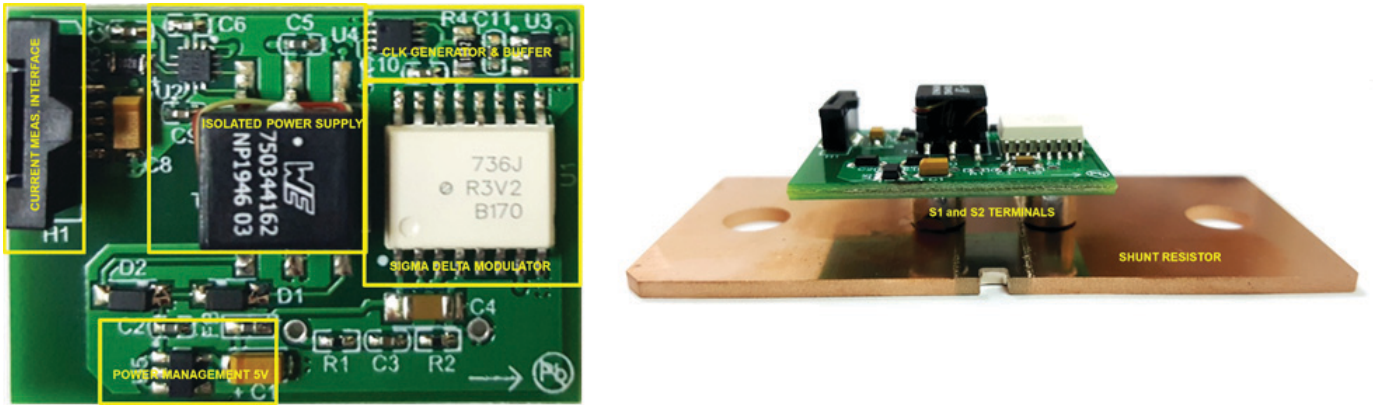
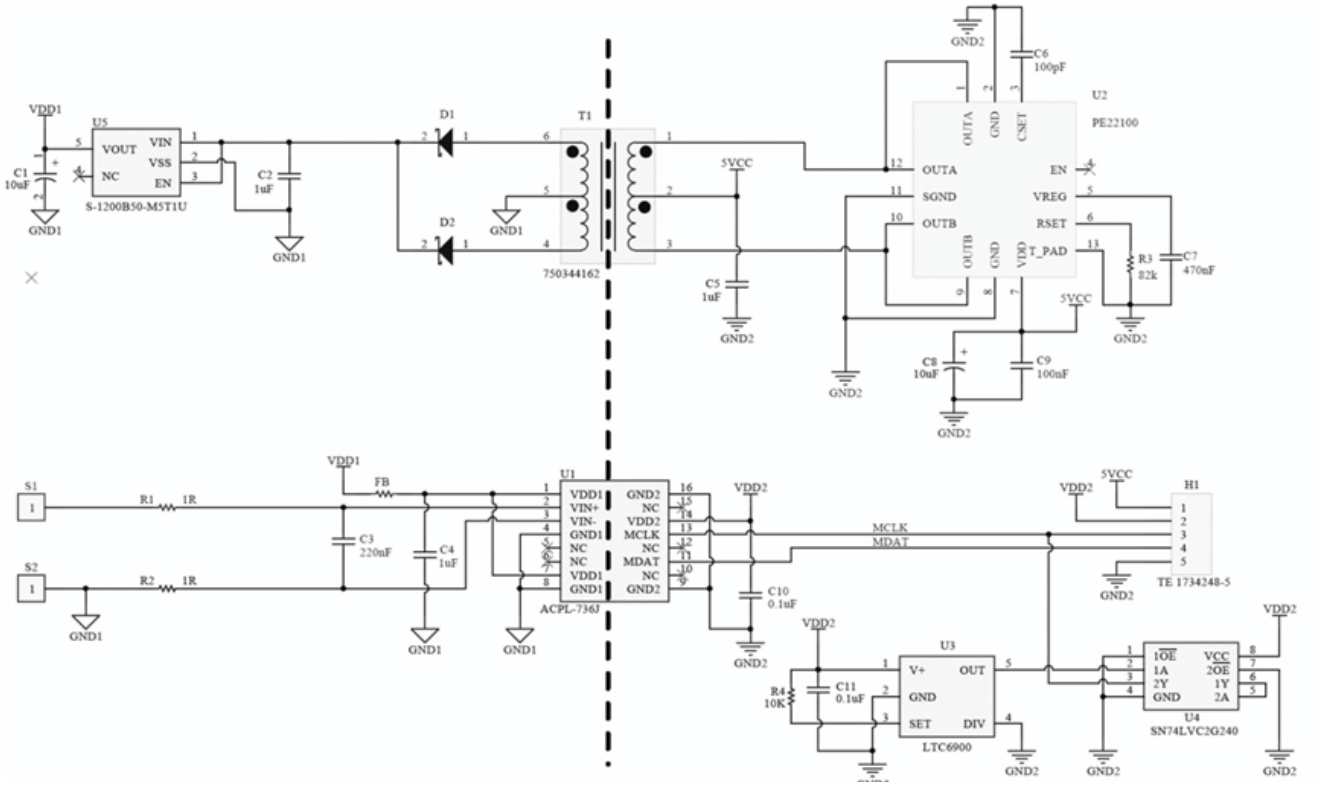


Figure 27: Connector J3 Schematic of the ACPL-736J Current Sensing Module



The ACPL-736J is a 1-bit, second-order sigma-delta modulator that converts an analog input signal into a high-speed data stream with galvanic isolation based on optical coupling technology. The ACPL-736J operates from a 3.3V or 5V power supply with a dynamic range of 80 dB.

The analog input is continuously sampled by means of sigma-delta over-sampling using external clock, coupled across the isolation barrier, which allows synchronous operation with any digital controller. The signal information is contained in the modulator data as a density of ones with a data rate up to 20 MHz, and the data is encoded and transmitted across the isolation boundary, where it is recovered and decoded into a high-speed data stream of digital ones and zeros. The original signal information can be reconstructed with a digital filter.

Combined with superior optical coupling technology, the modulator delivers high noise margins and excellent immunity against isolation-mode transients. With a 0.5-mm minimum distance through insulation (DTI), the ACPL-736J provides reliable double protection and high working insulation voltage, which is suitable for fail-safe designs.

WARNING! The EB1200M62-355JC gate driver evaluation board is designed to work with voltages up to 800V and thus requires that all safety precautions and national accident prevention rules be undertaken. Installation and use of the board should be reserved for skilled technical personnel. There is a danger of serious injury and property damage if the board is not properly used or installed. It is strongly recommended that a system aimed to supply the evaluation board be equipped with control and protection devices, in agreement with applicable safety standards.

ATTENTION: Signals dedicated for the high-side driver and low-side driver must have proper dead time. The board itself does not provide dead time generation. The recommended minimal dead time value is 500 ns.

3.5 Installation of the EB1200M62-355JC

Before starting with the evaluation of the board, consider and observe the following installation steps:

1. Before any installation, make a visual inspection of the board to ensure that it contains all components assembled except the module. See Section A.3, Bill of Materials, for the complete list of components. The EB1200M62-355JC, by default, does not contain an assembled module to avoid damage to the module and the evaluation board during transport, as well as to provide the customer the option to use other modules with the same footprint.
2. If a MOSFET module with a different part number from the default one is to be used, the high and low gate driving voltages should be adjusted according to Section 3.1, Power Management. In addition, turn-on and turn-off resistances of the gate driver circuit should be changed to accommodate the driven device.
3. Assemble the 62-mm module. The module gate/source driving pins must be soldered.
4. Make an electrical connection of +DC_bus and –DC_bus from the SiC module power terminals to the J6 and J7 terminals on the EB1200M62-355JC eval board. The connection can be made with flying wires, or the eval board can be directly attached to a custom-designed DC-link PCB over terminals J6 and J7 by screwing the terminals to the DC-link PCB.
5. Ensure that the over-current protection feature is well adjusted. Depending on the MOSFET module assembled, readjustment of the OC Zener diode D2 (D12 for the low-side MOSFET) should be considered, as well as the additional resistor R13 (R32 for the low-side MOSFET) for adjustment of the blanking time (see Section 3.2.3, Protection Features).
6. With the available jumper, select the desired voltage reference for the current measurement. Available references are 5V and 3.3V.
7. Connect the user interface connector. The PWM signals as well as the ACPL-355JC output fault signals should be connected to the control board with 5V logic.
8. Connect the +15V external power supply. The EB1200M62-355JC requests a +15V external power supply to enable +5V and +3.3V digital operations and +14V and –4V default gate driver high voltage side power supply. Although the polarity is marked, the board is reverse protected at the V_{CC} terminal of the +15V external supply.

3.6 Evaluation of the EB1200M62-355JC

The EB1200M62-355JC enables users to evaluate the following items:

- ACPL-355JC driver features
- ACPL-C87B precision voltage sensor features
- External current measurement based on ACPL-736J sigma-delta modulator features
- Switching characteristics of the SiC power semiconductors in a 62-mm package
- Half-bridge inverter basic features
- Buck-boost basic features

For the evaluation of the power semiconductor switching characteristics, with the EB1200M62-355JC, it is recommended to perform a double-pulse test and measure the switching transients related to the semiconductor and the ACPL-355JC gate driver circuit.

Chapter 4: Typical Switching and Over-Current Protection Characteristics

4.1 Typical Switching Waveforms with WAB300M12BM3

Switching waveforms during hard switching of the semiconductors are measured with an oscilloscope using the standard double-pulse test procedure. The SiC MOSFET module used for testing is the Wolfspeed SiC MOSFET WAB300M12BM3. Figure 28 shows the turn-on switching transient, while Figure 29 depicts the turn-off switching transient at different drain current levels. The switching performance measurements were carried out with the default gate resistor values, 2.95Ω for both On and Off resistors, and a +14V/–4V gate power supply.

Figure 28: Characteristic waveforms during the turn-on switching transients at different load currents. In the upper diagram, voltage waveforms are depicted with solid lines, and current waveforms are depicted with dashed lines.

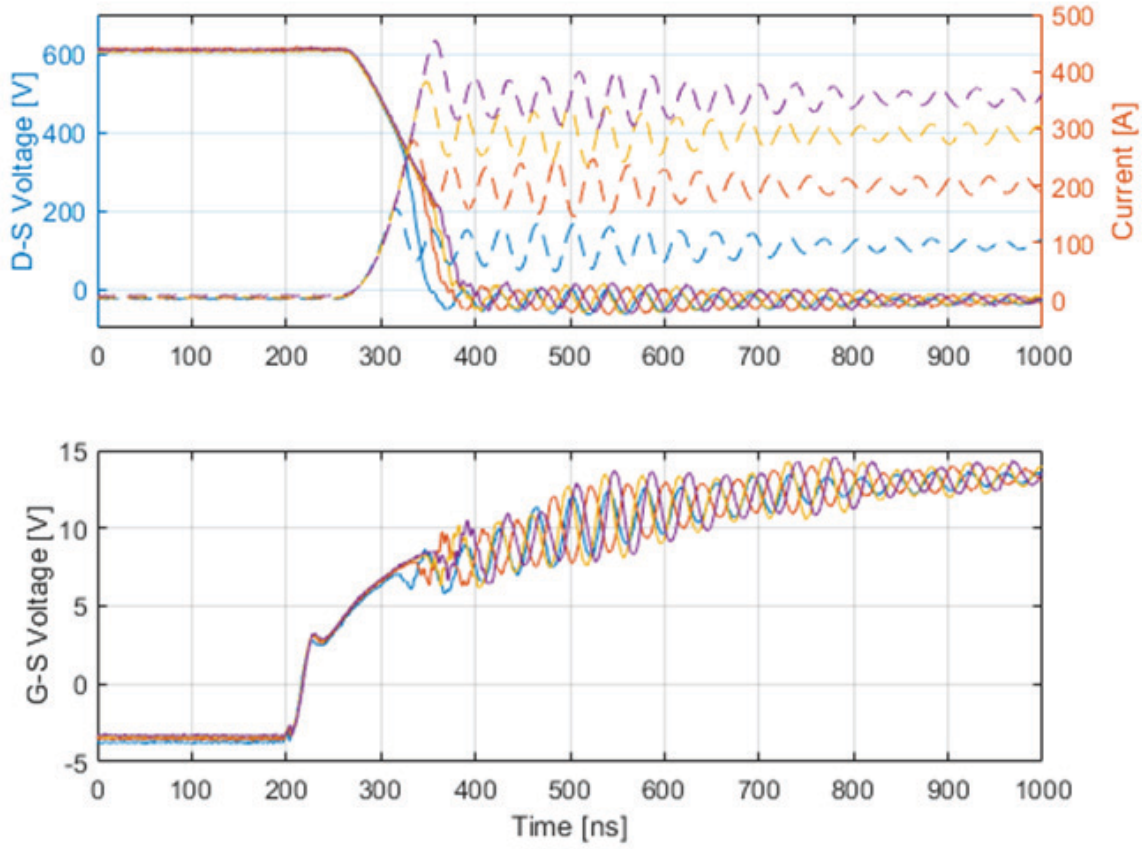
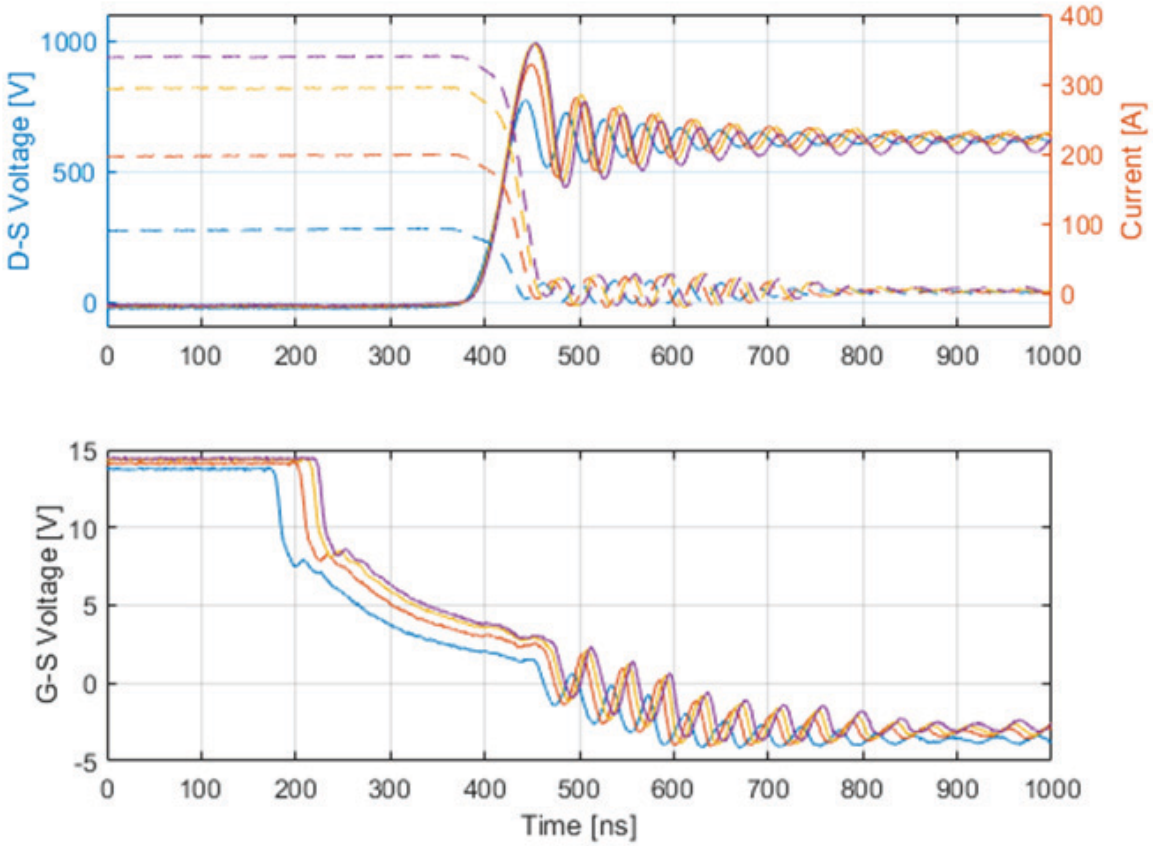


Figure 29: Characteristic waveforms during the turn-off switching transients at different load currents. In the upper diagram, voltage waveforms are depicted with solid lines, and current waveforms are depicted with dashed lines.



4.2 Typical Switching Losses with WAB300M12BM3

In Figure 30 instantaneous power during switching and the resulting turn-on switching energy loss are shown for a DC voltage of 600V, whereas in Figure 31 the same waveforms are shown for turn-off transient.

Figure 30: Turn-on switching energy loss at 600V DC bus. In the upper diagram, voltage waveforms are depicted with solid lines, and current waveforms are depicted with dashed lines.

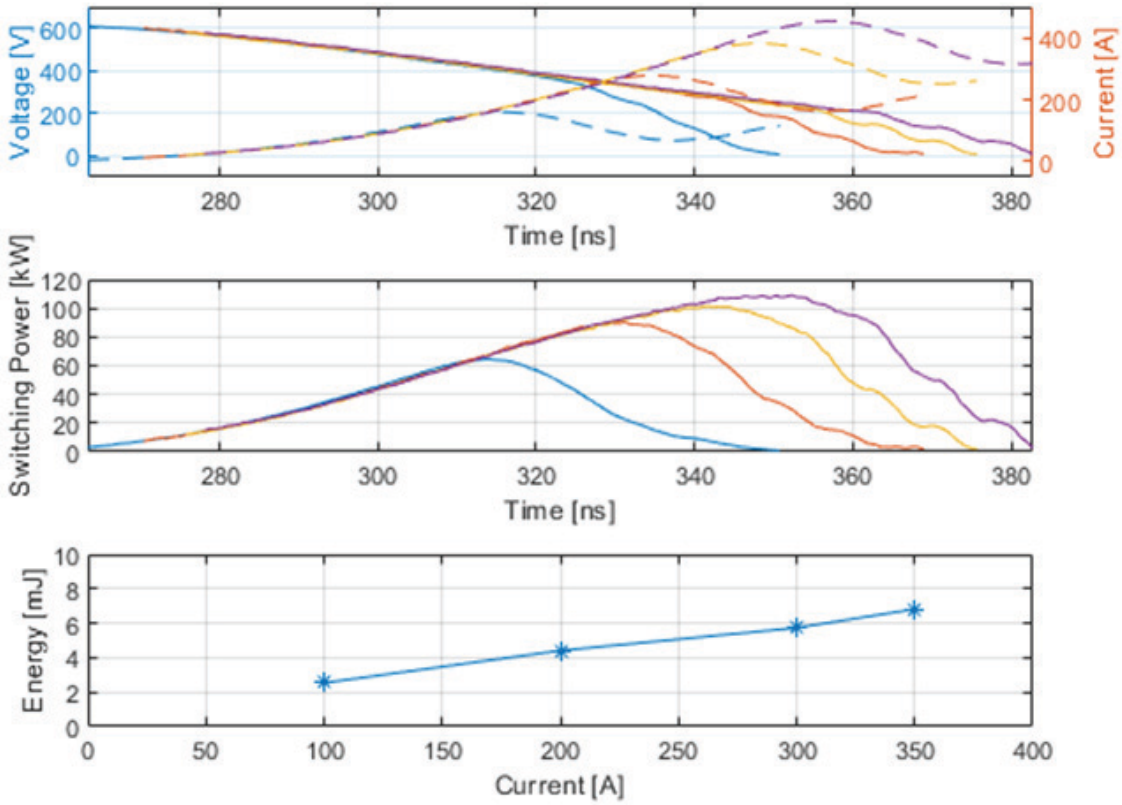
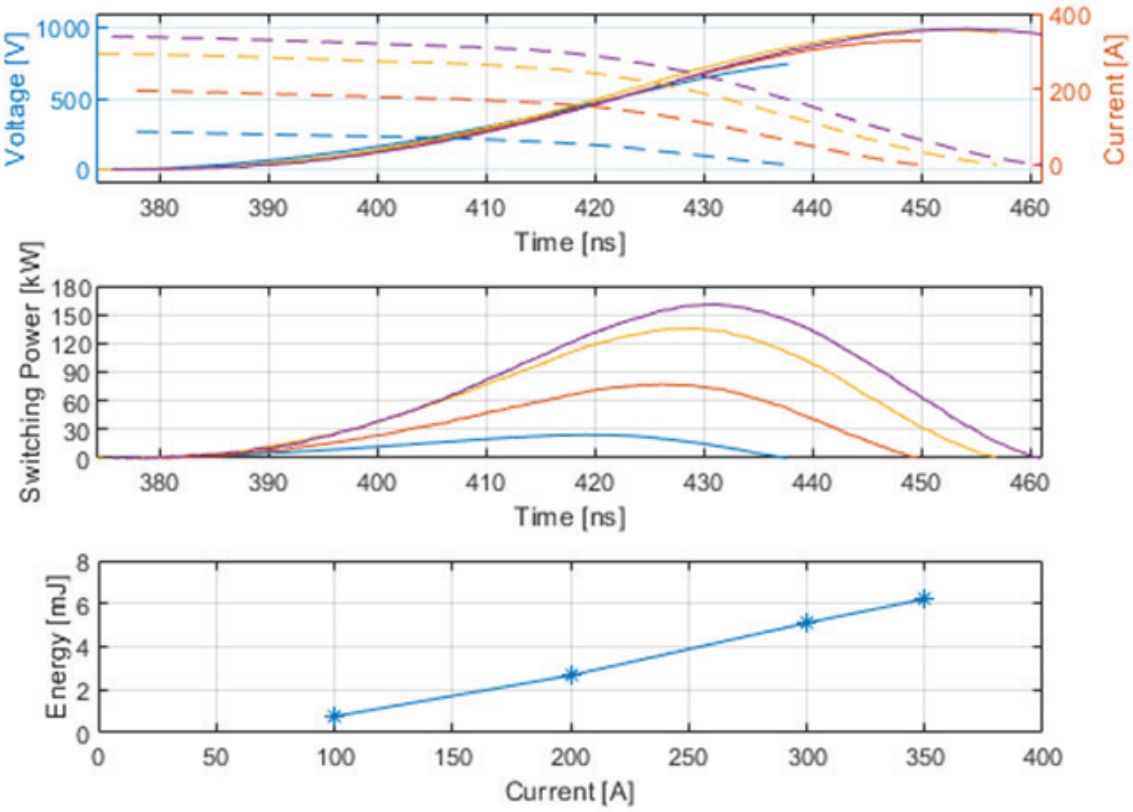


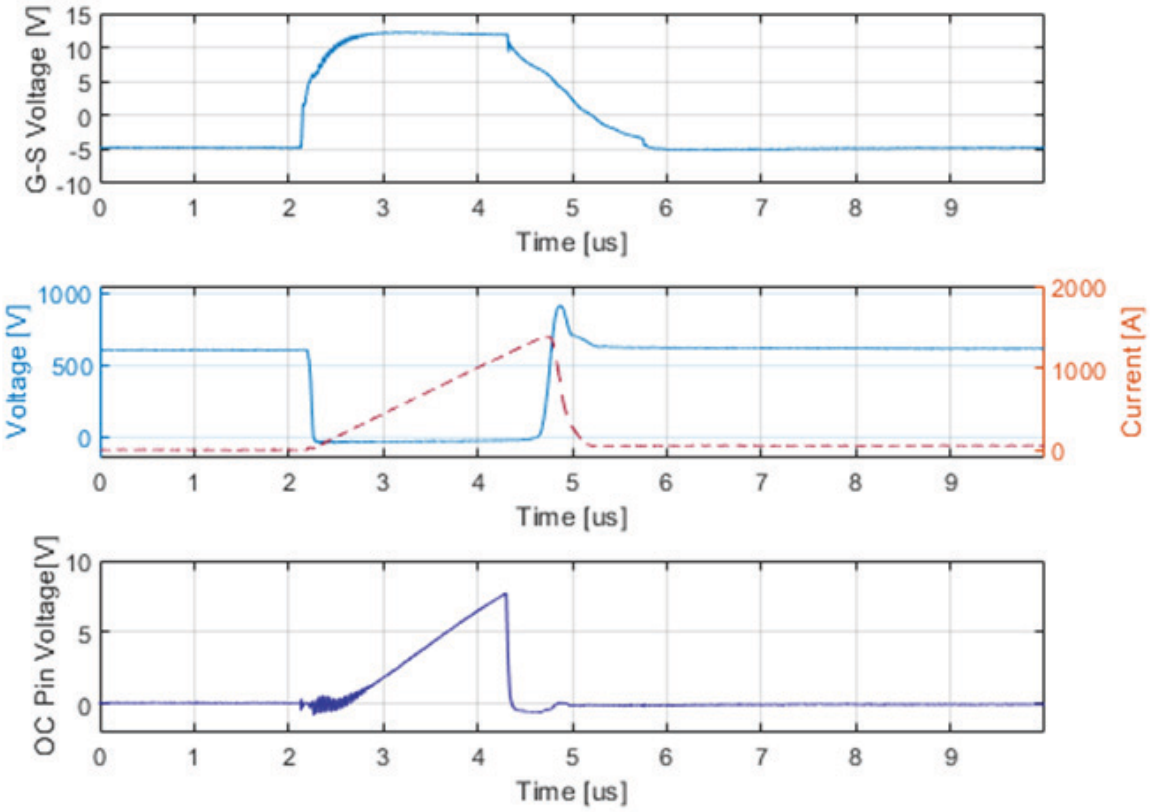
Figure 31: Turn-off switching energy loss at 600V DC bus. In the upper diagram, voltage waveforms are depicted with solid lines, and current waveforms are depicted with dashed lines.



4.3 Typical Over-Current Protection Performance with WAB300M12BM3

The over-current protection function is demonstrated by short-circuiting the output of the power module WAB300M12BM3. Figure 32 shows the measurement results. For safety reasons, gate driver over-current protection on this board is set to limit the current at approximately 1400A within 2.5 µs, as described in Section 3.2.3, Protection Features. This corresponds to a short circuit loop inductance of approximately 1.5 µH. It is recommended to use the board with a minimal short circuit limiting inductance of approximately 1 µH. Since the SiC MOSFET turns on significantly faster than a typical IGBT, direct short circuit (simultaneous turn-on of both the top and bottom switch) may result in extreme current values within a very short time, much shorter than the SC time specified by the module manufacturers. Please note that some of the manufactures do not specify the short circuit robustness at all, so if such a module is used, short circuit stress should be avoided. The soft turn-off function of the ACPL-335JC provides excellent protection from over-voltage during the turn-off phase after the short circuit detection, which can be observed on the voltage waveform in Figure 32.

Figure 32: Measurement results from over-current detection, soft short circuit at V_{dc} = 600V and short circuit inductance of $L \approx 1.5$ µH. In the second diagram, voltage waveforms are depicted with solid lines, and current waveforms are depicted with dashed lines.



4.4 Typical Switching Waveforms with FF6MR12KM1

Switching waveforms during hard switching of the semiconductors are measured with an oscilloscope using the standard double-pulse test procedure. The SiC MOSFET module used for testing is the Infineon SiC MOSFET FF6MR12KM1. Figure 33 shows the turn-on switching transient, whereas Figure 34 depicts the turn-off switching transient at different drain current levels. The switching performance measurements were done with the default gate resistor values, 4.03Ω for both On and Off resistors and a +15V/–5V gate power supply.

Figure 33: Characteristic waveforms during the turn-on switching transients at different load currents. In the upper diagram, voltage waveforms are depicted with solid lines, and current waveforms are depicted with dashed lines.

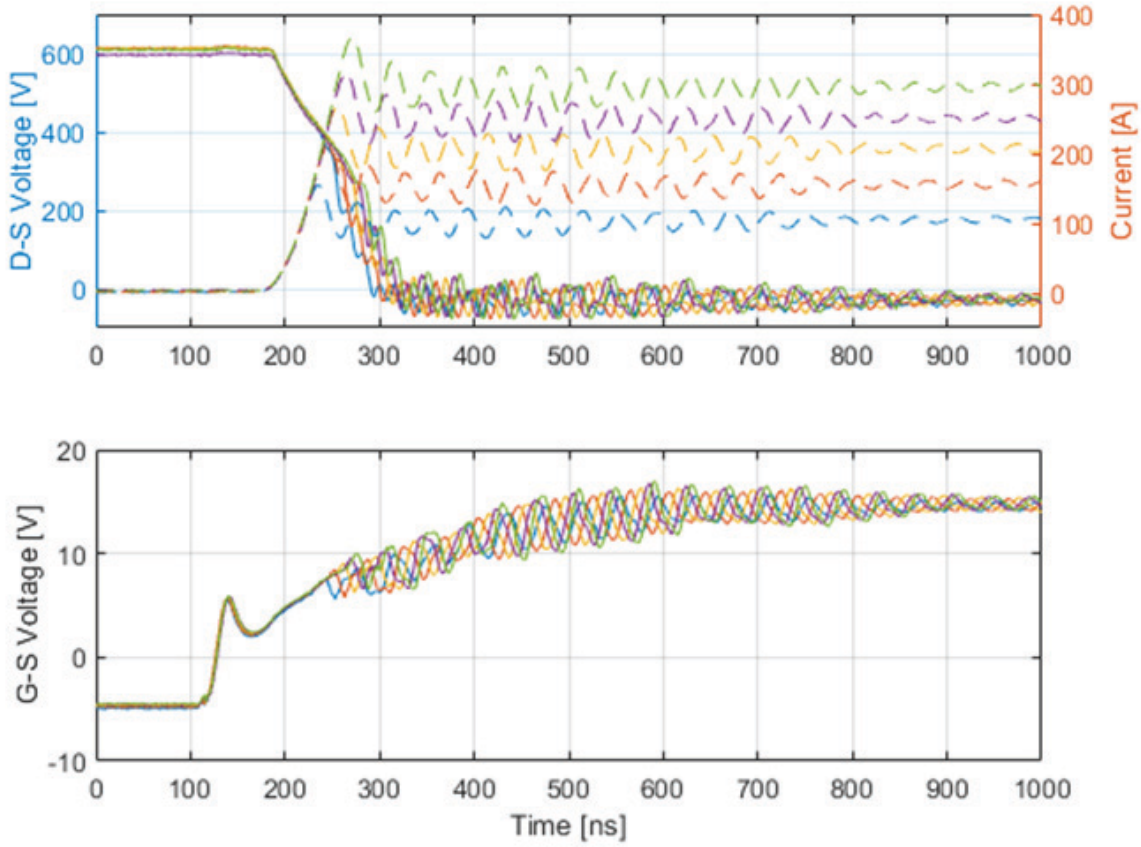
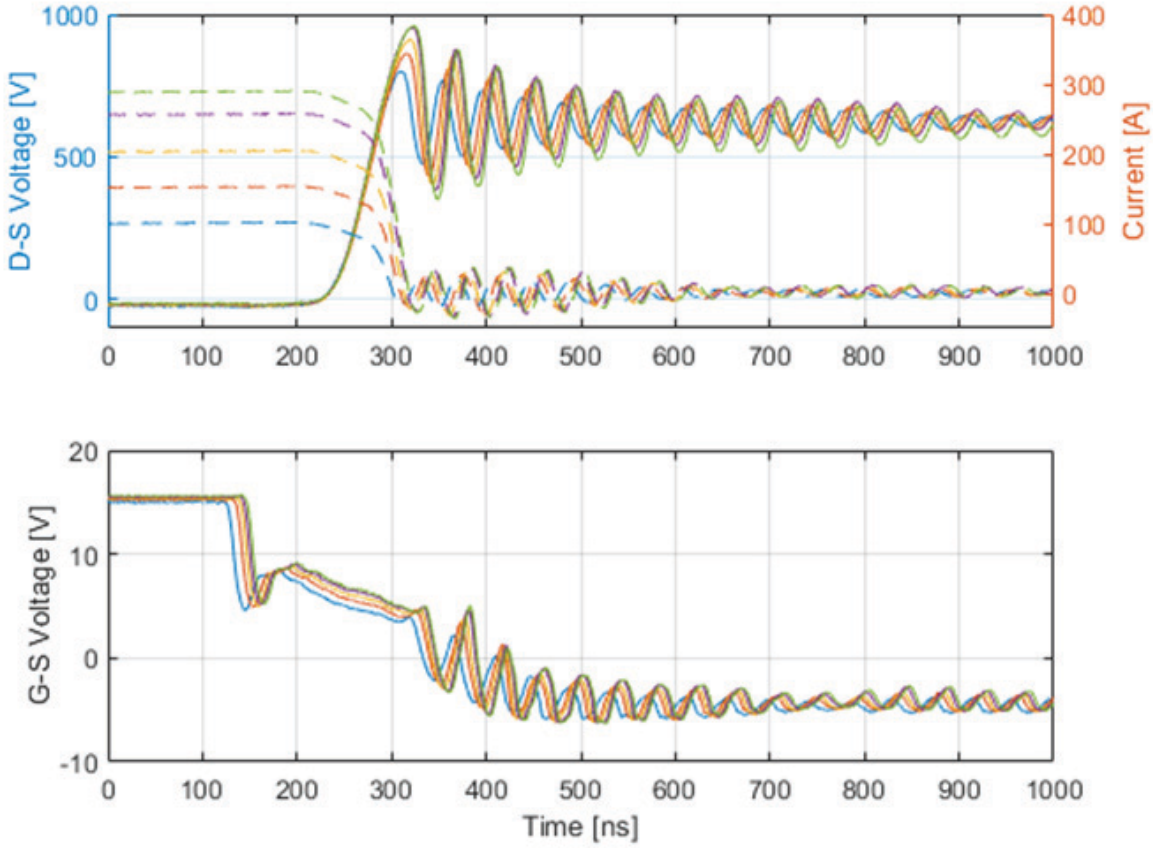


Figure 34: Characteristic waveforms during the turn-off switching transients at different load currents. In the upper diagram, voltage waveforms are depicted with solid lines, and current waveforms are depicted with dashed lines.



4.5 Typical Switching Losses with FF6MR12KM1

Figure 35 shows instantaneous power during switching and the resulting turn-on switching energy loss for a DC voltage of 600V, whereas Figure 36 shows the same waveforms for the turn-off transient.

Figure 35: Turn-on switching energy loss at 600V DC bus. In the upper diagram, voltage waveforms are depicted with solid lines, and current waveforms are depicted with dashed lines.

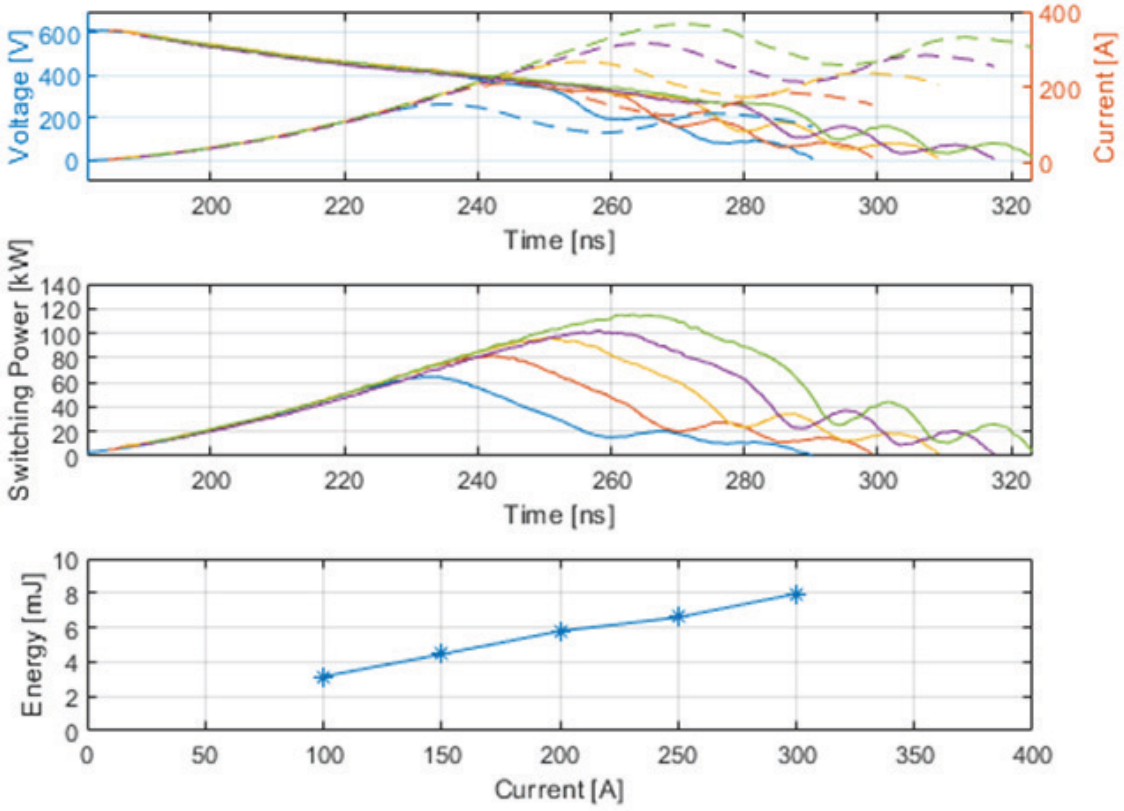
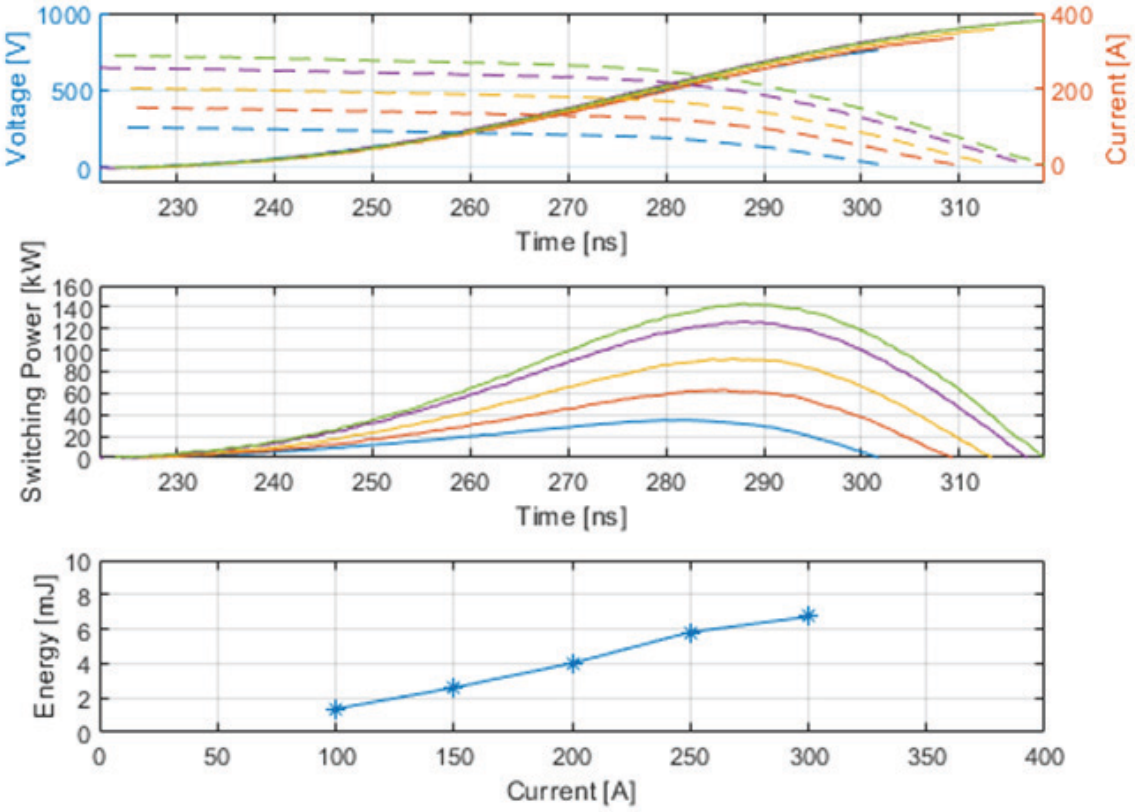


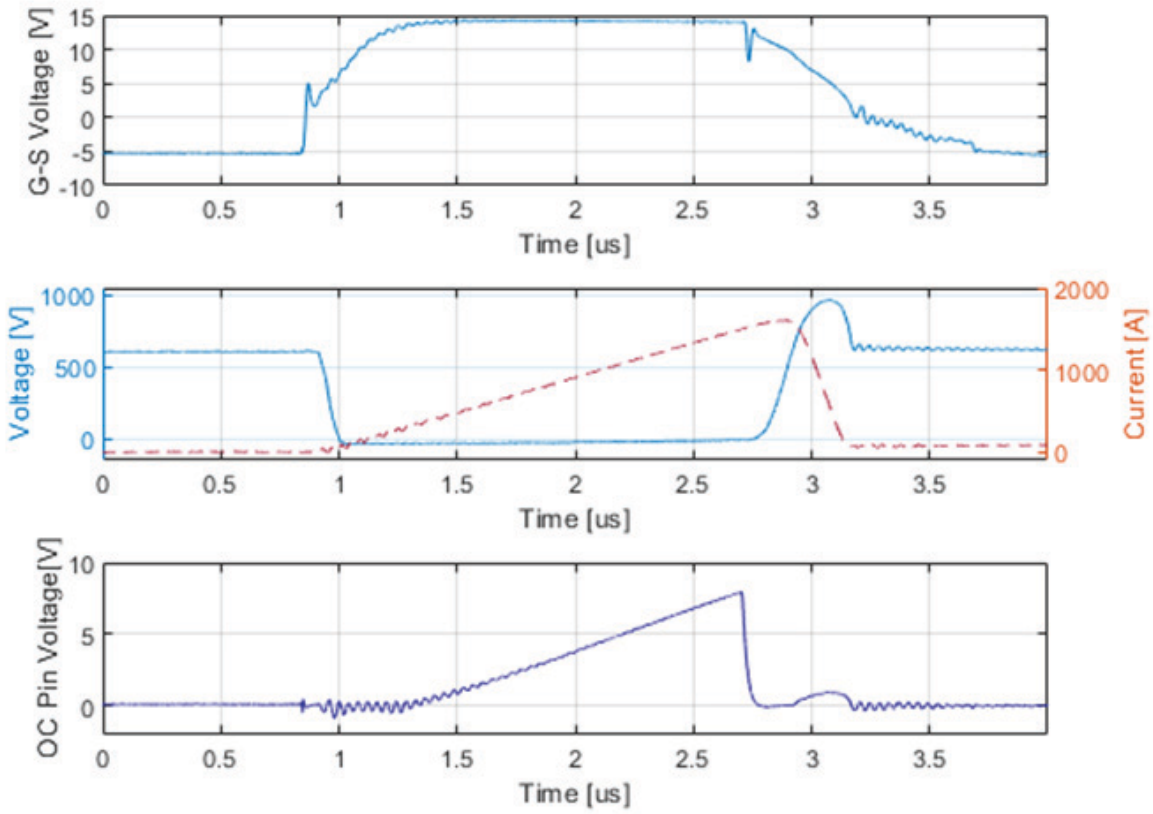
Figure 36: Turn-off switching energy loss at 600V DC bus. In the upper diagram, voltage waveforms are depicted with solid lines, and current waveforms are depicted with dashed lines.



4.6 Typical Over-Current Protection Performance with FF6MR12KM1

The over-current protection function is demonstrated by short-circuiting the output of the power module FF6MR12KM1. Figure 37 shows the measurement results.

Figure 37: Measurement results from over-current detection, soft short circuit at V_{dc} = 600V and short circuit inductance of $L \approx 1.5\ \mu H$. In the second diagram, voltage waveforms are depicted with solid lines, and current waveforms are depicted with dashed lines.



Appendix A: Schematics, Layout, and Bill of Materials

This appendix provides full schematics, layout, and the bill of materials for the EB1200M62-355JC. The intention behind providing this information is to enable customers to modify, copy, and qualify the design for production, according to specific requirements.

A.1 Schematics

Figure 38: EB1200M62-355JC – Top-Level Sheet

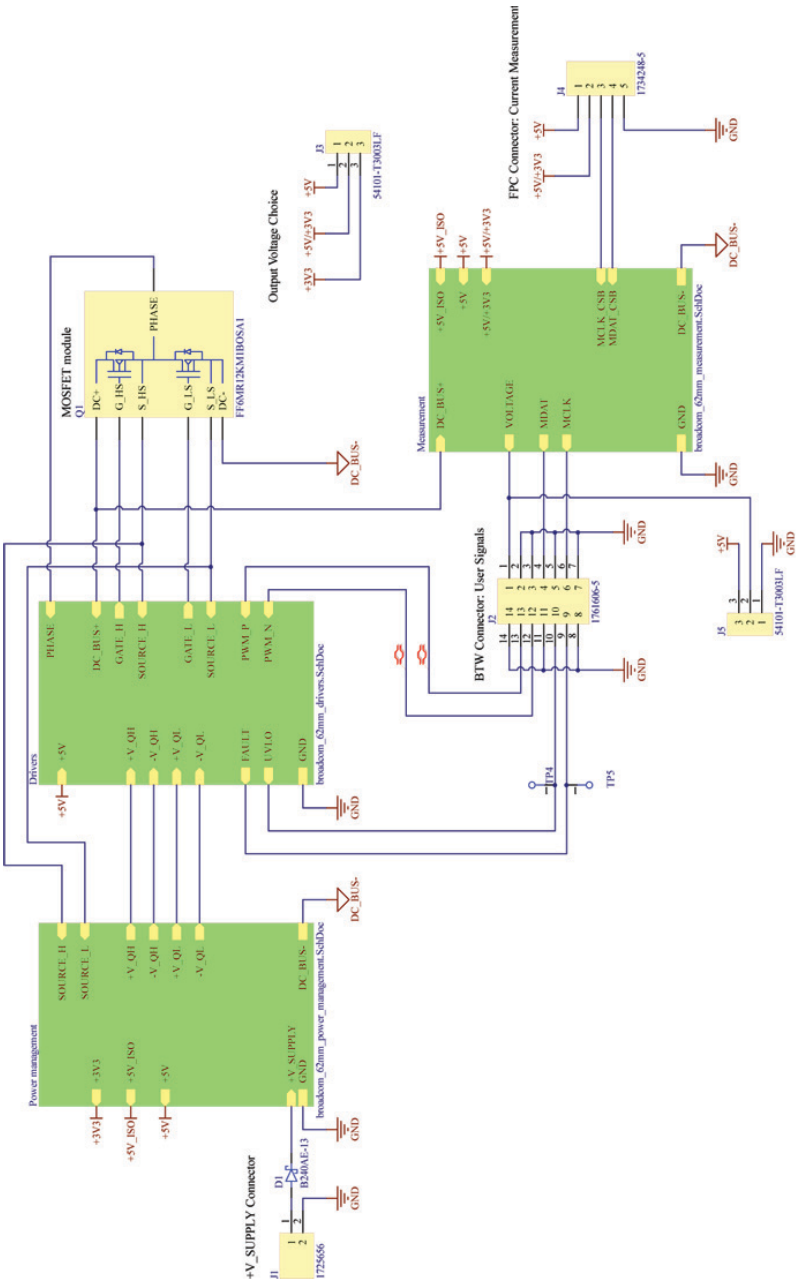


Figure 39: EB1200M62-355JC – Sheet 1 – Gate Drivers and Buffer

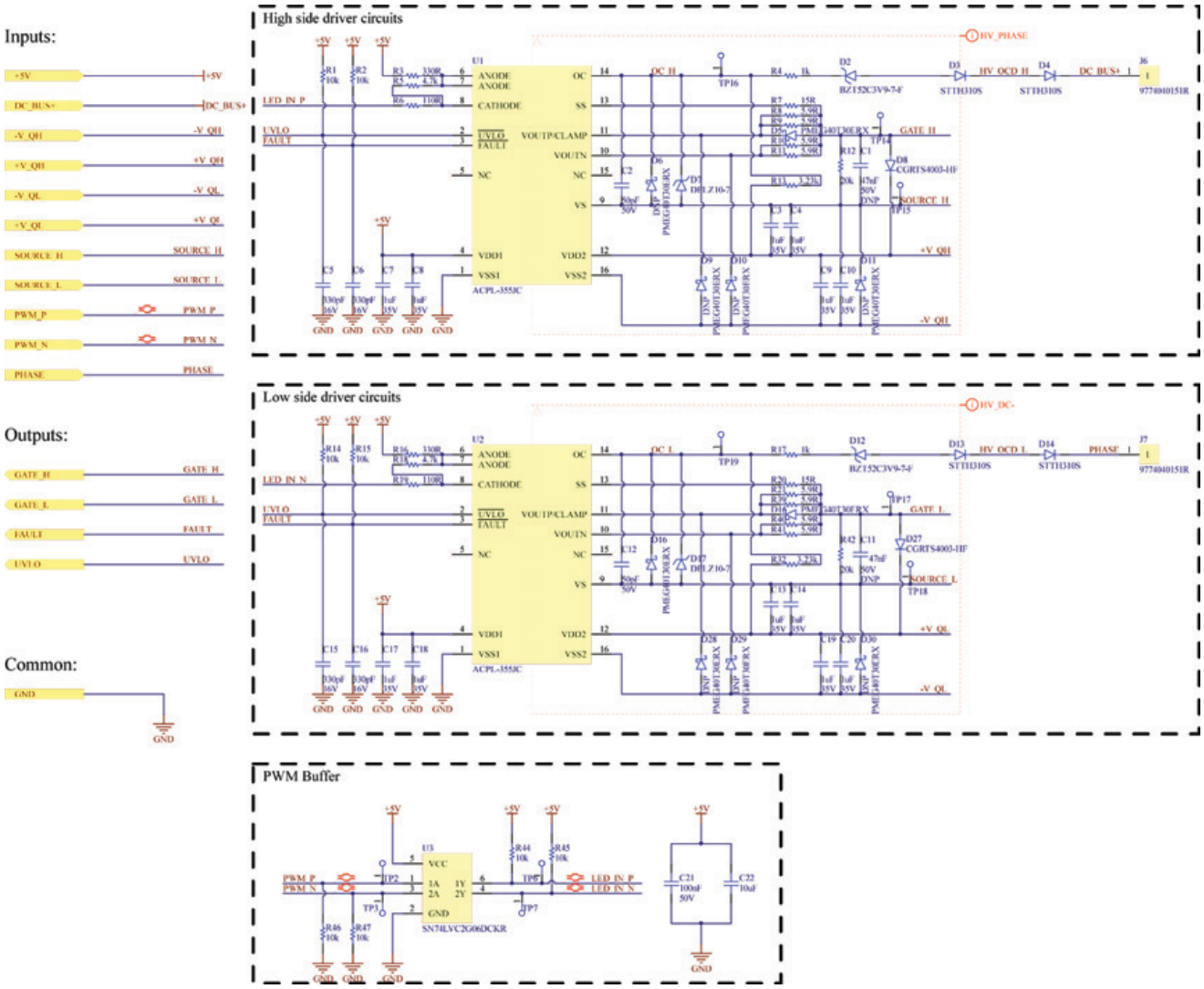


Figure 40: EB1200M62-355JC – Sheet 2 – Power Management

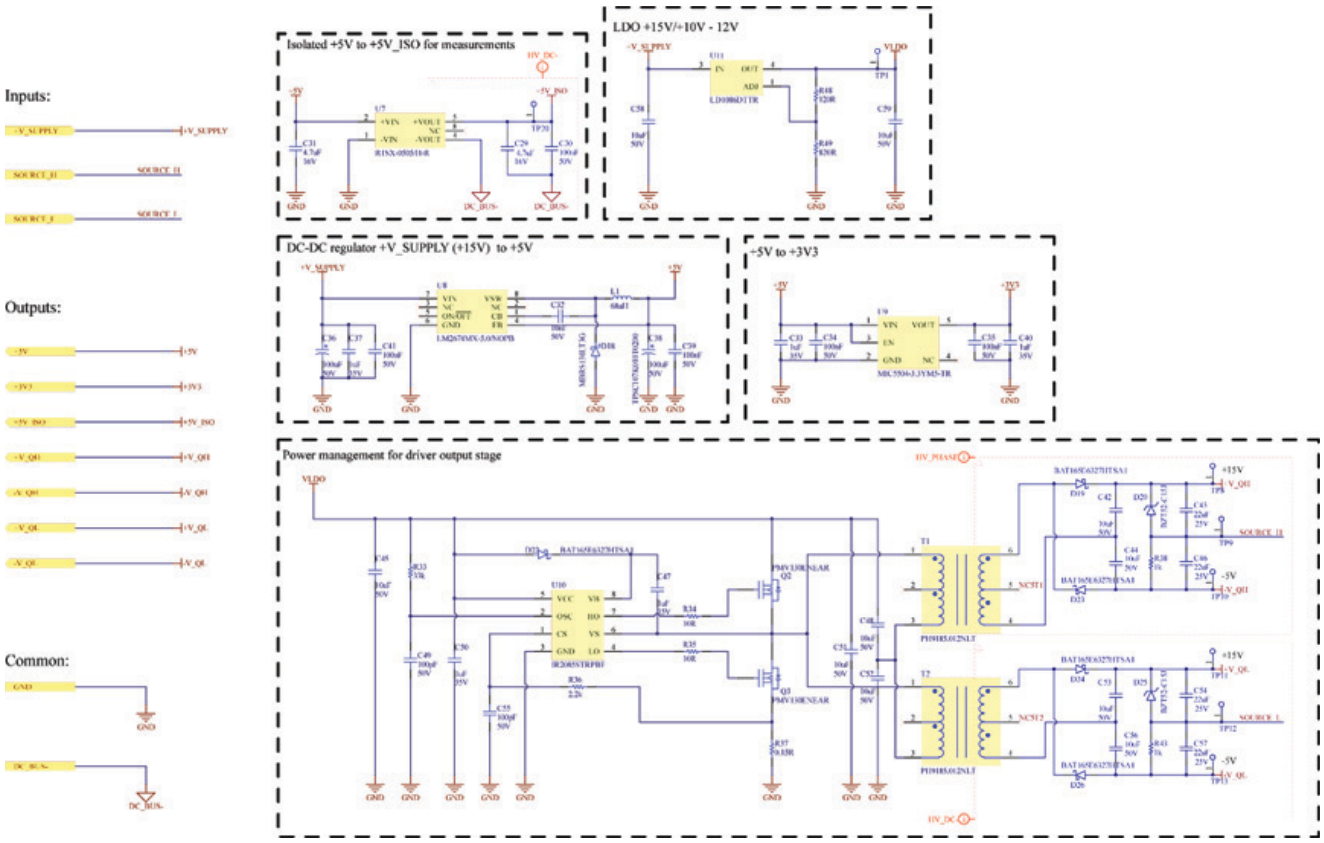
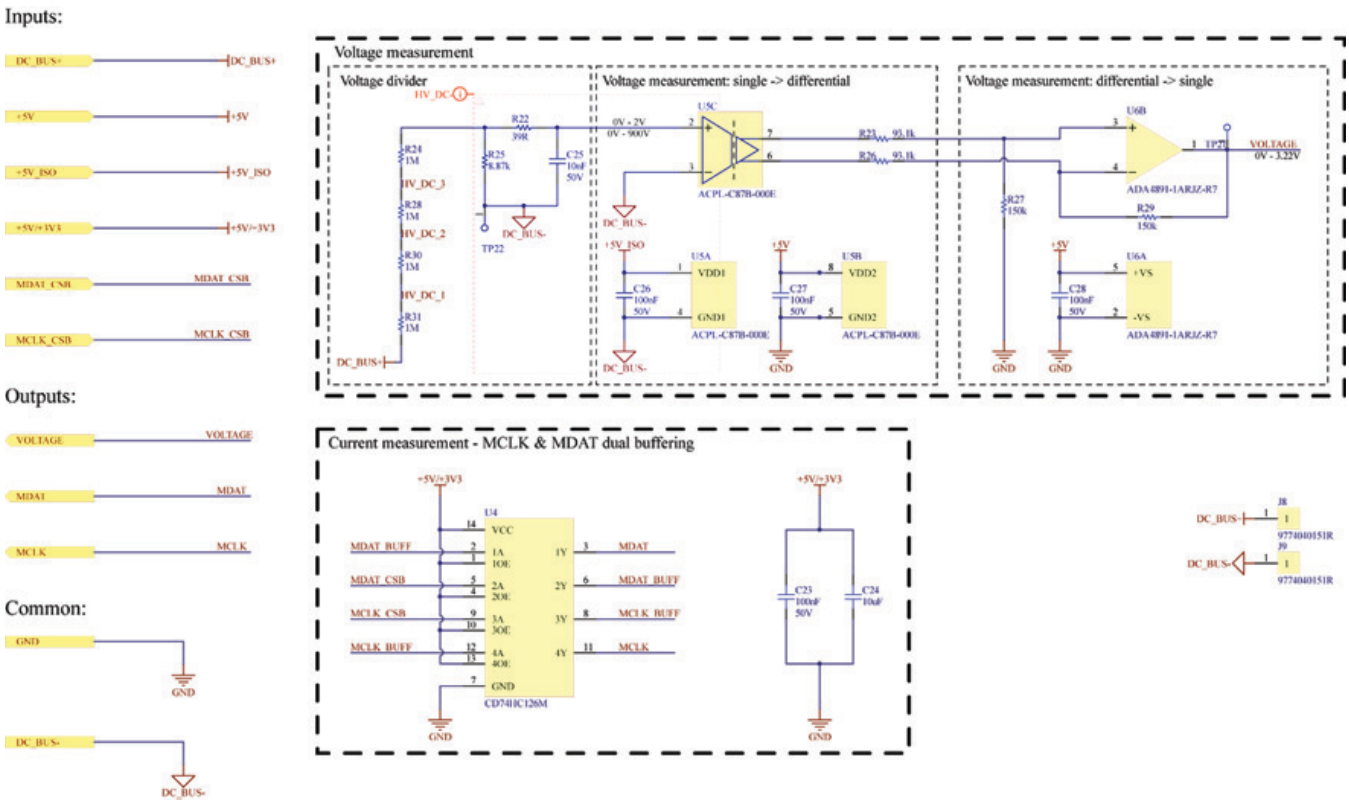


Figure 41: EB1200M62-355JC – Sheet 3 – Measurements



A.2 Layout

Figure 42: EB1200M62-355JC – Assembly Drawing

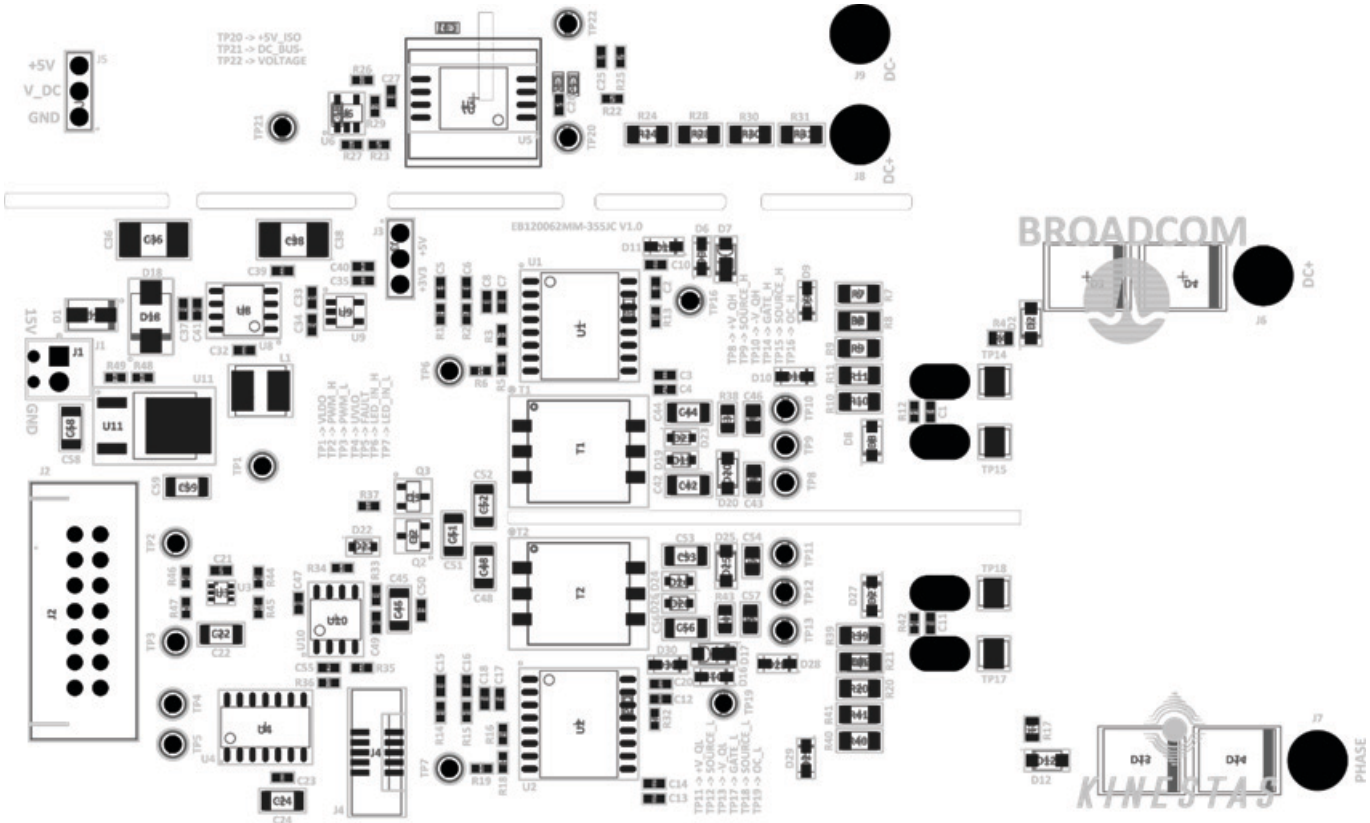


Figure 43: EB1200M62-355JC – Top Layer

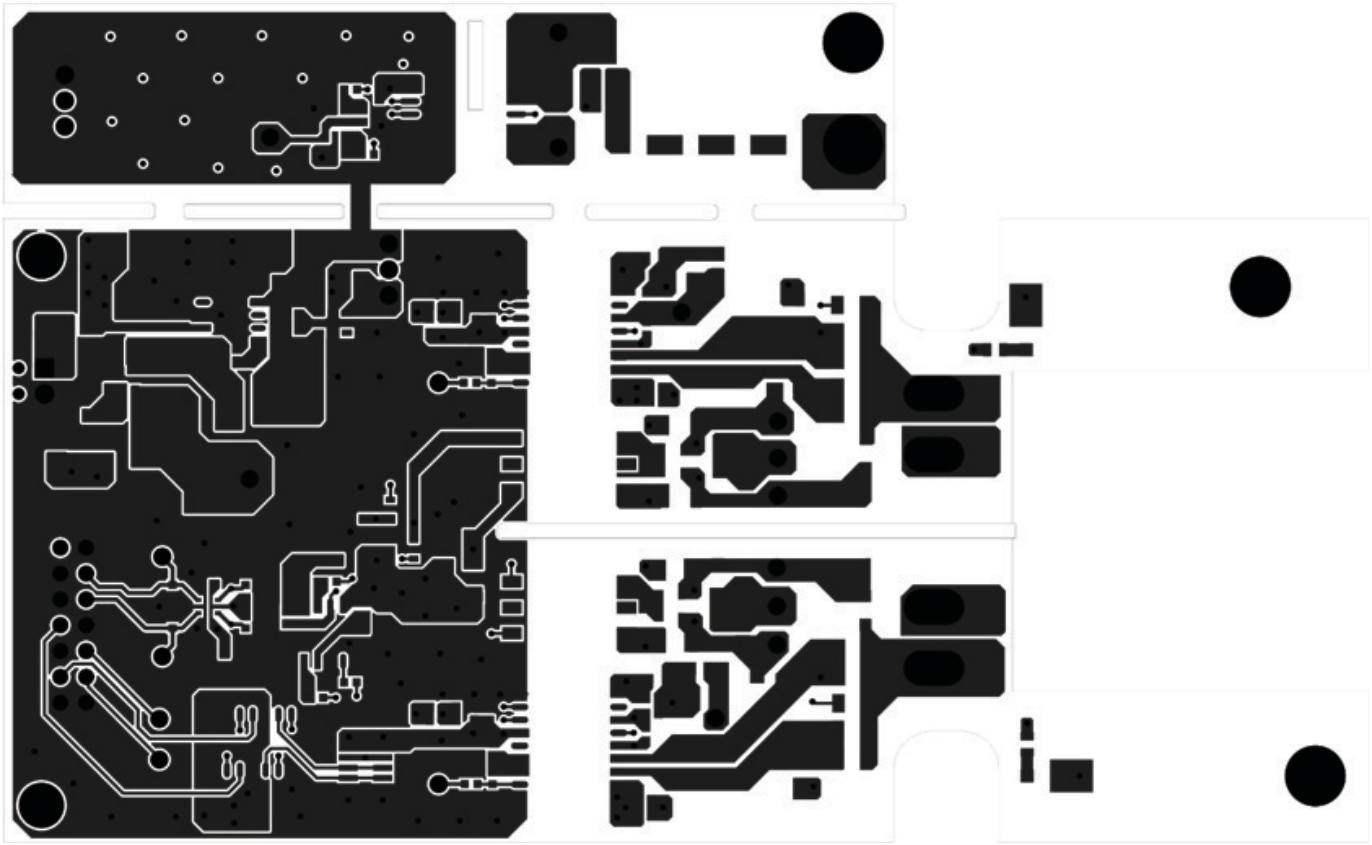


Figure 44: EB1200M62-355JC – Signal Layer 1

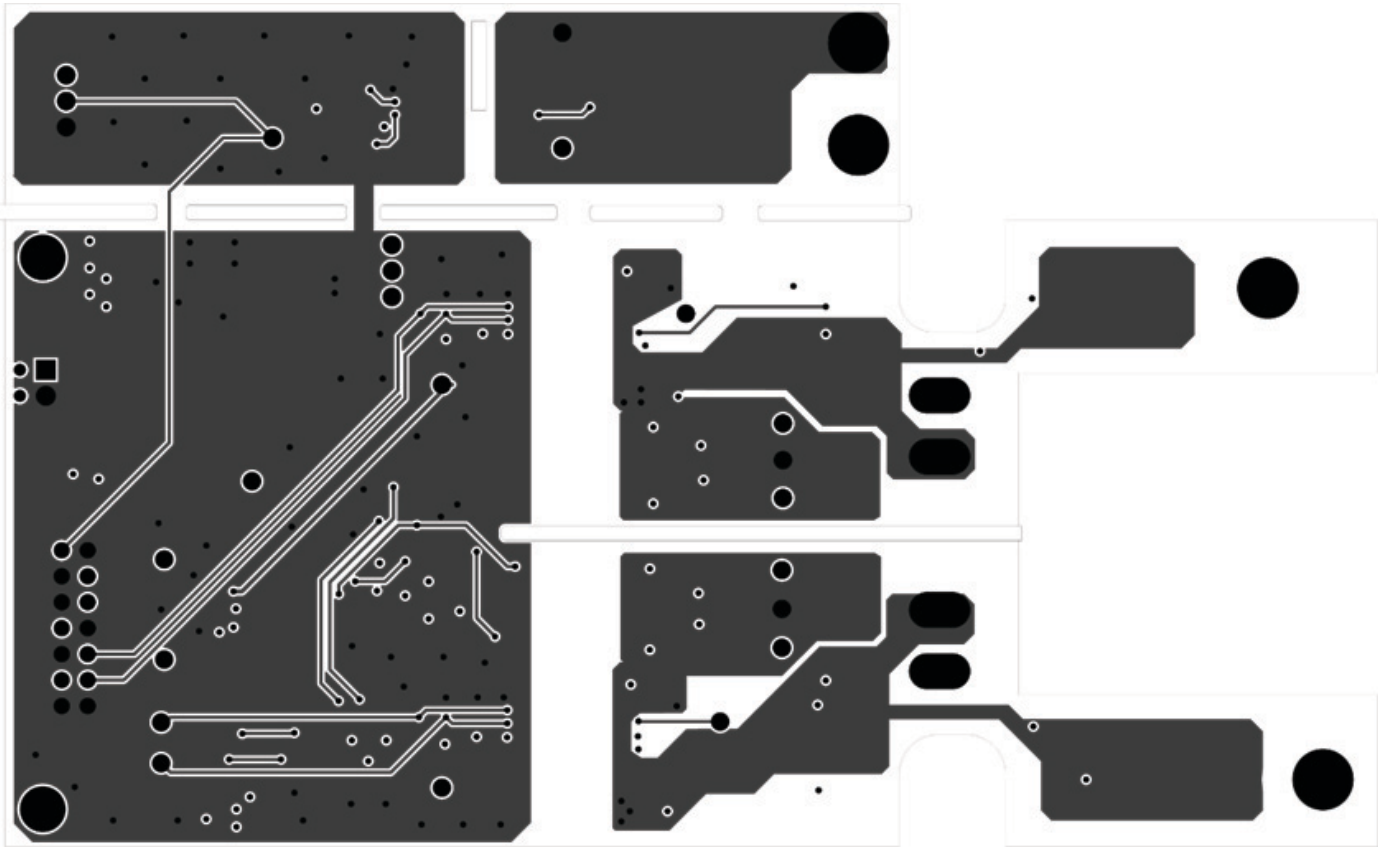


Figure 45: EB1200M62-355JC – Signal Layer 2

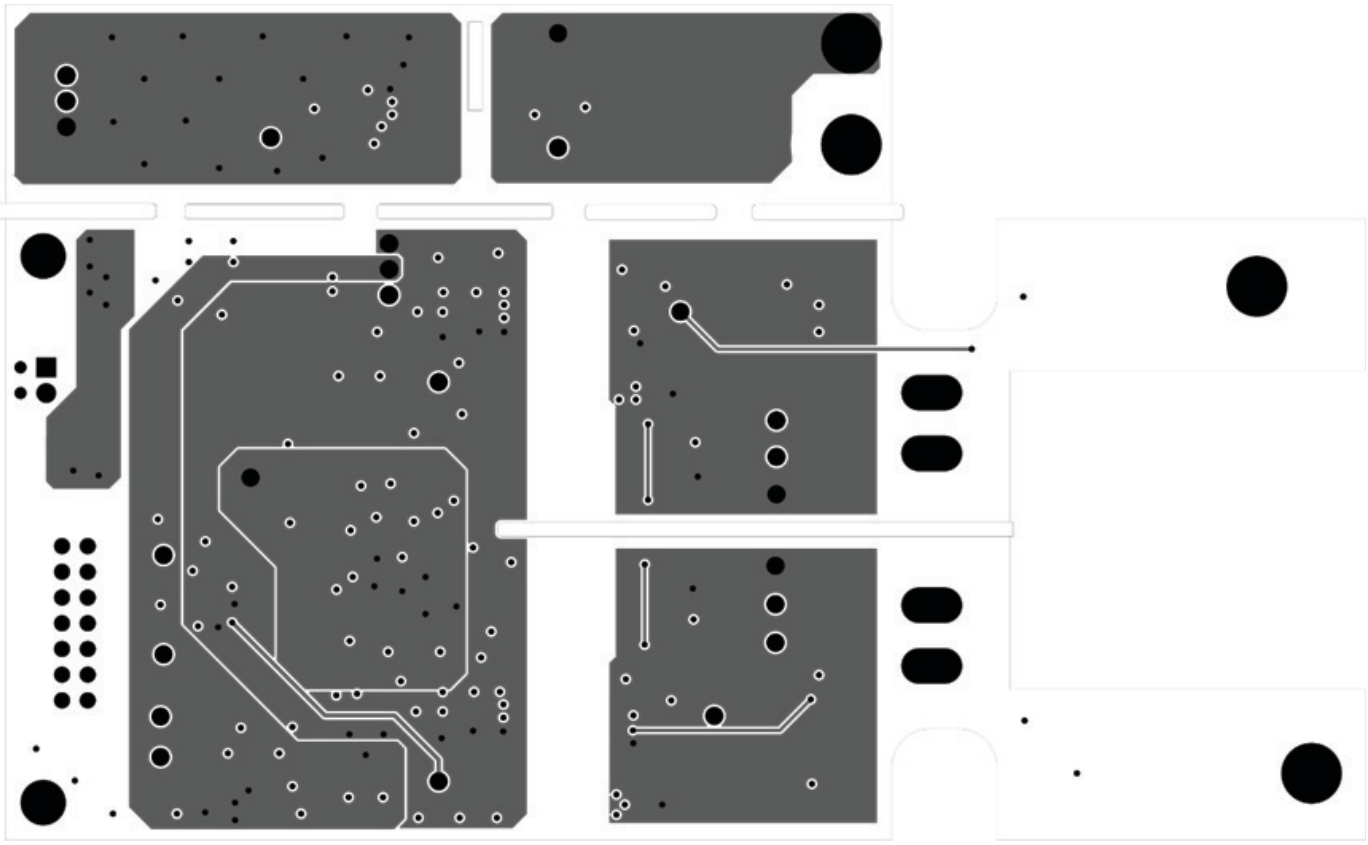
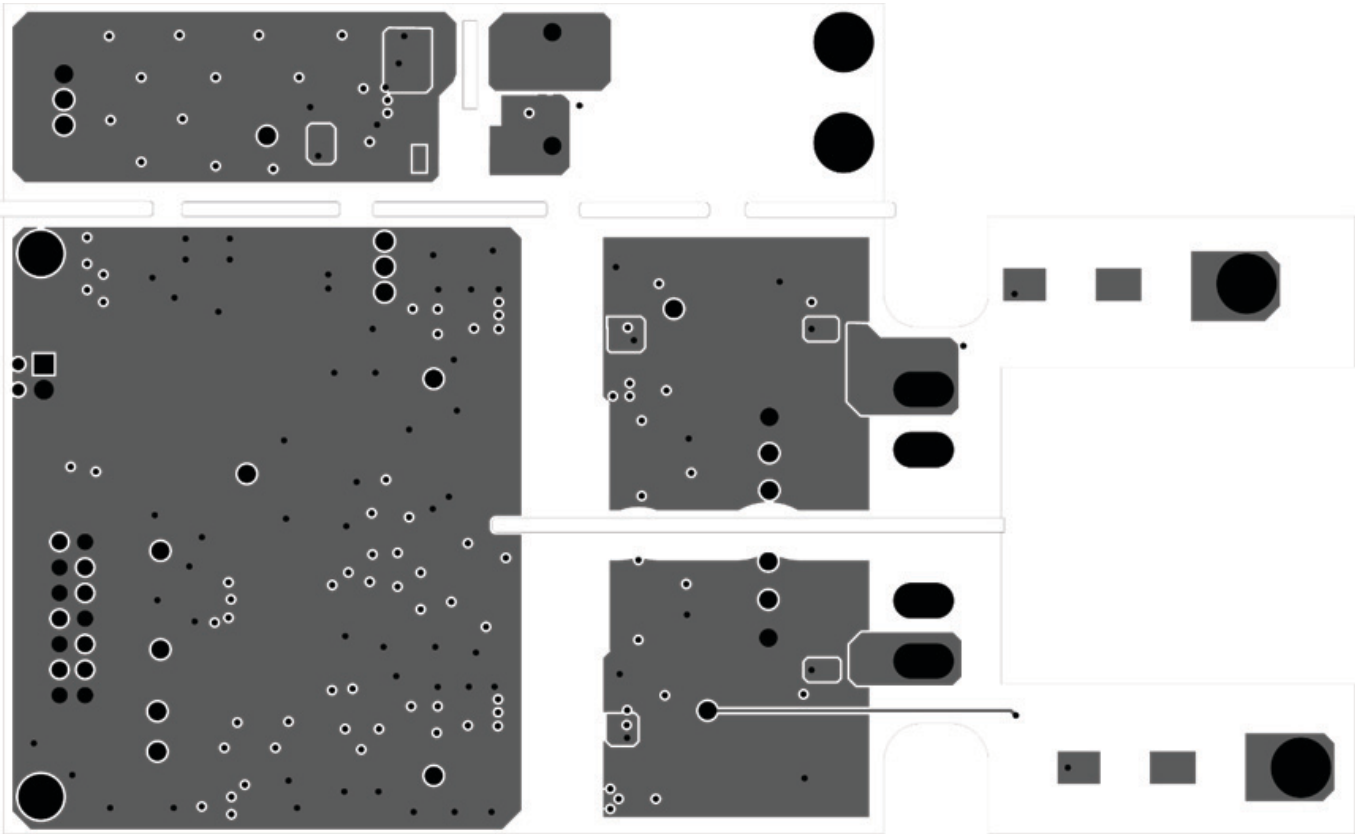


Figure 46: EB1200M62-355JC – Bottom Layer



A.3 Bill of Materials

Table 12 lists the bill of materials for the EB1200M62-355JC.

Table 12: Bill of Materials for the EB1200M62-355JC Evaluation Board

EB1200M62-355JC, BOM	
Designator	**MFPN**
C1, C11	CGA3E2X7R1H473K080AA
C2, C12	CC0603JRNPO9BN500
C3, C4, C7, C8, C9, C10, C13, C14, C17, C18, C19, C20, C33, C37, C40, C47, C50	CGA3E1X7R1V105K080AC
C5, C6, C15, C16	VJ0603Y331KXJPW1BC
C21, C23, C26, C27, C28, C30, C34, C35, C39, C41	885382206004
C22, C24, C42, C44, C45, C48, C51, C52, C53, C56, C58, C59	GRT31CR61H106ME01L
C25, C32	CL10B103KB8NNNC
C29, C31	CL10A475MO8NNNC
C36, C38	TPSC107K010T0200
C43, C46, C54, C57	GRM21BR61E226ME44L
C49, C55	06035C101KAT2A
D1	B240AE-13
D2, D12	PDZ3.9BGWJ(WAB300M12BM3) SZMMSZ4678T1G(FF6MR12KM1)
D3, D4, D13, D14	STTH310S
D5, D6, D9, D10, D11, D15, D16, D28, D29, D30	PMEG40T30ERX
D7, D17	DFLZ10-7
D8, D27	CGRTS4003-HF
D18	MBRS130LT3G
D19, D22, D23, D24, D26	BAT165E6327HTSA1
D20, D25	PDZ16BGWX
J1	1725656
J2	1761606-5
J3, J5	54101-T3003LF
J4	1734248-5
J6, J7, J8, J9	9774040151R
L1	VLS5045EX-680M
Q1	FF6MR12KM1BOSA1
Q2, Q3	PMV130ENEAR
R1, R2, R14, R15, R44, R45, R46, R47	ESR03EZPJ103
R3, R16	ERJ-PA3J331V
R4, R17	AS08J1001ET
R5, R18	ESR03EZPJ472
R6, R19	ERJ-PA3J111V
R7, R20	CRCW120615R0FKEAC
R8, R9, R10, R11, R21, R39, R40, R41	CRCW12068R06FKEA(FF6MR12KM1) RK73H2BTTD5R90F(WAB300M12BM3)
R12, R42	ESR03EZPJ203

Table 12: Bill of Materials for the EB1200M62-355JC Evaluation Board (Continued)

EB1200M62-355JC, BOM	
Designator	**MFPN**
R13, R32	ESR03EZPJ332
R22	ESR03EZPJ390
R23, R26	ERJ-PA3F9312V
R24, R28, R30, R31	RK73G2BTTD1004C
R25	ERJ-PA3F8871V
R27, R29	ESR03EZPJ154
R33	ESR03EZPJ333
R34, R35	ESR03EZPJ100
R36	ESR03EZPF2201
R37	KDV06FR150ET
R38, R43	ERJ-P06J102V
R48	ERJ-PA3J121V
R49	ERJ-UP3F8200V(WAB300M12BM3) ERJ-PA3F9530V(FF6MR12KM1)
T1, T2	PH9185.012NLT
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP16, TP19, TP20, TP21, TP22	5002
TP14, TP15, TP17, TP18	5190TR
U1, U2	ACPL-355JC
U3	SN74LVC2G06DCKR
U4	CD74HC126M
U5	ACPL-C87B-000E
U6	ADA4891-1ARJZ-R7
U7	R1SX-0505/H-R
U8	LM2674MX-5.0/NOPB
U9	MIC5504-3.3YM5-TR
U10	IR2085STRPBF
U11	LD1086D2TTR

A.4 Test Points

Table 13 lists the available test points for the EB1200M62-355JC.

Table 13: Available Test Points for the EB1200M62-355JC Evaluation Board

Test Point Designator	Signal
TP1	VLDO
TP2	PWM_H (before buffer)
TP3	PWM_L (before buffer)
TP4	UVLO
TP5	FAULT
TP6	LED_IN_H (after buffer)
TP7	LED_IN_L (after buffer)
TP8	+V_QH
TP9	SOURCE_H
TP10	–V_QH
TP11	+V_QL
TP12	SOURCE_L
TP13	–V_QL
TP14	GATE_H
TP15	SOURCE_H
TP16	OC_H
TP17	GATE_L
TP18	SOURCE_L
TP19	OC_L
TP20	+5V_ISO
TP21	VOLTAGE
TP22	DC_BUS–

Appendix B: Disclaimer

THIS APPLICATION NOTE CONTAINS INFORMATION THAT SHOULD SERVE ONLY AS A REFERENC FOR INITIAL EVALUATION AND IMPLEMENTATION OF THE BROADCOM INC. TECHNOLOGIES PRODUCTS. BROADCOM INC. DOES NOT TAKE RESPONSIBILITY FOR USING AND IMPLEMENTING THE PRODUCTS IN OTHER DESIGN.

Revision History

ACPL-355JC-62mmSiC-RM100; Version 1.0; March 25, 2022

Initial release.