ACPL-352J

Vincotech H6.5 3-Level IGBT flowPACK Module Evaluation Board

Reference Manual
Version 1.0

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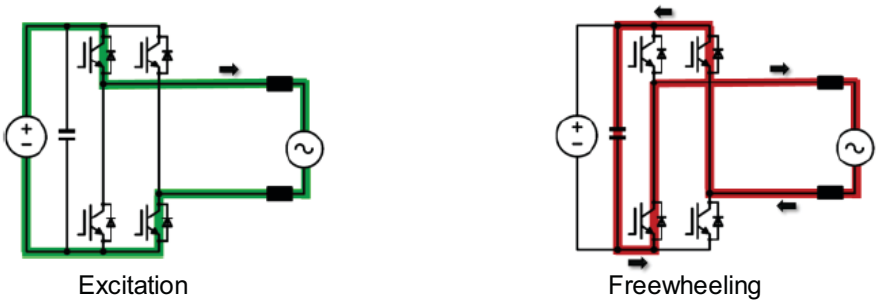
Chapter 1: Introduction

1.1 3-Level Topology

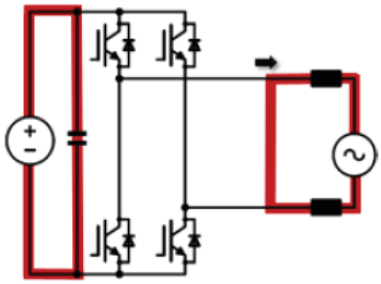
3-Level topology has two main advantages over conventional 2-Level topology, namely higher efficiency and reduction in filtering effort. 2-Level topology requires a large output filter and regenerates energy back to the DC bulk capacitor during freewheeling. The regenerated energy has to pass the inverter twice and will cause additional power dissipation.

Figure 1: 2-Level Topology during Excitation and Freewheeling



In a 3-Level topology, the excitation works the same as the 2-Level, but during freewheeling, the H-bridge is turned off and the filter's primary output is shorted. The switch voltage is reduced and the switching losses and the size of the output filter are minimized.

Figure 2: 3-Level Topology with H-bridge Turned Off and Output Shorted during Freewheeling



This reference design will discuss the evaluation board of Vincotech H6.5 3-Level IGBT module for 3-Level topology.

Chapter 2: Description of H6.5 Evaluation Board

2.1 Board Description

Figure 3: Evaluation Board for flowPACK 1 H6.5 Module

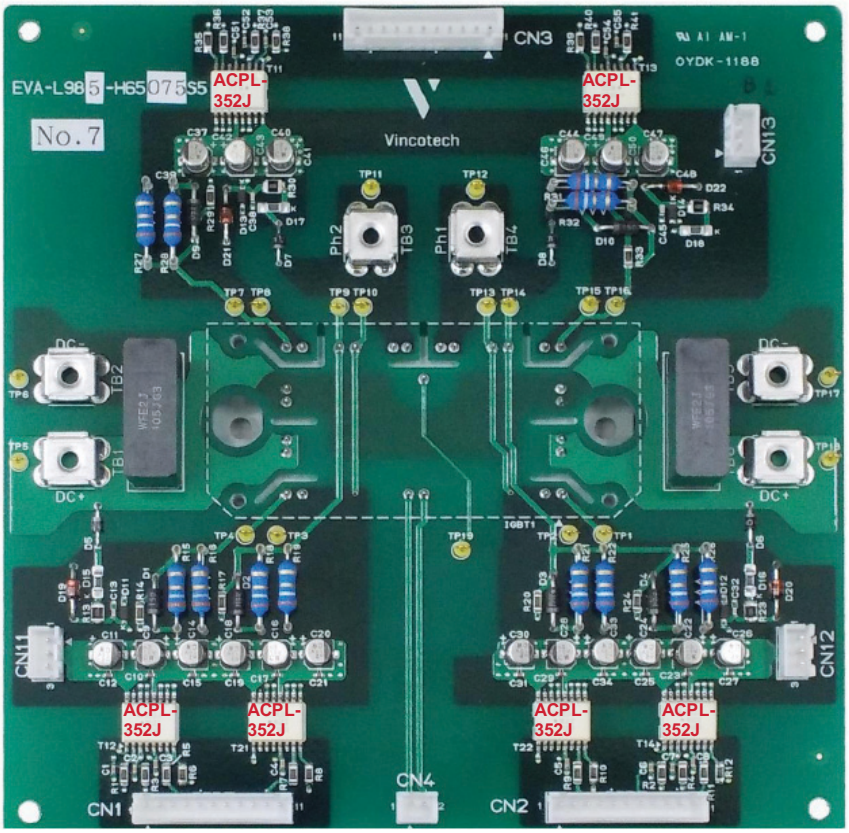
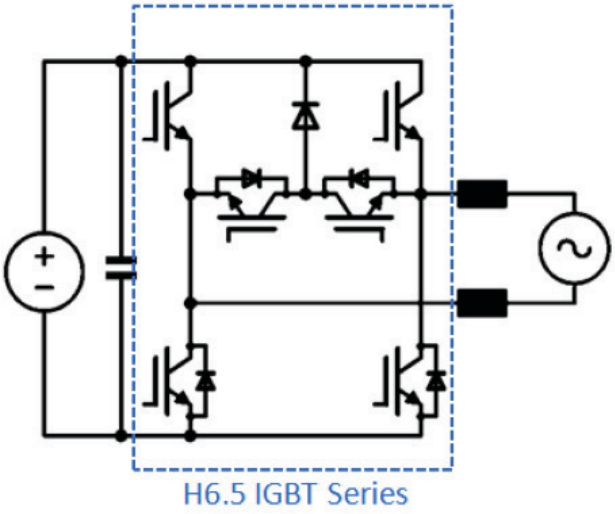


Figure 4 shows the simplified block diagram of the evaluation board and the applied circuit designed by Vincotech. It consists of a Vincotech flowPACK1 H6.5 module in a single phase H6.5 3-Level topology. The module has six 650V IGBTs and five diodes. The modules that can be used in this evaluation board come in three current ratings:

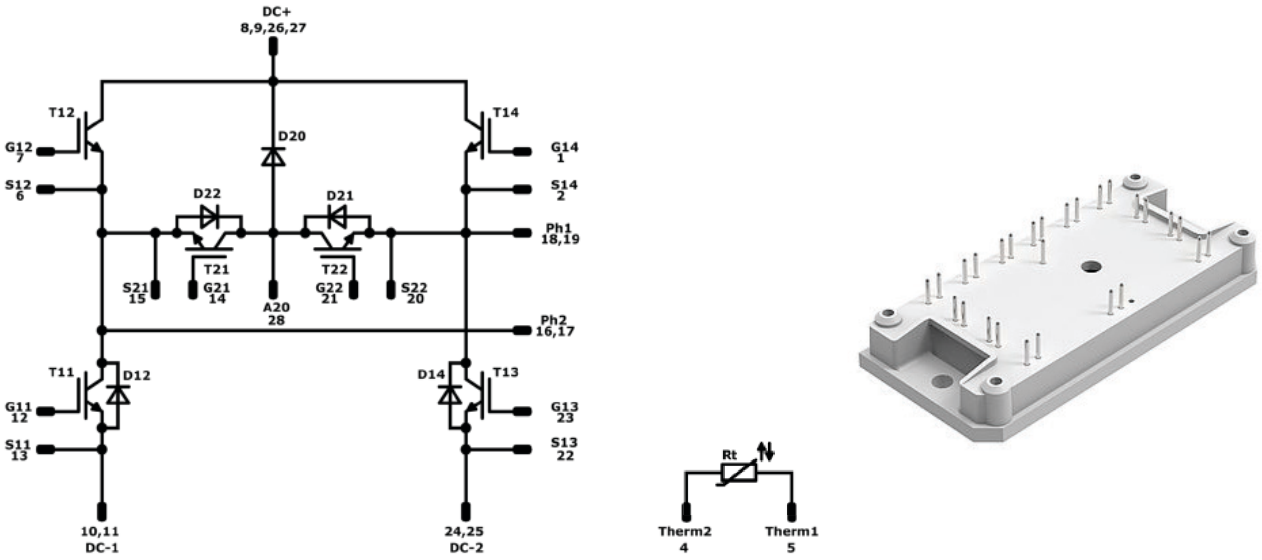
- 10-FY07HVA050S5-L984F08 – 650V/50A
- 10-FY07HVA075S5-L985F08 – 650V/75A
- 10-FY07HVA100S5-L986F08 – 650V/100A

Figure 4: Block Diagram of Vincotech flowPack1 H6.5 Module and Applied Circuit



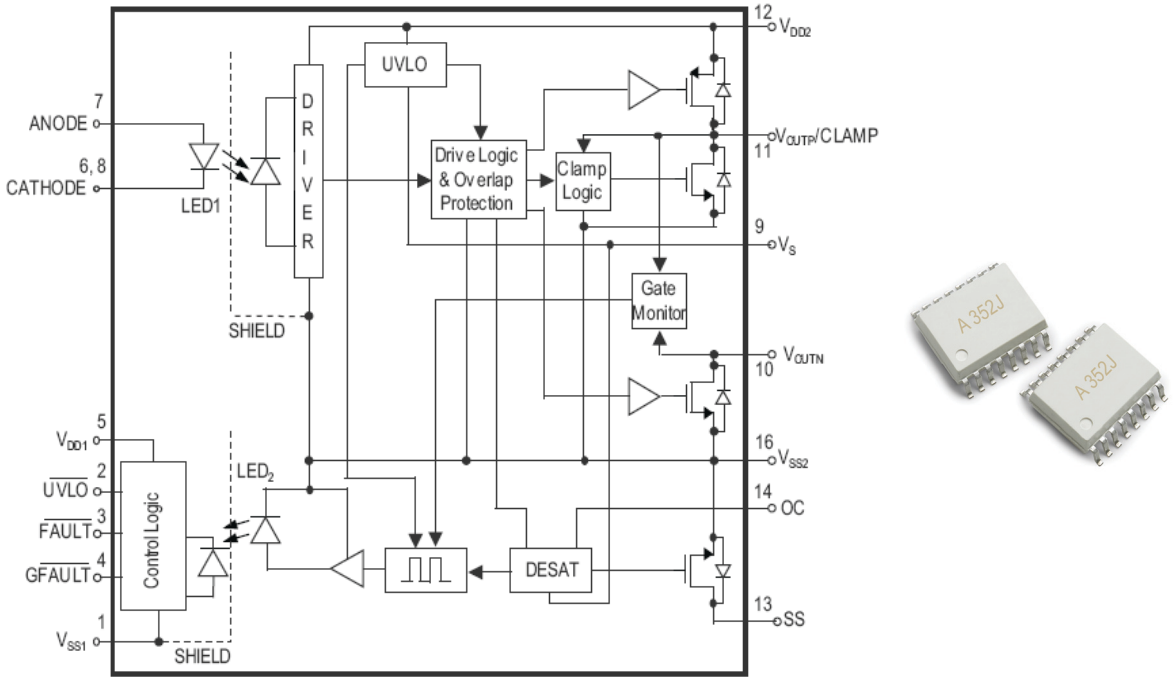
10-FY07HVA050S5 is housed in Vincotech flowPACK1 with convex shaped substrate for superior thermal contact. The IGBTs use S5 chip technology which allows high speed and smooth switching. The IGBTs have very low gate charge and very low collector emitter saturate voltage for optimum switching performance and efficiency.

Figure 5: Schematic of 10-FY07HVA050S5 and flowPACK1 Module



Six ACPL-352J gate drive optocouplers are used to drive the six IGBTs. The ACPL-352J is industry's highest output current, 5A smart gate drive optocoupler. The high peak output current, together with wide operating voltage make it ideal for driving the IGBT directly. The device features fast propagation delay of 100 ns with excellent timing skew performance and has very high common mode transient immunity (CMTI) of more than 100 kV/µs. It can provide IGBT with over current protection and fail-safe functional safety reporting. This full-featured gate drive optocoupler comes in a compact, surface-mountable SO-16 package with 8mm of creepage and clearance. It provides the reinforced insulation certified by safety regulatory IEC/EN/DIN, UL and CSA with working voltage of V_{IORM} = 1414 V_{PEAK}.

Figure 6: Block Diagram of ACPL-352J and SO-16 Package



This reference design will describe the basic operation of the evaluation board and the gate drive design. Other information like the layouts and BOM of the H6.5 evaluation board can be found in Vincotech reference design website:

https://www.vincotech.com/support-and-documents/evaluation-board-reference-design.html

2.2 Basic Operation

Figure 7: Basic Circuit of the Logical Control

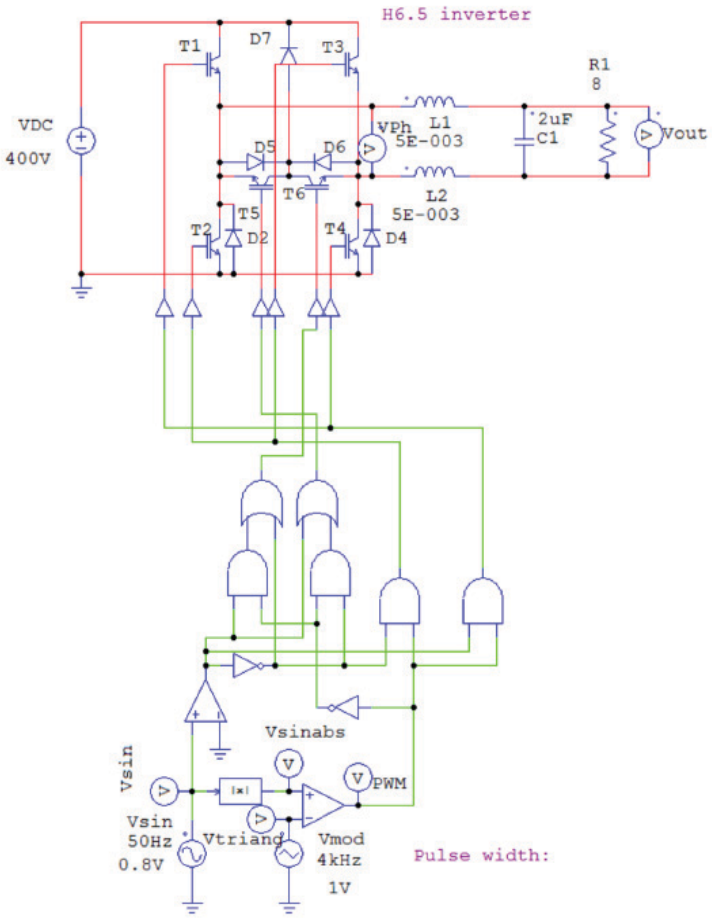
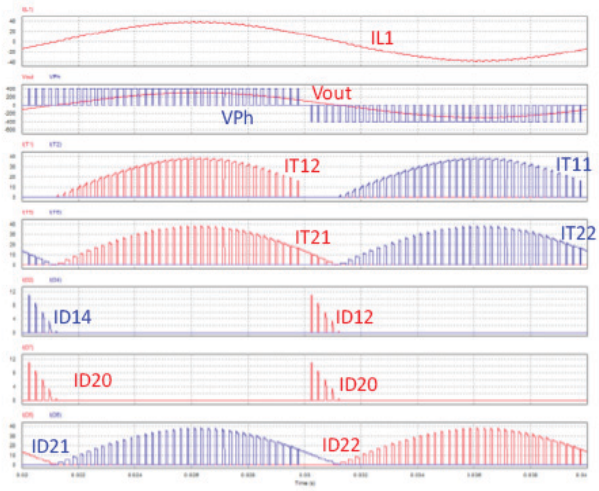


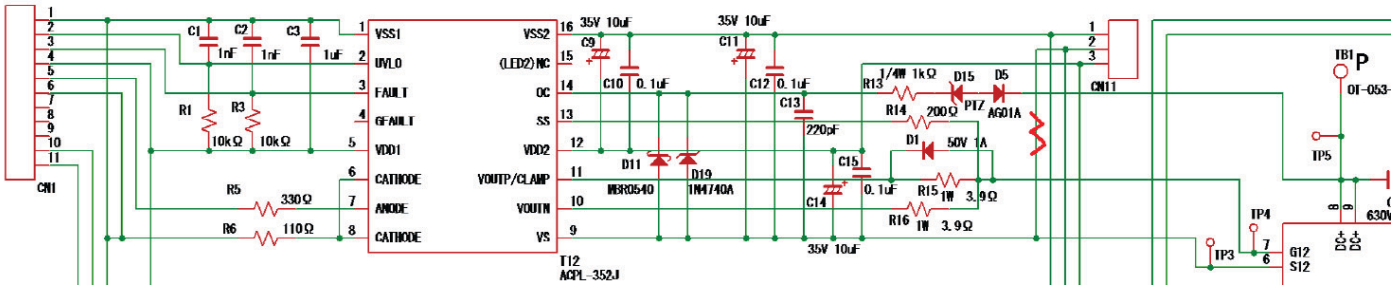
Figure 7 shows the circuit to control the logical switching sequence of the six IGBTs. Figure 8 shows the simulated waveforms.

Figure 8: Simulation of the Operating Waveform



2.3 Gate Drive Design

Figure 9: ACPL-352J Gate Drive Circuit



The schematic shows the gate drive design for IGBT, T12 of the H6.5 module.

The ACPL-352J has a LED input control input and three fault reporting mechanisms: namely V_{DD2} under voltage lockout (UVLO), IGBT over current (FAULT) and IGBT gate status (GFAULT). These open drain FAULT, UVLO and GFAULT outputs are connected to 10-kΩ pull-up resistors (R1/R3) and 1nF filtering capacitors (C1/C2) and are suitable for wired OR applications. UVLO has the highest fault priority and follows by FAULT and GFAULT (GFAULT is not used in this evaluation board).

The supplies (V_{DD1} and V_{DD2}) are connected to 1 µF (C3) and pairs of 10 µF/0.1 µF (C9/C10, C11/C12, C14/C15) bypass decoupling capacitors to provide the large transient currents necessary during a switching transition.

The two resistors (R5/R6) connected to input LED's anode and cathode are recommended to be split in the ratio of 3:1. They will help to balance the common mode impedances at the LED's anode and cathode. This helps to equalize the common mode voltage changes at the anode and cathode to give high CMR performance of more than100 kV/µs.

The OC pin of ACPL-352J is connected to the collector of IGBT T12 via a high voltage blocking diode, D5 and resistor R13. Zener diode, D15 is used to adjust the threshold voltage of over current detection. Blanking capacitor, C12 is used prevent false fault detection by filtering high frequency noise transient.

During overcurrent fault condition, the IGBT is soft shut down through the SS pin and the rate of shut down can be adjusted by R14.

The gate resistors (R15/R16) serve to limit gate current and indirectly control the IGBT switching times. Diode, D1 is used together with the CLAMP function to shunt parasitic IGBT Miller current during the off cycle.

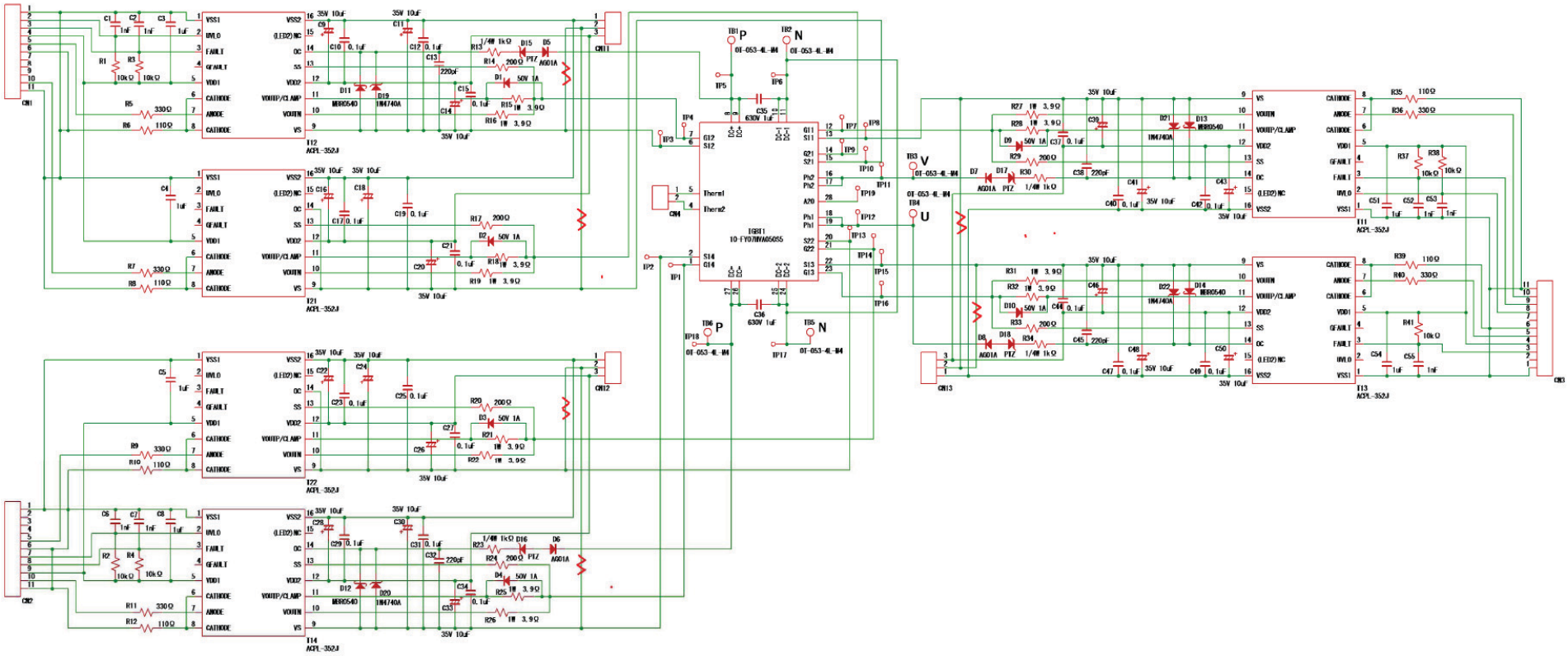
The gate resistors can be calculated from the secondary side power supply and $I_{O(PEAK)}$ specification of ACPL-352J:

$$R_G \geq \frac{V_{DD2}-V_{SS2}}{I_{OPEAK}} - R_{OUTN(MIN)}$$
$$= \frac{15-(-6)V}{5A} - 0.3\Omega$$
$$= 3.9\Omega$$

This negative going voltage spike is typically generated by inductive loads or reverse recovery spike of the IGBT freewheeling diodes. Zener diode, D14 and Schottky diode, D11 are used to prevent a false fault signal caused by positive and negative spikes.

The complete schematic is show in Figure 10.

Figure 10: Schematic of the Evaluation Board



Chapter 3: Test Circuit and Result

3.1 Test Setup and Waveform

The test items and corresponding test pins are shown in Figure 11.

Figure 11: Test Items and Test Pins

Test item	Test pin	Item	Test pin
T11 V_{GE}	TP11-TP8	T14 V_{GE}	TP18-TP2
T11 V_{CE}	TP7-TP8	T14 V_{CE}	TP1-TP2
T12 V_{GE}	TP5-TP3	T21 V_{GE}	TP19-TP10
T12 V_{CE}	TP4-TP3	T21 V_{CE}	TP9-TP10
T13 V_{GE}	TP12-TP15	T22 V_{GE}	TP19-TP13
T13 V_{CE}	TP16-TP15	T22 V_{CE}	TP14-TP13

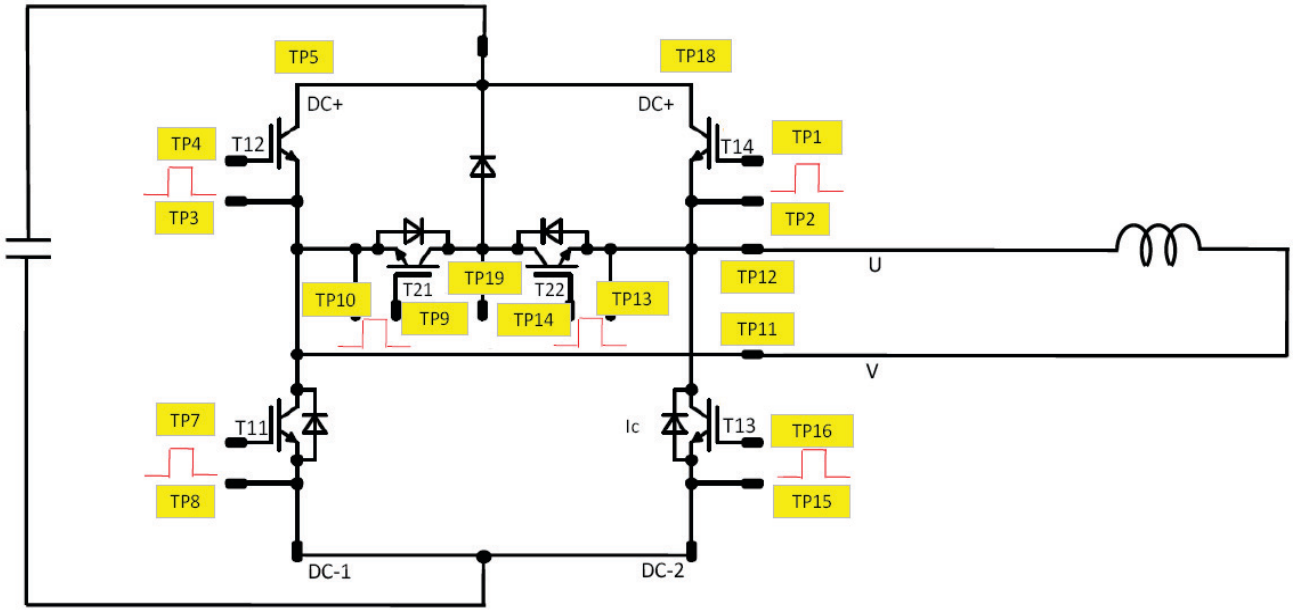
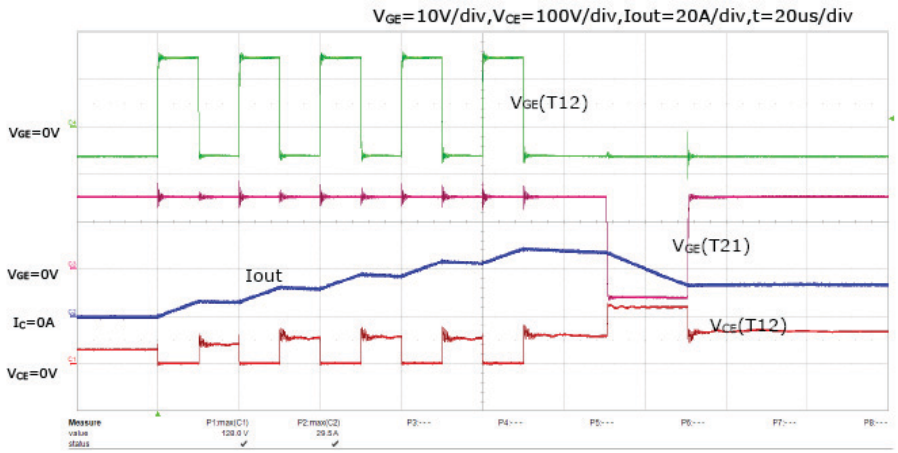


Figure 12 shows an example of the waveforms of IGBT, T12, andT21 and output current I_{OUT}.

Figure 12: Waveforms of 3-Level Operation



DC voltage=120V, V_{GE}=+15V/-6V,

Appendix A: References

1. “ACPL-352J 5.0 Amp Output Current IGBT and SiC/GaN MOSFET Gate Drive Optocoupler with Integrated Over Current Sensing, FAULT, GATE,and UVLO Status Feedback,” Broadcom Inc., pub-005603.
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3. "10-FY07HVA050S5-L984F08 Datasheet Rev1,” Vincotech.
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