ACPL-336J

Fuji Electric Small PIM Module (M728/M732) Evaluation Board

Reference Manual
Version 1.0

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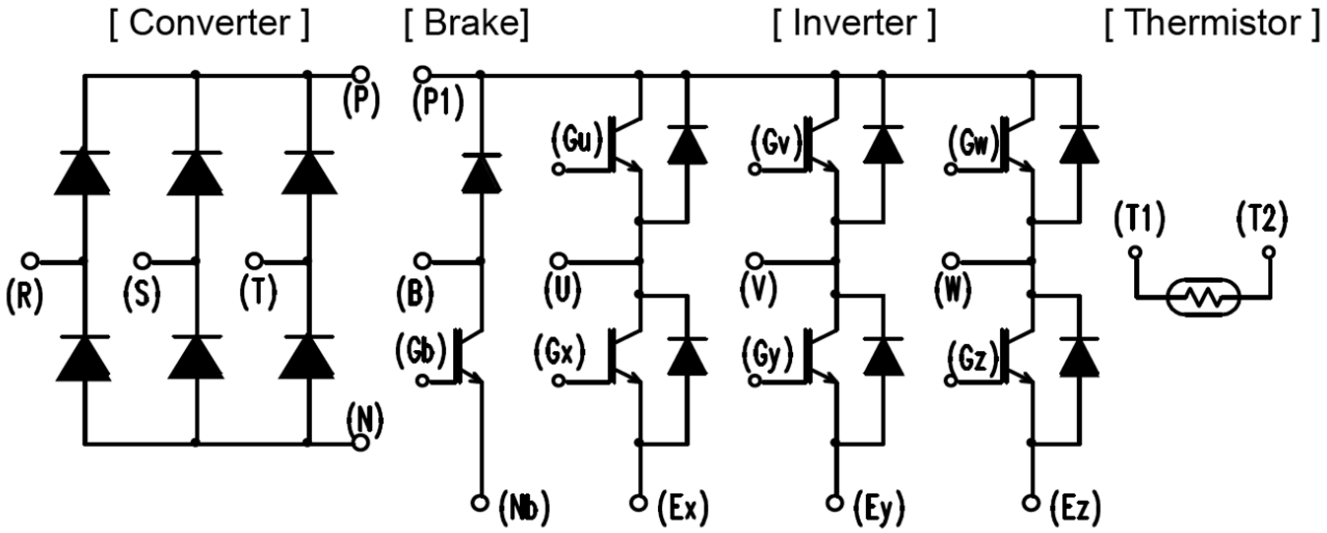
Chapter 1: Introduction

1.1 Power Integrated Module

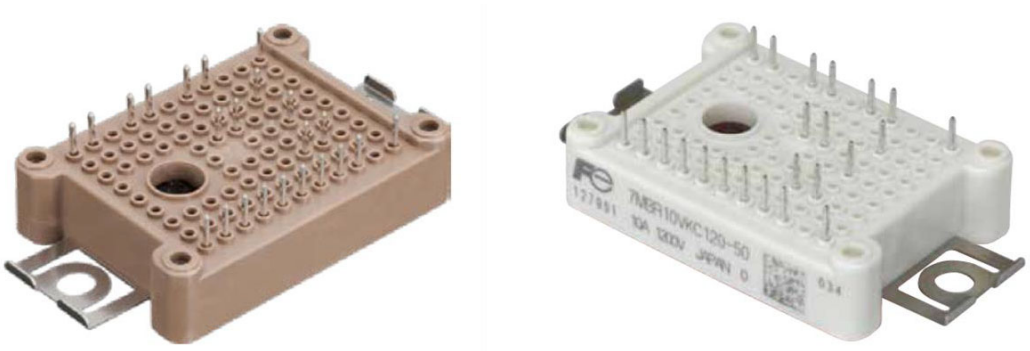
The Power Integrated Module (PIM) is a product that integrates a three-phase inverter circuit, a diode bridge circuit, and a braking circuit into a single module, making it possible to create a compact design for motor drive or uninterruptible power supply.

Figure 1: PIM Circuit Diagram



The evaluation board supports PIM module in small-capacity, compact and light-weight M728 and M732 package.

Figure 2: M728 and M732 Small Capacity PIM Package



M732 M728

M732 houses Fuji Electric 7th Generation IGBT (X Series) while M728 houses 6th Generation IGBT (V-series). Compared to the V-series, the latest X-series reduces power losses and contributes to energy saving. Maximum continuous operation temperature of X-series is also expanded from 150°C to 175°C.

M732 and M728 are available in the ratings shown in Table 1.

Table 1: Supported M728 and M732 Modules

Generation and Package	I_C	650V	1200V
7th Generation M732	10A	7MBR10XKC065-50	7MBR10XKC120-50
	15A	7MBR15XKC065-50	7MBR15XKC120-50
	20A	7MBR20XKC065-50	
	25A		7MBR25XKC120-50
	30A	7MBR30XKC065-50	
Generation and Package	**I_C**	**600V**	**1200V**
6th Generation M728	10A	7MBR10VKC060-50	7MBR10VKC120-50
	15A	7MBR15VKC060-50	7MBR15VKC120-50
	20A	7MBR20VKC060-50	
	30A	7MBR30VKC060-50	

Chapter 2: Description of the Evaluation Board

2.1 Board Description

Figure 3: Evaluation Board for Small PIM Module (M728/M732)

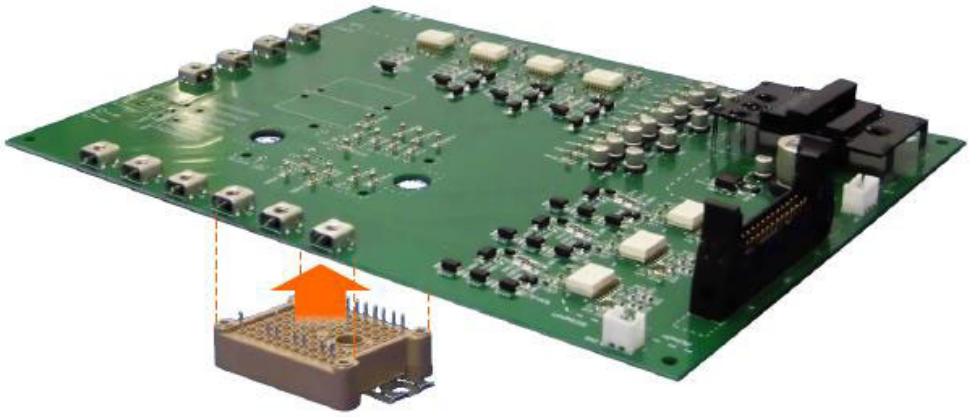


Figure 4 and Figure 5 show the layout of the evaluation board and the main circuit diagram.

Figure 4: Evaluation Board Layout

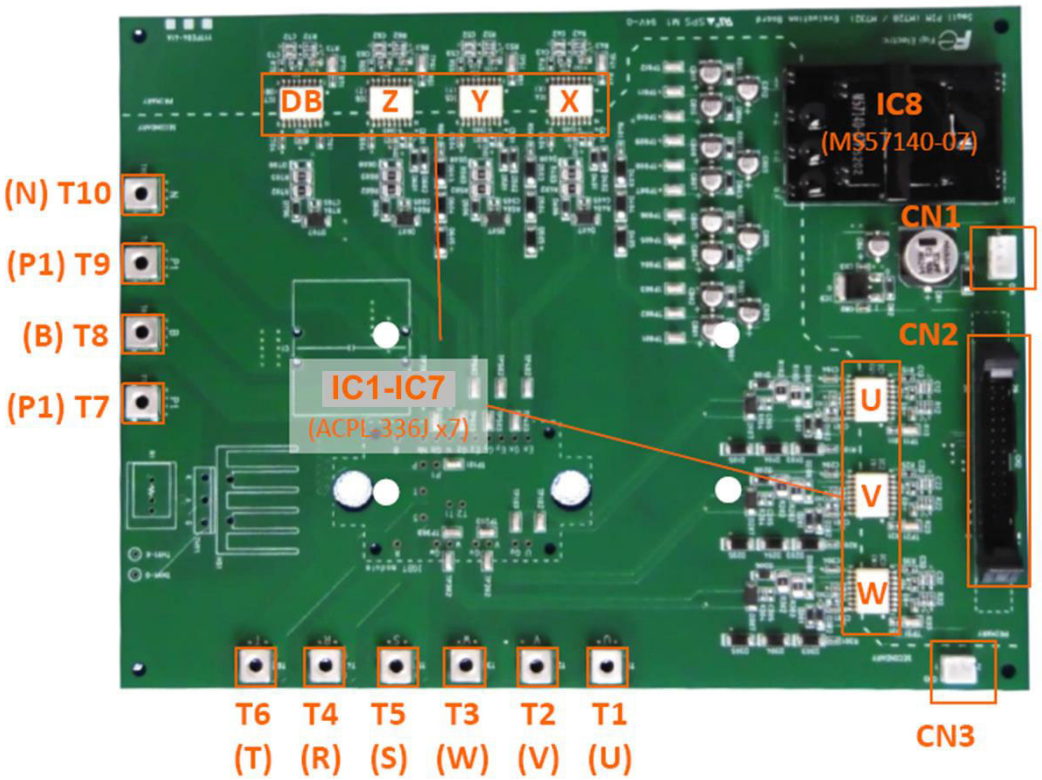
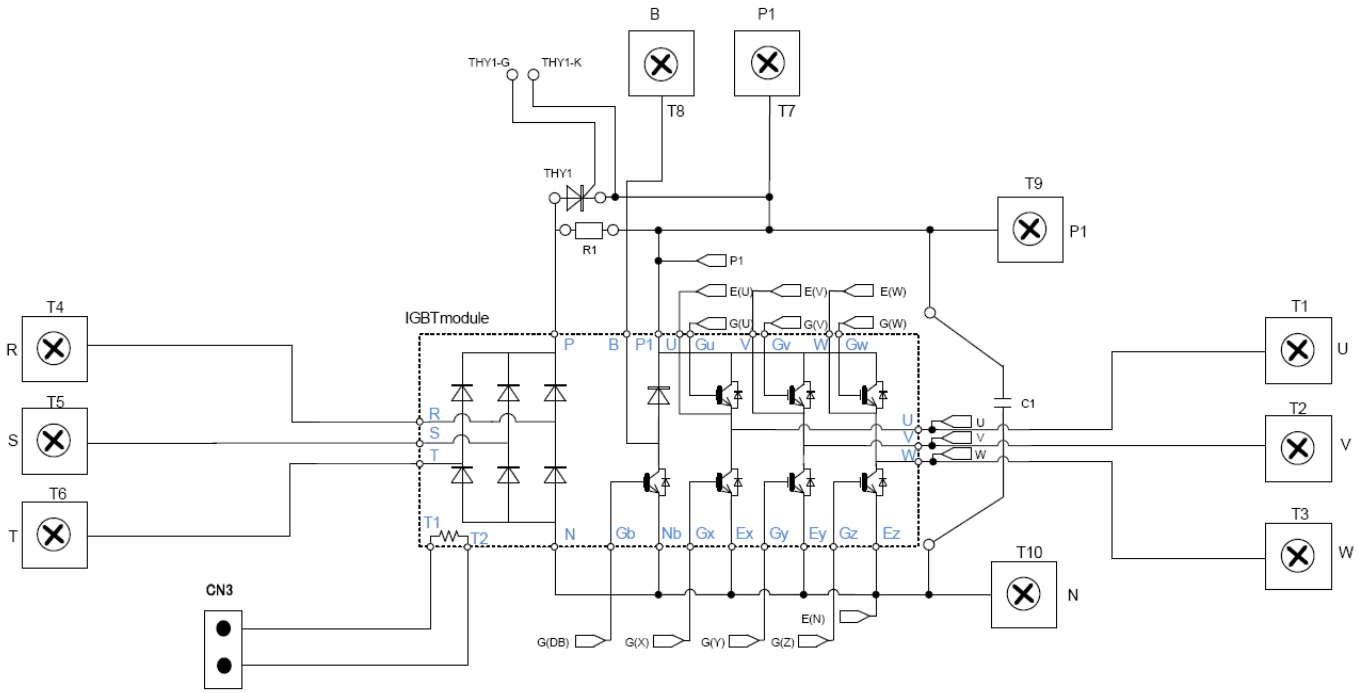


Figure 5: Evaluation Board Main Circuit Diagram



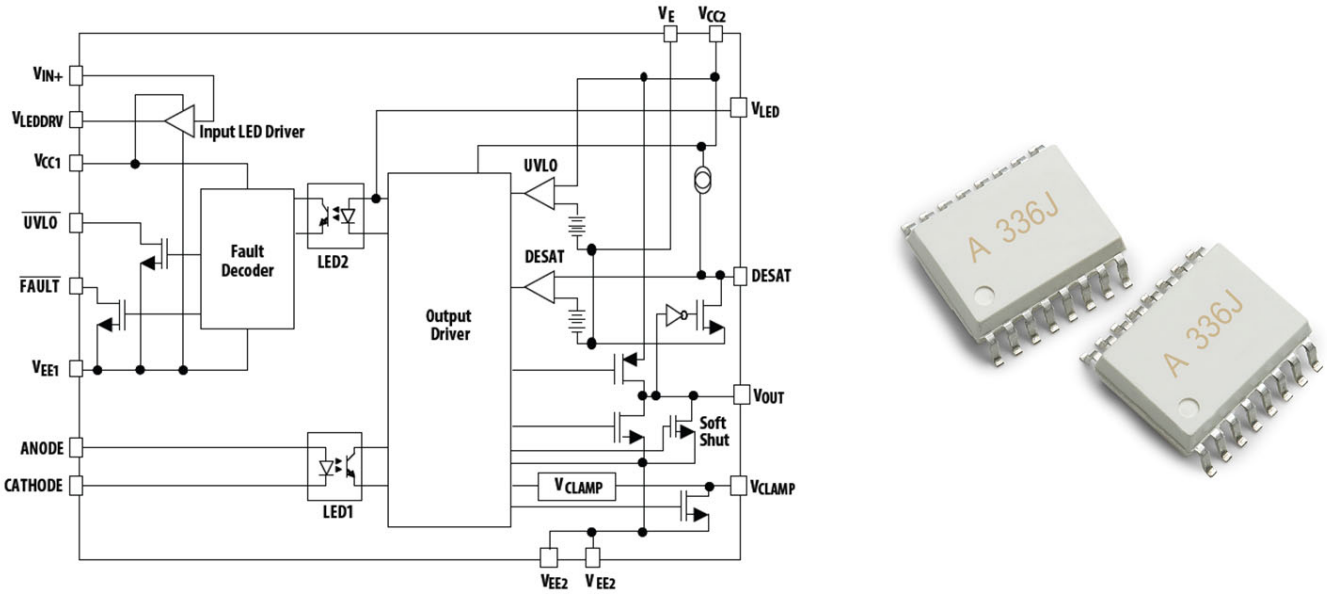
T4, T5, and T6 are the three-phase AC input terminals, R, S, and T. They are connected to the diode bridge circuit, which will rectify the AC input to DC+/DC- bus voltage. T1, T2, and T3 are the three-phase AC output terminals U, V, and W that can be connected to a three-phase motor. The DC+, DC-, and brake terminals can be accessed from terminals T7/T9, T10, and T8, respectively. The thermistor of the PIM can be accessed from NTC connector CN3. The PWM input signals from the controller board can be connected to the inverter using the 30-pin XG-Series flat cable PCB connector CN2. The fault signals from the ACPL-336J gate drive optocouplers are fed back to the controller using the same connector CN2.

Six ACPL-336J gate drive optocouplers, IC1 to IC6, are used to drive the six IGBTs of the three-phase inverter, and IC7 is used to drive the braking IGBT. The evaluation board has an isolated DC/DC power supply MS57140-07, IC8 to provide power for the gate drive optocouplers. The DC/DC power supply converts DC +20V from connector CN1 to +15V/–6V gate drive voltage.

The reference design describes the gate drive and isolated power supply designs and testing. Other details, such as the full schematic, bill of material, and PCB layouts can be found in Fuji Electric website:
http://www.fujielectric.com/products/semiconductor/model/igbt/evaluation/box/doc/pdf/MT5F36187_E.pdf

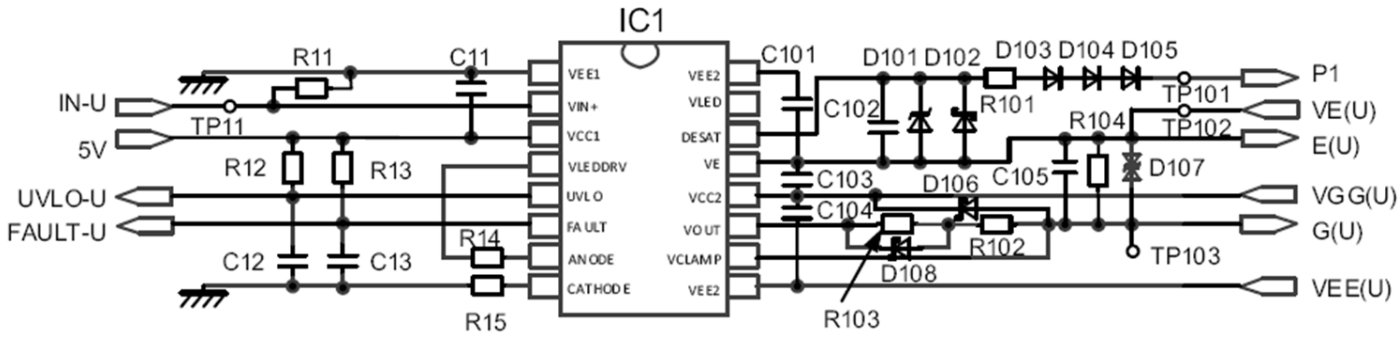
2.2 Gate Drive Design

Figure 6: Block Diagram of ACPL-336J and SO-16 Package



The ACPL-336J is a fully featured 2.5A smart gate drive optocoupler device capable of driving 600V, 650V, or 1200V, up to 100A IGBT directly. The device features rail-to-rail output, integrated LED driver, active Miller clamp, high desaturation (DESAT) blanking current source, and Under Voltage Lock-Out (ULVO) feedback control circuit, providing a complete cost-effective gate drive solution for motor control and power inverter applications. The ACPL-336J is available in a compact, surface-mountable SO-16 package with 8 mm of creepage and clearance. It provides the reinforced insulation certified by safety regulatory IEC/EN/DIN, UL, and CSA with working voltage of V_{IORM} = 1414V_{PEAK}.

Figure 7: ACPL-336J Gate Drive Circuit



The schematic shows the gate drive design for the top bridge, U-phase IGBT using ACPL-336J (IC1). Other phases (V and W), bottom bridge, and braking IGBTs use the same gate drive circuits.

The ACPL-336J has an integrated input LED driver with high impedance input (VIN+) for interfacing with the controller. The LED driver's output (VLEDDRV) must be connected with the recommended split resistors to LED1 to achieve the rated high CMR performance of more than 50kV/μs. If the LED driver is not used, LED1 can still be driven directly by other means of discrete driver configuration.

It is recommended that the two resistors (R14/R15) connected to input LED's anode and cathode are split in the ratio 1:1. They will help to balance the common mode impedances at the LED's anode and cathode. This helps to equalize the common mode voltage changes at the anode and cathode to give high CMR performance. In this case, R14 and R15 are 150Ω resistors to limit LED1 current to about 10 mA based on 5V VCC1 supply.

The primary side has two open drain FAULT and UVLO feedback outputs suitable for wired 'OR' applications. ACPL-336J monitors the output power supply constantly. When secondary side power supply is lower than undervoltage lockout (UVLO) threshold, the gate driver output will shut off to protect IGBT from low voltage bias. The low output power supply fault will be reported through the UVLO feedback. In this way, the UVLO feedback can also serve as a READY signal to the controller during power up. These open drain FAULT and UVLO outputs are connected to 10 kΩ pull-up resistors (R12/R13) and 330 pF filtering capacitors (C12/C13).

The supplies, VCC1 and VCC2 are connected to C11, C101, C103 and C104 (1 μF) bypass decoupling capacitors to provide the large transient currents necessary during a switching transition.

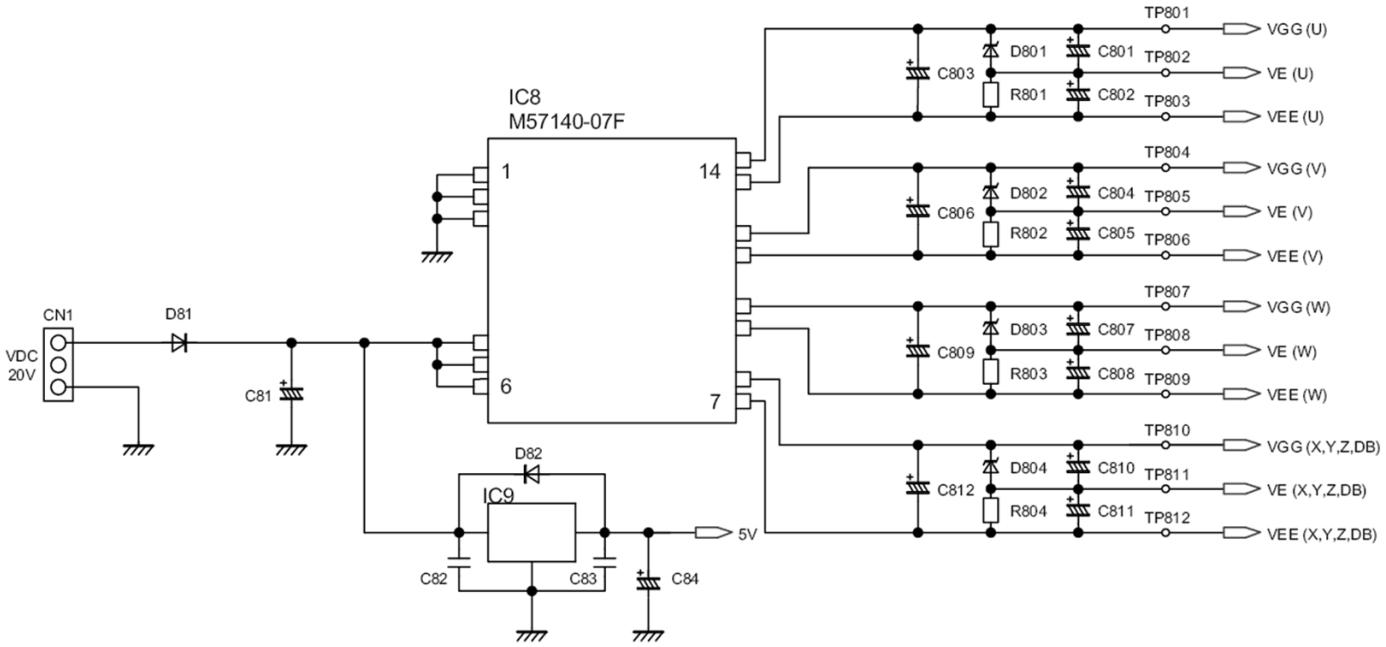
The ACPL-336J monitors the saturation (collector) voltage of the IGBT and triggers a local shutdown sequence if the collector voltage exceeds a predetermined threshold of 7V during short circuit or over current fault condition. The DESAT pin is connected to the collector of IGBT (P1) via 600V high voltage blocking diodes, D103, D104, D105, and resistor R101 (1 kΩ). Blanking capacitor, C102 (470 pF) is used to prevent false fault detection by filtering high frequency noise transient. The VCLAMP pin is connected directly to the gate of the IGBT and can sink 2.5A of parasitic Miller current during switching to prevent false turn on of the IGBT.

The gate resistors R102 (15Ω) and R103 (0Ω) serve to limit gate current and indirectly control the IGBT switching time. Diode, D108, is used to bypass resistor R103 and control the gate current and slew rate during IGBT gate discharging. It should be noted that the gate resistor must limit ACPL-336J peak output current to within 2.5A absolute maximum.

This negative going voltage spike is typically generated by inductive loads or reverse recovery spike of the IGBT freewheeling diodes. Zener diode, D101, and Schottky diode, D101, are used to prevent a false fault signal caused by positive and negative spikes.

2.3 DC/DC Power Supply Design

Figure 8: Schematic of the DC/DC Power Supply



M57140-07F is an isolated DC-to-DC converter with an input of DC 20V.It supplies four 21.5V outputs. Isolation is provided from primary to secondary (V_{ISO} 2.5 kV_{RMS}/min) and also between the secondary (V_{ISO} 1.5 kV_{RMS}/min). The 21.5V outputs are split into +15V and –6V supplies by 15V diodes D801 to D804. The +15V/–6V supplies are connected to the seven ACPL-336J to provide bipolar gate drive voltages.

IC9 is a TA7805F voltage regulator to regulate the 20V input to 5V supply for the primary side of the ACPL-336J.

Chapter 3: Evaluation Board Test and Result

3.1 Switching Waveform

The following figures show the turn on, turn off, and reverse recovery switching waveforms of the evaluation board with PIM 7MBR15VKC120-50. The PIM was tested with 600V DC bus voltage with collector and reverse recovery current at 30A. The gate resistors were adjusted from 15Ω to 39Ω for optimum switching performance without ringing.

Figure 9: Turn On Switching Waveforms

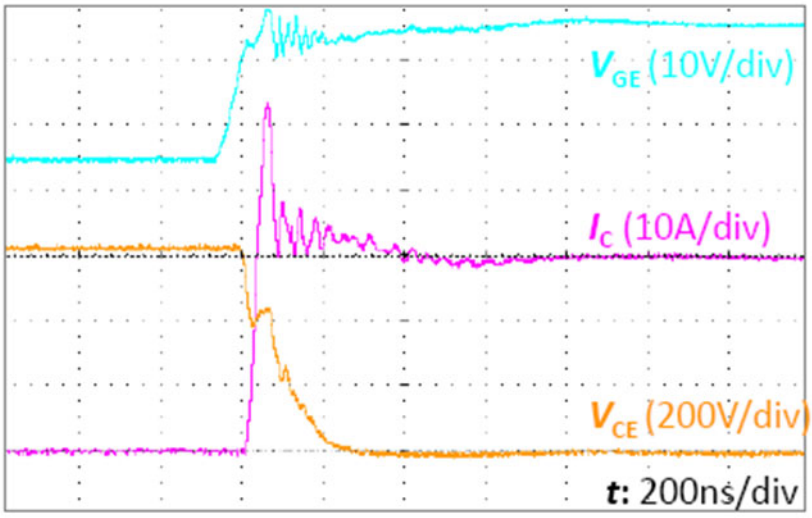


Figure 10: Turn Off Switching Waveforms

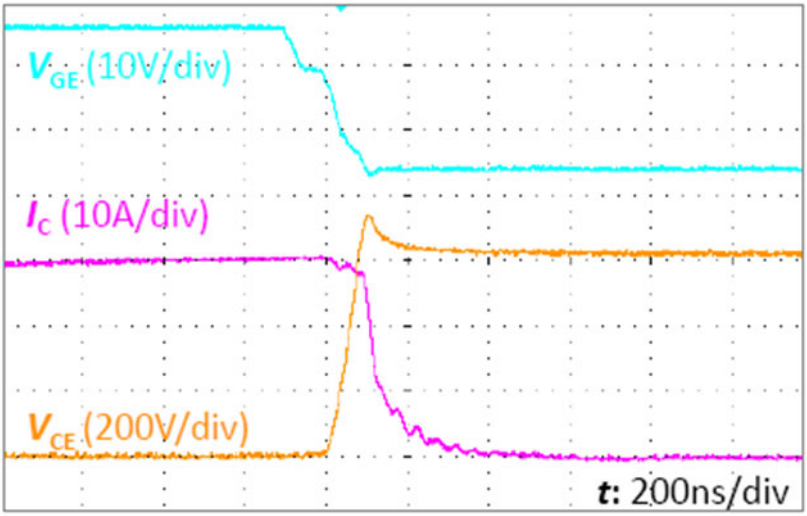
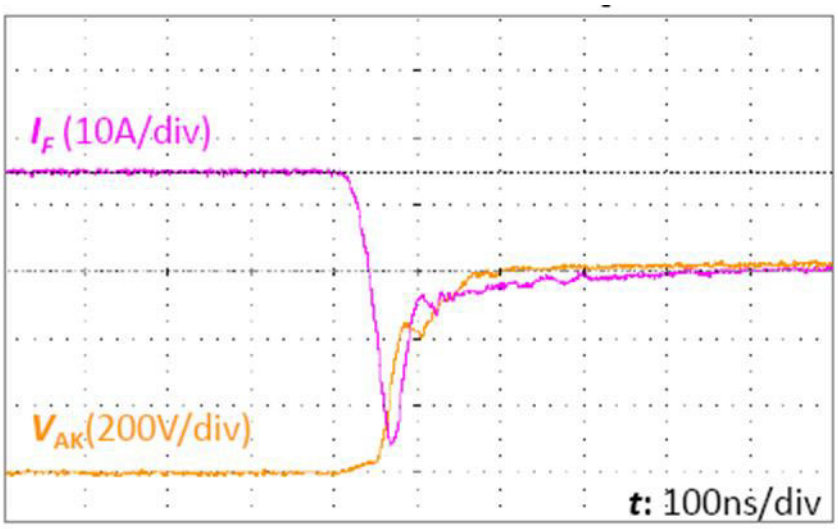


Figure 11: Reverse Recovery Waveforms



3.2 Short Circuit Protection (DESAT)

The following figures show the short circuit and FAULT report waveforms of the evaluation board with PIM 7MBR15VKC120-50. The PIM was tested with 800V DC bus voltage and short circuit current of about 75A. The DESAT of ACPL-336J was triggered causing the output or V_{GE} to soft shutdown. The primary side FAULT pin of the ACPL-336J was being pulled low, indicating a short circuit fault had occurred to the controller.

Figure 12: Short Circuit Waveforms

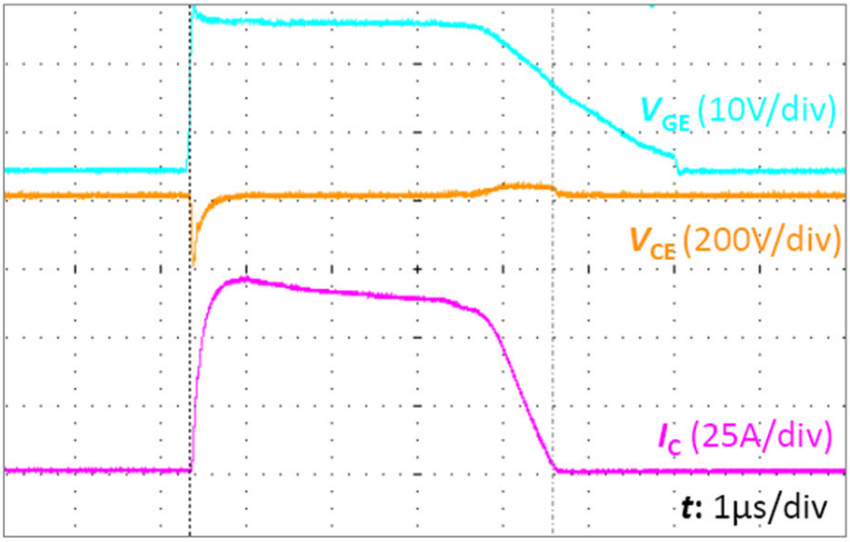
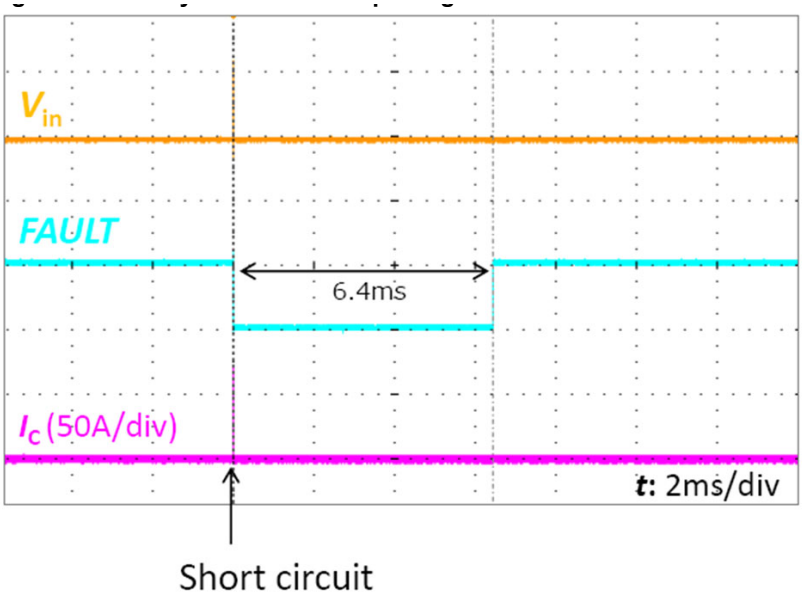


Figure 13: Primary Side FAULT Reporting Waveforms



Appendix A: References

1. ACPL-336J 2.5 Amp Gate Drive Optocoupler with Integrated (VCE) Desaturation Detection, Active Miller Clamping, Fault and UVLO Status Feedback," Broadcom Inc., AV02-4319EN.
   https://docs.broadcom.com/docs/AV02-4391EN
2. "Small PIM module (M728/M732)Evaluation Board," Fuji Electric MT5F36187.
   http://www.fujielectric.com/products/semiconductor/model/igbt/evaluation/box/doc/pdf/MT5F36187_E.pdf
3. "7MBR15VKC120-50 IGBT Module (V Series) 1200V/15A PIM Datasheet Rev1493b," Fuji Electric.
   http://www.fujielectric.com/products/semiconductor/model/igbt/pim.html
4. "M57140-07F Datasheet", Isahaya Electronics Corporation.

Revision History

Version 1.0, November 26, 2018

Initial document release.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