BROADCOM®

Data Sheet

# ACPL-334J/338J

## 3A IGBT Gate Drive Optocoupler with Integrated ($V_{CE}$) Desaturation Detection and FAULT Feedback, UVLO, and Active Miller Clamping

## Overview

The Broadcom® ACPL-334J/338J is an advanced 3A output current, easy-to-use, intelligent gate driver that makes IGBT protection compact, affordable, and easy to implement. Features such as integrated $V_{CE}$ detection, under-voltage lockout (UVLO), *soft* IGBT turn-off, isolated open collector fault feedback, and active Miller clamping provide maximum design flexibility and circuit protection.

The ACPL-334J/338J contains an AlGaAs LED. The LED is optically coupled to an integrated circuit with a power output stage. The ACPL-334J/338J is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The voltage and current supplied by this optocoupler make it ideally suited for directly driving IGBTs with ratings up to 1200V and 150A. For IGBTs with higher ratings, the ACPL-334J/338J can be used to drive a discrete power stage that drives the IGBT gate. The ACPL-334J/338J provides reinforced insulation, certified by safety regulatory UL, CSA, and IEC.

## Features

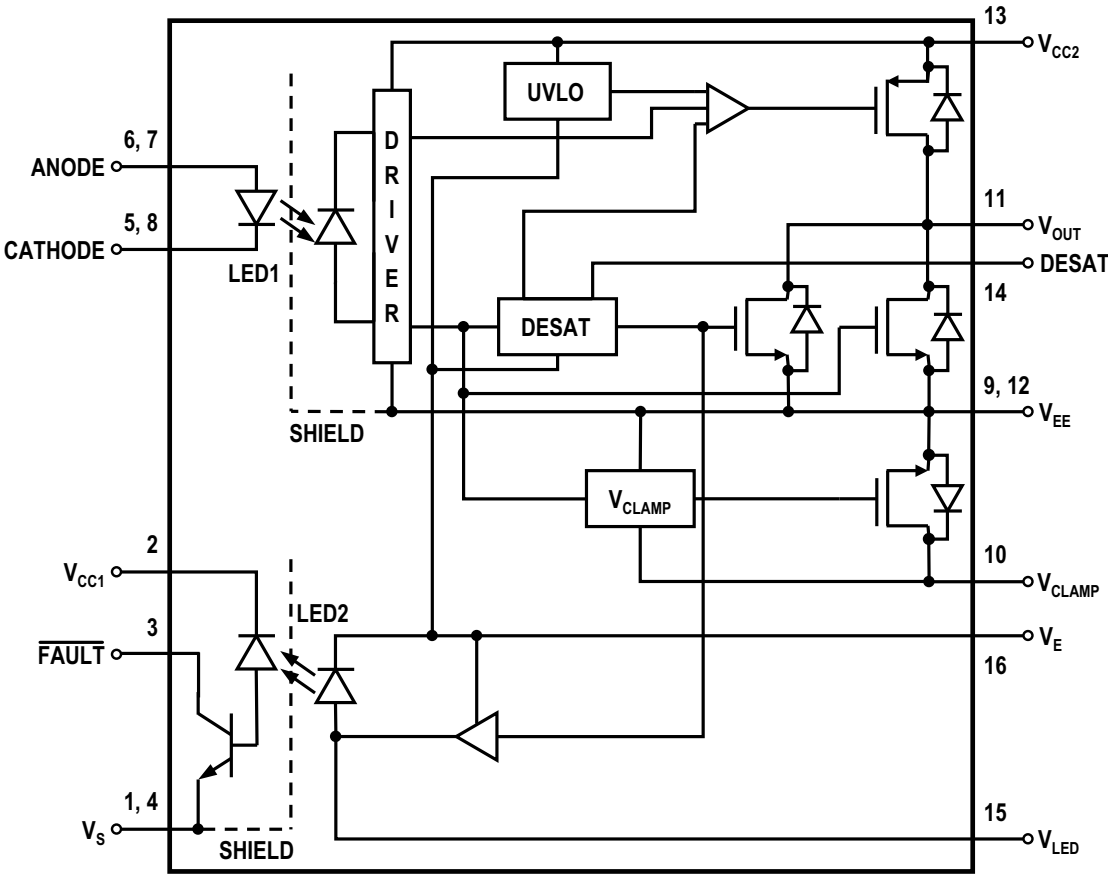
- 3A maximum peak output current
- 135-ns maximum propagation delay
- 1.7A active Miller clamp
- Desaturation detection with *soft* shutdown and FAULT feedback
- Under-voltage lockout (UVLO) with hysteresis
- Fault reset by next LED turn-on after mute time (ACPL-334J)
- Automatic fault reset after mute time of 32 µs (ACPL-338J)
- 100-kV/µs minimum common mode rejection (CMR) at $V_{CM}$ = 1500V
- 15V to 30V wide operating $V_{CC2}$ range
- –40°C to 125°C industrial temperature range
- SO16 package with 8.3-mm creepage and clearance
- Regulatory approvals:
  - UL1577 5 $kV_{RMS}$ for 1 minute
  - CSA
  - IEC 60747-5-5 $V_{IORM}$ = 1414 $V_{PEAK}$

## Applications

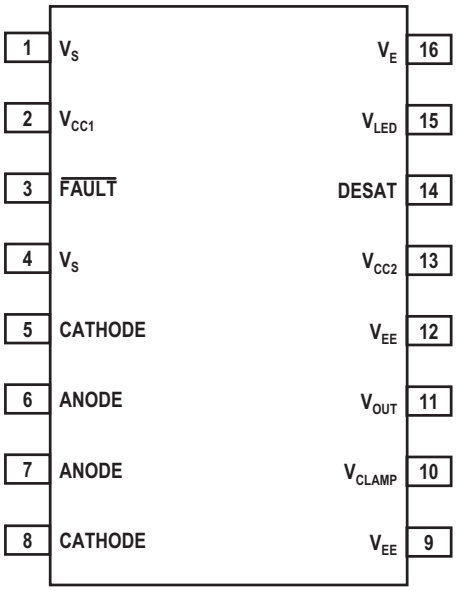
- Motor drive for industrial automation and robotics
- Power supply and charger
- Renewable energy inverter and storage

**CAUTION!** Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The component featured in this data sheet is not to be used in military or aerospace applications or environments. The component is also not AEC-Q100 qualified and not recommended for automotive applications.

# Functional Diagram



# Pin Description




| Pin | Symbol | Description |
|---|---|---|
| 1 | $V_S$ | Input ground. |
| 2 | $V_{CC1}$ | Positive input supply voltage (3.3V to 5.5V). |
| 3 | FAULT | Fault output. FAULT changes from a high impedance state to a logic low output within 0.8 µs of the voltage on the DESAT pin exceeding an internal reference voltage of 6.5V. FAULT is an open collector output that allows the FAULT outputs from all ACPL-334J/338J in the circuit to be wired OR together. This forms a single fault bus for interfacing directly to the microcontroller. |
| 4 | $V_S$ | Input ground. |
| 5 | CATHODE | Input LED cathode. |
| 6 | ANODE | Input LED anode. |
| 7 | ANODE | Input LED anode. |
| 8 | CATHODE | Input LED cathode. |
| 9 | $V_{EE}$ | Negative output power supply. |
| 10 | $V_{CLAMP}$ | Miller clamp. |
| 11 | $V_{OUT}$ | Driver output to turn on IGBT or MOSFET gate. |
| 12 | $V_{EE}$ | Negative output power supply. |
| 13 | $V_{CC2}$ | Positive output power supply. |
| 14 | DESAT | Desaturation voltage input. When the voltage on DESAT exceeds an internal reference voltage of 6.5V while the IGBT/MOSFET is on, the FAULT output is changed from logic high to low state within 0.8 µs. |
| 15 | $V_{LED}$ | LED anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.) |
| 16 | $V_E$ | Common (IGBT emitter) output supply voltage. |

# Ordering Information

| Part Number | Option (RoHS Compliant) | Package | Surface Mount | Tape and Reel | IEC/EN/DIN EN 60747-5-5 | Quantity |
|---|---|---|---|---|---|---|
| ACPL-334J/338J | -000E | SO-16 | X | | X | 45 per tube |
| | -500E | | X | X | X | 850 per reel |

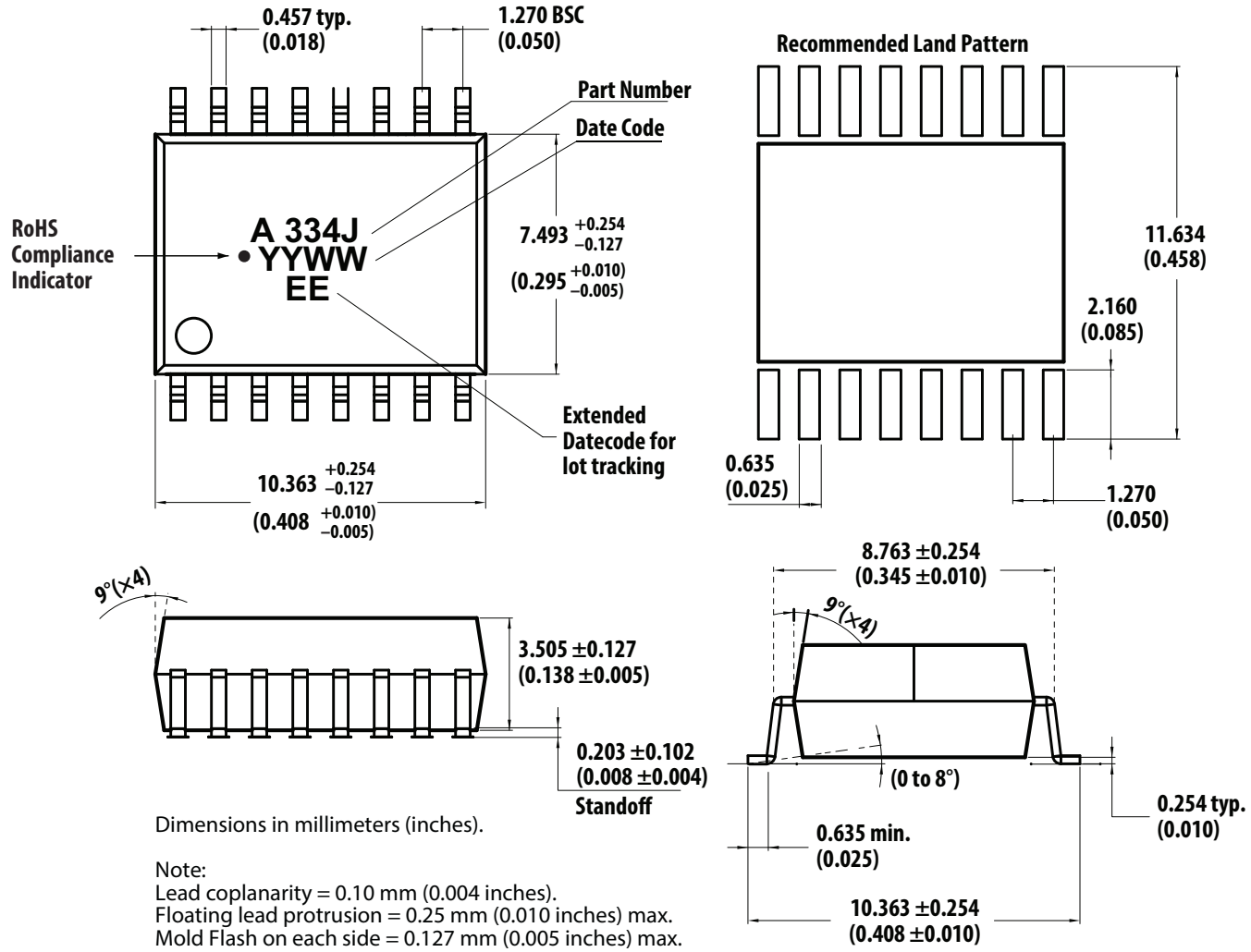
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

**Example:**

ACPL-334J-500E to order product of SO-16 surface-mount package in tape and reel packaging with IEC/EN/DIN EN 60747-5-5 safety approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

# Package Outline Drawing




Dimensions in millimeters (inches).

Note:
Lead coplanarity = 0.10 mm (0.004 inches).
Floating lead protrusion = 0.25 mm (0.010 inches) max.
Mold Flash on each side = 0.127 mm (0.005 inches) max.

# Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

# Regulatory Information

The ACPL-334J/338J is approved by the following organizations:

| | |
|---|---|
| UL | Approval under UL 1577, component recognition program up to $V_{ISO}$ = 5000 $V_{RMS}$ expected prior to product release. |
| CSA | Approval under CSA Component Acceptance Notice #5, File CA 88324. |
| IEC/EN/DIN EN 60747-5-5 | IEC 60747-5-5, EN 60747-5-5, DIN EN 60747-5-5. |

# IEC/EN/DIN EN60747-5-5 Insulation Characteristics

**NOTE:** Isolation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in application. Surface-mount classification is class A in accordance with CECCOO802.

| Description | Symbol | Characteristic | Unit |
|---|---|---|---|
| Insulation Classification per DIN VDE 0110/1.89, Table 1<br>For Rated Mains Voltage ≤ 600 $V_{RMS}$<br>For Rated Mains Voltage ≤ 1000 $V_{RMS}$ | — | <br>I – IV<br>I – III | — |
| Climatic Classification | — | 40/125/21 | — |
| Pollution Degree (DIN VDE 0110/1.89) | — | 2 | — |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 1414 | $V_{PEAK}$ |
| Input to Output Test Voltage, Method b [a]<br>$V_{IORM}$ × 1.875 = $V_{PR}$, 100% Production Test with $t_m$ = 1 second, Partial Discharge < 5 pC | $V_{PR}$ | 2652 | $V_{PEAK}$ |
| Input to Output Test Voltage, Method a [a]<br>$V_{IORM}$ × 1.6 = $V_{PR}$, Type and Sample Test, $t_m$ = 10 seconds, Partial Discharge < 5 pC | $V_{PR}$ | 2262 | $V_{PEAK}$ |
| Highest Allowable Overvoltage (Transient Overvoltage $t_{ini}$ = 60 seconds) | $V_{IOTM}$ | 8000 | $V_{PEAK}$ |
| Safety-Limiting Values – maximum values allowed in the event of a failure<br>Case Temperature<br>Input Power<br>Output Power | <br>$T_S$<br>$P_{S,INPUT}$<br>$P_{S,OUTPUT}$ | <br>175<br>400<br>1200 | <br>°C<br>mW<br>mW |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500V | $R_S$ | > $10^9$ | Ω |

a. Refer to the IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the *Broadcom Regulatory Guide to Isolation Circuits*, AV02-2041EN, for a detailed description of Method a and Method b partial discharge test profiles.

# Insulation and Safety Related Specifications

| Parameter | Symbol | Value | Unit | Conditions |
|---|---|---|---|---|
| Minimum External Air Gap (Clearance) | L(101) | 8.3 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (Creepage) | L(102) | 8.3 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | — | 0.5 | mm | Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector. |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | IIIa | | Material Group (DIN VDE 0110) |

**NOTE:** All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended land pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques, such as grooves and ribs, that may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

# Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | –55 | 150 | °C | |
| Operating Temperature | $T_A$ | –40 | 125 | °C | a |
| Output IC Junction Temperature | $T_J$ | — | 150 | °C | a |
| Average Input Current | $I_{F(AVG)}$ | — | 25 | mA | b |
| Peak Transient Input Current (<1 µs pulse width, 300 pps) | $I_{F(TRAN)}$ | — | 1.0 | A | |
| Reverse Input Voltage | $V_R$ | — | 5 | V | |
| High Peak Output Current | $I_{OH(PEAK)}$ | — | 3 | A | c |
| Low Peak Output Current | $I_{OL(PEAK)}$ | — | 3 | A | c |
| Positive Input Supply Voltage | $V_{CC1}$ | –0.5 | 7 | V | |
| FAULT Output Current | $I_{FAULT}$ | — | 8 | mA | |
| FAULT Pin Voltage | $V_{FAULT}$ | –0.5 | $V_{CC1}$ | V | |
| Total Output Supply Voltage | $(V_{CC2} – V_{EE})$ | –0.5 | 35 | V | |
| Negative Output Supply Voltage | $(V_E – V_{EE})$ | –0.5 | 15 | V | |
| Positive Output Supply Voltage | $(V_{CC2} – V_E)$ | –0.5 | $35 – (V_E – V_{EE})$ | V | |
| Gate Drive Output Voltage | $V_{O(PEAK)}$ | $V_{EE} – 0.5$ | $V_{CC2} + 0.5$ | V | |
| Peak Clamp Sinking Current | $I_{CLAMP}$ | — | 1.7 | A | |
| Miller Clamp Pin Voltage | $V_{CLAMP}$ | $V_{EE} – 0.5$ | $V_{CC2} + 0.5$ | V | |
| DESAT Voltage | $V_{DESAT}$ | $V_E – 0.5$ | $V_{CC2} + 0.5$ | V | |
| Output IC Power Dissipation | $P_O$ | — | 600 | mW | a |
| Input LED Power Dissipation | $P_I$ | — | 150 | mW | a |

a. To achieve the absolute maximum power dissipation specified, pins 1, 4, 9, and 12 require ground plane connections and might require airflow. See the Thermal Calculation section for details about how to estimate junction temperature and power dissipation. In most cases, the absolute maximum output IC junction temperature is the limiting factor. The actual power dissipation achievable will depend on the application environment (PCB layout, airflow, part placement, and so on). Output IC power dissipation is derated linearly at 20 mW/°C above 123°C for high conductivity board and at 14 mW/°C above 105°C for low conductivity board. Input IC power dissipation does not require derating.

b. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.

c. Maximum pulse width = 10 µs. The output must be limited to 3A of peak current by external resistors.

# Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Operating Temperature | $T_A$ | –40 | 125 | °C | |
| Total Output Supply Voltage | $(V_{CC2} – V_{EE})$ | 15 | 30 | V | |
| Negative Output Supply Voltage | $(V_E – V_{EE})$ | 0 | 15 | V | |
| Positive Output Supply Voltage | $(V_{CC2} – V_E)$ | 15 | $30 – (V_E – V_{EE})$ | V | |
| Input Current (ON) | $I_{F(ON)}$ | 8 | 12 | mA | |
| Input Voltage (OFF) | $V_{F(OFF)}$ | –3.6 | 0.8 | V | |

# Electrical Specifications (DC)

All typical values at $T_A$ = 25°C, $V_{CC2} – V_{EE}$ = 30V, $V_E$ - $V_{EE}$ = 0V. All minimum and maximum specifications are at recommended operating conditions, unless otherwise noted.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| FAULT Logic Low Output Voltage | $V_{FAULT}$ | — | 0.06 | 0.4 | V | $I_{FAULT}$ = 1.1 mA, $V_{CC1}$ = 5.5V | | |
| | | — | 0.06 | 0.4 | V | $I_{FAULT}$ = 1.1 mA, $V_{CC1}$ = 3.3V | | |
| FAULT Logic High Output Current | $I_{FAULTH}$ | — | 0.01 | 0.5 | µA | $V_{FAULT}$ = 5.5V, $V_{CC1}$ = 5.5V | | |
| | | — | 0.004 | 0.3 | µA | $V_{FAULT}$ = 3.3V, $V_{CC1}$ = 3.3V | | |
| $V_{OUT}$ High Level Peak Output Current | $I_{OH}$ | 2 | 2.6 | — | A | $V_{CC2} – V_{OUT}$ = 15V | 4 | a |
| $V_{OUT}$ Low Level Peak Output Current | $I_{OL}$ | 2 | 3 | — | A | $V_{OUT} – V_{EE}$ = 15V | 5 | a |
| $V_{OUT}$ Low Level Output Current During Fault Condition | $I_{OLF}$ | 90 | 145 | 230 | mA | $V_{OUT} – V_{EE}$ = 14V | 6 | |
| $V_{OUT}$ High Level Output Voltage | $V_{OH}$ | $V_{CC2}$ – 0.60 | $V_{CC2}$ – 0.3 | — | V | $I_{OH}$ = –100 mA, $I_F$ = 10 mA | 2 | b, c |
| $V_{OUT}$ Low Level Output Voltage | $V_{OL}$ | — | $V_{EE}$ + 0.12 | $V_{EE}$ + 0.60 | V | $I_{OL}$ = 100 mA, $V_F$ = 0V | 3 | |
| Clamp Threshold Voltage | $V_{TH\_CLAMP}$ | — | 1.85 | 2.2 | V | | | |
| Clamp Low Level Sinking Current | $I_{CLAMP}$ | 0.35 | 1 | — | A | $V_{CLAMP}$ = $V_{EE}$ + 2.5V | 7 | |
| Clamp Low Level Peak Sinking Current | $I_{CLAMPPK}$ | — | 1.6 | — | A | $V_{CLAMP}$ = $V_{EE}$ + 10V | | |
| High Level Output Supply Current ($V_{CC2}$) | $I_{CC2H}$ | — | 5 | 8 | mA | $I_F$ = 10 mA, No Load | 8 | |
| Low Level Output Supply Current ($V_{CC2}$) | $I_{CC2L}$ | — | 4 | 8 | mA | $V_F$ = 0V, No Load | 8 | |
| Output Supply Current during DESAT FAULT ($V_{CC2}$) | $I_{CC2\_FAULT}$ | — | 18 | — | mA | $I_F$ = 10 mA, $V_{DESAT}$ = 7V | | |
| Blanking Capacitor Charging Current | $I_{CHG}$ | 0.9 | 1 | 1.1 | mA | $V_{DESAT}$ = 2V | 12 | c, d |
| Blanking Capacitor Discharge Current | $I_{DSCHG}$ | 10 | 30 | — | mA | $V_{DESAT}$ = 7V | 13 | c, d |
| DESAT Sensing Voltage Threshold | $V_{DESAT}$ | 6 | 6.5 | 7 | V | $V_{CC2} – V_E > V_{UVLO+}$ | 11 | c |
| UVLO Threshold, $V_{CC2} – V_E$ | $V_{UVLO+}$ | 10.5 | 11.5 | 12.5 | V | $I_F$ = 10 mA, $V_{OUT} – V_E$ > 5V | | b, c, e |
| | $V_{UVLO–}$ | 9.5 | 10.5 | 11.5 | V | $I_F$ = 10 mA, $V_{OUT} – V_E$ < 5V | | b, c, f |
| UVLO Hysteresis, $V_{CC2} – V_E$ | $V_{UVLO+} – V_{UVLO–}$ | 0.5 | 1 | — | V | | | |
| Input Threshold Current Low to High | $I_{FLH}$ | 0.5 | 2.2 | 6.5 | mA | | 9, 10 | |
| Input Threshold Voltage High to Low | $V_{FHL}$ | 0.8 | — | — | V | | | |
| Input Forward Voltage | $V_F$ | 1.2 | 1.6 | 1.95 | V | $I_F$ = 10 mA | | |
| Temperature Coefficient of Input Forward Voltage | $\Delta V_F/\Delta T_A$ | — | –1.3 | — | mV/°C | $I_F$ = 10 mA | | |
| Input Reverse Breakdown Voltage | $BV_R$ | 5 | — | — | V | $I_R$ = 100 mA | | |
| Input Capacitance | $C_{IN}$ | — | 70 | — | pF | f = 1 MHz, $V_F$ = 0V | | |

a. Output is sourced at 2A with a maximum pulse width = 10 µs.

b. 15V is the recommended minimum operating positive supply voltage ($V_{CC2} – V_E$) to ensure adequate margin in excess of the maximum $V_{UVLO+}$ threshold of 12.5V. For High Level Output Voltage testing, $V_{OUT}$ is measured with a 50-µs pulse load current. When driving capacitive loads, $V_{OUT}$ will approach $V_{CC2}$ as $I_{OUT}$ approaches zero units.

c. Once the system is out of UVLO ($V_{CC2} – V_E > V_{UVLO+}$), the DESAT detection feature of the ACPL-334J/338J will be the primary source of IGBT/MOSFET protection. The UVLO must be unlocked to ensure DESAT is functional. Once $V_{CC2}$ exceeds the $V_{UVLO+}$ threshold, DESAT will remain functional until $V_{CC2}$ is below the $V_{UVLO–}$ threshold. The DESAT detection and UVLO features of the ACPL-334J/338J work in conjunction to ensure constant IGBT/MOSFET protection.

d. See DESAT Fault Detection Blanking Time for further details.

e. This is the *increasing* (that is, turn-on or *positive-going* direction) of $V_{CC2} – V_E$.

f. This is the *decreasing* (that is, turn-off or *negative-going* direction) of $V_{CC2} – V_E$.

# Switching Specifications (AC)

All typical values at $T_A$ = 25°C, $V_{CC2}$ – VE = 30V, $V_E – V_{EE}$ = 0V. All minimum and maximum specifications are at recommended operating conditions, unless otherwise noted.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to High $V_{OUT}$ Output Level | $t_{PLH}$ | 35 | 60 | 135 | ns | $R_G$ = 10Ω, $C_G$ = 10 nF, f = 10 kHz, Duty Cycle = 50%, $V_{IN}$ = 5V, $R_{IN}$ = 330Ω | 1, 14 | a |
| Propagation Delay Time to Low $V_{OUT}$ Output Level | $t_{PHL}$ | 35 | 67 | 135 | ns | | | b |
| Pulse Width Distortion | PWD | –30 | 7.5 | 30 | ns | | | c |
| Propagation Delay Difference Between Any Two Parts | PDD ($t_{PLH} – t_{PHL}$) | –25 | — | 5 | ns | | | d |
| Propagation Delay Skew | $t_{PSK}$ | — | — | 15 | ns | | | e |
| 20% to 80% Rise Time on $V_{OUT}$ | $t_R$ | — | 20 | | ns | | | |
| 80% to 20% Fall Time on $V_{OUT}$ | $t_F$ | — | 10 | | ns | | | |
| DESAT Sense to 90% $V_{OUT}$ Delay | $t_{DESAT(90\%)}$ | — | 0.25 | 0.5 | µs | $R_G$ = 10Ω, $C_G$ = 10 nF, f = 10 kHz, Duty Cycle = 50%, $V_{IN}$ = 5V, $R_{IN}$ = 330Ω, $C_F$ = 330 pF, $R_F$ = 2.1 kΩ, $C_{BLANK}$ = 330 pF | 15, 20, 21 | f |
| DESAT Sense to 10% $V_{OUT}$ Delay | $t_{DESAT(10\%)}$ | — | 2 | 3 | µs | | 16, 17, 18, 20, 21 | g |
| DESAT Sense to Low Level FAULT Signal Delay | $t_{DESAT(FAULT)}$ | — | 0.45 | 0.8 | µs | | 20, 21 | h |
| DESAT Sense to DESAT Low Propagation Delay | $t_{DESAT(LOW)}$ | — | 0.35 | — | µs | | 20, 21 | i |
| DESAT Mute Time | $t_{DESAT(MUTE)}$ (ACPL-334J) | 4.5 | 6.5 | — | µs | | 20, 21 | j |
| | $t_{DESAT(MUTE)}$ (ACPL-338J) | 22 | 32 | 42 | | | | k |
| RESET to High Level FAULT Signal Delay | $t_{RESET(FAULT)}$ (ACPL-334J) | 0.3 | 1.1 | 2.2 | µs | $C_F$ = 330 pF, $R_F$ = 2.1 kΩ, $V_{CC1}$ = 5.5V | 20 | |
| | | 0.5 | 1.7 | 3.2 | µs | $C_F$ = 330 pF, $R_F$ = 2.1 kΩ, $V_{CC1}$ = 3.3V | | |

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| Output High Level Common Mode Transient Immunity | $\|CM_H\|$ | 100 | — | — | kV/µs | $T_A$ = 25°C, $V_{CM}$ = 1500V, $V_{CC1}$ = 5V, $C_F$ = 330 pF, $R_F$ = 2.1 kΩ, $I_F$ = 10 mA | | l, m |
| Output Low Level Common Mode Transient Immunity | $\|CM_L\|$ | 100 | — | — | kV/µs | $T_A$ = 25°C, $V_{CM}$ = 1500V, $V_{CC1}$ = 5V, $C_F$ = 330 pF, $R_F$ = 2.1 kΩ, $V_F$ = 0V | | n, m |

a. $t_{PLH}$ is defined as propagation delay from 50% of LED input $I_F$ to 50% of $V_{OUT}$ high level output.

b. $t_{PHL}$ is defined as propagation delay from 50% of LED input $I_F$ to 50% of $V_{OUT}$ low level output.

c. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given unit.

d. Propagation Delay Difference (PDD) is the difference between $t_{PHL}$ and $t_{PLH}$ between any two units under the same test condition.

e. Propagation Delay Skew ($t_{PSK}$) is the difference in $t_{PHL}$ or $t_{PLH}$ between any two units under the same test condition.

f. The amount of time from when DESAT threshold is exceeded to 90% of $V_{OUT}$ at mentioned test conditions.

g. The amount of time from when DESAT threshold is exceeded to 10% of $V_{OUT}$ at mentioned test conditions.

h. The amount of time from when DESAT threshold is exceeded to FAULT output low.

i. The amount of time from when DESAT threshold is exceeded to 50% of DESAT low voltage.

j. The amount of time when DESAT threshold is exceeded, output is muted to LED input. The fault mechanism can be reset by the next LED turn-on after the 4.5-µs (minimum) mute time. See the description of operation topic in the FAULT Reset section.

k. The amount of time when DESAT threshold is exceeded, output is muted to LED input. The fault mechanism will automatically reset the FAULT pin after a fixed mute time of 32 µs (typical). See the description of operation topic in the FAULT Reset section.

l. Common mode transient immunity in the high state is the maximum tolerable $dV_{CM}/dt$ of the common mode pulse, $V_{CM}$, to ensure that the output will remain in the high state (that is, $V_{CC2} - V_{OUT} < 1.0V$ or FAULT > 2V). $V_{DD2}$ must be higher than $V_{UVLO+}$.

m. Split resistor network in the ratio 2:1 with 226Ω at the anode and 113Ω at the cathode.

n. Common mode transient immunity in the low state is the maximum tolerable $dV_{CM}/dt$ of the common mode pulse, $V_{CM}$, to ensure that the output will remain in a low state (that is, $V_{OUT} - V_{EE} < 1.0V$ or FAULT > 2V). $V_{CC2}$ must be higher than $V_{UVLO+}$.

# Package Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| Input-Output Momentary Withstand Voltage | $V_{ISO}$ | 5000 | — | — | $V_{RMS}$ | $R_H$ < 50%, t = 1 min. $T_A$ = 25°C | a, b, c |
| Resistance (Input-Output) | $R_{I-O}$ | — | $10^9$ | — | Ω | $V_{I-O}$ = 500 $V_{DC}$ | c |
| Capacitance (Input-Output) | $C_{I-O}$ | — | 1.3 | — | pF | f = 1 MHz | |
| **High Conductivity Board** | | | | | | | |
| Junction to Ambient Thermal Resistance of: | | | | | °C/W | | d |
| Input IC Due to Heating of Input IC | $R_{11}$ | — | 79.15 | — | | | |
| Input IC Due to Heating of LED1 | $R_{12}$ | — | 24.11 | — | | | |
| Input IC Due to Heating of Output IC | $R_{13}$ | — | 18.83 | — | | | |
| Input IC Due to Heating of LED2 | $R_{14}$ | — | 28.77 | — | | | |
| Input LED1 Due to Heating of Input IC | $R_{21}$ | — | 21.71 | — | | | |
| Input LED1 Due to Heating of LED1 | $R_{22}$ | — | 121.2 | — | | | |
| Input LED1 Due to Heating of Output IC | $R_{23}$ | — | 25.96 | — | | | |
| Input LED1 Due to Heating of LED2 | $R_{24}$ | — | 19.62 | — | | | |
| Output IC Due to Heating of Input IC | $R_{31}$ | — | 13.21 | — | | | |
| Output IC Due to Heating of LED1 | $R_{32}$ | — | 19.22 | — | | | |
| Output IC Due to Heating of Output IC | $R_{33}$ | — | 43.42 | — | | | |
| Output IC Due to Heating of LED2 | $R_{34}$ | — | 16.94 | — | | | |
| Input LED2 Due to Heating of Input IC | $R_{41}$ | — | 30.78 | — | | | |
| Input LED2 Due to Heating of LED1 | $R_{42}$ | — | 21.44 | — | | | |
| Input LED2 Due to Heating of Output IC | $R_{43}$ | — | 23.35 | — | | | |
| Input LED2 Due to Heating of LED2 | $R_{44}$ | — | 120.7 | — | | | |
| **Low Conductivity Board** | | | | | | | |
| Junction to Ambient Thermal Resistance of: | | | | | °C/W | | d |
| Input IC Due to Heating of Input IC | $R_{11}$ | — | 130.3 | — | | | |
| Input IC Due to Heating of LED1 | $R_{12}$ | — | 56.07 | — | | | |
| Input IC Due To Heating of Output IC | $R_{13}$ | — | 50.85 | — | | | |
| Input IC Due to Heating of LED2 | $R_{14}$ | — | 67.37 | — | | | |
| Input LED1 Due to Heating of Input IC | $R_{21}$ | — | 54.84 | — | | | |
| Input LED1 Due to Heating of LED1 | $R_{22}$ | — | 156.5 | — | | | |
| Input LED1 Due to Heating of Output IC | $R_{23}$ | — | 60.81 | — | | | |
| Input LED1 Due to Heating of LED2 | $R_{24}$ | — | 51.46 | — | | | |
| Output IC Due to Heating of Input IC | $R_{31}$ | — | 35.54 | — | | | |
| Output IC Due to Heating of LED1 | $R_{32}$ | — | 42.64 | — | | | |
| Output IC Due to Heating of Output IC | $R_{33}$ | — | 71.91 | — | | | |
| Output IC Due to Heating of LED2 | $R_{34}$ | — | 40.73 | — | | | |
| Input LED2 Due to Heating of Input IC | $R_{41}$ | — | 68.48 | — | | | |
| Input LED2 Due to Heating of LED1 | $R_{42}$ | — | 50.75 | — | | | |
| Input LED2 Due to Heating of Output IC | $R_{43}$ | — | 56.86 | — | | | |
| Input LED2 Due to Heating of LED2 | $R_{44}$ | — | 163.9 | — | | | |

a. In accordance with UL1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 $V_{RMS}$ for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in the IEC/EN/DIN EN60747-5-5 Insulation Characteristics table, if applicable.

b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or the IEC/EN/DIN EN60747-5-5 Insulation Characteristics table.

c. The device is considered a two-terminal device: Pins 1 to 8 are shorted together, and pins 9 to 16 are shorted together.

d. The device was mounted on thermal conductivity test board per JEDEC 51-7. For further details, see the Thermal Calculation section.

**Figure 1: $V_{OUT}$ Propagation Delay Waveforms**

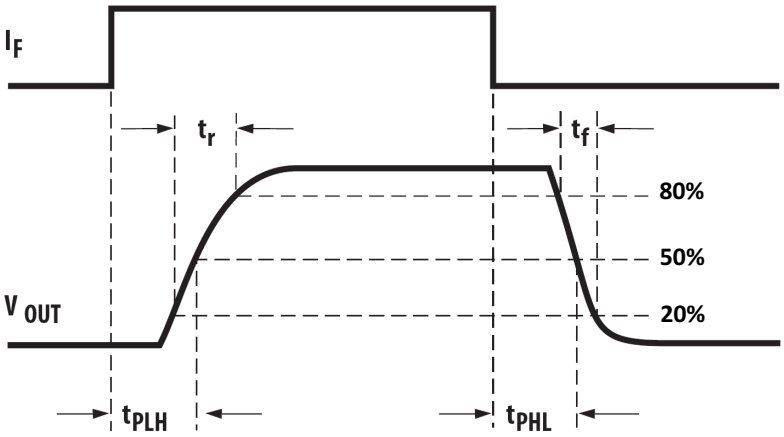


**Figure 2: $V_{OH}$ vs. Temperature**

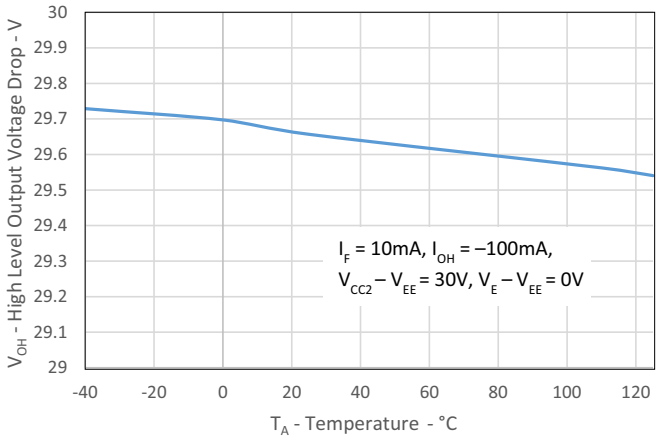



**Figure 3: $V_{OL}$ vs. Temperature**

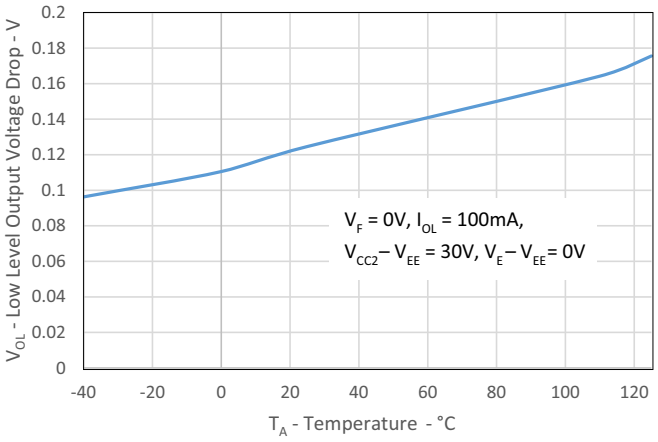



**Figure 4: $I_{OH}$ vs. $V_{OH}$**

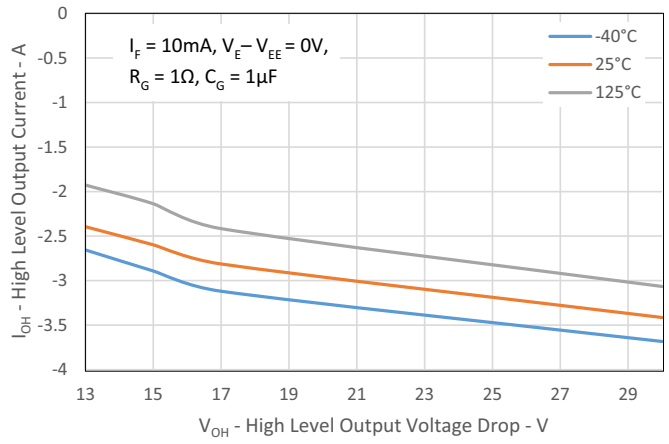



**Figure 5: $I_{OL}$ vs. $V_{OL}$**

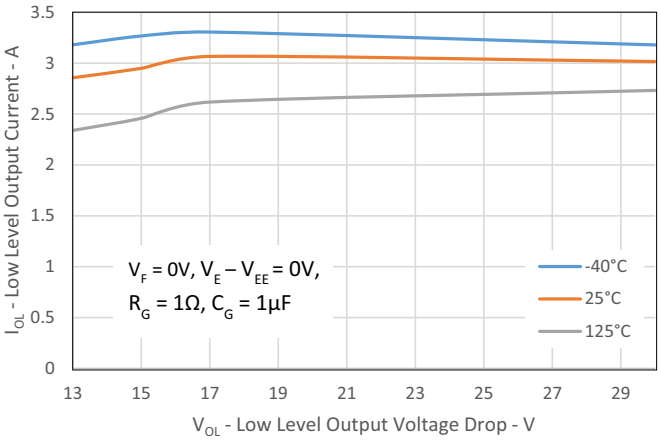



**Figure 6: $I_{OLF}$ vs. $V_{OUT}$**

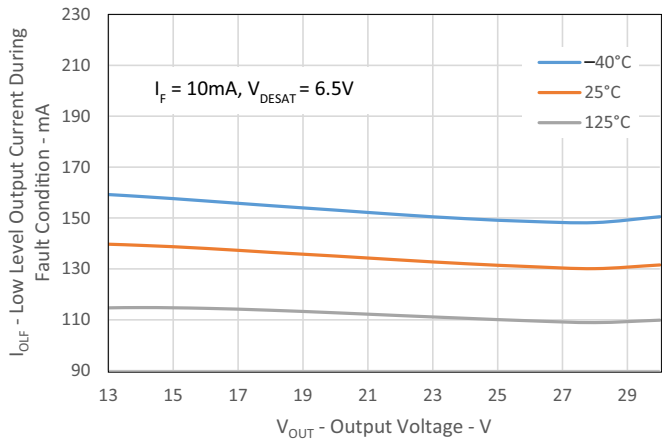



**Figure 7: $I_{CLAMP}$ vs. Temperature**

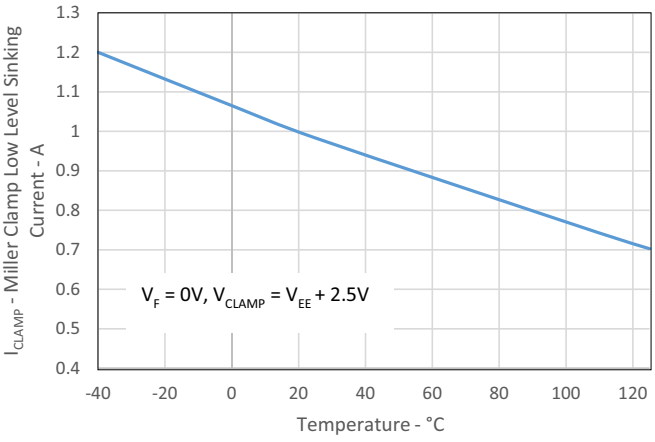


**Figure 8: $I_{CC2H}/I_{CC2L}$ vs. Temperature**

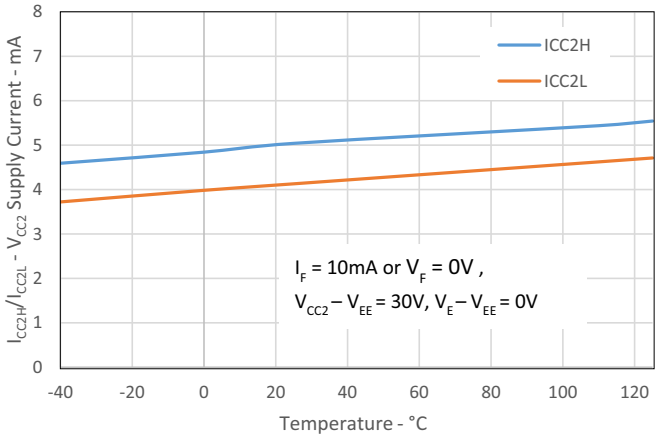



**Figure 9: $V_{OUT}$ vs. $I_F$**

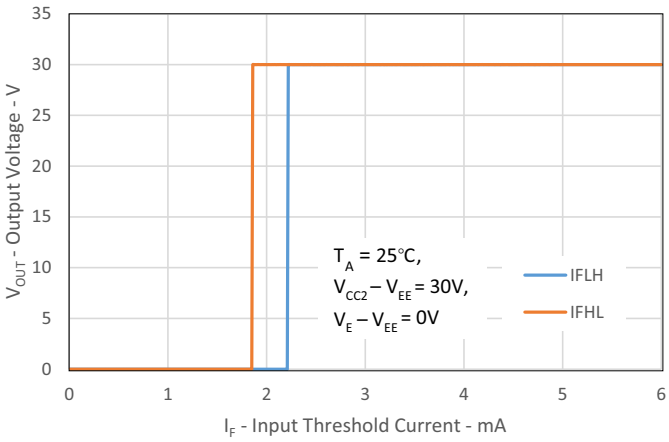



**Figure 10: $I_{FLH}$ vs. Temperature**

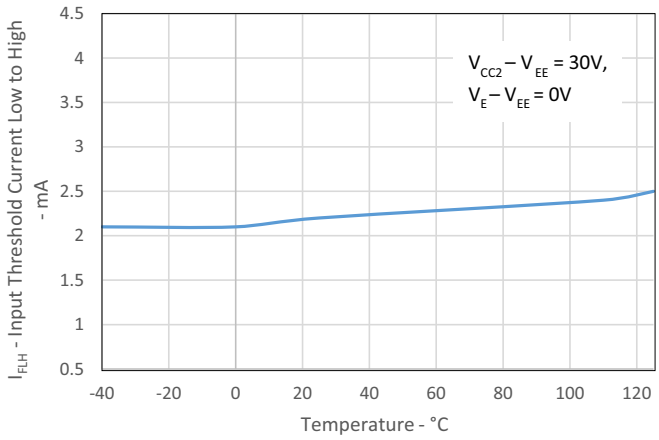



**Figure 11: $V_{DESAT}$ vs. Temperature**

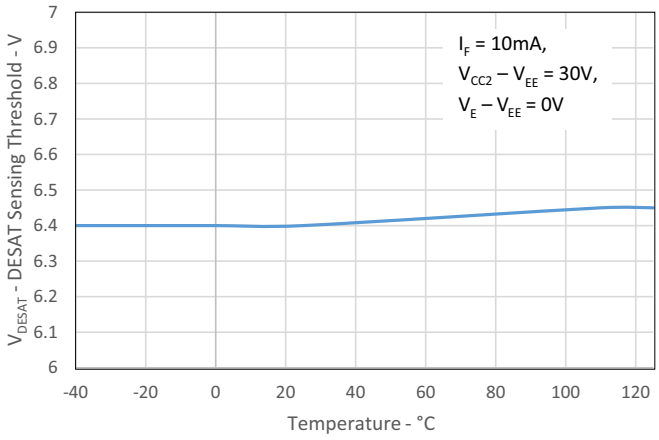



**Figure 12: $I_{CHG}$ vs. Temperature**

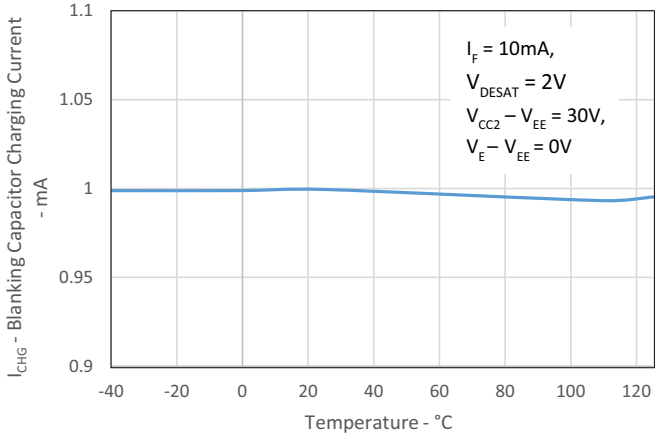



**Figure 13: $I_{DSCHG}$ vs. Temperature**

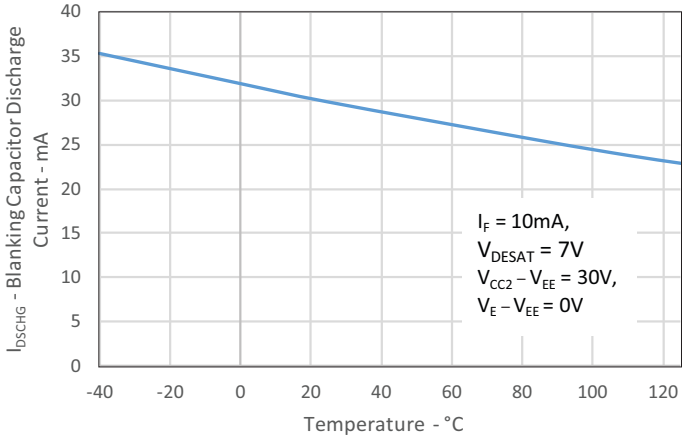


**Figure 14: $t_{PLH}/t_{PHL}$ vs. Temperature**

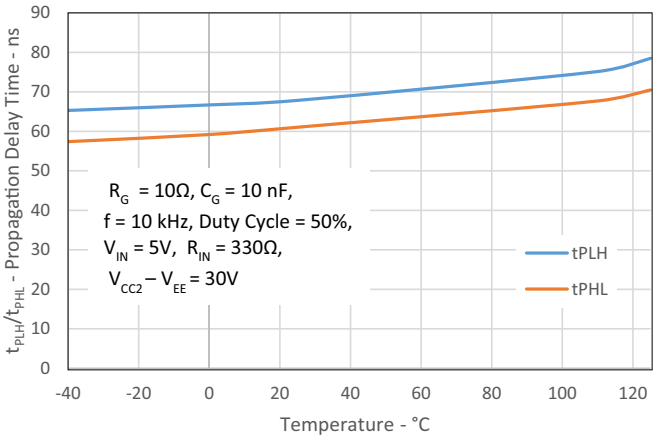



**Figure 15: $t_{DESAT(90\%)}$ vs. Temperature**

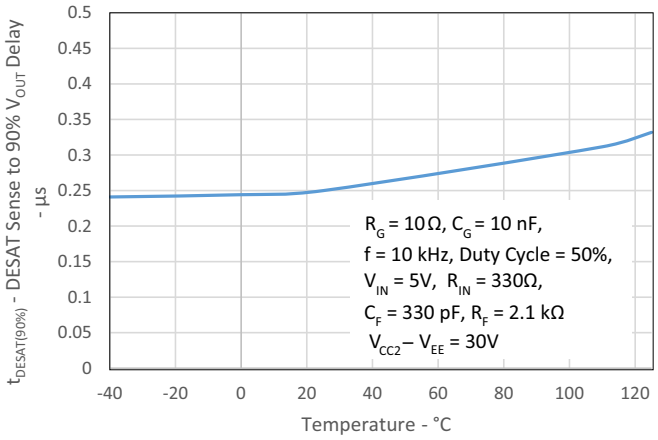



**Figure 16: $t_{DESAT(10\%)}$ vs. Temperature**

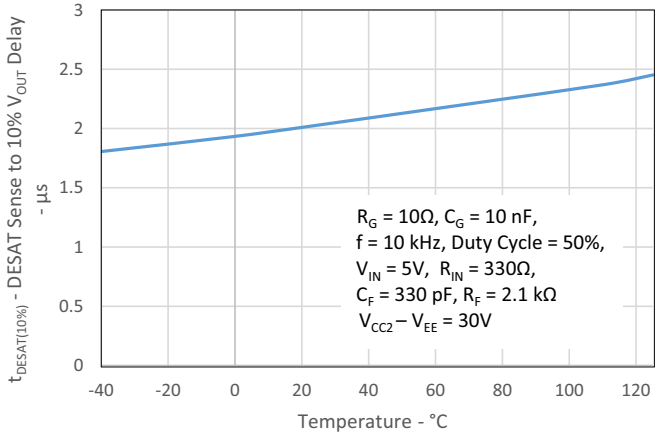



**Figure 17: $t_{DESAT(10\%)}$ vs. Load Resistance**

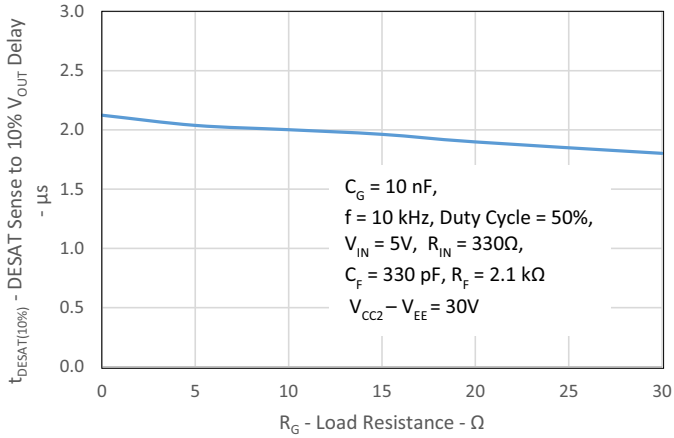
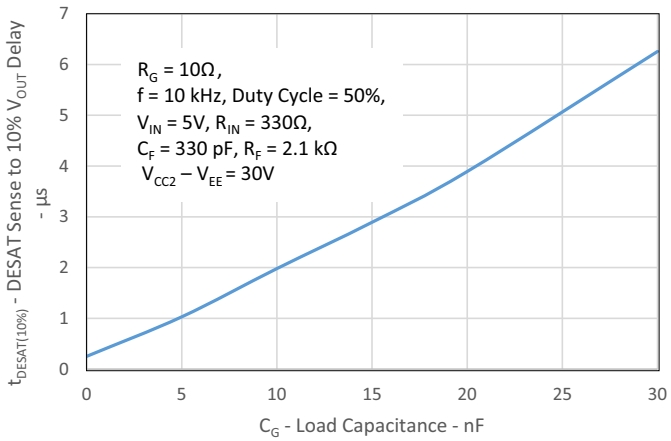


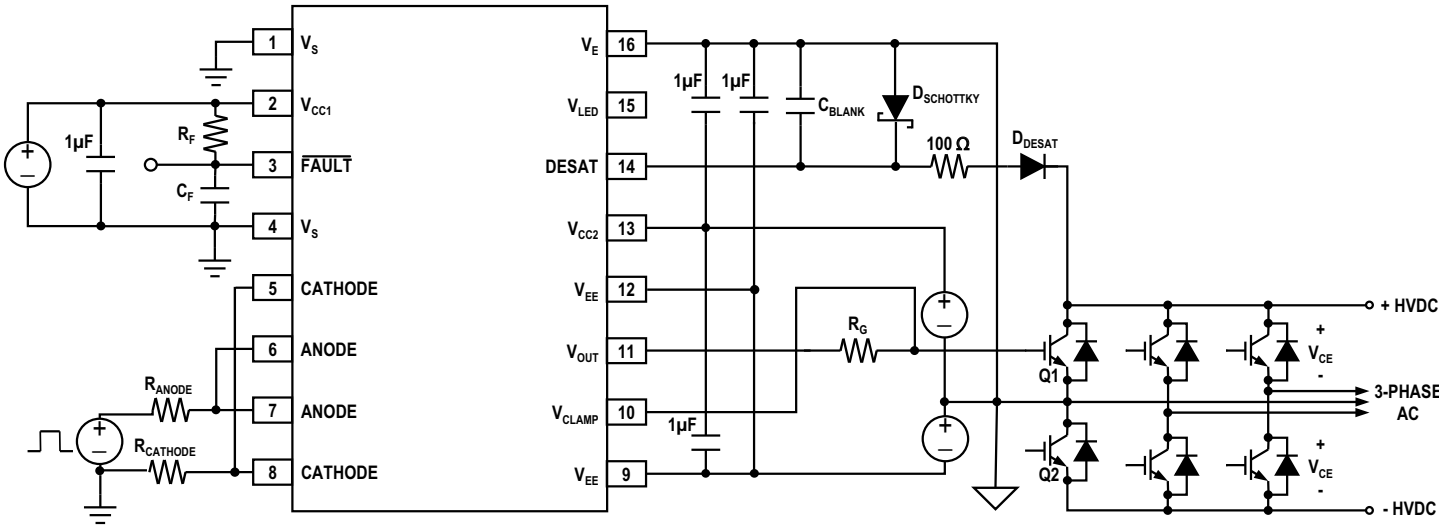

**Figure 18: $t_{DESAT(10\%)}$ vs. Load Capacitance**



# Applications Information

## Recommended Application Circuit

**Figure 19: Recommended Application Circuit for ACPL-334J/338J**




The ACPL-334J/338J has an LED input gate control, and an open collector fault output suitable for wired OR applications. The recommended application circuit shown in Figure 19 illustrates a typical gate drive implementation using the ACPL-334J/338J. The following describes about driving IGBT. However, it is also applicable to MOSFET.

The supply bypass capacitors (1 µF) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (7 mA to 8 mA) power supply suffices.

The blocking diode $D_{DESAT}$, 100Ω resistor, and Schottky diode $D_{SCHOTTKY}$ are necessary components to protect the DESAT pin 14. $D_{DESAT}$ should be a 600V or 1200V, fast recovery diode with $t_{rr}$ below 75 ns (for example, ERA34-10). $D_{SCHOTTKY}$ should be a 40V or 60V, low $V_F$ diode (for example, MBR0540). The 330-pF capacitor, $C_{BLANK}$, is used to adjust the DESAT blanking time to disable the DESAT detection for a short period of time during when the IGBT switch on.

The gate resistor $R_G$ serves to limit the gate charge current and controls the IGBT collector voltage rise and fall times. The open collector fault output has a 2.1 kΩ pull-up resistor and a 330 pF filtering capacitor, $C_F$.

The two resistors, $R_{ANODE}$ and $R_{CATHODE}$, are connected to the input LED's anode and cathode and are recommended to be split in the ratio of 2:1. They will help to balance the common mode impedances at the LED's anode and cathode. This helps to equalize the common mode voltage changes at the anode and cathode to give high CMR performance.

# Description of Operation

## Normal Operation

During normal operation, $V_{OUT}$ of the ACPL-334J/338J is controlled by the input LED current $I_F$ (pins 5, 6, 7, and 8), with the IGBT collector-to-emitter voltage being monitored through DESAT. The FAULT output is high. See Figure 20 and Figure 21.

## Fault Condition

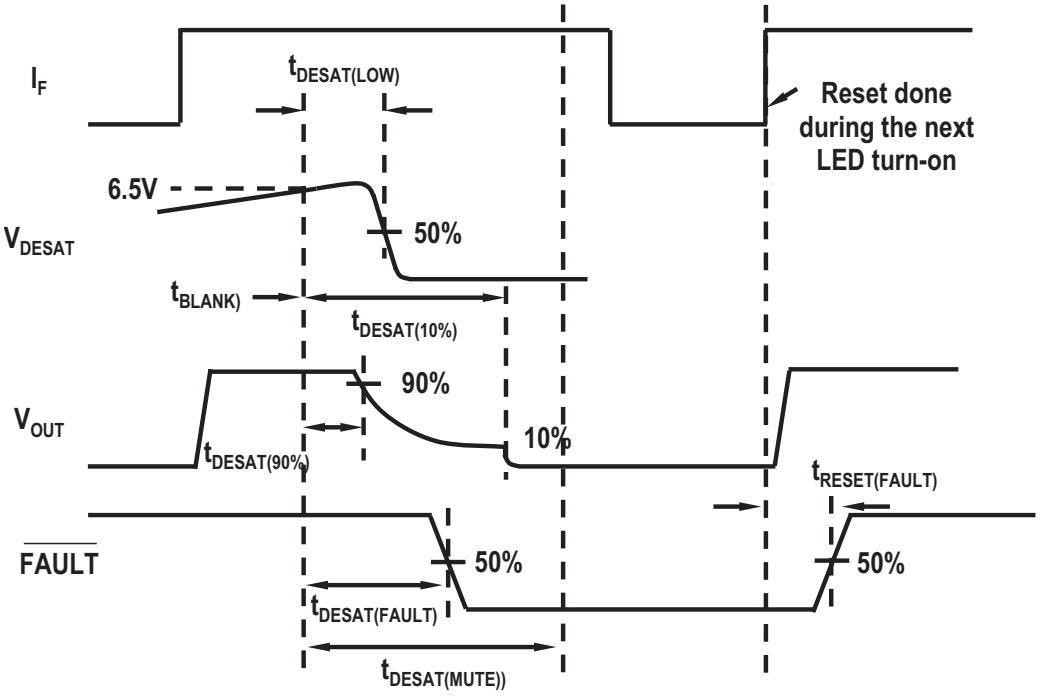
The DESAT pin monitors the IGBT $V_{CE}$ voltage. When the voltage on the DESAT pin exceeds 6.5V while the IGBT is on, $V_{OUT}$ is slowly brought low in order to *softly* turn off the IGBT and prevent large di/dt induced voltages. Also activated is an internal feedback channel that brings the FAULT output low for the purpose of notifying the microcontroller of the fault condition.

## FAULT Reset

### ACPL-334J

Once a fault is detected, the output will be muted for 4.5 µs (minimum). All input LED signals will be ignored during the mute period to allow the driver to completely soft shut down the IGBT. The fault mechanism can be reset by the next LED turn-on after the 4.5 µs (minimum) mute time. See Figure 20.

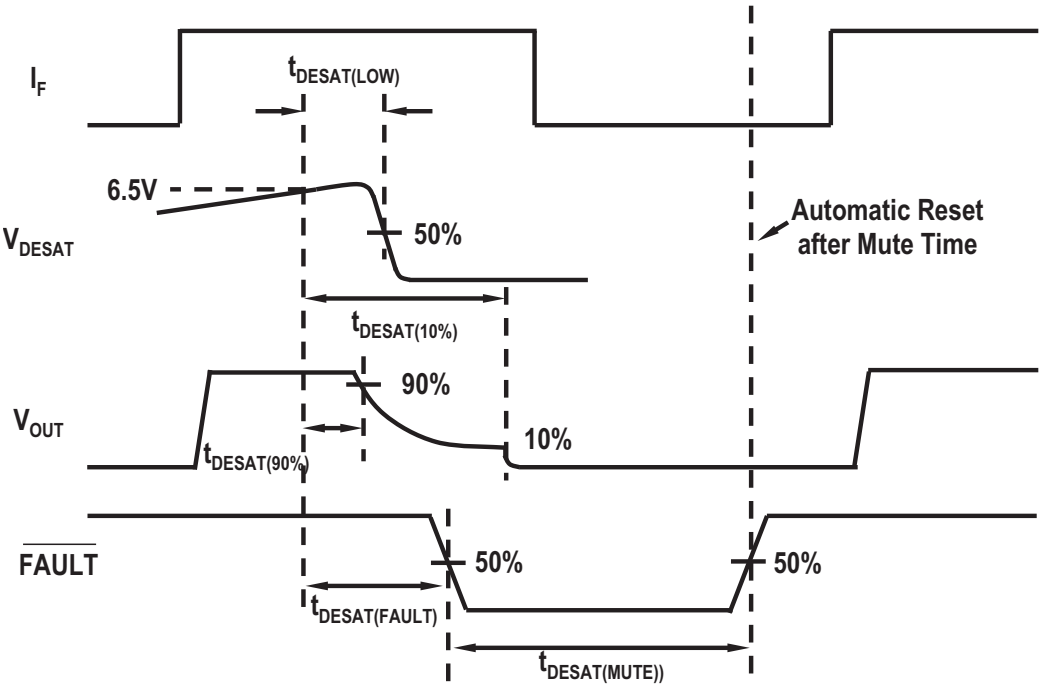
**Figure 20: ACPL-334J FAULT Timing Diagram**



## ACPL-338J

Once a fault is detected, the output will be a soft shutdown to low. All input LED signals will be ignored during the fault period to allow the driver to completely soft shut down the IGBT. The driver will automatically reset the FAULT pin after a fixed mute time of 32 µs (typical). See Figure 21.

**Figure 21: ACPL-338J FAULT Timing Diagram**




### Output Control

The outputs ($V_{OUT}$ and FAULT) of the ACPL-334J/338J are controlled by the combination of $I_F$, UVLO and a detected IGBT DESAT condition. Once UVLO is not active ($V_{CC2} – V_E > V_{UVLO}$), $V_{OUT}$ is allowed to go high, and the DESAT (pin 14) detection feature of the ACPL-334J/338J will be the primary source of IGBT protection. Once $V_{CC2}$ is increased from 0V to above $V_{UVLO+}$, DESAT will remain functional until $V_{CC2}$ is decreased below $V_{UVLO-}$. Thus, the DESAT detection and UVLO features of the ACPL-334J/338J work in conjunction to ensure constant IGBT protection.

### Desaturation Detection and High Current Protection

The ACPL-334J/338J satisfies these criteria by combining a high-speed, high output current driver, high-voltage optical isolation between the input and output, local IGBT desaturation detection and shutdown, and an optically isolated fault status feedback signal into a single 16-pin surface-mount package.

The fault detection method, which is adopted in the ACPL-334J/338J, is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off state of the IGBT, the fault detect circuitry is simply disabled to prevent false *fault* signals.

The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the ACPL-334J/338J limits the power dissipation in the IGBT even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly conservative overcurrent threshold is not needed to protect the IGBT.

## Slow IGBT Gate Discharge during Fault Condition

When a desaturation fault is detected, a weak pull-down device in the ACPL-334J/338J output drive stage will turn on to *softly* turn off the IGBT. This device slowly discharges the IGBT gate to prevent fast changes in drain current that could cause damaging voltage spikes due to lead and wire inductance. During the slow turn off, the large output pull-down device remains off until the output voltage falls below $V_{EE}$ + 2V, at which time the large pull-down device clamps the IGBT gate to $V_{EE}$.

## DESAT Fault Detection Blanking Time

The DESAT fault detection circuitry must remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the DESAT threshold. This time period, called the DESAT blanking time, is controlled by the internal DESAT charge current, the DESAT voltage threshold, and the external DESAT capacitor.

The nominal blanking time is calculated in terms of external capacitance ($C_{BLANK}$), FAULT threshold voltage ($V_{DESAT}$), and DESAT charge current ($I_{CHG}$) as $t_{BLANK} = C_{BLANK} \times V_{DESAT}/I_{CHG}$. The nominal blanking time with the recommended 330-pF capacitor is 330 pF × 6.5V/1000 µA = 2.145 µs.

The capacitance value can be scaled slightly to adjust the blanking time, though a value smaller than 330 pF is not recommended. This nominal blanking time represents the longest time it will take for the ACPL-334J/338J to respond to a DESAT fault condition. If the IGBT is turned on while the collector and emitter are shorted to the supply rails (switching into a short), the soft shutdown sequence will begin after approximately 2 µs. If the IGBT collector and emitter are shorted to the supply rails after the IGBT is already on, the response time will be much quicker due to the parasitic parallel capacitance of the DESAT diode. The recommended 330-pF capacitor should provide adequate blanking as well as fault response times for most applications.

| $I_F$ | UVLO ($V_{CC2} - V_E$) | DESAT Function | Pin 3 (FAULT) Output | $V_{OUT}$ |
|---|---|---|---|---|
| ON | Active | Not Active | High | Low |
| ON | Not Active | Active (with DESAT fault) | Low (FAULT) | Low |
| ON | Not Active | Active (no DESAT fault) | High (or no fault) | High |
| OFF | Active | Not Active | High | Low |
| OFF | Not Active | Not Active | High | Low |

## Under-Voltage Lockout

The under-voltage lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to the IGBT by forcing the ACPL-334J/338J output low during power-up. IGBTs typically require gate voltages of 15V to achieve their rated $V_{CE(ON)}$ voltage. At gate voltages below 13V, the $V_{CE(ON)}$ voltage increases dramatically, especially at higher currents. At very low gate voltages below 10V, the IGBT may operate in the linear region and quickly overheat. The UVLO function causes the output to be clamped whenever insufficient operating supply ($V_{CC2}$) is applied. Once $V_{CC2}$ exceeds $V_{UVLO+}$ (the positive-going UVLO threshold), the UVLO clamp is released to allow the device output to turn on in response to input signals. As $V_{CC2}$ is increased from 0V (at some level below $V_{UVLO+}$), first the DESAT protection circuitry becomes active. As $V_{CC2}$ is further increased (above $V_{UVLO+}$), the UVLO clamp is released. Before the time the UVLO clamp is released, the DESAT protection is already active. Therefore, the UVLO and DESAT fault detection feature work together to provide seamless protection regardless of supply voltage ($V_{CC2}$).

## Active Miller Clamp

An active Miller clamp allows the control of the Miller current during a high dv/dt situation and can eliminate the use of a negative supply voltage in most of the applications. During turn-off, the gate voltage is monitored and the clamp output is activated when gate voltage goes below 2V (relative to $V_{EE}$). The clamp voltage is $V_{OL}$ + 2.5V typical for a Miller current up to 1 A. The clamp is disabled when the LED input is triggered again.

## DESAT Pin Protection Resistor

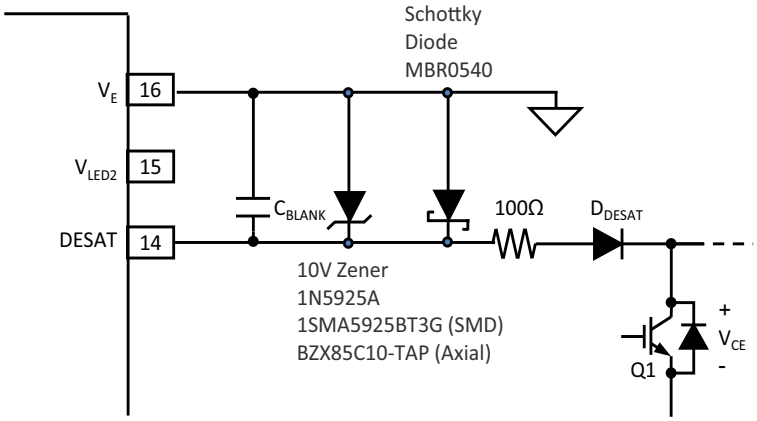
The freewheeling of flyback diodes connected across the IGBTs can have large instantaneous forward voltage transients, which greatly exceed the nominal forward voltage of the diode. This may result in a large negative voltage spike on the DESAT pin, which will draw substantial current out of the driver if protection is not used. To limit this current to levels that will not damage the driver IC, a 100Ω resistor should be inserted in series with the DESAT diode. The added resistance will not alter the DESAT threshold or the DESAT blanking time. But as the $I_{CHG}$ is 1 mA, it is to be noted that there will be a 0.1V contribution to the DESAT sensing path together with $D_{DESAT}$ and $V_{CE}$(IGBT).

## False Fault Prevention Diodes

One of the situations that may cause the driver to generate a false fault signal is if the substrate diode of the driver becomes forward biased. This can happen if the reverse recovery spikes coming from the IGBT/MOSFET freewheeling diodes bring the DESAT pin below ground. Hence, the DESAT pin voltage will be *brought* above the threshold voltage. These negative-going voltage spikes are typically generated by inductive loads or reverse recovery spikes of the IGBT/MOSFETs free-wheeling diodes. In order to prevent a false fault signal, it is highly recommended to connect a Zener diode and Schottky diode across the DESAT pin and $V_E$ pin.

This circuit solution is shown in Figure 22. The Schottky diode will prevent the substrate diode of the gate driver optocoupler from being forward biased while the Zener diode (value around 10V) is used to prevent any positive high transient voltage to affect the DESAT pin.

**Figure 22: False Fault Prevention Diodes**



# Thermal Calculation

The temperature at the LED and IC junctions of the optocoupler can be calculated using the equations below. Application and environmental design for ACPL-334J/338J needs to ensure that the junction temperature of the internal ICs and LED do not exceed 150°C.

$$T_{E1} = R_{21} \times P_{E1} + R_{22} \times P_I + R_{23} \times P_O + R_{24} \times P_{E2} + T_A$$

$$T_I = R_{11} \times P_{E1} + R_{12} \times P_I + R_{13} \times P_O + R_{14} \times P_{E2} + T_A$$

$$T_O = R_{31} \times P_{E1} + R_{32} \times P_I + R_{33} \times P_O + R_{34} \times P_{E2} + T_A$$

$$T_{E2} = R_{41} \times P_{E1} + R_{42} \times P_I + R_{43} \times P_O + R_{44} \times P_{E2} + T_A$$

- $T_{E1}$: LED1 junction temperature
- $T_I$: Input IC junction temperature
- $T_O$: Output IC junction temperature
- $T_{E2}$: LED2 junction temperature
- $P_{E1}$: LED1 power dissipation
- $P_I$: Input IC power dissipation
- $P_O$: Output IC power dissipation
- $P_{E2}$: LED2 power dissipation
- $T_A$: Ambient temperature

**Table 1: Thermal Resistance**

| Thermal Resistance | Symbol | Typ. °C/W |
|---|---|---|
| **High Conductivity Board** | | |
| Junction to Ambient Thermal Resistance of: | | |
| Input IC Due to Heating of Input IC | $R_{11}$ | 79.15 |
| Input IC Due to Heating of LED1 | $R_{12}$ | 24.11 |
| Input IC Due to Heating of Output IC | $R_{13}$ | 18.83 |
| Input IC Due to Heating of LED2 | $R_{14}$ | 28.77 |
| Input LED1 Due to Heating of Input IC | $R_{21}$ | 21.71 |
| Input LED1 Due to Heating of LED1 | $R_{22}$ | 121.2 |
| Input LED1 Due to Heating of Output IC | $R_{23}$ | 25.96 |
| Input LED1 Due to Heating of LED2 | $R_{24}$ | 19.62 |
| Output IC Due to Heating of Input IC | $R_{31}$ | 13.21 |
| Output IC Due to Heating of LED1 | $R_{32}$ | 19.22 |
| Output IC Due to Heating of Output IC | $R_{33}$ | 43.42 |
| Output IC Due to Heating of LED2 | $R_{34}$ | 16.94 |
| Input LED2 Due to Heating of Input IC | $R_{41}$ | 30.78 |
| Input LED2 Due to Heating of LED1 | $R_{42}$ | 21.44 |
| Input LED2 Due to Heating of Output IC | $R_{43}$ | 23.35 |
| Input LED2 Due to Heating of LED2 | $R_{44}$ | 120.7 |

**Table 1: Thermal Resistance (Continued)**

| Thermal Resistance | Symbol | Typ. °C/W |
|---|---|---|
| **Low Conductivity Board** | | |
| Junction to Ambient Thermal Resistance of: | | |
| Input IC Due to Heating of Input IC | $R_{11}$ | 130.3 |
| Input IC Due to Heating of LED1 | $R_{12}$ | 56.07 |
| Input IC Due to Heating of Output IC | $R_{13}$ | 50.85 |
| Input IC Due to Heating of LED2 | $R_{14}$ | 67.37 |
| Input LED1 Due to Heating of Input IC | $R_{21}$ | 54.84 |
| Input LED1 Due to Heating of LED1 | $R_{22}$ | 156.5 |
| Input LED1 Due to Heating of Output IC | $R_{23}$ | 60.81 |
| Input LED1 Due to Heating of LED2 | $R_{24}$ | 51.46 |
| Output IC Due to Heating of Input IC | $R_{31}$ | 35.54 |
| Output IC Due to Heating of LED1 | $R_{32}$ | 42.64 |
| Output IC Due to Heating of Output IC | $R_{33}$ | 71.91 |
| Output IC Due to Heating of LED2 | $R_{34}$ | 40.73 |
| Input LED2 Due to Heating of Input IC | $R_{41}$ | 68.48 |
| Input LED2 Due to Heating of LED1 | $R_{42}$ | 50.75 |
| Input LED2 Due to Heating of Output IC | $R_{43}$ | 56.86 |
| Input LED2 Due to Heating of LED2 | $R_{44}$ | 163.9 |

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