

ACNT-H511/H511C

Open-Collector Output Optocoupler in a 15-mm Stretched SO-8 Package

Overview

The ACNT-H511/H511C is a single-channel open-collector output optocoupler in a stretched SO-8 footprint. The ACNT-H511C is a high-CTI optocoupler that can meet a wider range of creepage values for a higher working voltage or rated insulation voltage. With high CTI, material group upgrade to I, the overall creepage requirements will reduce by half.

The ACNT-H511/H511C uses an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional phototransistor coupler by reducing the base-collector capacitance.

The ACNT-H511/H511C with a 15-mm creepage/clearance and high-voltage insulation capability is suitable for isolated communication logic interface and control in high-voltage power systems such as 690-VAC drives, renewable inverters, energy storage, and medical equipment.

Figure 1: Functional Diagram

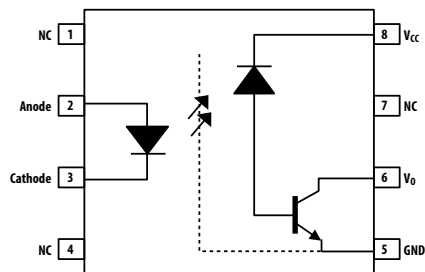


Table 1: Truth Table

LED	Output
ON	L
OFF	H

A 0.1-μF bypass capacitor must be connected between pins V_{CC} and GND.

Features

- CTI 600V, Material Group I (ACNT-H511C)
- TTL compatible
- Package: 15-mm stretched SO-8 package
- Open-collector output
- 40-kV/μs typical common-mode rejection at V_{CM} = 1500V
- Guaranteed performance within temperature range: -40°C to +105°C
- Worldwide safety approval:
 - UL1577 recognized: 7500 V_{RMS} for 1 minute
 - CSA approval
 - IEC 60747-5-5 approval for reinforced insulation

Applications

- High-voltage power systems, for example, 690-VAC drives
- Renewable energy inverters
- Feedback elements in switching power supplies
- Digital isolation for A/D, D/A conversion digital field
- Communications interface
- MCU interface

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage and degradation that might be induced by ESD. The components featured in this data sheet are not recommended to be used in military or aerospace applications or environments.

Ordering Information

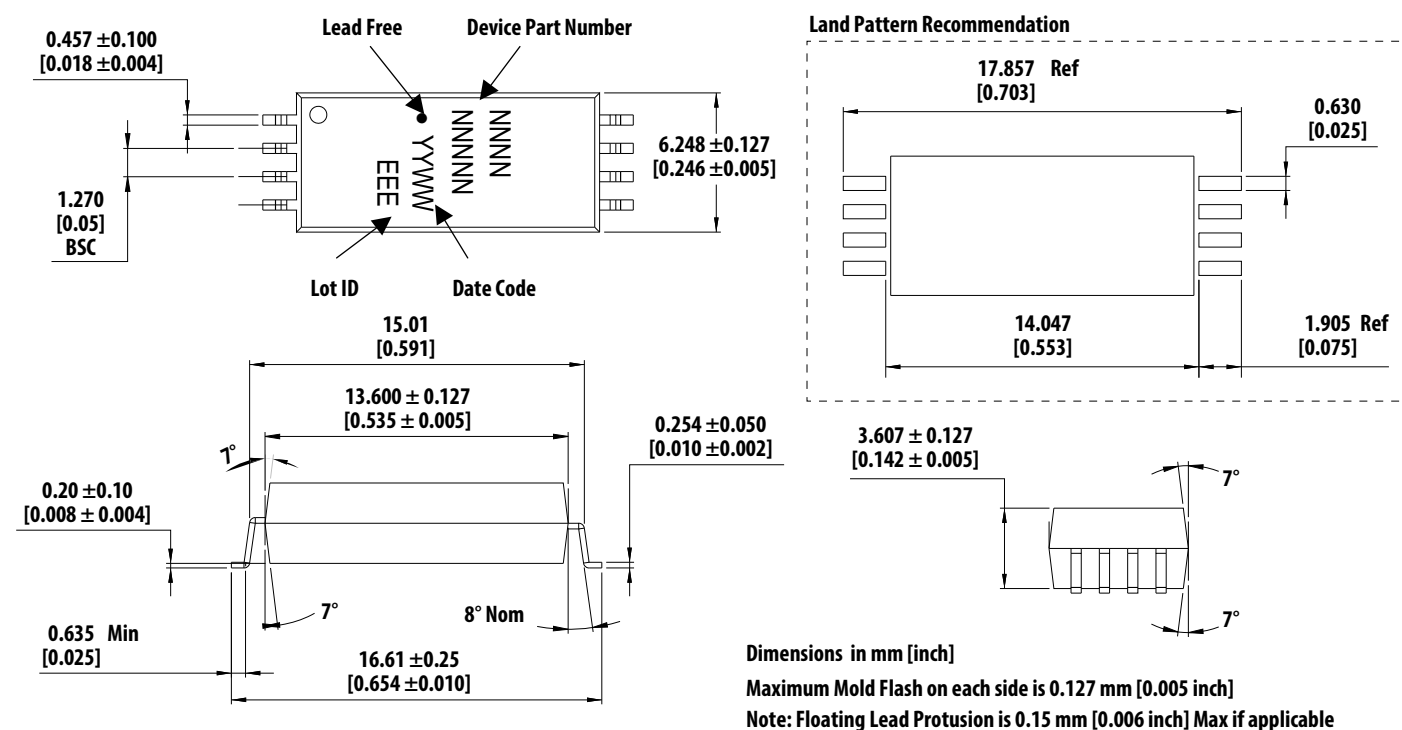
The ACNT-H511/H511C is UL recognized with 7500 V_{RMS} for 1 minute per UL1577.

Part Number	Option RoHS Compliant	Package	Surface Mount	Tape and Reel	UL 1577	IEC 60747-5-5	Quantity
ACNT-H511/H511C	-000E	15-mm Stretched SO-8	X		X	X	80 per tube
	-500E		X	X	X	X	1000 per reel

To form an order entry, choose a part number from the Part Number column and combine it with the desired option from the Option column.

Package Outline Drawing

ACNT-H511/H511C Stretched SO-8 Package



Solder Reflow Profile

The recommended reflow conditions are as per JEDEC standard J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACNT-H511/H511C is approved by the following organizations:

UL	Approval under UL 1577, component recognition program up to $V_{ISO} = 7500 V_{RMS}$ File E55361.
CSA	Approval under CSA Component Acceptance Notice #5, File CA 88324.
IEC 60747-5-5	Maximum repetitive peak isolation voltage $V_{IORM} = 2262 V_{PEAK}$.

Insulation and Safety Related Specifications

Parameter	Symbol	ACNT-H511	ACNT-H511C	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	14.2		mm	Measured from input terminals to output terminals, shortest distance through the air.
Minimum External Tracking (External Creepage)	L(102)	15		mm	Measured from input terminals to output terminals, shortest distance path along the body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.5		mm	Through insulation distance conductor to conductor, usually the straight-line distance thickness between the emitter and the detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>300	≥600	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group	—	IIIa	I	—	Material Group (DIN VDE 0110, 1/89, Table 1).

IEC 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110/39, Table 1 For rated mains voltage $\leq 600 V_{RMS}$ For rated mains voltage $\leq 1000 V_{RMS}$	—	I – IV I – IV	—
Climatic Classification	—	40/105/21	—
Pollution Degree (DIN VDE 0110/39)	—	2	—
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	2262	V_{PEAK}
Input to Output Test Voltage, Method b ^a $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ second, Partial Discharge < 5 pC	V_{PR}	4241	V_{PEAK}
Input to Output Test Voltage, Method a ^a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, $t_m = 10$ seconds, Partial Discharge < 5 pC	V_{PR}	3619	V_{PEAK}
Maximum Working Isolation Voltage ^a	V_{IOWM}	2262 (Reinforced)	V_{DC}
		2827 (Basic)	V_{DC}
		1600 (Reinforced)	V_{RMS}
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60$ seconds)	V_{IOTM}	12000	V_{PEAK}
Safety-Limiting Values – Maximum Values Allowed in the Event of a Failure			
Case Temperature	T_S	150	$^{\circ}C$
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	1000	mW
Insulation Resistance at T_S , $V_{IO} = 500V$	R_S	$>10^9$	Ω

a. Refer to the optocoupler section of the *Isolation and Control Components Designer's Catalog*, under the Product Safety Regulations section (IEC 60747-5-5) for a detailed description of the Method a and Method b partial discharge test profiles.

NOTE: These optocouplers are suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety limit data shall be ensured by means of protective circuits.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	−55	125	°C
Operating Temperature	T_A	−40	105	°C
Average Forward Input Current	$I_{F(AVG)}$	—	20	mA
Peak Forward Input Current ($<1\ \mu\text{s}$ Pulse Width, $<10\%$ Duty Cycle)	$I_{F(PEAK)}$	—	80	mA
Peak Transient Input Current ($\leq 1\ \mu\text{s}$ pulse width, $<300\ \text{ps}$)	$I_{F(TRANS)}$	—	1	A
Reversed Input Voltage	V_R	—	5	V
Input Power Dissipation	P_{IN}	—	35	mW
Output Power Dissipation	P_O	—	100	mW
Output Current	I_O	—	12	mA
Supply Voltage	V_{CC}	−0.5	30	V
Output Voltage	V_O	−0.5	24	V
Lead Solder Temperature	T_{LS}	260°C for 10 seconds, 1.6 mm below the seating plane.		
Solder Reflow Temperature Profile	—	See the Solder Reflow Profile section.		

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	4.5	24	V
Input Current, High Level	I_{FH}	10	18	mA
Operating Temperature	T_A	−40	105	°C
Forward Input Voltage (OFF)	$V_{F(OFF)}$	—	0.8	V

Electrical Specifications (DC)

Over recommended operating $T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, supply voltage ($4.5\text{V} \leq V_{CC} \leq 24\text{V}$) unless otherwise specified. All typical values are at $T_A = 25^{\circ}\text{C}$.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions			Figure
Current Transfer Ratio	CTR ^a	31	50	80	%	$T_A = 25^{\circ}\text{C}$	$V_O = 0.4\text{V}$	$V_{CC} = 5\text{V}$ $I_F = 12\text{ mA}$	3
		21	—	—	%	—	$V_O = 0.5\text{V}$	—	
Logic Low Output Voltage	V_{OL}	—	0.2	0.4	V	$T_A = 25^{\circ}\text{C}$	$I_O = 3\text{ mA}$	$V_{CC} = 5\text{V}$ $I_F = 12\text{ mA}$	
		—	0.2	0.5	V	—	$I_O = 1.6\text{ mA}$	—	
Logic High Output Current	I_{OH}	—	0.014	0.5	μA	$T_A = 25^{\circ}\text{C}$	$V_O = V_{CC} = 5.5\text{V}$	$I_F = 0\text{ mA}$	5
		—	0.06	1			$V_O = V_{CC} = 24\text{V}$		
		—	—	80		—	$V_O = V_{CC} = 24\text{V}$		
Logic Low Supply Current	I_{CCL}	—	200	400	μA	—	$I_F = 12\text{ mA}$, $V_O = \text{open}$, $V_{CC} = 24\text{V}$	—	
Logic High Supply Current	I_{CCH}	—	—	2	μA	—	$I_F = 0\text{ mA}$, $V_O = \text{open}$, $V_{CC} = 24\text{V}$	—	
Input Forward Voltage	V_F	1.10	1.45	1.70	V	—	$I_F = 12\text{ mA}$	—	2
Input Reversed Breakdown Voltage	BV_R	7	—	—	V	—	$I_R = 10\text{ }\mu\text{A}$	—	
Temperature Coefficient of Forward Voltage	$\Delta V_F / \Delta T_A$	—	-1.5	—	$\text{mV}/^{\circ}\text{C}$	—	$I_F = 12\text{ mA}$	—	
Input Capacitance	C_{IN}	—	20	—	pF	—	$f = 1\text{ MHz}$, $V_F = 0$	—	

a. The current transfer ratio in percent is defined as the ratio of the output collector current, I_O , to the forward LED input current, I_F , times 100%.

Switching Specifications

Over recommended operating ($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$), $I_F = 12\text{ mA}$, ($4.5\text{V} \leq V_{CC} \leq 24\text{V}$), unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure
Propagation Delay Time to Logic Low at Output	T_{PHL}	—	0.1	2.0	μs	$T_A = 25^\circ\text{C}$ Pulse: $f = 10\text{ kHz}$, Duty cycle = 50%, $V_{CC} = 5.0\text{V}$, $R_L = 1.6\text{ k}\Omega$, $C_L = 15\text{ pF}$, $V_{THHL} = 1.5\text{V}$	13
		—	—	2.0	μs	—	6, 13
		—	0.15	2.0	μs	$T_A = 25^\circ\text{C}$ Pulse: $f = 10\text{ kHz}$, Duty cycle = 50%, $V_{CC} = 24\text{V}$, $R_L = 8.2\text{ k}\Omega$, $C_L = 15\text{ pF}$, $V_{THHL} = 1.5\text{V}$	13
		—	—	2.0	μs	—	7, 13
Propagation Delay Time to Logic High at Output	T_{PLH}	—	0.4	2.0	μs	$T_A = 25^\circ\text{C}$ Pulse: $f = 10\text{ kHz}$, Duty cycle = 50%, $V_{CC} = 5.0\text{V}$, $R_L = 1.6\text{ k}\Omega$, $C_L = 15\text{ pF}$, $V_{THLH} = 2.0\text{V}$	13
		—	—	2.0	μs	—	6, 13
		—	0.4	2.0	μs	$T_A = 25^\circ\text{C}$ Pulse: $f = 10\text{ kHz}$, Duty cycle = 50%, $V_{CC} = 24\text{V}$, $R_L = 8.2\text{ k}\Omega$, $C_L = 15\text{ pF}$, $V_{THLH} = 2.0\text{V}$	13
		—	—	2.0	μs	—	7, 13
Propagation Delay Difference Between Any Two Parts ^a	t_{psk}	—	0.3	2.0	μs	$T_A = 25^\circ\text{C}$ Pulse: $f = 10\text{ kHz}$, Duty cycle = 50%, $V_{CC} = 5.0\text{V}$, $R_L = 1.6\text{ k}\Omega$, $C_L = 15\text{ pF}$, $V_{THHL} = 1.5\text{V}$, $V_{THLH} = 2.0\text{V}$	
		—	0.3	2.0	μs	$T_A = 25^\circ\text{C}$ Pulse: $f = 10\text{ kHz}$, Duty cycle = 50%, $V_{CC} = 24\text{V}$, $R_L = 8.2\text{ k}\Omega$, $C_L = 15\text{ pF}$, $V_{THHL} = 1.5\text{V}$, $V_{THLH} = 2.0\text{V}$	
Common-Mode Transient Immunity at Logic High Output ^b	$ CM_H $	—	40	—	$\text{kV}/\mu\text{s}$	$T_A = 25^\circ\text{C}$ $V_{CM} = 1500\text{V}$, $I_F = 0\text{ mA}$, $R_L = 1.0\text{ k}\Omega$ or $1.6\text{ k}\Omega$, $V_{CC} = 5\text{V}$	14
Common-Mode Transient Immunity at Logic Low Output ^c	$ CM_L $	—	40	—	$\text{kV}/\mu\text{s}$	$T_A = 25^\circ\text{C}$ $V_{CM} = 1500\text{V}$, $I_F = 12\text{ mA}$, $R_L = 1.6\text{ k}\Omega$, $V_{CC} = 5\text{V}$	14

a. The difference between t_{PLH} and t_{PHL} between any two parts under the same test condition.

b. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common-mode pulse, V_{CM} , to ensure that the output remains in a Logic High state.

c. Common-mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common-mode pulse signal, V_{CM} , to ensure that the output remains in a Logic Low state.

Package Characteristics

All typical at $T_A = 25^\circ\text{C}$.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input-Output Momentary Withstand Voltage ^a	V_{ISO}	7500	—	—	V_{RMS}	$RH \leq 50\%$, $t = 1\text{ minute}$, $T_A = 25^\circ\text{C}$
Input-Output Resistance ^a	R_{I-O}	—	10^{14}	—	Ω	$V_{I-O} = 500\text{VDC}$
Input-Output Capacitance ^a	C_{I-O}	—	0.6	—	pF	$f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$

a. The device is considered a two-terminal device: pins 2 and 3 are shorted together, and pins 5, 6, and 8 are shorted together.

Figure 2: Input Current vs. Forward Voltage

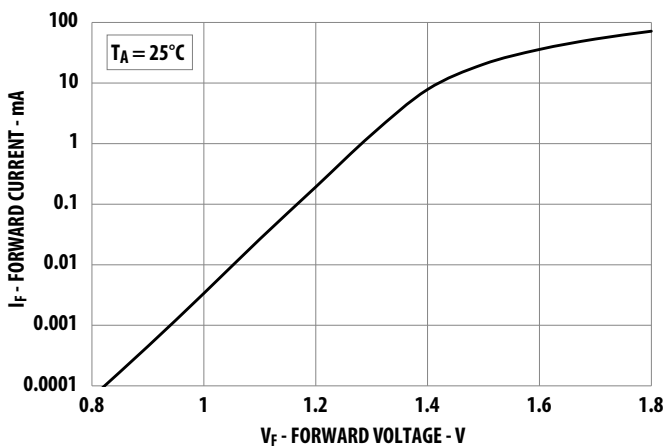


Figure 3: Typical Current Transfer Ratio vs. Temperature

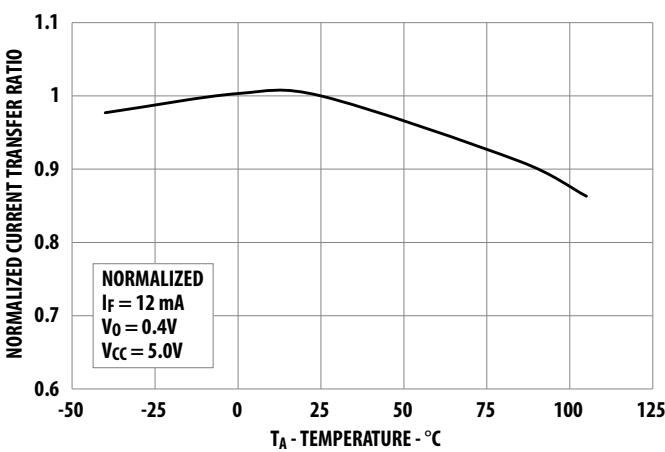


Figure 4: Typical Current Transfer Ratio vs. Temperature

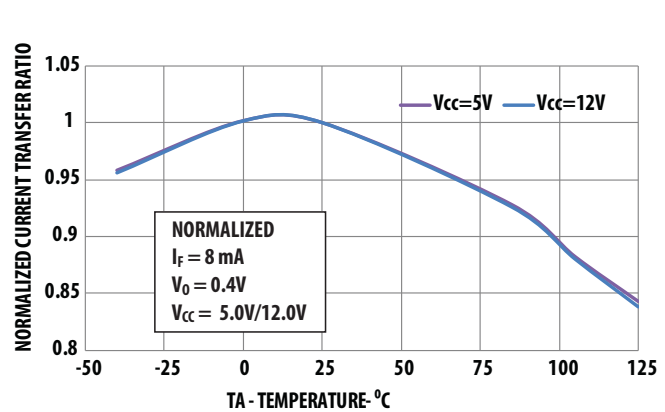


Figure 5: Typical Logic High Output Current vs. Temperature

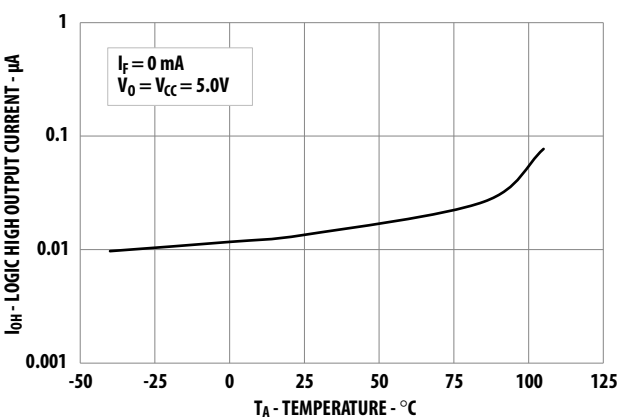


Figure 6: Typical Propagation Delay vs. Temperature

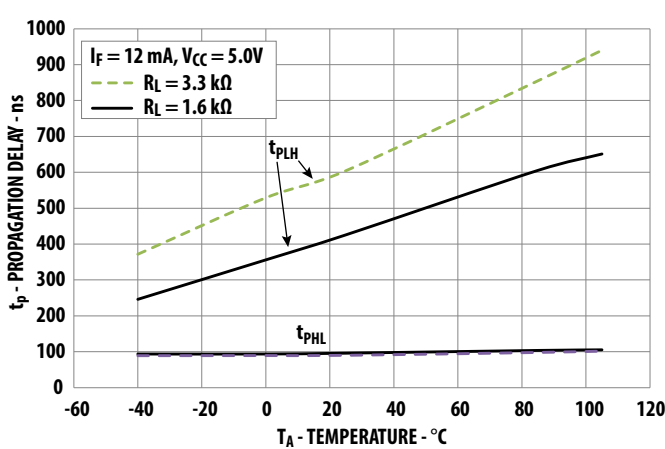


Figure 7: Typical Propagation Delay vs. Temperature

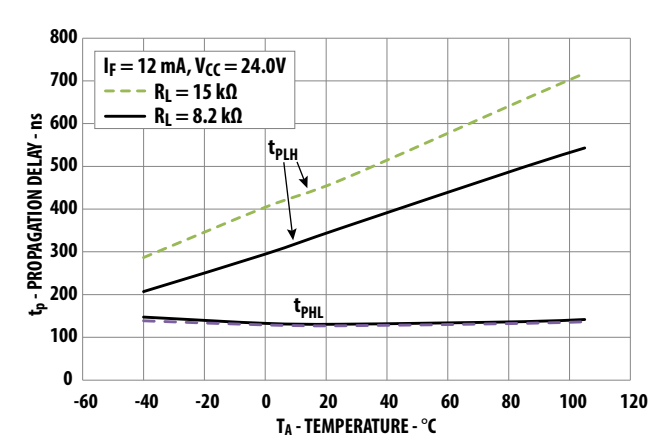


Figure 8: Typical Propagation Delay vs. Load Resistance

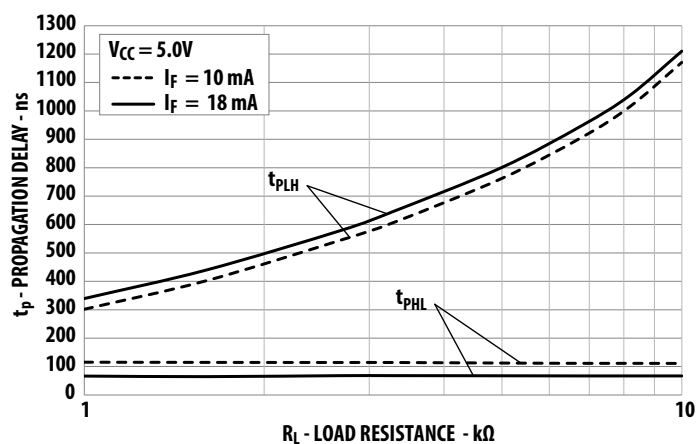


Figure 9: Typical Propagation Delay vs. Supply Voltage

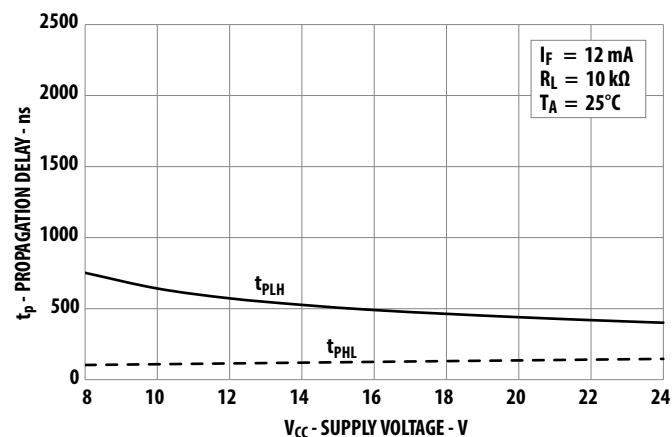


Figure 10: Typical Propagation Delay vs. Input Current

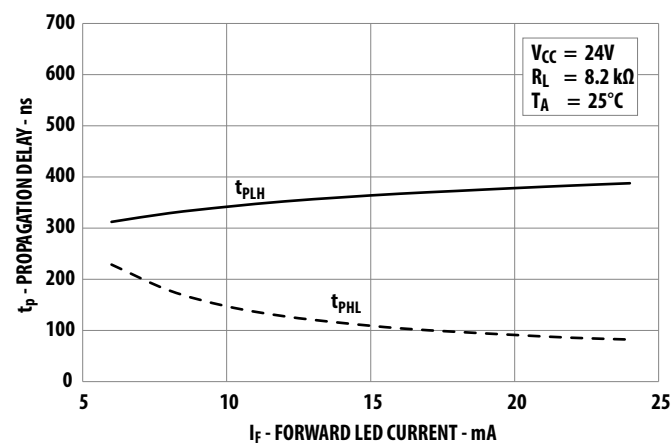


Figure 11: Current Transfer Ratio vs Input Current

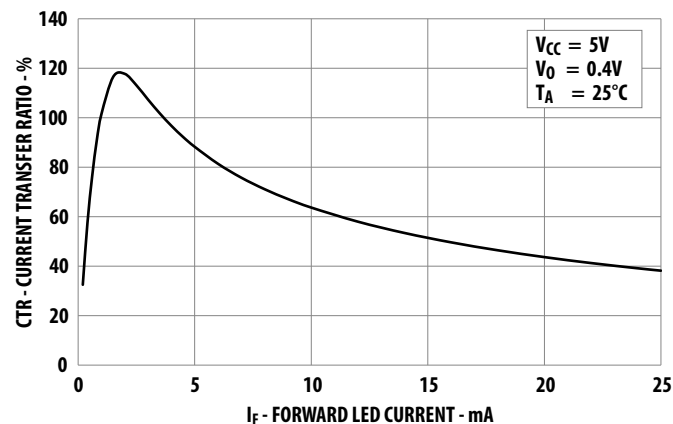
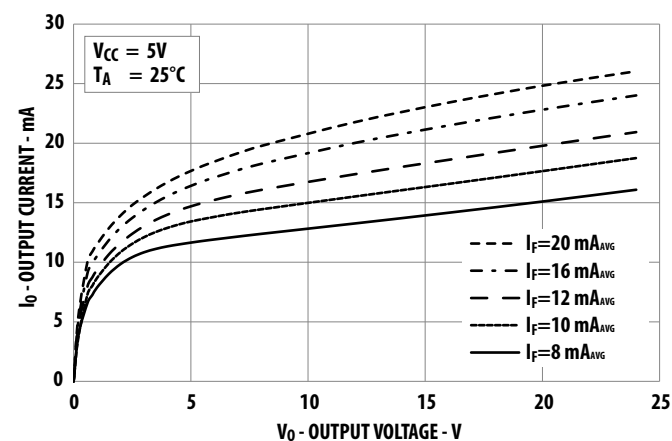


Figure 12: DC Pulse Transfer Characteristic



Test Circuits

Figure 13: Switching Test Circuits

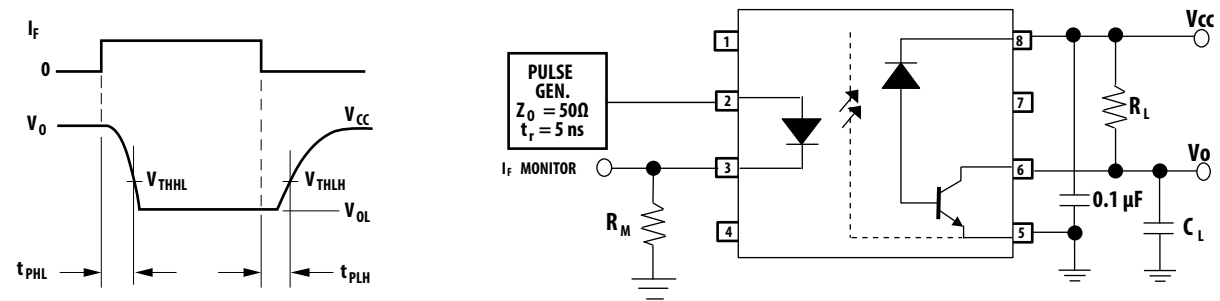
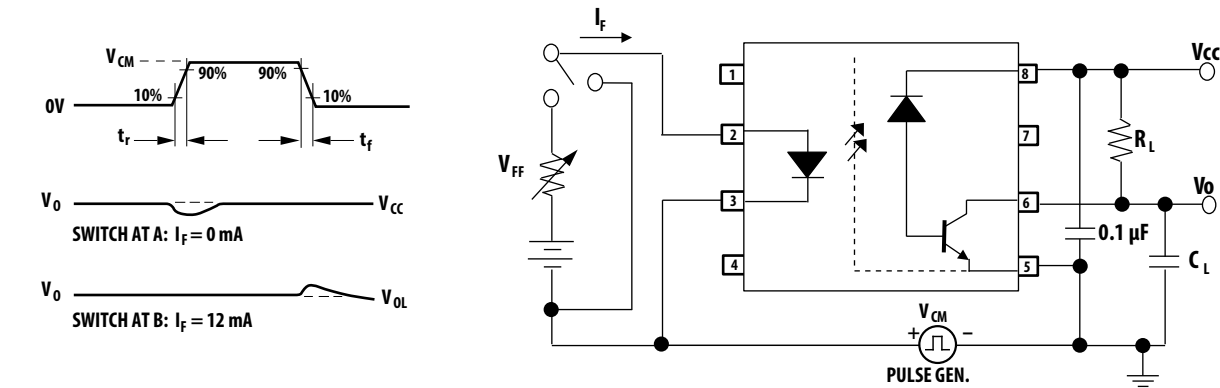


Figure 14: Test Circuit for Transient Immunity and Typical Waveforms



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