Data Sheet

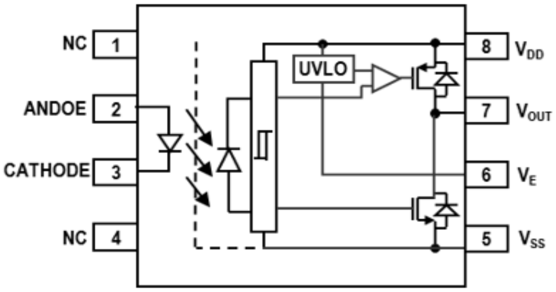
ACNT-H343

5-Amp Gate Drive Optocoupler in 15-mm SSO8 Package with 100-kV/μs Noise Immunity

Description

The Broadcom® ACNT-H343 is a 5A gate drive optocoupler device in a 15-mm SSO8 package designed for high voltage, space-constrained industrial applications, including motor drives and solar inverters. This package platform features wide 15-mm creepage and 14.2-mm clearance, high insulation voltage of V_{IORM} = 2262 V_{PEAK}, and a compact package footprint. The ACNT-H343 has common mode transient immunity (CMTI) greater than 100 kV/μs and a propagation delay faster than 150 ns, enabling high frequency switching to improve efficiency in driving IGBT and SiC/GaN MOSFET.

Figure 1: Functional Diagram



NOTE: A 1-μF bypass capacitor must be connected between pins V_{DD} and V_{SS}.

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage, degradation, or both that might be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Features

- 5.0A maximum peak output current
- 15-mm creepage and 14.2-mm clearance
- Rail-to-rail output voltage
- UVLO with V_E reference for negative power supply
- 150-ns maximum propagation delay
- 90-ns maximum propagation delay difference
- LED current input with hysteresis
- 100 kV/μs minimum Common Mode Rejection (CMR) at V_{CM} = 1500V
- I_{DD} = 5.0 mA maximum supply current
- Under Voltage Lock-Out Protection (UVLO) with hysteresis
- Wide Operating V_{DD} Range: 15 to 30V
- Industrial Temperature Range: –40°C to 110°C
- The following Safety Approvals:
  - UL Recognized 7500 V_{RMS} for 1 minute
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 2262 V_{PEAK}

Applications

- High Power System – 690 V_{AC} Drives
- IGBT/MOSFET gate drive
- AC and brushless DC motor drives
- 1500V Renewable energy inverters
- Industrial inverters
- Switching power supplies

Table 1: Truth Table

LED	$V_{DD} – V_E$ ***POSITIVE GOING*** **(That is, TURN-ON)**	$V_{DD} – V_E$ ***NEGATIVE GOING*** **(That is, TURN-OFF)**	V_{OUT}
OFF	0 – 30V	0 – 30V	LOW
ON	0 – 11.9V	0 – 10.9V	LOW
ON	11.9 – 13.2V	10.9 – 12.2V	TRANSITION
ON	13.2 – 30V	12.2 – 30V	HIGH

Ordering Information

Part Number	Option RoHS Compliant	Package	Tape and Reel	UL1577	IEC/EN/DIN EN 60747-5-5	Quantity
ACNT-H343	-000E	15 mm SSO8	—	X	X	80 per tube
	-500E		X	X	X	1000 per reel

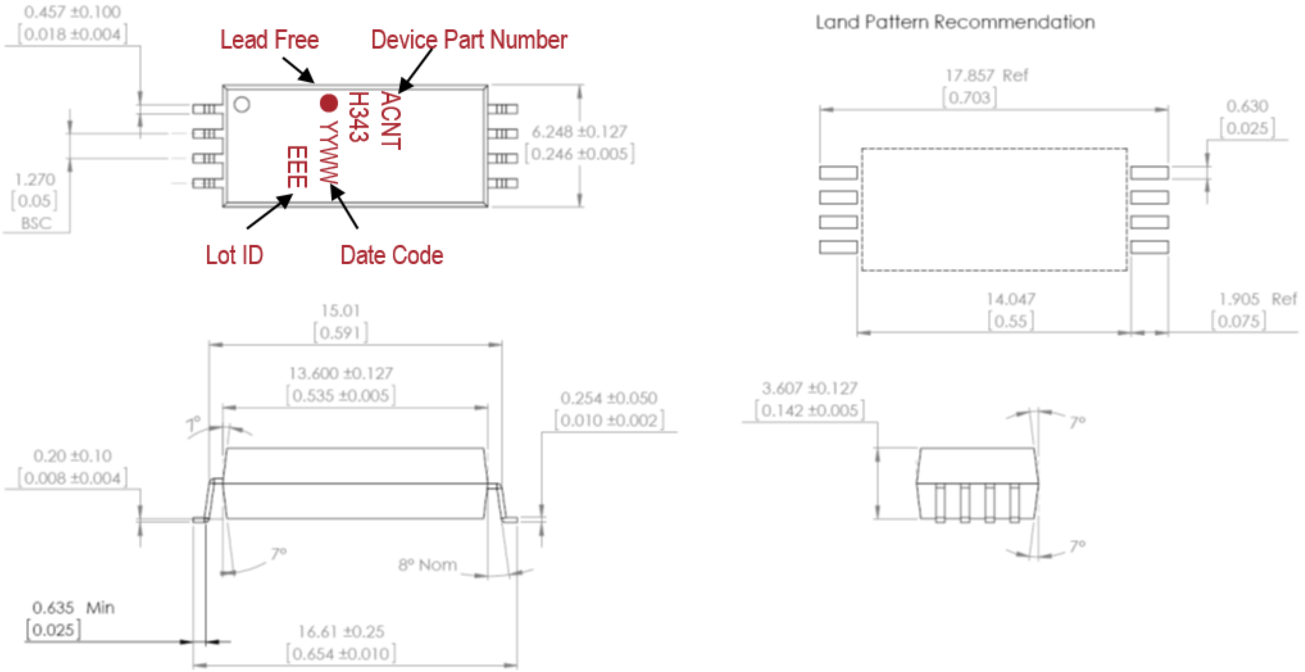
To order, choose a part number from the part number column and combine it with the desired option from the option column to form an order entry.

> **Example:** Part number ACNT-H343-500E describes a product with a Surface Mount package; delivered in Tape and Reel packaging; with IEC/EN/DIN EN 60747-5-5 and UL1577 7500 V_{RMS}/min Safety Approval; and RoHS compliance.

Options data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawings

Figure 2: ACNT-H343 Outline Drawing (15-mm SSO8 Package)



Dimensions in millimeters (inches) are as follows:

- Lead Coplanarity – 0.1 mm (0.004 inches).
- Maximum Mold Flash on each side – 0.127 mm (0.005 inches).
- Floating Lead Protrusion maximum – 0.15 mm (0.006 inches), if applicable.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACNT-H343 is approved by the following organizations:

- **UL** – Recognized under UL 1577, component recognition program up to V_{ISO} = 7500 V_{RMS}, File E55361
- **CSA** – CSA Component Acceptance Notice #5, File CA 88324
- **IEC/EN/DIN EN 60747-5-5** – Maximum Working Insulation Voltage V_{IORM} = 2262 V_{PEAK}

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics[a]

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/39, Table 1 For Rated Mains Voltage ≤ 600 V_{RMS} For Rated Mains Voltage ≤ 1000 V_{RMS}	—	I – IV I – IV	—
Climatic Classification	—	40/110/21	—
Pollution Degree (DIN VDE 00110/39)	—	2	—
Maximum Working Insulation Voltage	V_{IORM}	2262	V_{PEAK}
Input to Output Test Voltage, Method b[a] V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial discharge < 5 pC	V_{PR}	4242	V_{PEAK}
Input to Output Test Voltage, Method a[a] V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial discharge < 5 pC	V_{PR}	3619	V_{PEAK}
Highest Allowable Overvoltage[a] (Transient Overvoltage t_{ini} = 60 seconds)	V_{IORM}	12000	V_{PEAK}
Safety-limiting values – maximum values allowed in the event of a failure[b] Case Temperature Input Current Output Power	 T_S $I_{S,\ INPUT}$ $P_{S,\ OUTPUT}$	 175 230 1000	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

[a] Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the Avago Regulatory Guide to Isolation Circuits, AV02-2041EN for a detailed description of Method a and Method b partial discharge test profiles.

[b] This optocoupler is suitable for “safe electrical isolation” only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A in accordance with CECC 00802.

Insulation and Safety Related Specifications

Parameter	Symbol	ACNT-H343	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	14.2	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	15	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 300	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group	—	IIIa	—	Material Group (DIN VDE 0110, 1/89, Table 1)

NOTE: All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended Land Pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

Absolute Maximum Ratings

Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Note**
Storage Temperature	T_S	–55	125	°C	—
Operating Temperature	T_A	–40	110	°C	—
Average Input Current	$I_{F(AVG)}$	—	25	mA	a
Peak Transient Input Current (<1 µs-pulse width, 300 pps)	$I_{F(TRAN)}$	—	1	A	—
Reverse Input Voltage	V_R	—	5	V	—
"High" Peak Output Current	$I_{OH(PEAK)}$	—	5.0	A	b
"Low" Peak Output Current	$I_{OL(PEAK)}$	—	5.0	A	b
Total Output Supply Voltage	$(V_{DD} – V_{SS})$	–0.5	35	V	—
Negative Output Supply Voltage	$(V_E – V_{SS})$	–0.5	15	V	—
Positive Output Supply Voltage	$(V_{DD} – V_E)$	–0.5	$35 – (V_E – V_{SS})$	V	—
Output Voltage	$V_{O(PEAK)}$	–0.5	V_{DD}	V	—
Output IC Power Dissipation	P_O	—	800	mW	c
Total Power Dissipation	P_T	—	850	mW	d
Lead Solder Temperature	260°C for 10 seconds, 1.6 mm below seating plane.				

a. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.

b. Maximum pulse width = 10 µs. This value is intended to allow for component tolerances for designs with I_O peak minimum = 4A. See the applications section for additional details on limiting I_{OH} peak.

c. Derate linearly above 85°C free-air temperature at a rate of –20 mW/°C.

d. Derate linearly above 85°C free-air temperature at a rate of –21.25 mW/°C. The maximum LED junction temperature should not exceed 125°C.

Recommended Operating Conditions

Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Note**
Operating Temperature	T_A	–40	110	°C	—
Output Supply Voltage	$(V_{DD} – V_{SS})$	15	30	V	—
Negative Output Supply Voltage	$(V_E – V_{SS})$	0	15	V	—
Positive Output Supply Voltage	$(V_{DD} – V_E)$	15	$30 – (V_E – V_{SS})$	V	—
Input Current (ON)	$I_{F(ON)}$	12	16	mA	—
Input Voltage (OFF)	$V_{F(OFF)}$	–3.6	0.5	V	—

Electrical Specifications (DC)

All typical values are at T_A = 25°C, $V_{DD} – V_E$ = 15V, and $V_E – V_{SS}$ = 15V. All minimum and maximum specifications are at recommended operating conditions (T_A = –40 to 110°C, $I_{F(ON)}$ = 12 to 16 mA, $V_{F(OFF)}$ = –3.6 to 0.5V, and $V_{DD} – V_E$ = 15V, $V_E – V_{SS}$ = 15V), unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Peak Output Current	I_{OH}	–4.0	–7.5	—	A	$V_{DD} – V_O = 15$	4, 5	a
Low Level Peak Output Current	I_{OL}	4.0	6.5	—	A	$V_O – V_{SS} = 15$	7 8	a
High Output Transistor RDS(ON)	$R_{DS,OH}$	0.5	1.1	2.1	Ω	I_{OH} = 4 A	9	b
Low Output Transistor RDS(ON)	$R_{DS,OL}$	0.2	0.7	1.3	Ω	I_{OL} = –4 A	10	b
High Level Output Voltage	V_{OH}	V_{DD} – 0.3	V_{DD} – 0.08	—	V	I_O = –100 mA	3	c, d
High Level Output Voltage	V_{OH}	—	V_{DD}	—	V	I_O = 0 mA, I_F = 14 mA	—	—
Low Level Output Voltage	V_{OL}	—	0.05	0.25	V	I_O = 100 mA	6	—
High Level Output Supply Current (V_{DD})	I_{DDH}	—	3	5	mA	I_F = 14 mA	11	—
Low Level Output Supply Current (V_{DD})	I_{DDL}	—	2.6	5	mA	V_F = 0V	11	
V_E High Level Output Supply Current	I_{EH}	–1.3	–0.75	—	mA	I_F = 14 mA	12	—
V_E Low Level Output Supply Current	I_{EL}	–1.0	–0.65	—	mA	V_F = 0V	12	—
Threshold Input Current Low to High	I_{FLH}	0.50	5	10	mA	V_O > 5 V	13	—
Threshold Input Voltage High to Low	V_{FHL}	0.5	—	—	V		—	—
Input Forward Voltage	V_F	1.2	1.5	1.85	V	I_F = 14 mA	17	—
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.5	—	mV/°C	I_F = 14 mA	—	—
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	I_R = 100 µA	—	—
Input Capacitance	C_{IN}	—	23	—	pF	f = 1 MHz, V_F = 0 V	—	—
UVLO Threshold	V_{UVLO+}	11.9	12.6	13.2	V	V_O > 5 V, I_F = 14 mA	—	—
	V_{UVLO-}	10.9	11.6	12.2				—
UVLO Hysteresis	$UVLO_{HYS}$	—	1.0	—	V	—		—

a. Maximum pulse width = 10 µs.

b. Output is sourced at –4.0A/4.0A with a maximum pulse width = 10 µs.

c. In this test, V_{OH} is measured with a dc load current. When driving capacitive loads, V_{OH} will approach V_{DD} as I_{OH} approaches zero amps.

d. Maximum pulse width = 1 ms.

Switching Specifications (AC)

All typical values are at T_A = 25°C, $V_{DD} – V_E$ = 15V, and $V_E – V_{SS}$ = 15V. All minimum and maximum specifications are at recommended operating conditions (T_A = –40 to 110°C, $I_{F(ON)}$ = 12 to 16 mA, $V_{F(OFF)}$ = –3.6 to 0.5V, $V_{DD} – V_E$ = 15 V, and $V_E – V_{SS}$ = 15V), unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	50	80	150	ns	R_g = 7.5Ω C_g = 25 nF, f = 10 kHz, Duty Cycle = 50%, I_F = 14 mA	14, 15, 18	—
Propagation Delay Time to Low Output Level	t_{PHL}	50	70	150	ns			
Pulse Width Distortion	PWD	—	—	80	ns		18	a
Propagation Delay Difference Between Any Two Parts	PDD ($t_{PHL} – t_{PLH}$)	–90	—	90	ns		18	b
Propagation Delay Skew	t_{PSK}	—	—	80	ns		18	c
Rise Time	t_R	—	26	50	ns		16, 18	—
Fall Time	t_F	—	7.5	30	ns			—
Output High Level Common Mode Transient Immunity	$\lvert CM_H \rvert$	100	—	—	kV/µs	T_A = 25°C, I_F = 14 mA, V_{CM} = 1500 V	19	d, e
Output Low Level Common Mode Transient Immunity	$\lvert CM_L \rvert$	100	—	—	kV/µs	T_A = 25°C, V_F = 0 V, V_{CM} = 1500 V		d, f

a. Pulse Width Distortion (PWD) is defined as | $t_{PHL} – t_{PLH}$ | for any given device.

b. The difference between t_{PHL} and t_{PLH} between any two ACNT-H343 parts under the same test condition.

c. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.

d. Split resistor network in the ratio 1:1 with 124Ω at the anode and 124Ω at the cathode based on 5V supply and 14 mA LED current.

e. Common mode transient immunity in the high state is the maximum tolerable dVCM/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (that is, V_O > 15.0 V).

f. Common mode transient immunity in a low state is the maximum tolerable dVCM/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (that is, V_O < 1.0 V).

Package Characteristics

Unless otherwise noted, all typical values are at T_A = 25°C; all minimum and maximum specifications are at recommended operating conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	7500	—	—	V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C	—	a, b
Input-Output Resistance	R_{I-O}	—	10^{12}	—	Ω	V_{I-O} = 500 V_{DC}	—	b
Input-Output Capacitance	C_{I-O}	—	0.5	—	pF	f =1 MHz	—	—
LED-to-Ambient Thermal Resistance	R_{11}	—	87	—	°C/W	Thermal Model in the following Application Notes	—	c
LED-to-Detector Thermal Resistance	R_{12}	—	23	—				
Detector-to-LED Thermal Resistance	R_{21}	—	30	—				
Detector-to-Ambient Thermal Resistance	R_{22}	—	47	—				

a. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 9000 Vrms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA).

b. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.

c. The device was mounted on a high-conductivity test board as per JEDEC 51-7.

Figure 3: V_{OH} Versus Temperature

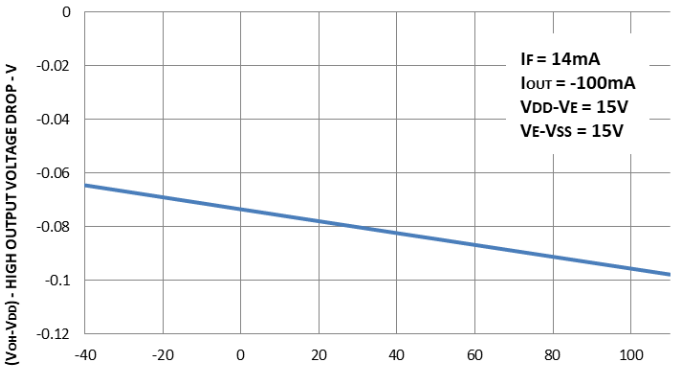


Figure 4: I_{OH} Versus Temperature

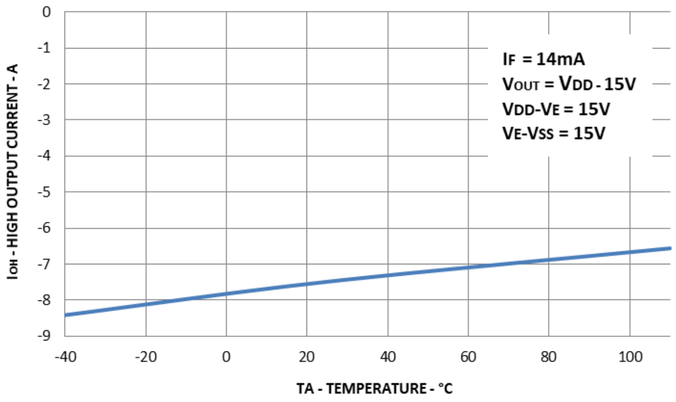


Figure 5: I_{OH} Versus V_{OH}

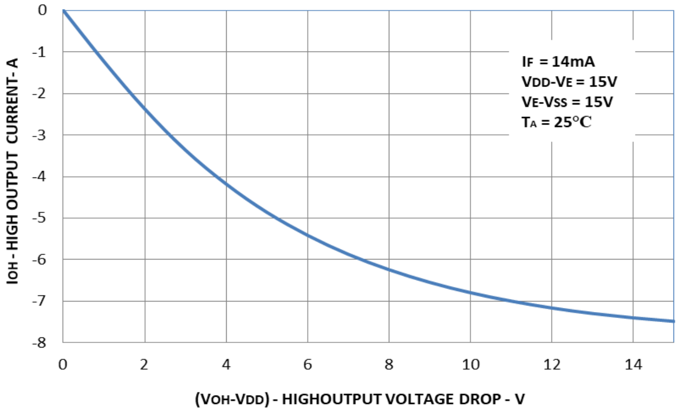


Figure 6: V_{OL} Versus Temperature

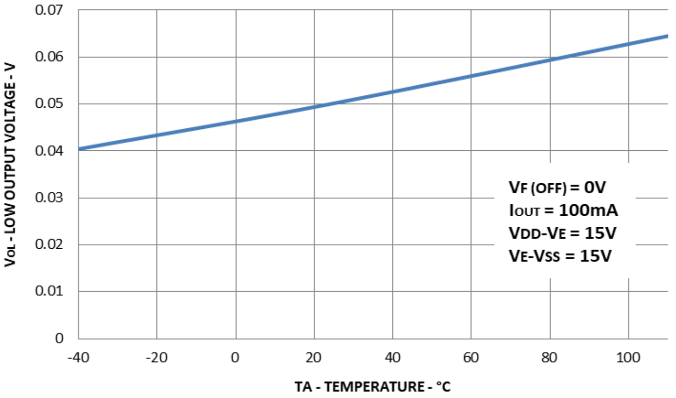


Figure 7: I_{OL} Versus Temperature

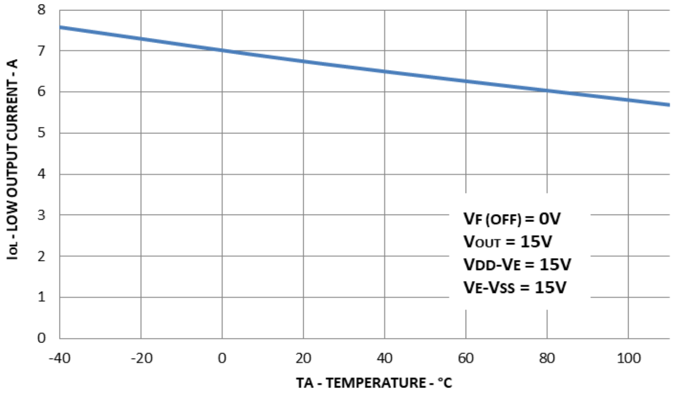


Figure 8: I_{OL} Versus V_{OL}

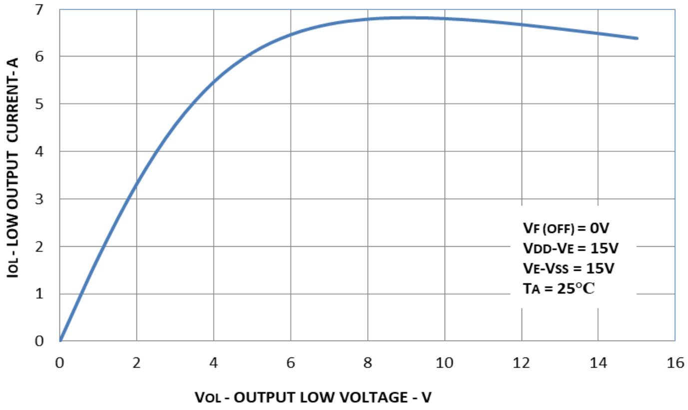


Figure 9: $R_{DS,OH}$ Versus Temperature

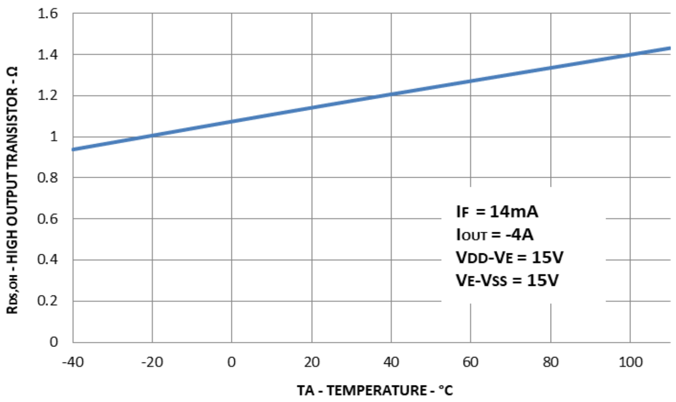


Figure 10: $R_{DS,OL}$ Versus Temperature

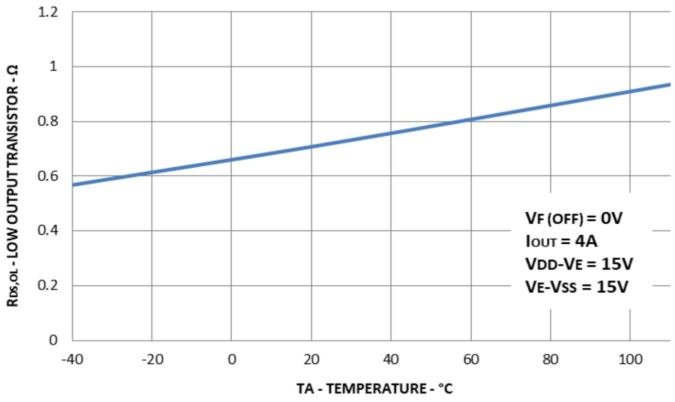


Figure 11: I_{DD} Versus Temperature

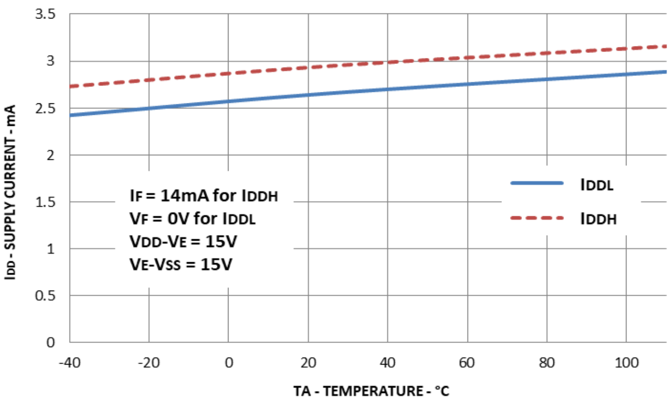


Figure 12: I_E Versus Temperature

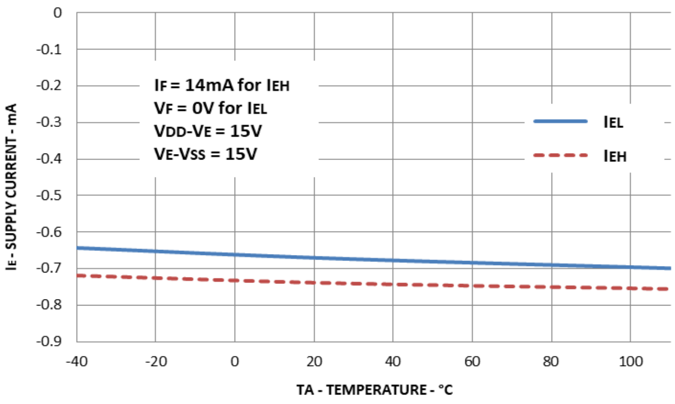


Figure 13: I_{FLH} Versus Temperature

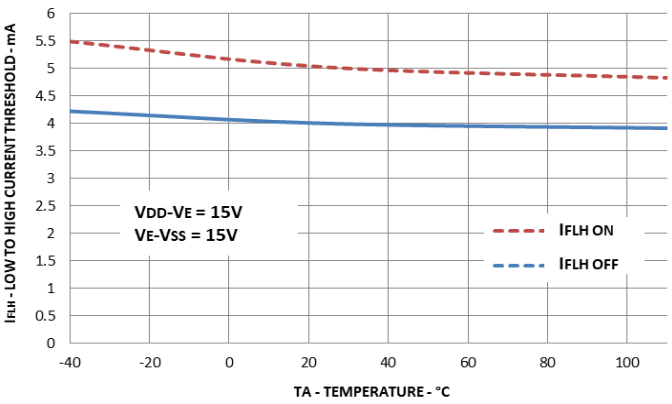


Figure 14: Propagation Delay Versus I_F

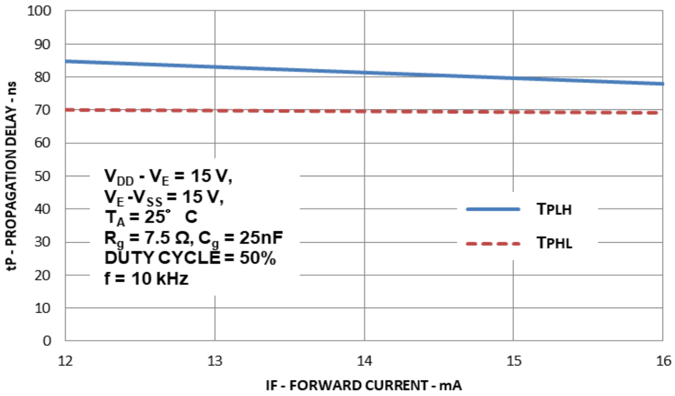


Figure 15: Propagation Delay Versus Temperature

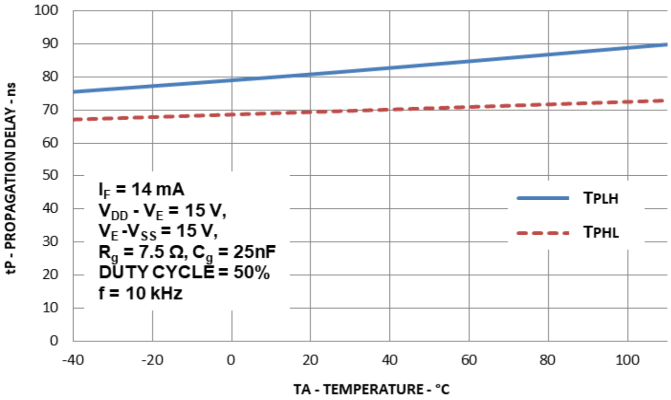


Figure 16: Rise and Fall Time Versus Temperature

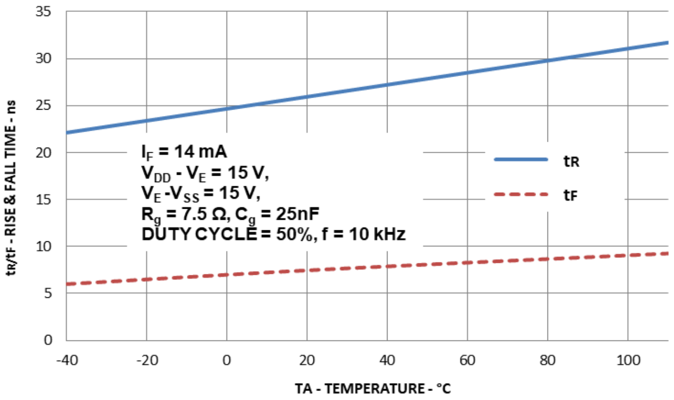


Figure 17: Input Current Versus Forward Voltage

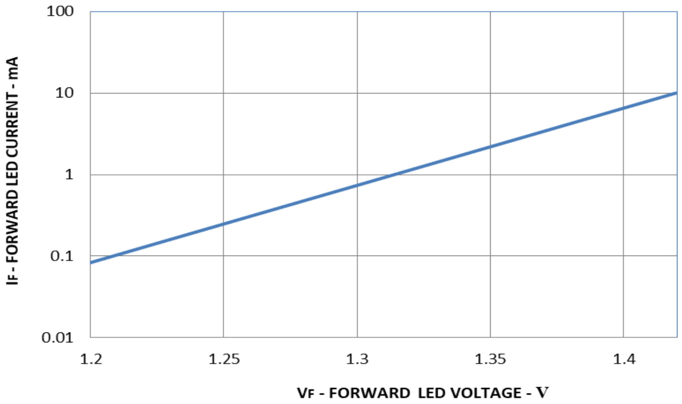


Figure 18: t_{PLH}, t_{PHL}, PWD, PDD, t_{PSK}, t_r and t_f Test Circuit and Waveforms

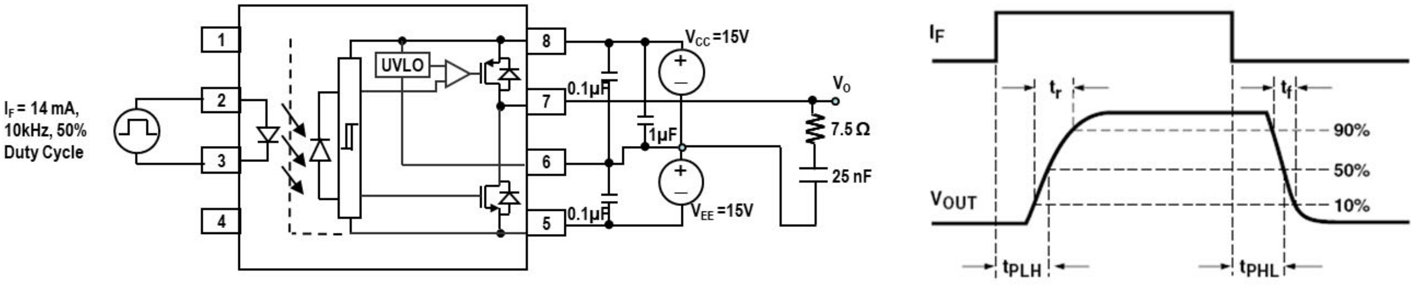
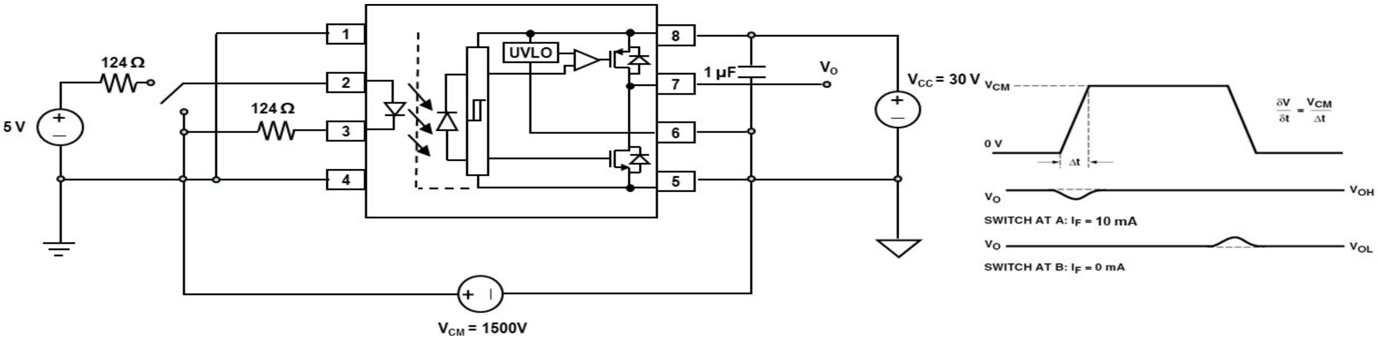


Figure 19: CMR Test Circuit with Split Resistors Network and Waveforms



Application Information

Product Overview Description

The ACNT-H343 is an optically isolated power output stage capable of driving IGBT or power MOSFET. Based on BCDMOS technology, this gate drive optocoupler delivers higher peak output current, better rail-to-rail output voltage, and faster speed than the previous generation of products.

The high peak output current and short propagation delay are needed for fast IGBT switching to reduce dead time and improve system overall efficiency. Rail-to-rail output voltage ensures that the IGBT/MOSFET's gate voltage is driven to the optimum intended level with no power loss across the IGBT/MOSFET. This helps the designer lower the system power which is suitable for bootstrap power supply operation.

The ACNT-H343 has a V_E pin that allows of use negative power supply without affecting the UVLO monitoring the positive power supply. It has very high CMR (common mode rejection) rating which allows the microcontroller and the IGBT/MOSFET to operate at very large common mode noise found in industrial motor drives and other power switching applications. The input is driven by direct LED current and has a hysteresis that prevents output oscillation if insufficient LED driving current is applied. This will eliminates the need of additional Schmitt trigger circuit at the input LED.

Recommended Application Circuit

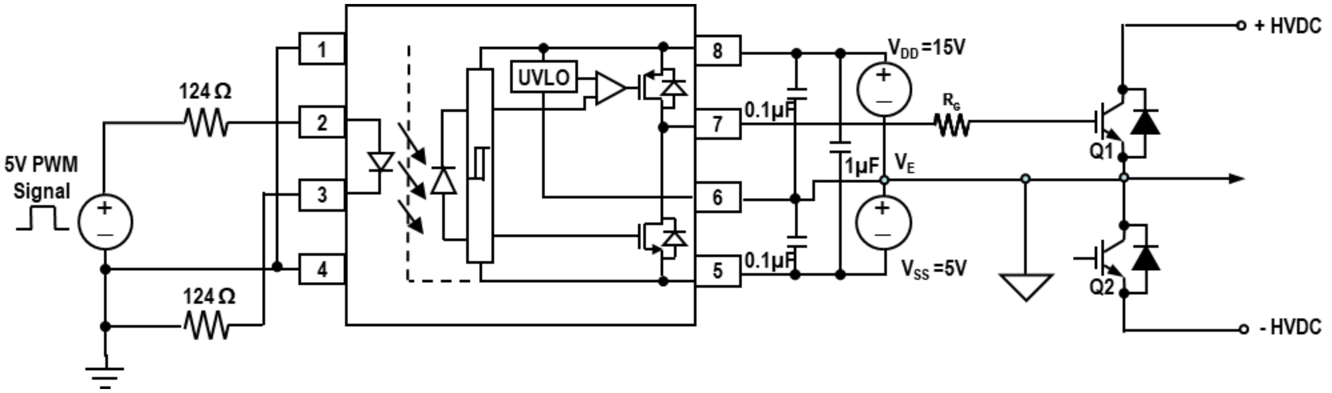
The recommended application circuit shown in the following figure illustrates a typical gate drive implementation using the ACNT-H343.

The supply bypass capacitors provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (5.0 mA) power supply will be enough to power the device. The split resistors (in the ratio of 1:1) across the LED will provide a high CMR response by providing a balanced resistance network across the LED.

The gate resistor R_G serves to limit gate charge current and controls the IGBT switching times.

In PC board design, care should be taken to avoid routing the IGBT's collector or emitter traces close to the ACNT-H343 input as this can result in unwanted coupling of transient signals into ACNT-H343 and degrade performance.

Figure 20: Recommended Application Circuit with Split Resistors LED Drive

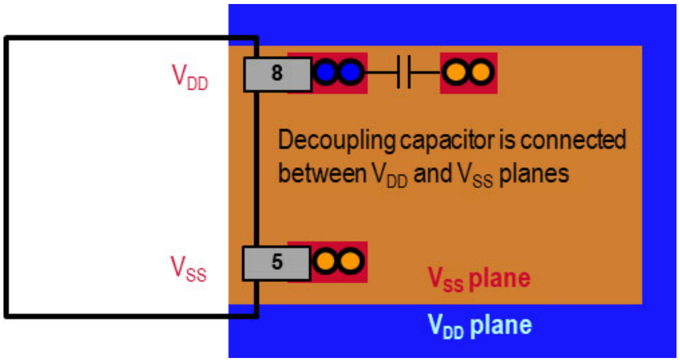


Recommended Supply and Ground Planes Layout

At 5A-rated high current switching, the decoupling capacitor must be close to the V_{DD} and V_{SS} pins.

Due to fast switching, large V_{DD} and V_{SS} planes are recommended to prevent noise by lowering the parasitic inductance.

Figure 21: Recommended Supply and Ground Planes Layout



Thermal Model for ACNT-H343 15-mm SSO8 Package Optocoupler

Definitions are as follows:

- R_{11}: Junction to Ambient Thermal Resistance of LED due to heating of LED
- R_{12}: Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)
- R_{21}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.
- R_{22}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).
- P_1: Power dissipation of LED (W).
- P_2: Power dissipation of Detector / Output IC (W).
- T_1: Junction temperature of LED (˚C).
- T_2: Junction temperature of Detector (˚C).
- T_A: Ambient temperature.
- Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25 cm above optocoupler at ~23 ˚C in still air.

Thermal Resistance	°C/W
R_{11}	87
R_{12}	23
R_{21}	30
R_{22}	47

This thermal model assumes that an 8-pin single-channel plastic package optocoupler is soldered into a 7.62 cm x 7.62 cm printed circuit board (PCB) per JEDEC standards. The temperature at the LED and Detector junctions of the optocoupler can be calculated using the following equations:

$T_1 = (R_{11} * P_1 + R_{12} * P_2) + T_A$ -- (1)

$T_2 = (R_{21} * P_1 + R_{22} * P_2) + T_A$ -- (2)