Data Sheet

ACFL-6213T

Automotive High-Speed, Low-Power Digital Optocoupler with R²Coupler™ Isolation in a Stretched 12-Pin Surface-Mount Plastic Package

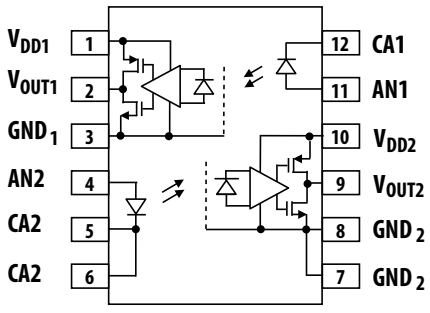
Overview

The Broadcom® ACFL-6213T is an automotive-grade dual-channel, bidirectional, high-speed digital CMOS optocoupler. The SO-12 stretched package outline is designed to be compatible with the standard surface-mount processes.

This digital optocoupler uses an insulating layer between the light-emitting diode and an integrated photo detector to provide electrical insulation between input and output. Each channel of the digital optocoupler has a CMOS detector IC with an integrated photodiode, a high-speed trans-impedance amplifier, and a voltage comparator with an output driver. Each channel is also isolated from the other.

The Broadcom R²Coupler™ provides reinforced insulation and reliability that delivers safe-signal isolation critical in automotive and high-temperature industrial applications.

Functional Diagram



NOTE: Connect a 1-µF bypass capacitor between pins 1 and 3, and pins 10 and 7/8 (or 7 and 8).

Features

- Qualified to AEC-Q100 Grade 1 test guidelines
- Automotive wide temperature range: –40°C to +125°C
- 5V CMOS compatibility
- 80 kV/µs common-mode transient immunity at V_{CM} = 1000V (typical)
- Low propagation delay: 27 ns @ I_F = 2 mA (typical)
- Compact, auto-insertable stretched SO-12 package
- Worldwide safety approval:
  - UL 1577 recognized, 5 kV_{RMS}/1 minute
  - CAN/CSA-C22.2 No. 62368-1
  - IEC/EN 60747-5-5

Applications

- Automotive IPM driver for DC-DC converters and motor inverters
- CANBus and SPI communications interface
- High-temperature digital/analog signal isolation
- Power transistor isolation

Table 1: Truth Table

LED	V_O
ON	LOW
OFF	HIGH

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage, degradation, or both that might be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Pin Description

Pin No.	Pin Name	Description
1	V_{DD1}	Primary-Side Power Supply
2	V_{OUT1}	Output 1
3	GND1	Primary-Side Ground
4	AN2	Anode 2
5	CA2	Cathode 2
6	CA2	Cathode 2

Pin No.	Pin Name	Description
7	GND2	Secondary-Side Ground
8	GND2	Secondary-Side Ground
9	V_{OUT2}	Output 2
10	V_{DD2}	Secondary-Side Power Supply
11	AN1	Anode 1
12	CA1	Cathode 1

Ordering Information

Part Number	Option (RoHS-Compliant)	Package	Surface Mount	Tape and Reel	UL 5000 V_{rms} / 1 Minute Rating	IEC/EN 60747-5-5	Quantity
ACFL-6213T	-000E	Stretched SO-12	X	—	X	—	80 per tube
	-500E		X	X	X	—	1000 per reel
	-560E		X	X	X	X	1000 per reel

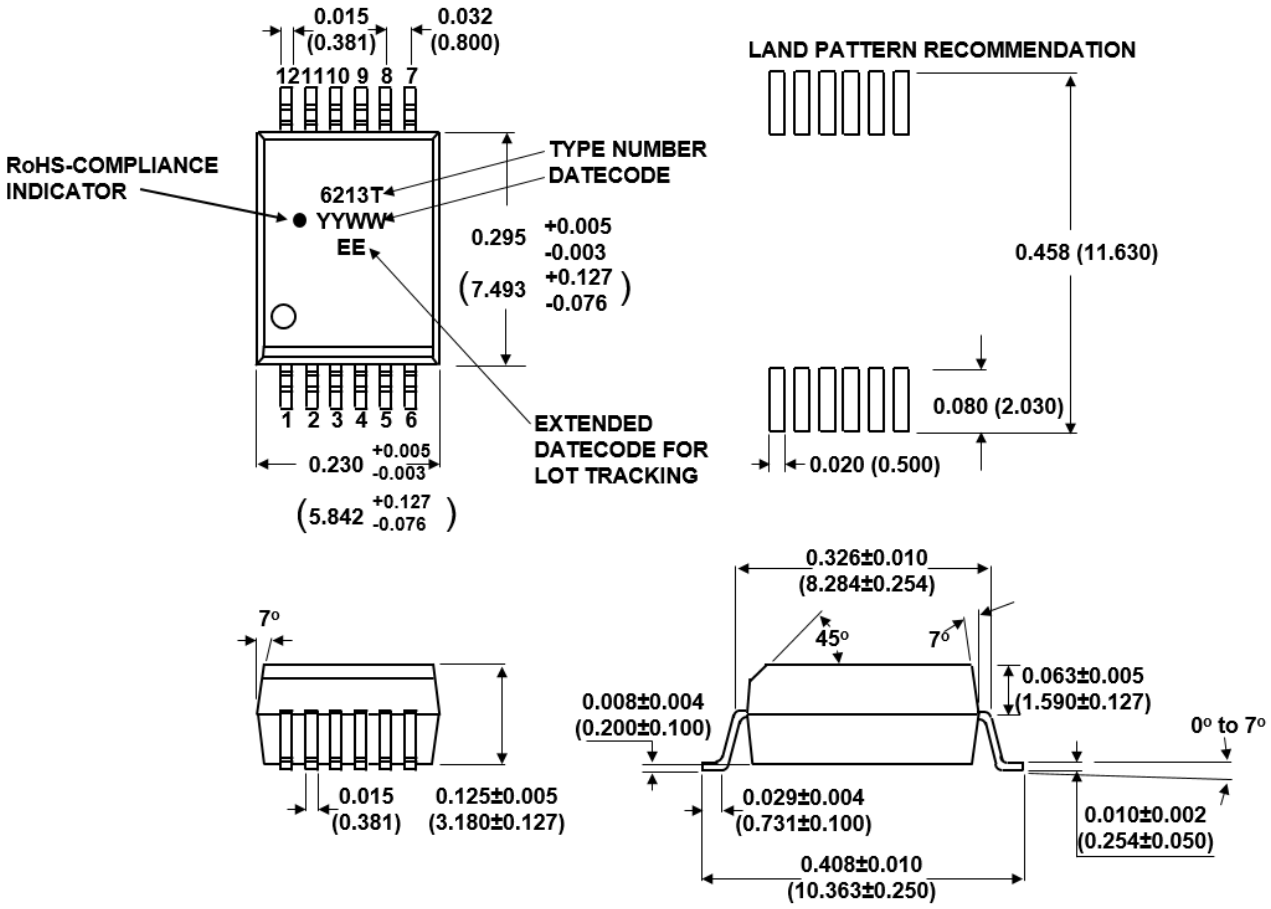
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example: Select ACFL-6213T-560E to order the product consisting of a SSO-12 surface-mount package in tape and reel packaging with IEC/EN 60747-5-5 safety approval that is RoHS compliant.

NOTE: Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawing

Figure 1: 12-Lead Surface Mount



NOTE: Dimensions are in inches (millimeters). Lead coplanarity = 0.004 inches (0.1 mm).

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Use non-halide flux.

Regulatory Information

The ACFL-6213T is approved by the following organizations.

UL	UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}
CSA	CAN/CSA-C22.2 No. 62368-1
IEC/EN	IEC/EN 60747-5-5 Maximum working insulation voltage, V_{IORM} = 1140 V_{PEAK} Highest allowable overvoltage, V_{IOTM} = 6000 V_{PEAK}

Insulation-Related and Safety-Related Specifications

Parameter	Symbol	ACFL-6213T	Unit	Conditions
Minimum External Air Gap (Clearance)	L (101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L (102)	8.5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group (DIN VDE 0109)	—	IIIa	—	Material Group (DIN VDE 0109).

IEC/EN 60747-5-5 Insulation Characteristics for Option 560E

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110/1.89, Table 1			
For Rated Mains Voltage ≤ 600 V_{rms}	—	I-III	—
Climatic Classification	—	40/125/21	—
Pollution Degree (DIN VDE 0110/1.89)	—	2	—
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{PEAK}
Input to Output Test Voltage, Method b	V_{PR}	2137	V_{PEAK}
V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial Discharge < 5 pC			
Input to Output Test Voltage, Method a	V_{PR}	1824	V_{PEAK}
V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC			
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 seconds)	V_{IOTM}	6000	V_{PEAK}
Safety-Limiting Values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$	Ω

ESD Ratings

Parameter	Classification	Note
Human Body Model	2	Per AEC Q100-002-Rev-E
Charged Device Model	C2a	Per AEC Q100-011-Rev-D

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Condition
Storage Temperature	T_S	–55	+150	°C	—
Ambient Operating Temperature	T_A	–40	+125	°C	—
Junction Temperature	T_J	—	+150	°C	—
Supply Voltages	V_{DD}	0	6.5	V	—
Output Voltage	V_O	–0.5	V_{DD} +0.5	V	—
Average Forward Input Current	I_F	—	5	mA	—
Peak Transient Input Current (I_F at 1-µs pulse width, <10% duty cycle)	$I_{F\ (TRAN)}$	—	1 80	A mA	<1-µs pulse width, 300 pps <1-µs pulse width, <10% duty cycle
Reverse Input Voltage	V_r	—	5	V	—
Input Power Dissipation	P_I	—	40	mW	—
Average Output Current	I_o	—	10	mA	—
Output Power Dissipation	P_o	—	30	mW	—

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Supply Voltage	V_{DD}	3.0	5.5	V	—
Operating Temperature	T_A	–40	125	°C	—
Forward Input Current	$I_{F\ (ON)}$	0.8	2.3	mA	—
Forward Off State Voltage	$V_{F\ (OFF)}$	—	0.8	V	—
Input Threshold Current	I_{TH}	—	0.65	mA	—

Electrical Specifications

Over recommended operating conditions. All typical specifications are at T_A = 25°C, V_{DD} = 5V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
LED Forward Voltage	V_F	1.15	1.40	1.70	V	I_F = 2 mA	Figure 2, Figure 3	
V_F Temperature Coefficient	—	—	–1.3	—	mV/°C	—	Figure 2	
Input Threshold Current	I_{TH}	—	0.20	0.65	mA	—	Figure 3	
Input Capacitance	C_{IN}	—	13	—	pF	—	—	
Input Reverse Breakdown Voltage	BV_R	5.0	—	—	V	I_R = 10 µA	—	
Logic High Output Voltage	V_{OH}	V_{DD} – 0.6	—	—	V	I_{OH} = –3.2 mA	Figure 5	
Logic Low Output Voltage	V_{OL}	—	—	0.6	V	I_{OL} = 4 mA	Figure 4	
Logic Low Output Supply Current (per channel)	I_{DDL}	—	0.9	1.3	mA	—	—	
Logic High Output Supply Current (per channel)	I_{DDH}	—	0.9	1.3	mA	—	—	
Propagation Delay Time to Logic Low Output	t_{PHL}	—	40	55	ns	V_{IN} = 5V, R_{IN} = 3.6 kΩ, (I_F = 1 mA), C_L = 15 pF	Figure 6, Figure 8, Figure 10	a, b, c
Propagation Delay Time to Logic High Output[a]	t_{PLH}	—	30	55	ns	Output low threshold = 0.8V Output high threshold = 80% of V_{DD}	—	
Pulse Width Distortion	PWD	—	10	25	ns		—	
Propagation Delay Skew	t_{PSK}	—	—	30	ns		—	
Output Rise Time (10% – 90%)	t_R	—	10	—	ns		—	
Output Fall Time (90% – 10%)	t_F	—	10	—	ns		—	
Propagation Delay Time to Logic Low Output	t_{PHL}	—	27	35	ns	V_{IN} = 5V, R_{IN} = 1.8 kΩ, (I_F = 2 mA), C_L = 15 pF	Figure 7, Figure 8, Figure 10	a, b, c
Propagation Delay Time to Logic High Output	t_{PLH}	—	27	35	ns	Output low threshold = 0.8V Output high threshold = 80% of V_{DD}		
Pulse Width Distortion	PWD	—	0	12	ns			
Propagation Delay Skew	t_{PSK}	—	—	15	ns			
Output Rise Time (10% – 90%)	t_R	—	10	—	ns			
Output Fall Time (90% – 10%)	t_F	—	10	—	ns			
Common Mode Transient Immunity at Logic High Output	$\lvert CM_H \rvert$	50	80	—	kV/µs	V_{in} = 0V, V_{CM} = 1000V, T_A = 25°C	Figure 11, Figure 12	d
Common Mode Transient Immunity at Logic High Output	$\lvert CM_L \rvert$	50	80	—	kV/µs	V_{in} = 5V, V_{CM} = 1000V, T_A = 25°C	Figure 11, Figure 12	e

a. The t_{PHL} propagation delay is measured from the 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 0.8V of V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{IN} or I_F) on the falling edge of the input pulse to the 80% level of the rising edge of the V_O signal.

b. The PWD is defined as $|t_{PHL} – t_{PLH}|$.

c. The t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is seen between units at any given temperature within the recommended operating conditions.

d. The CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output remains in a high logic state.

e. The CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output remains in a low logic state.

Package Characteristics

All typical specifications are at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{rms}	RH ≤ 50%, t = 1 minute T_A = 25°C	a, b
Input-Output Resistance	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500V_{DC}	a
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f = 1 MHz, T_A = 25°C	a

a. Device considered a two terminal device: pins 1 to 6 shorted together, and pins 7 to 12 shorted together.

b. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second.

Typical Performance Plots

Figure 2: Typical Diode Input Forward Current Characteristic

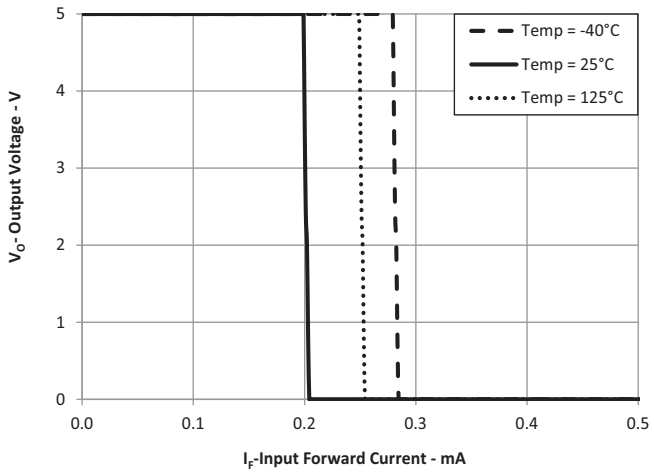


Figure 3: Typical Output Voltage vs. Input Forward Current

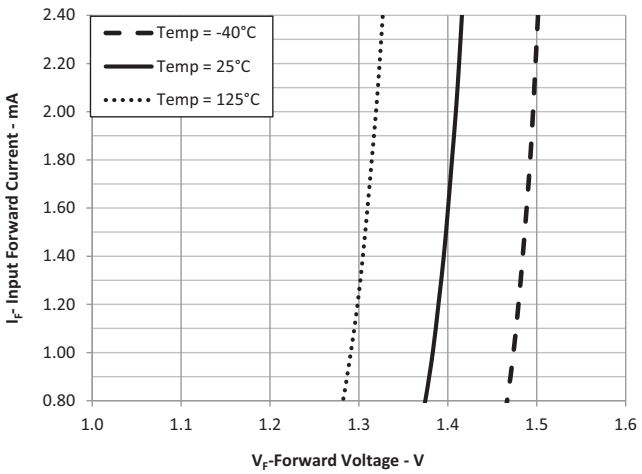


Figure 4: Typical Logic Low Output Voltage vs. Logic Low Output Current

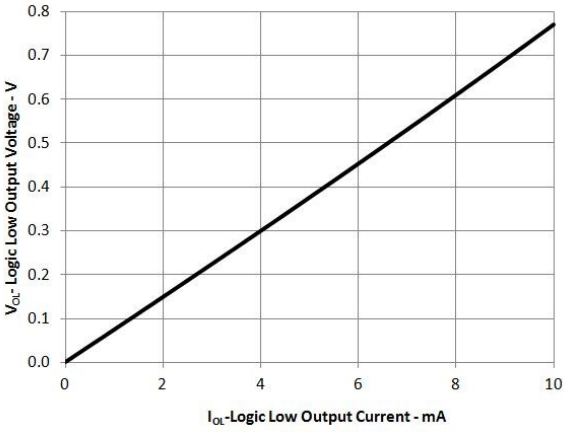


Figure 5: Typical Logic High Output Voltage vs. Logic High Output Current

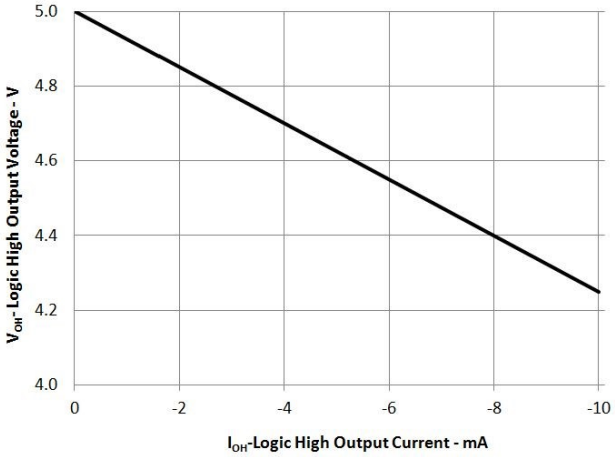


Figure 6: Typical Propagation Delay vs. Temperature Test Condition: I_F = 1 mA

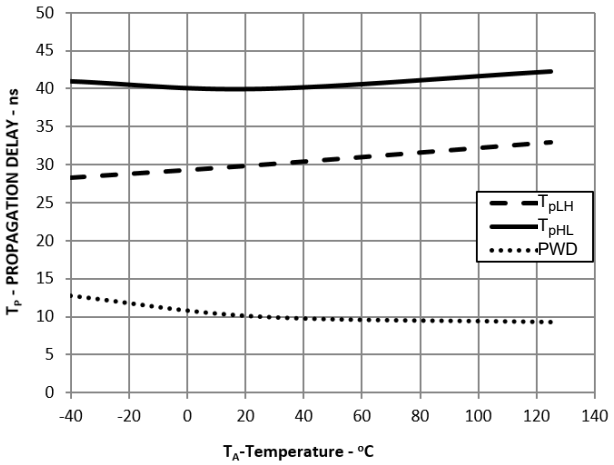


Figure 7: Typical Propagation Delay vs. Temperature Test Condition: I_F = 2 mA

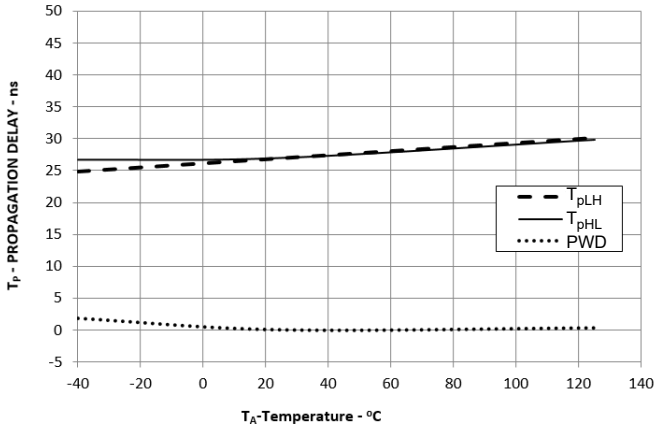
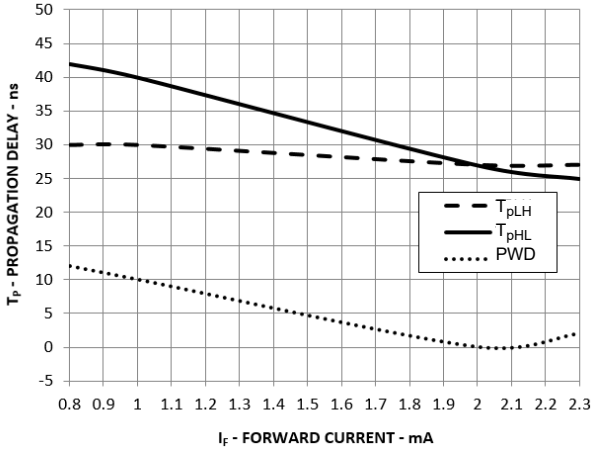
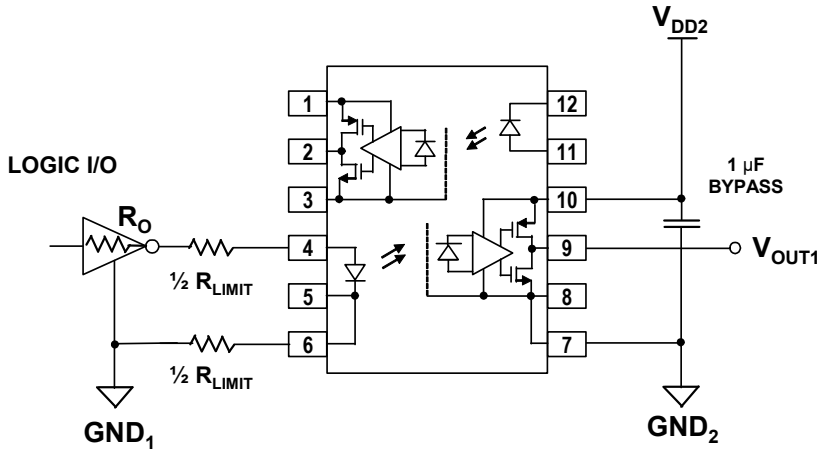


Figure 8: Typical Propagation Delay vs. Input Forward Current



Application Circuits

Figure 9: Recommended Application Circuit

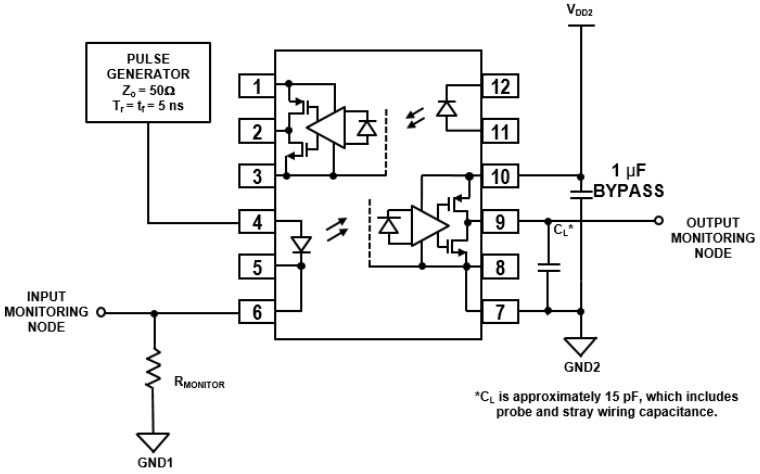


TRUTH TABLE

INPUT	LED	OUTPUT
L	ON	L
H	OFF	H

Test Circuits

Figure 10: Test circuit for t_{PHL}, t_{PLH}, t_F, and t_R



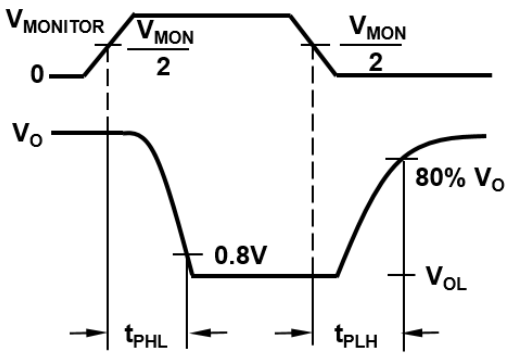


Figure 11: Common Mode Transient Immunity Test (Channel 1)

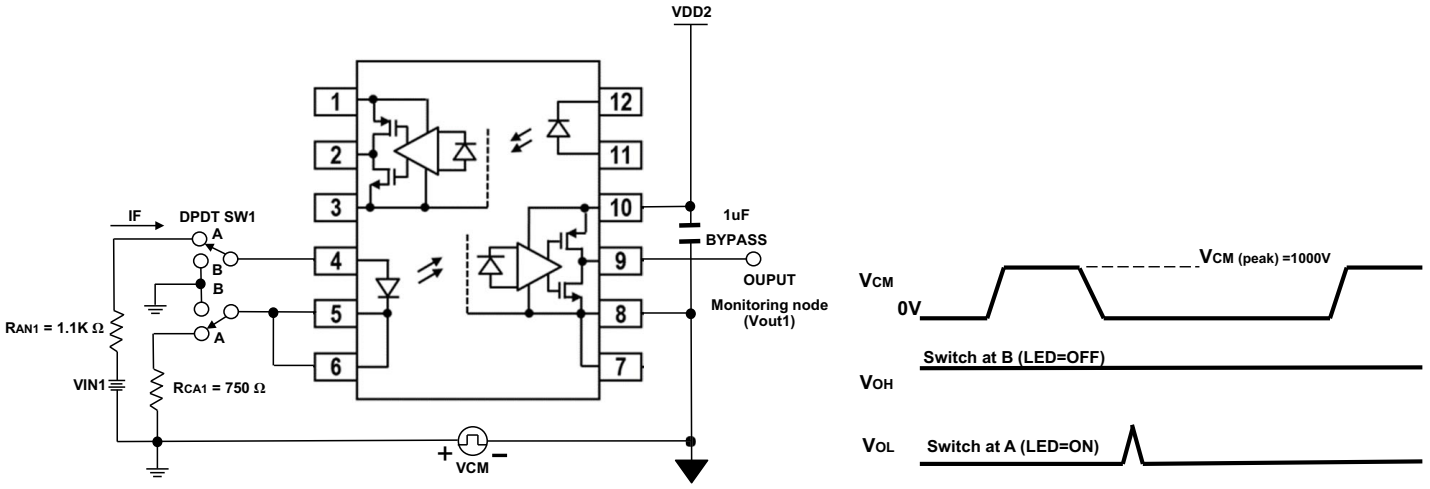
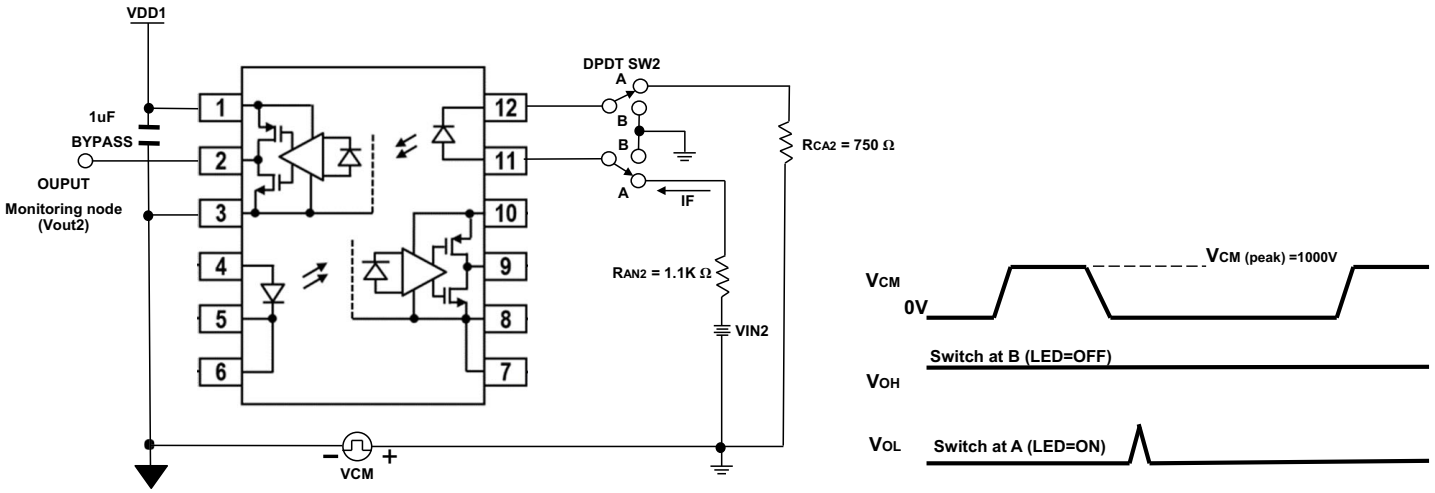


Figure 12: Common Mode Transient Immunity Test (Channel 2)



Thermal Resistance Measurement

The diagram of ACFL-6213T for measurement is shown in Figure 13. This is a multi-chip package with four heat sources, the effect of heating of one die due to the adjacent dice are considered by applying the theory of linear superposition. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated and all the dice temperatures are recorded and so on until the fourth die is heated. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4×4 matrix for our case of two heat sources.

$$\begin{vmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{vmatrix} \times \begin{vmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{vmatrix}$$

R_{11}: Thermal Resistance of Die1 due to heating of Die1 (°C/W)
R_{12}: Thermal Resistance of Die1 due to heating of Die2 (°C/W)
R_{13}: Thermal Resistance of Die1 due to heating of Die3 (°C/W)
R_{14}: Thermal Resistance of Die1 due to heating of Die4 (°C/W)

R_{21}: Thermal Resistance of Die2 due to heating of Die1 (°C/W)
R_{22}: Thermal Resistance of Die2 due to heating of Die2 (°C/W)
R_{23}: Thermal Resistance of Die2 due to heating of Die3 (°C/W)
R_{24}: Thermal Resistance of Die2 due to heating of Die4 (°C/W)

R_{31}: Thermal Resistance of Die3 due to heating of Die1 (°C/W)
R_{32}: Thermal Resistance of Die3 due to heating of Die2 (°C/W)
R_{33}: Thermal Resistance of Die3 due to heating of Die3 (°C/W)
R_{34}: Thermal Resistance of Die3 due to heating of Die4 (°C/W)

R_{41}: Thermal Resistance of Die4 due to heating of Die1 (°C/W)
R_{42}: Thermal Resistance of Die4 due to heating of Die2 (°C/W)
R_{43}: Thermal Resistance of Die4 due to heating of Die3 (°C/W)
R_{44}: Thermal Resistance of Die4 due to heating of Die4 (°C/W)

P_1: Power dissipation of Die1 (W)
P_2: Power dissipation of Die2 (W)
P_3: Power dissipation of Die3 (W)
P_4: Power dissipation of Die4 (W)

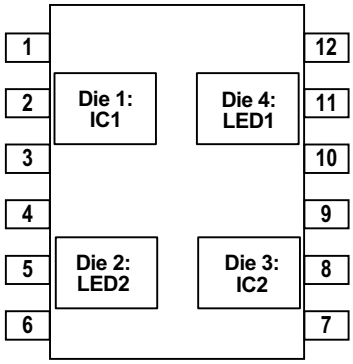
T_1: Junction temperature of Die1 due to heat from all dice (°C)
T_2: Junction temperature of Die2 due to heat from all dice (°C)
T_3: Junction temperature of Die3 due to heat from all dice (°C)
T_4: Junction temperature of Die4 due to heat from all dice (°C)

T_a: Ambient temperature.

ΔT_1: Temperature difference between Die1 junction and ambient (°C)
ΔT_2: Temperature deference between Die2 junction and ambient (°C)
ΔT_3: Temperature difference between Die3 junction and ambient (°C)
ΔT_4: Temperature deference between Die4 junction and ambient (°C)

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + T_a \quad (1)$$
$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + T_a \quad (2)$$
$$T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + T_a \quad (3)$$
$$T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + T_a \quad (4)$$

Figure 13: Diagram of ACFL-6213T for Measurement



Thermal Resistance Calculation	Measurement Data on a Low Conductivity (K) Board	Measurement Data on a High Conductivity (K) Board
R_{11}	181°C/W	117°C/W
R_{21}	103°C/W	37°C/W
R_{31}	82°C/W	35°C/W
R_{41}	110°C/W	47°C/W
R_{12}	91°C/W	42°C/W
R_{22}	232°C/W	161°C/W
R_{32}	97°C/W	53°C/W
R_{42}	86°C/W	30°C/W
R_{13}	85°C/W	32°C/W
R_{23}	109°C/W	39°C/W
R_{33}	180°C/W	114°C/W
R_{43}	101°C/W	29°C/W
R_{14}	112°C/W	60°C/W
R_{24}	91°C/W	33°C/W
R_{34}	91°C/W	34°C/W
R_{44}	277°C/W	189°C/W