# ACFL-3161

## TO-247 SiC MOSFET EB1200-3161 Evaluation Board

**Reference Manual**
**Version 1.0**

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# ACFL-3161: TO-247 SiC MOSFET EB1200-3161 Evaluation Board

## 1 Introduction

Evaluation board EB1200-3161 features Broadcom® dual output isolated gate drive optocouplers, ACFL-3161, that drive SiC MOSFETs in a discrete TO-247 package. The board features an integrated capacitor DC Bus with optimized layout that minimizes the commutation loop inductance and shunt-based source current measurement. The EB1200-3161, shown in Figure 1, is developed to support Broadcom customers during their first steps in designing power converter applications with ACFL-3161 drivers. Properties of the board are described in the following sections.

Components were selected considering lead-free reflow soldering. The design was tested and verified with basic measurements described in this document, but it is not qualified for the operation in the entire operating temperature range or lifetime. The board was subjected to functional testing only.

**Figure 1: Evaluation Gate Driver Board EB120-3161**


With adequate adjustments regarding gate resistors and the isolated auxiliary power supply, the EB1200-3161 supports devices from different manufacturers in the same packaging, rated up to 1200V and having the same pin assignment.

## 1.1 Design Features

The EB1200-3161 includes the following main features:

- Two isolated ACFL-3161 gate drive optocouplers with following features:
  - UVLO (under voltage lockout) protection
  - Dual output drive to control turning on and off transients
- Electrically and mechanically suitable for TO-247 4 pin packages
- With adjustment of the gate resistors and isolated auxiliary power supply, the evaluation board supports the following SiC MOSFETs:
  - STM SCTWA70N120G2V4
  - Wolfspeed C3M0021120K
- DC Bus and balancing/discharge resistors
- Isolated SMPS for gate drivers
- Resistor shunt-based, low side switch current measurement over the BNC interface
- Access to PWM input signals.
- Continuous operation in buck/boost configuration up to 3-kW output power and 50-kHz switching frequency. The user must provide and integrate an appropriate heat sink in case of continuous operation.

## 1.2 Target Applications

The Broadcom ACFL-3161 gate drive optocouplers target the following applications:

- Motor drive for industrial automation and robotics
- Power supply and battery charger
- Renewable energy inverter and storage.

## 1.3 Warnings

The board operates at high voltages. Take care to avoid risk of injury and endangering of life. While operating the board, take into consideration the following safety precautions:

- If the board is powered up, do not touch the board, especially exposed metal parts.
- Pay attention to the maximum ratings.
- Use of a protection cover made of insulating materials is mandatory.
- If the board is used to drive continuous load, mount an appropriately sized heat sink on the SiC semiconductors. The board may rise to high temperatures, and any contact with the human body must be avoided.
- Whenever a change in the test setup is performed (for example, changing the probe position), turn off the power supply and ensure that the DC Bus is fully discharged to avoid injuries and the destruction of the board.
- The board itself does not provide dead-time generation. The recommended minimal dead time is 300 ns.

# 2 System Description

This section provides essential electrical and mechanical specifications of the EB1200-3161 evaluation board.

## 2.1 Key Specifications

Absolute maximum ratings of the EB1200-3161 evaluation board are listed in Table 1. Note that this table contains only key parameters related to the EB1200-3161. Constraints from the ACFL-3161 data sheet, as well as specification of other key components, must be considered when the EB1200-3161 is used.

**Table 1: Absolute Maximum Ratings of the EB1200-3161**

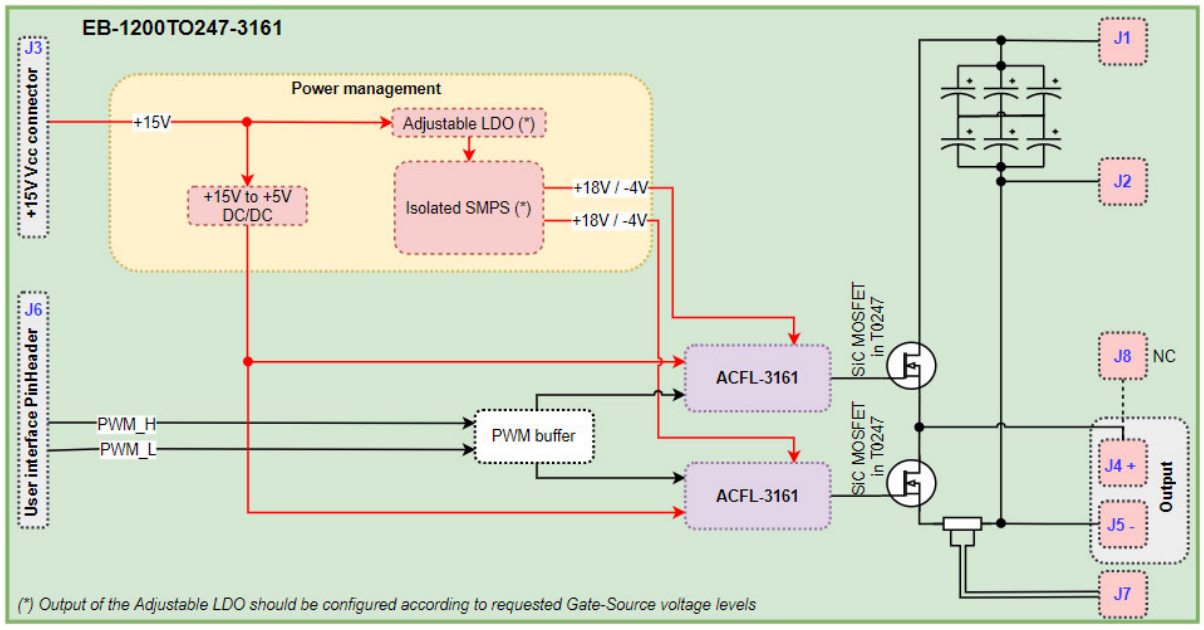
| Parameter | Values | | | Units | Notes |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| DC Bus supply voltage | — | 600 | 800 | V | Limited by the DC Bus capacitors' voltage rating |
| MOSFET half-bridge output current (RMS) | — | 15 | 30 | A | Limited by the PCB copper traces |
| $V_{cc}$ input voltage | 15 | 15 | 15 | V | External DC input power supply for digital circuitry. Limited by the SMPS range for gate drivers. |
| PWM logic input level | 0 | 3.3 | 5 | V | External PWM inputs for gate drivers. |

## 2.2 Functional Block Diagram

The functional block diagram and disposition of the functional blocks of the EB1200-3161 gate driver evaluation board are shown in Figure 2 and Figure 3. The block diagram shows several functional blocks:

- Power management:
  - +15V/+12V LDO
  - +15V/+5V step-down DC/DC regulator
- Isolated SMPS with two dual outputs (one for the high side driver and one for the low side driver)
- High and low side ACFL-3161 gate drivers with circuitry
- DC Bus and balancing resistors for the voltage symmetry
- DC Bus supply terminals
- User interface connector
- +15V $V_{cc}$ power supply connector
- Half-bridge output terminal

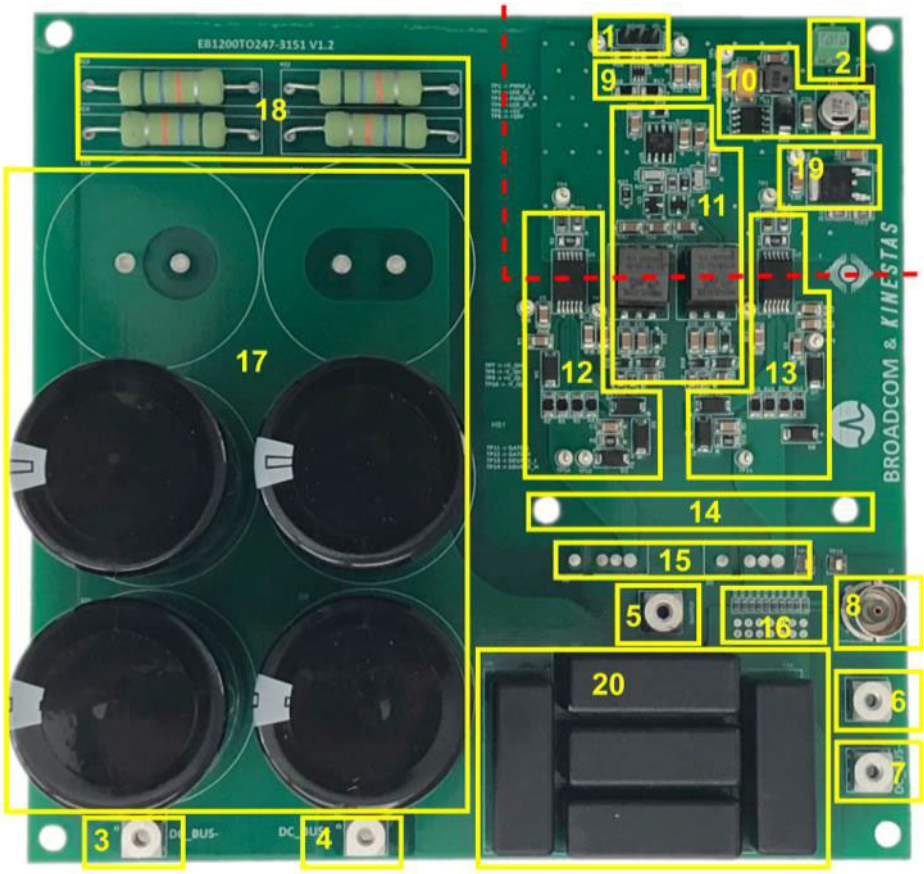
**Figure 2: Functional Block Diagram of the EB1200-3161**



According to Figure 3, marked functional blocks are as follows:

1. J6 – PWM input
2. J3 – Aux supply +15V
3. J2 – Power connector DC_Bus +
4. J1 – Power connector DC_Bus -
5. J4 – Power connector Phase Output
6. J8 – NC
7. J5 – Power connector DC_Bus -
8. J7 – BNC interface for low side switch current measurement
9. PWM buffering
10. Switched power supply 15V/5V
11. Isolated SMPS for gate drivers
12. High side SiC MOSFET driver based on the ACFL-3161
13. Low side SiC MOSFET driver based on the ACFL-3161
14. Mounting holes for heatsink
15. SiC MOSFETs
16. Resistor shunts for low side switch current measurement
17. DC Bus electrolytic capacitors
18. Balancing resistors
19. Adjustable LDO
20. DC Bus filtering support – film capacitors

**Figure 3: Functional Blocks Disposition of the EB1200-3161. The isolation border is marked with red dashes.**




## 2.3 Pin Assignment

Pin assignments for all connectors on the EB1200-3161 are listed in the following paragraphs.

### 2.3.1 Power Interface

The J3 power supply connector supplies all ICs and provides the gate driver voltage supply, and its pin assignment is shown in Table 2. Four screw terminals (J1, J2, J5, J4) connect the DC Bus voltage and the output of the half-bridge (the AC output of the MOSFET half-bridge). To enable easy connection with the connector J4, one more auxiliary NC screw connector J8 is placed, intended to provide galvanic extension of the half-bridge output by involving the bridge wire. Table 3 lists the functions for each of the mentioned connectors.

**Table 2: Pin Assignment of Connector J1 (Power Supply Connector)**

| Pin | Label | Function |
|---|---|---|
| 1 | +V_SUPPLY | External power supply for low voltage side. |
| 2 | GND | Ground. |

**Table 3: Power Connectors J1, J2, J4, J5, J8**

| Designator | Label | Function |
|---|---|---|
| J1 | DC+ | DC Bus power supply – positive terminal |
| J2 | DC- | DC Bus power supply – negative terminal |
| J4 | OUTPUT | AC output of the half-bridge MOSFET module (switching node) |
| J5 | DC- | DC Bus negative power supply |
| J8 | NC | Auxiliary place holder connector |

### 2.3.2 Signal Interface

Table 4 lists the pin assignments of connector J6.

**Table 4: Pin Assignment of Pin-Header J6**

| Pin | Label | Function | Direction |
|---|---|---|---|
| 1 | PWM_L | PWM signal for low side driver | Input |
| 2 | GND | Ground | Bidirectional |
| 3 | PWM_H | PWM signal for high side driver | Input |

## 2.4 Mechanical Data

Table 5 lists the basic mechanical data of the evaluation board.

**Table 5: Mechanical Characteristics of the EB1200-3161 Evaluation Board**

| Description | Value |
|---|---|
| Number of layers | 4 |
| PCB copper thickness | 70 µm to all layers |
| PCB insulating material | FR4 |
| Board length | 160 mm |
| Board width | 155 mm |
| Board height | 65 mm |
| PCB thickness | 1.6 mm |

# 3 Circuit Description

This section provides an in-depth insight of the EB1200-3161 gate driver evaluation board features.

## 3.1 Power Management

Figure 4 shows the auxiliary power management block diagram of the EB1200-3161. The evaluation board, by default, is supplied from an external +15V source.

The EB1200-3161 is equipped with a nonisolated switch mode power supply (SMPS), which provides 5V for the ICs on the low voltage side. The 15V/5V power supply is realized with an LM2674 DC-DC switching regulator, as shown in Figure 5. The +5V output supplies the low voltage side of the ACFL-3161 gate drivers and the isolated SMPS controller IC. The +5V power supply can drive a 500-mA load and supply all ICs on the board.

**Figure 4: Power Management**

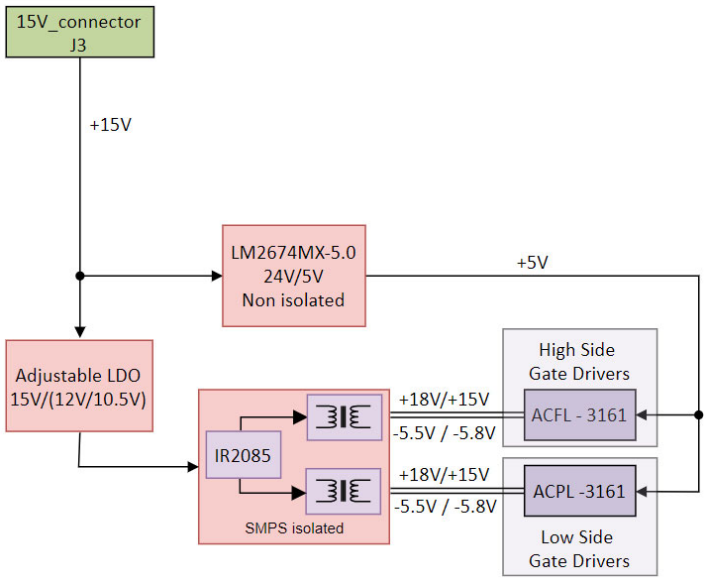
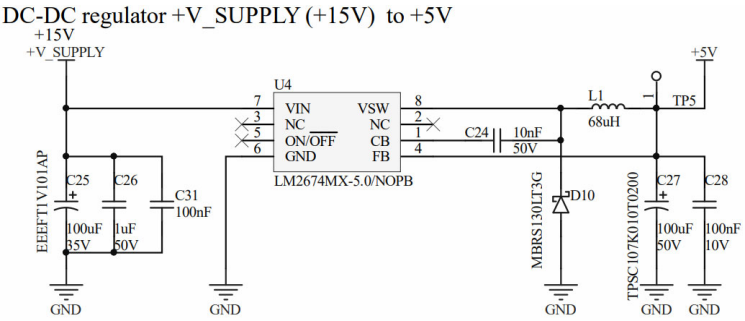



**Figure 5: Step-Down Voltage Regulator 15V/5V**




The power for the high voltage side of the gate drivers is realized with the isolated SMPS, which provides two dual outputs of +18V(+15V) and -5.5V(-5.8V).

Because SiC MOSFETs from various manufacturers have different recommended gate voltage levels, the power supply for the gate driver high voltage side is configurable. Two board adjustments must be set before the board is used:

- Configure the input voltage of the isolated SMPS by the adjusting the feedback resistor R43 of the adjustable LDO voltage regulator, Figure 6. The output of the adjustable LDO LD1086 is calculated as follows:

$$V_o = 1.25V \cdot \left(1 + \frac{R_{43}}{120}\right)$$

  The minimum value for $V_o$ is limited by isolated SMPS on 10V. Do not adjust $V_o$ less than 10V to avoid unexpected board behavior.
- Place the Zener diodes D12 and D17 in the output stage of the SMPS, which defines the positive gate driver voltage, Figure 7. Use diodes with Zener voltage equal with recommended positive gate voltage level.

**Figure 6: Adjustable LDO +15V/(+10V... 12V)**

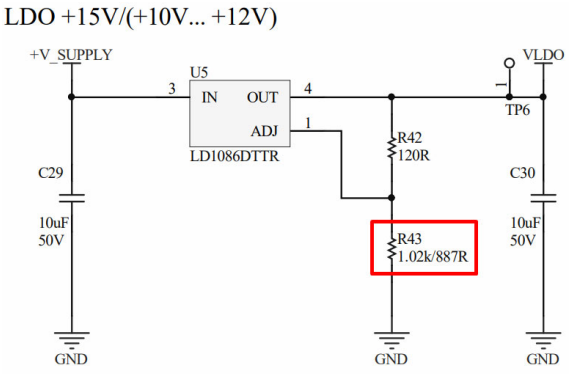
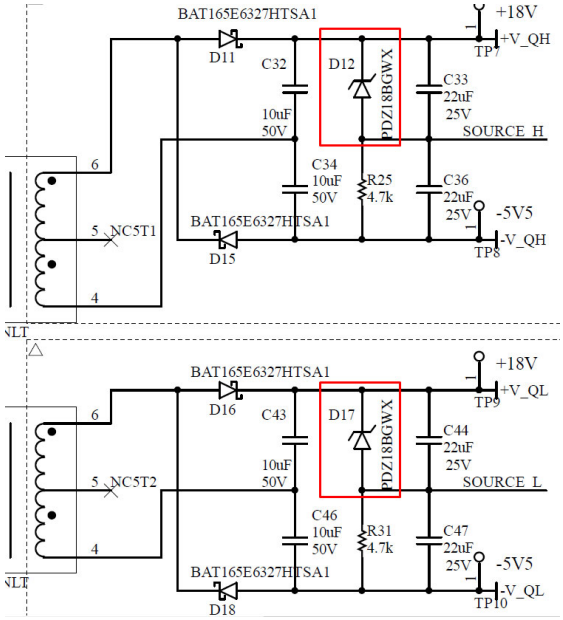



**Figure 7: Output Stage of the Isolated SMPS**



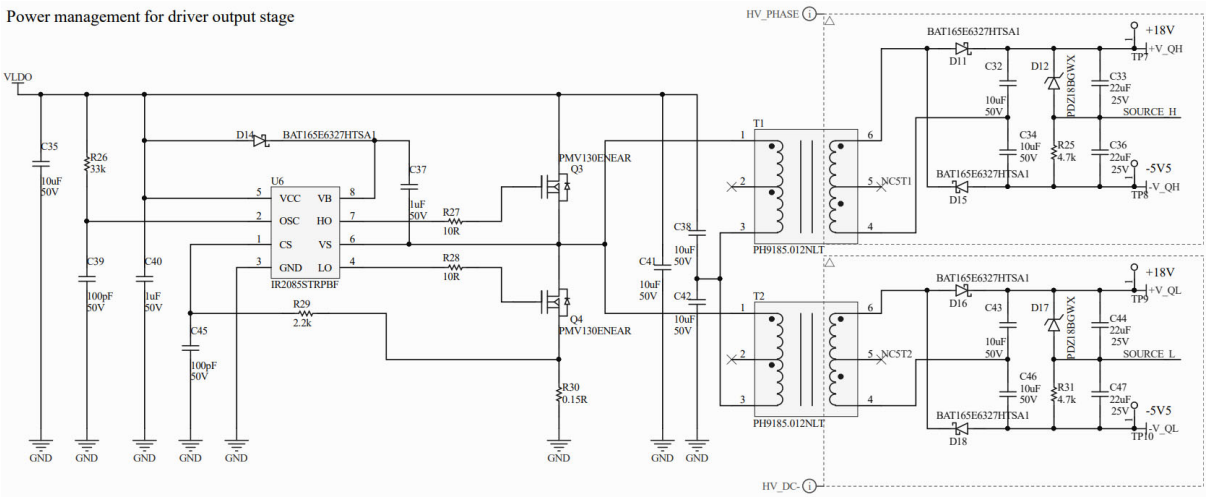

The isolated SMPS circuitry is shown in Figure 8. SMPS is based on IR2085 self-oscillating half-bridge gate driver and two transformers with a 1:2 ratio. The output voltage of the isolated SMPS is adjusted by correctly selecting the Zener diodes D12 and D17.

Table 6 shows the recommended power supply configurations for the SCTWA70N120G2V4 and C3M0021120K.

**Table 6: Power Supply Configurations**

| Device | Vgs_pos | Vgs_neg | R43 | D12 and D17 |
|---|---|---|---|---|
| SCTWA70N120G2V4 | +18V | -5.5V | 1.02k | 18V Zener diode |
| C3M0021120K | +15V | -5.8V | 887R | 15V Zener diode |

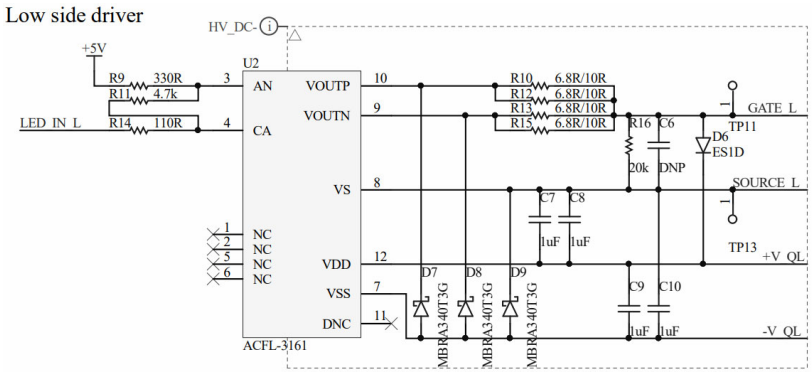
**Figure 8: Isolated SMPS for Gate Driver Output Stage**




## 3.2 Gate Driver Circuit

This section describes the gate driver circuitry on the EB1200-3161, which is shown in Figure 9.

**Figure 9: ACFL-3161 Gate Driver Circuitry**



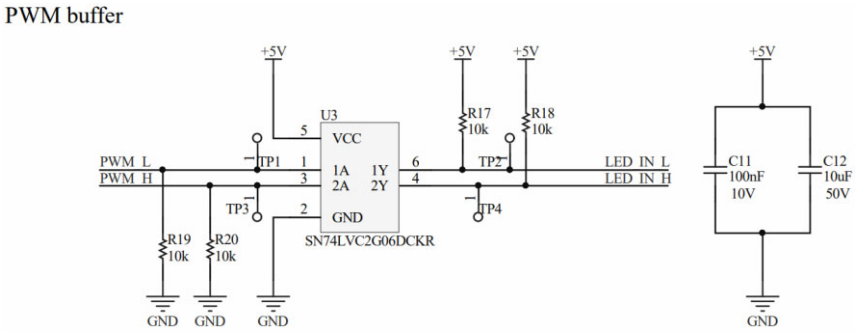

The ACFL-3161 driver is a 10A peak, rail-to-rail output gate drive optocoupler. The ACFL-3161 comes in a compact, surface-mountable SO-12 package to save space. It provides an isolation voltage of 5-kV RMS between input and output channels. The ACFL-3161 has high peak driving current capability to ensure optimum performance for direct driving SiC MOSFETs or IGBTs in various applications. The ACFL-3161 features fast propagation delay and tight dead time distortion that makes it ideal for driving SiC MOSFETs and IGBTs at high frequency DC-DC and AC-DC converter applications. Broadcom isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

The low voltage side of the gate drive circuitry contains resistors for preconditioning the input signal for the LED anode and cathode.

The resistor responsible for the LED forward current setting is split in two, and those resistors are placed on anode pin 3 and cathode pin 4 to balance the common mode impedances at the LED's anode and cathode. This helps to equalize the common mode voltage change. Resistors values are selected as referred in data sheet of the gate driver.

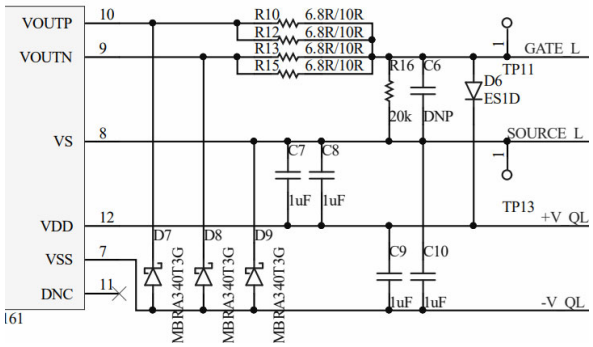
While the input LED is directly polarized and there is no UVLO fault, the turn-on command is transferred to the high-voltage side and VOUTP pin of ACFL-3161 will set high. External PWM signals that propagate through user interface connector are buffered with inverting buffer IC, as it is shown on Figure 10. As buffer is featuring an open drain output, inputs of the buffer are pulled down while outputs of the buffer are pulled high, to ensure that MOSFET module is off in case that input PWM input signals are in high impedance states. ANODE pin is pulled high via resistor R9. Buffered input signal LED_IN_L is connected to the CATHODE pin. When the input PWM signal is set high, buffered LED_IN_L signal is low LED is directly polarized and MOSFET is turned on. In case then input PWM signal is set to low, signal LED_IN_L is high, voltage across LED and two resistors is low, therefore LED is not conducting and the MOSFET is in off state.

**Figure 10: PWM Buffer**




The secondary side of the gate drive circuitry, shown on Figure 11, includes separate turn-on and turn-off outputs that are connected to the gate of the SiC MOSFET device through two parallel turn-on resistors R10 and R12 and two parallel turn-off resistors R13 and R15

**Figure 11: Gate Driver Circuit: High-Voltage Side**




When the gate driver input is set to high, VOUTP becomes high and +18V(+15V) is supplied to the MOSFET gate through two 10Ω (default value) parallel resistors. When the gate driver input is set to low, VOUTN pin becomes active and -5.5V(-5.8V) is supplied to the MOSFET gate through two 10Ω (default value) parallel resistors, and when VOUTN is low -5.5V is connected to the MOSFET gate. These voltages are referred to the source of the respective MOSFET. The switching time is determined by the gate charging and discharging process. Smaller gate resistors lead to the higher peak gate current that decreases turn-on and turn-off time, subsequently reducing switching losses. However, small gate resistors may introduce voltage spikes and current oscillations on the MOSFET or can overload the gate driver IC. For the proper selection of the gate resistors, several criteria must be fulfilled.

First is the limit of the gate peak current. Consider the MOSFET internal $R_{Gint}$ when calculating the ideal value for the gate resistor and internal minimum turn on resistance of driver $R_{VOUTP}$. The data sheet for the ACFL-3161 provides the equation for the gate resistor calculation.

$$R_G \geq \frac{V_{DD2}-V_{SS2}}{I_{O(PEAK)}} - R_{Gint} - R_{VOUTP}$$

The next step in choosing the correct gate resistor is checking the power dissipation of ACFL-3161 gate driver. If the power dissipation is too high, increase the resistance of the gate resistor. For instructions on choosing the gate resistor, consider the data sheet for the ACFL-3161.

Finally, measure the switching performance, especially turn-off speed, because the fast-switching transients in combination with parasitic inductances in the switching loop can generate high overvoltages and oscillations.

To ensure the previous constraints during the worst-case conditions, the EB1200-3161 comes with 5Ω equivalent gate resistors for positive and 5Ω equivalent gate resistor for negative gating. Both resistances are realized with two parallel resistors to increase the power dissipation capacity of the gate circuit. In addition, the evaluation board enable Broadcom customers to evaluate the switching characteristics of the semiconductors by changing or combining turn-on and turn-off resistors.

Additionally, place clamping diodes D7, D8, and D9 to clamp the eventual overvoltage on the gate driver IC pins that might occur during switching transients. ESD diode D6 provides additional protection of the MOSFET gate pin.

### 3.2.1 Protection Features

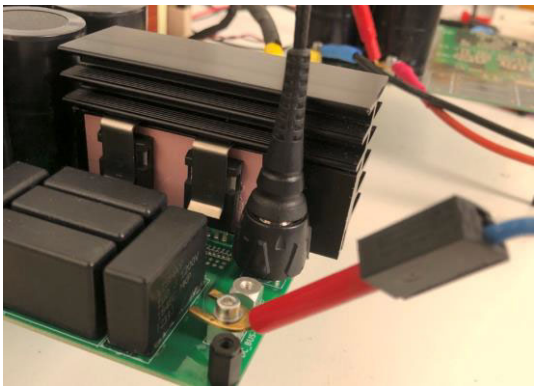
#### UVLO

Insufficient gate voltage on the MOSFET during turn-on phase can increase the voltage drop across the MOSFET. This results in a large power loss and MOSFET damage due to high heat dissipation. The ACFL-3161 monitors the output power supply constantly. If the power supply voltage is lower than UVLO threshold, driver output turns off to protect the MOSFET from low voltage bias.

### 3.2.2 Switch Current Measurement

The EB1200-3161 is equipped with the planar current measurement shunt placed between the power source and DC-. The planar shunt is realized by placing 10 pieces of 1Ω SMD resistors in parallel, which results in the shunt resistance of 100 mΩ (Figure 3, position 16). This is done to achieve a like structure that minimizes the stray inductance added to the switching loop. The BNC connector is the interface to the measured current signal, which minimizes the noise and quality of the measured signal.

**Figure 12: Shunt-based Low Side Switch Current Measurement over BNC Interface**



**ATTENTION:** If the board is used in continuous operation, replace shunt resistors with 0Ω resistors or remove and replace them with copper foil or a similar structure, to avoid thermal overstress and damage of the shunt.

## 3.3 Connectors

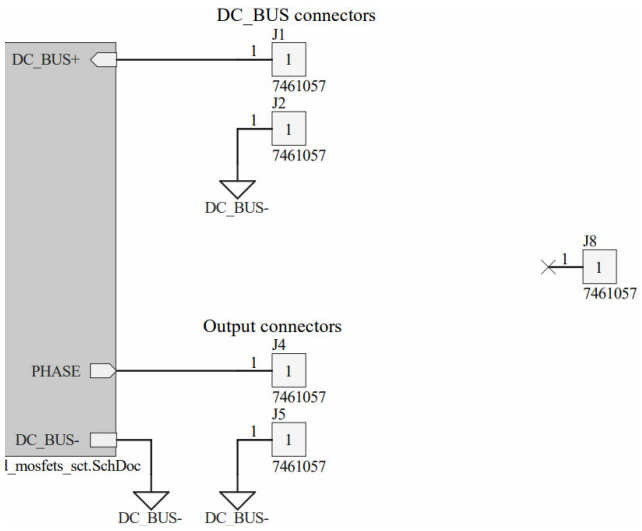
Connectors of the EB1200-3161 are described in the following sections.

### 3.3.1 Power Connectors for the High Voltage Side

The board is supplied with the power connectors realized with screw (M3 screw) terminals. The following power connectors are available on the board:

- J4 for the DC+
- J5 and J7 for the DC-
- J6 for the half-bridge output
- J8 auxiliary NC connector

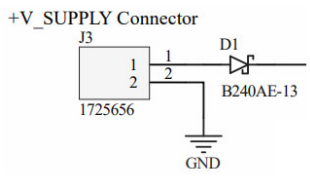
**Figure 13: Power Connectors Schematic**



### 3.3.2 Vcc +15V connector

The auxiliary power supply connector +15V is a standard two-pin PCB terminal block. This connector supports the wire cross-section of maximum 0.5 $mm^2$. Figure 14 shows the connector schematic.

**Figure 14: +15V Power Supply Connector**




For the reversed voltage protection, a Schottky diode is placed in series with the main power supply.

# 4 Setup in Use

**WARNING!** The EB1200-3161 gate driver evaluation board works with voltages up to 800V and thus requires that all safety precautions and national accident prevention rules to be undertaken. Installation and use of the board should be reserved for the skilled technical personnel. There is a danger of serious injury and damage of property if the board is not properly used or installed. Equip a system that supplies the evaluation board with control and protection devices, in agreement with applicable safety standards.

**ATTENTION:** Signals dedicated for high-side driver and low-side driver must have proper dead time. The board itself does not provide dead time generation. The recommended minimal dead time value is 300 ns.

## 4.1 Installation of EB1200-3161

Before starting with the evaluation of the board, consider and observed the following installation steps:

1. Before any installation, make a visual inspection of the board to make sure it contains all of the assembled components (see Section 6.3, Bill of Materials, for the list of components). The EB1200-3161, by default, does not contain assembled SiC transistors to avoid damage during transport and to provide the customer an option to use other transistors with the same footprint.
2. Assemble the MOSFET device in a TO247-4 pin package.
3. If the board will be used to drive a continuous load, prepare and assemble an appropriately sized heat sink.
4. Ensure that the appropriate gate voltage configuration is adjusted.
5. Connect the user interface connector. Connect the PWM signals to the control board with 5V logic.
6. Connect the 15V external power supply. Although the polarity is marked, the board is reverse-protected at the $V_{CC}$ terminal of +15V external supply.
7. Connect the DC Bus power supply and load to the board.

## 4.2 Evaluation of EB1200-3161

The EB1200-3161 enables users to evaluate the following items:

- ACFL-3161 driver features
- Switching characteristics of the SiC power semiconductors in a TO-247 4 pin package
- Half-bridge inverter basic features
- Buck-boost features

For the power semiconductor switching characteristics evaluation, with the EB1200-3161, perform a double pulse test, and measure the switching transients related to the semiconductor and the ACFL-3161 gate driver circuit.

For continuous operation in buck/boost mode, make sure you have prepared the following external hardware components:

- Appropriately sized and assembled heat sink
- Appropriately sized magnetic choke
- Properly sized output capacitor bank
- Electronic or adjustable resistive load properly sized

# 5 Measurement Results

## 5.1 Typical Switching Waveforms and Switching Loss Performance

This section provides measurement results obtained with an oscilloscope during the standard double pulse test procedure. The SiC MOSFET devices used for testing are SCTWA70N120G2V4 and C3M0021120K. Adjusted parameters during switching performance testing are given in Table 7.

**Table 7: Adjusted Parameters Used for Double Pulse Test Measurement**

| SiC MOSFET Device | External Gate Resistance [Ω] | Gate-Source Voltage [V] |
|---|---|---|
| SCTWA70N120G2V4 | 2.5 | +18V/-5.5V |
| C3M0021120K | 2.5 | +15V/-5.8V |

### 5.1.1 Typical Switching Waveforms of the SCTWA70N120G2V4

Switching waveforms during hard switching of the semiconductors are measured with an oscilloscope using the standard double pulse test procedure. The SiC MOSFET module used for testing is SCTWA70N120G2V4. Figure 15 shows the turn-on switching transient, while in Figure 16, the turn-off switching transient is depicted, at the different drain current levels. The switching performance measurements were done with the default gate resistor values, 2.5Ω for both On and Off resistors and +18V/-5.5V gate power supply.

**Figure 15: Characteristic Waveforms during the Turn-On Switching Transients at Different Load Currents**

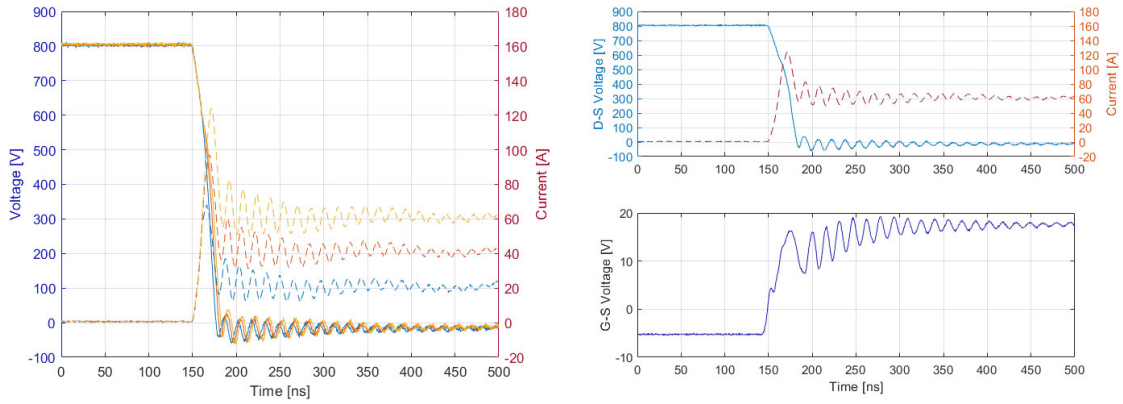
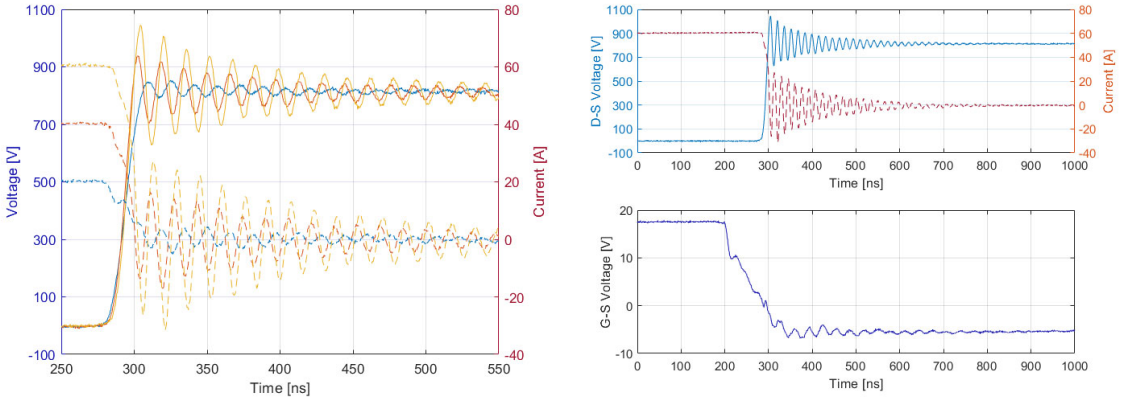


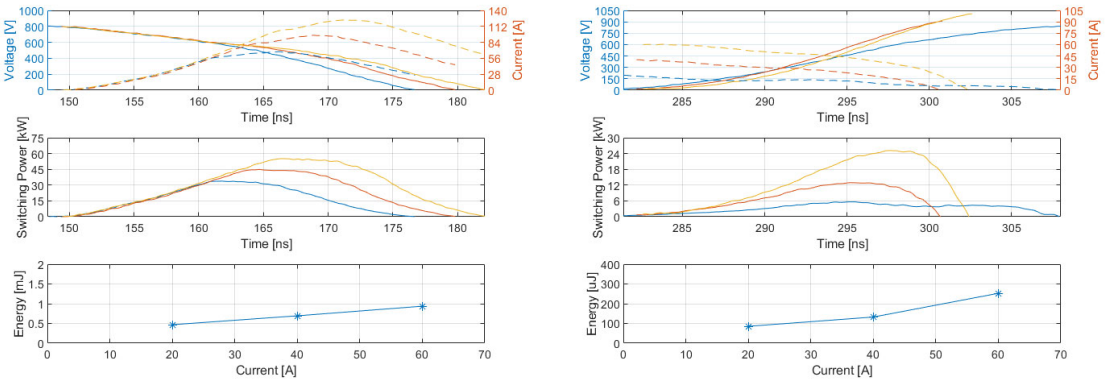

**Figure 16: Characteristic Waveforms during the Turn-Off Switching Transients at Different Load Currents**




## 5.1.2 Typical Switching Loss Performance of the SCTWA70N120G2V4

In Figure 17, instantaneous power during switching and resulting turn-on (left) and turn-off (right) switching energy loss is shown for the SCTWA70N120G2V4 switching device at an 800V DC Bus.

**Figure 17: Turn-On (Left) and Turn-Off (Right) Switching Energy Loss at 800V DC Bus**



## 5.1.3 Typical Switching Waveforms of the C3M0021120K

Switching waveforms during hard switching of the semiconductors are measured with an oscilloscope using the standard double pulse test procedure. The SiC MOSFET module used for testing is C3M0021120K. Figure 18 shows the turn-on switching transient, while in Figure 19, the turn-off switching transient is depicted, at the different drain current levels. The switching performance measurements were done with the default gate resistor values, 2.5Ω for both On and Off resistors, and a +15V/-5.8V gate power supply.

**Figure 18: Characteristic Waveforms during the Turn-On Switching Transients at Different Load Currents**

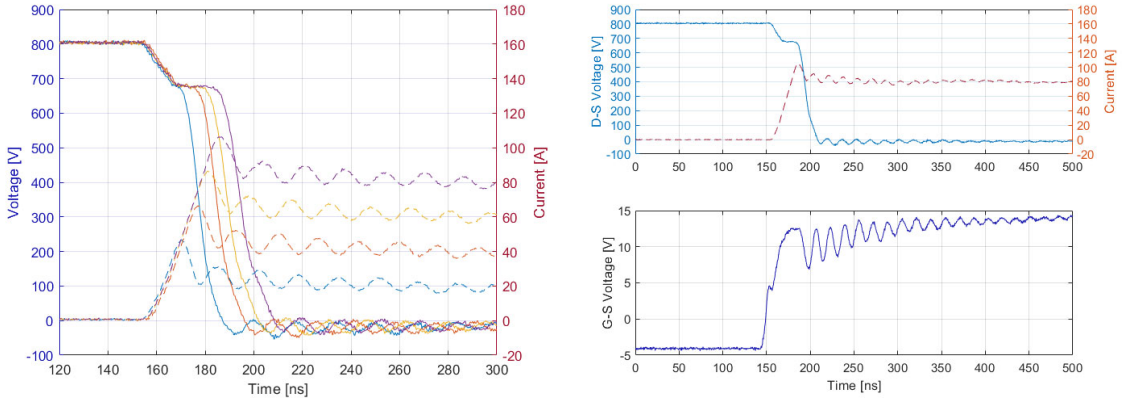
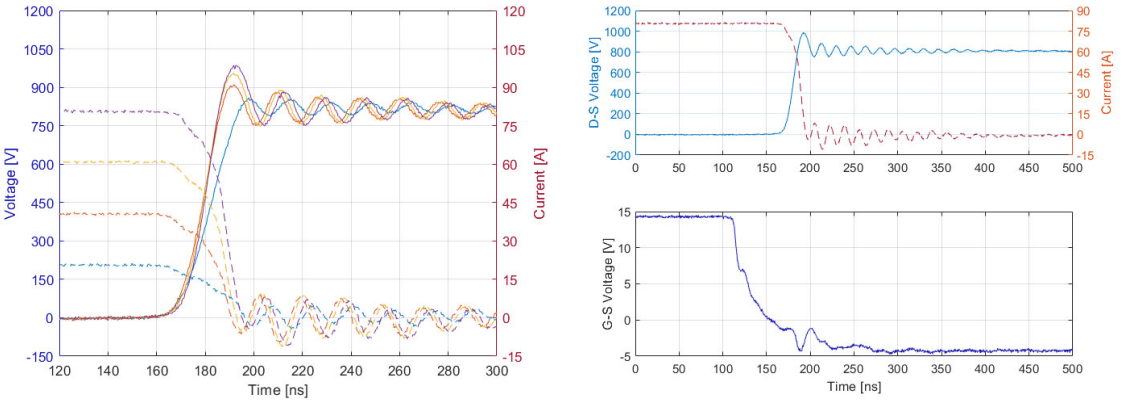


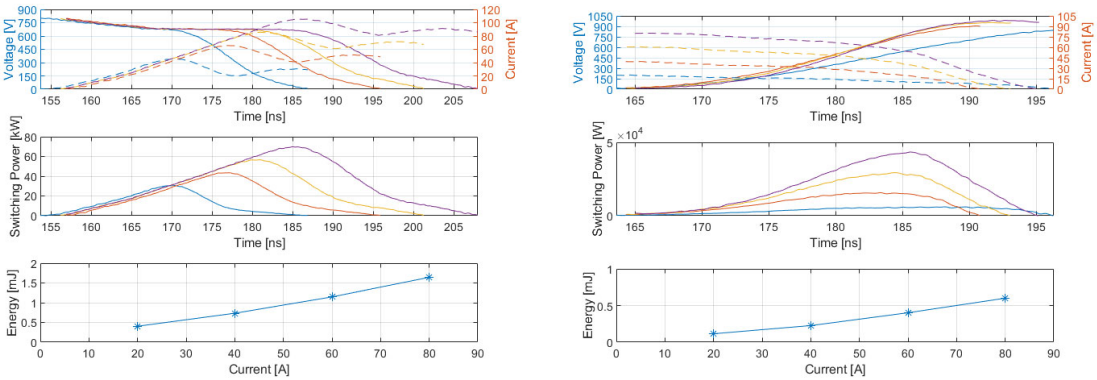

**Figure 19: Characteristic Waveforms during the Turn-Off Switching Transients at Different Load Currents**




## 5.1.4 Typical Switching Loss Performance of the C3M0021120K

In Figure 20, instantaneous power during switching and resulting turn-on (left) and turn-off (right) switching energy loss is shown for the C3M0021120K switching device at 800V DC Bus.

**Figure 20: Turn-On (Left) Turn-Off (Right) Switching Energy Loss at 800V DC Bus**




## 5.2 Buck/Boost Measurement Results

This section gives measurement results, obtained during continuous operation, related to efficiency of the EB1200-3161 board in the buck and boost working regime. Table 8 lists the buck/boost adjusted parameters used during the efficiency measurement.

**Table 8: Buck/Boost Parameters**

| SiC MOSFET Device | Rg [Ω] | Vgs [V] | Buck | | Boost | |
|---|---|---|---|---|---|---|
| | | | Vin | Vout | Vin | Vout |
| SCTWA70N120G2V4 | 5 | +18V/-5.5V | 600 | 400 | 400 | 600 |
| C3M0021120K | 2.5 | +15V/-5.8V | | | | |

External hardware used during testing is an external custom-made choke of 1-mH, DC-link capacitor bank of 705 µF in total and adjustable resistive load. The efficiency was measured at ambient temperature of 22°C with a high-precision power analyzer. For using the EB1200- 3161 in continuous operation, a commercial heat sink sk489 by Fischer Elektronik, dedicated for use with TO247 package devices, is mounted on SiC semiconductors, Figure 21. Highest measured heat sink temperature at 3.1-kW output power was 74°C. Efficiencies as opposed to output power for tested SiC MOSFET devices are shown in Figure 22 and Figure 23.

**Figure 21: EB1200-3161 Assembled for Continuous Operation**

**Figure 22: Measured Efficiencies of Buck (Left) and Boost (Right) Mode Operation with Wolfspeed C3M0021120K SiC MOSFET Devices at 50-kHz Switching Frequency**

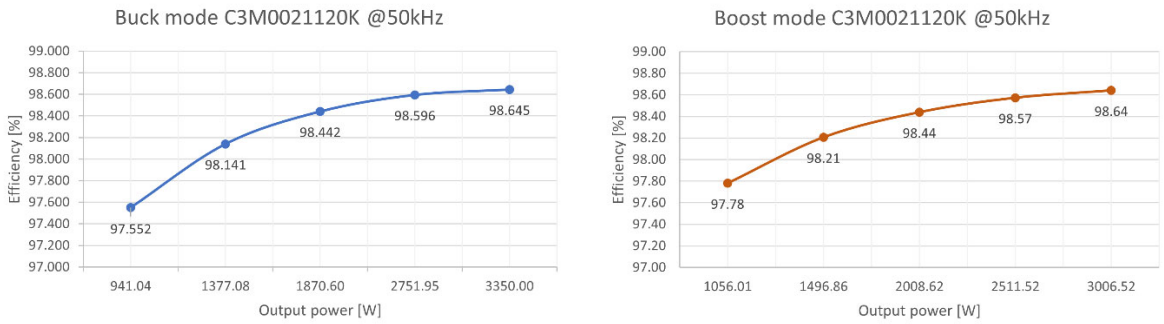
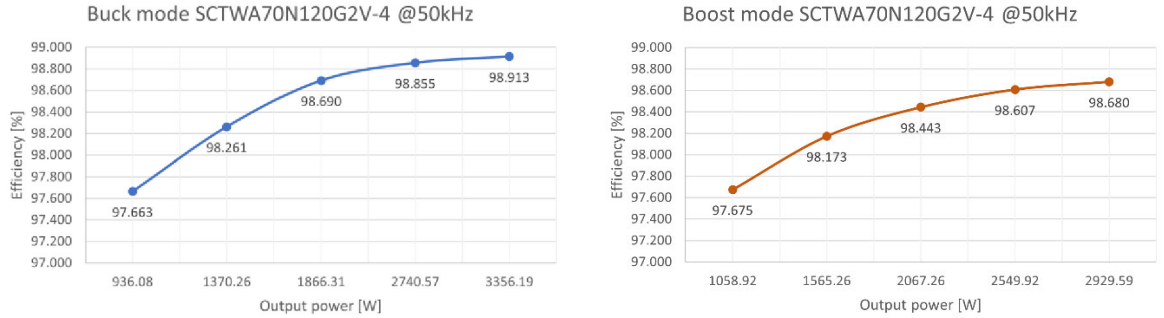



**Figure 23: Measured Efficiencies of Buck (Left) and Boost (Right) Mode Operation with STM SCTWA70N120G2V-4 SiC MOSFET Devices at 50-kHz Switching Frequency**




# 6 Appendix

This section gives full schematics, layout, and bill of materials of the EB1200-3161. Hopefully, this information will enable customers to modify, copy, and qualify the design for production, according to specific requirements.

# 6.1 Schematics

**Figure 24: EB1200-3161 – Top Level Sheet**

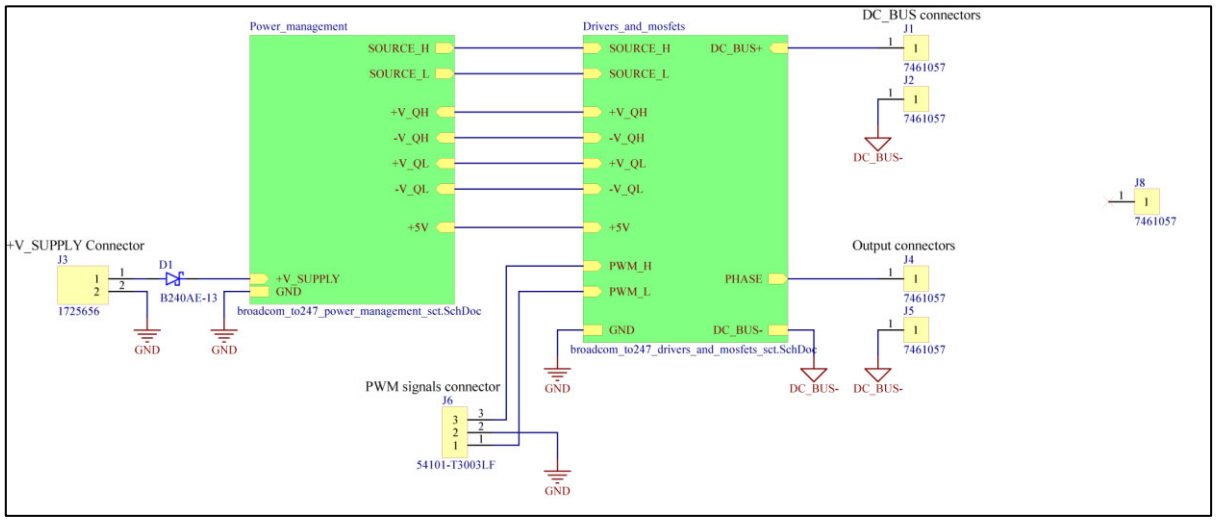



**Figure 25: EB1200-3161 – Sheet 1 – Driver**

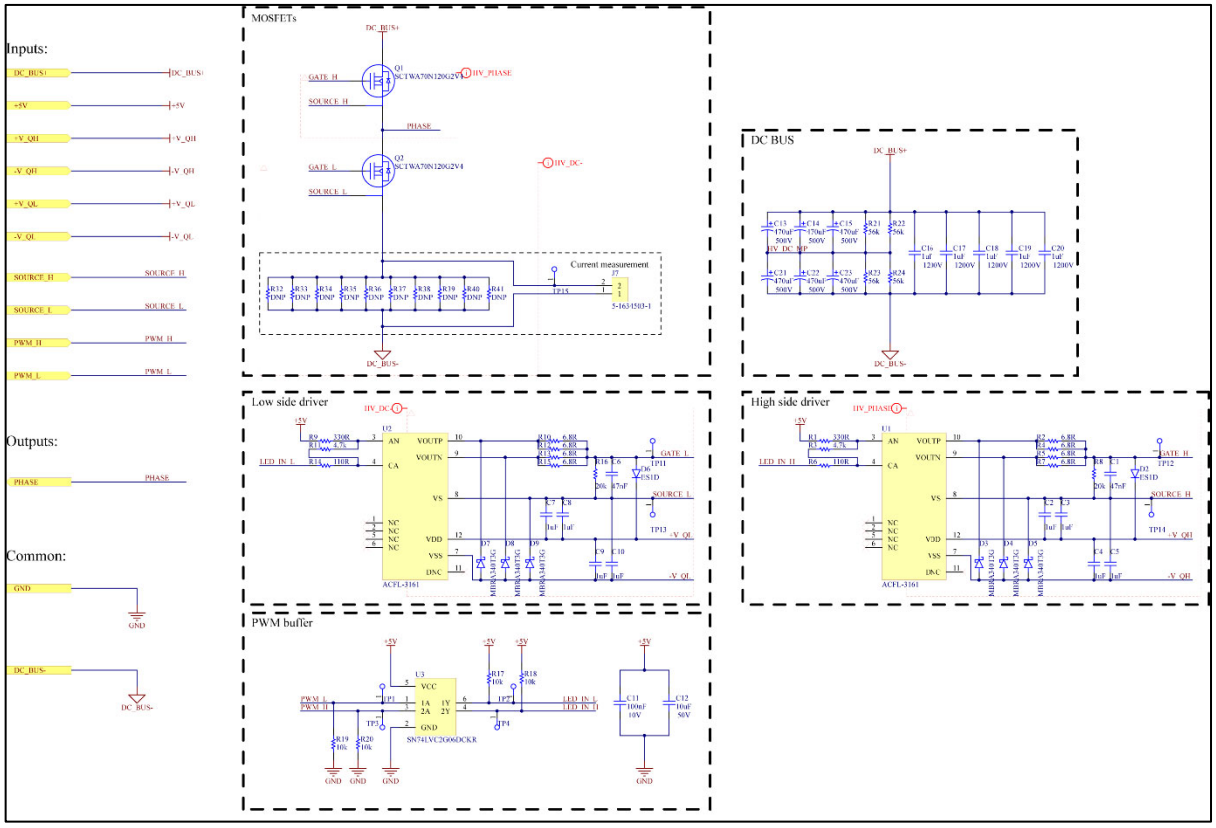
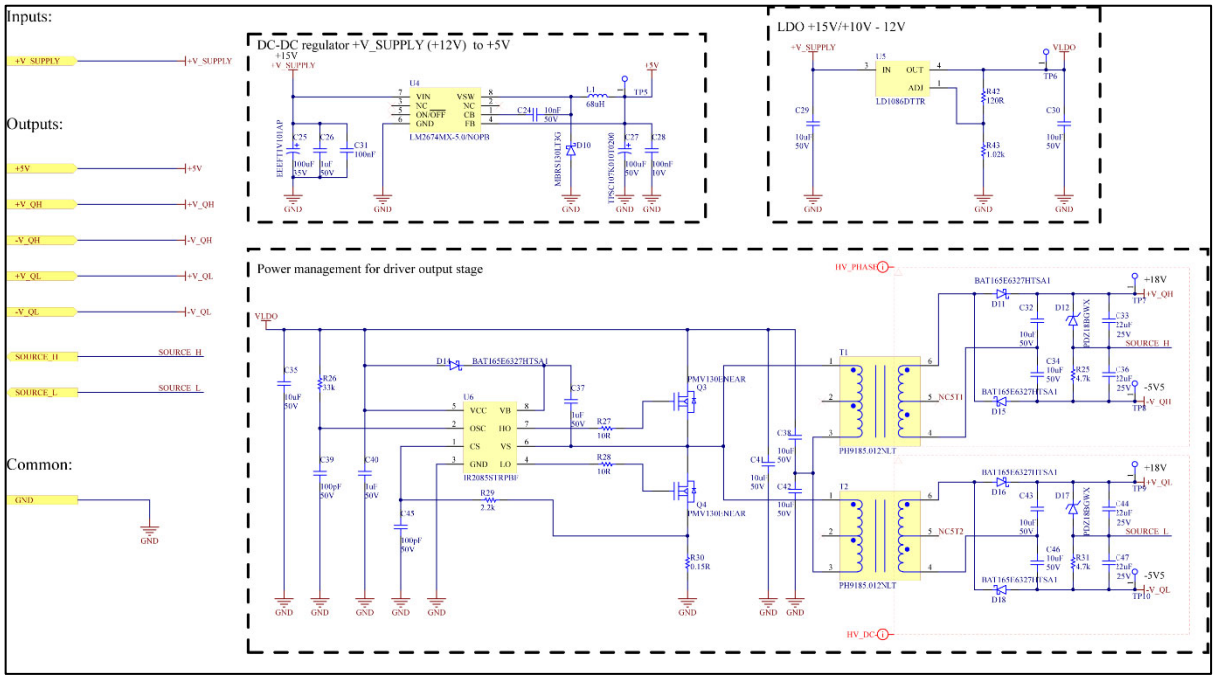


**Figure 26: EB1200-3161 – Sheet 2 – Power Management**



# 6.2 PCB Prints

**Figure 27: EB1200-3161 – Assembly Drawing**

| Layer | Name | Material | Thickness | Constant | Board Layer Stack |
|---|---|---|---|---|---|
| 1 | Top Overlay | | | | |
| 2 | Top Solder | Solder Resist | 0.010mm | 3.5 | |
| 3 | Top Layer | Copper | 0.070mm | | |
| 4 | Dielectric 1 | FR-4 | 0.400mm | 4.2 | |
| 5 | Signal Layer 1 | Copper | 0.070mm | | |
| 6 | Dielectric 3 | | 0.450mm | 4.2 | |
| 7 | Signal Layer 2 | Copper | 0.070mm | | |
| 8 | Dielectric 2 | | 0.400mm | 4.2 | |
| 9 | Bottom Layer | Copper | 0.070mm | | |
| 10 | Bottom Solder | Solder Resist | 0.010mm | 3.5 | |
| 11 | Bottom Overlay | | | | |

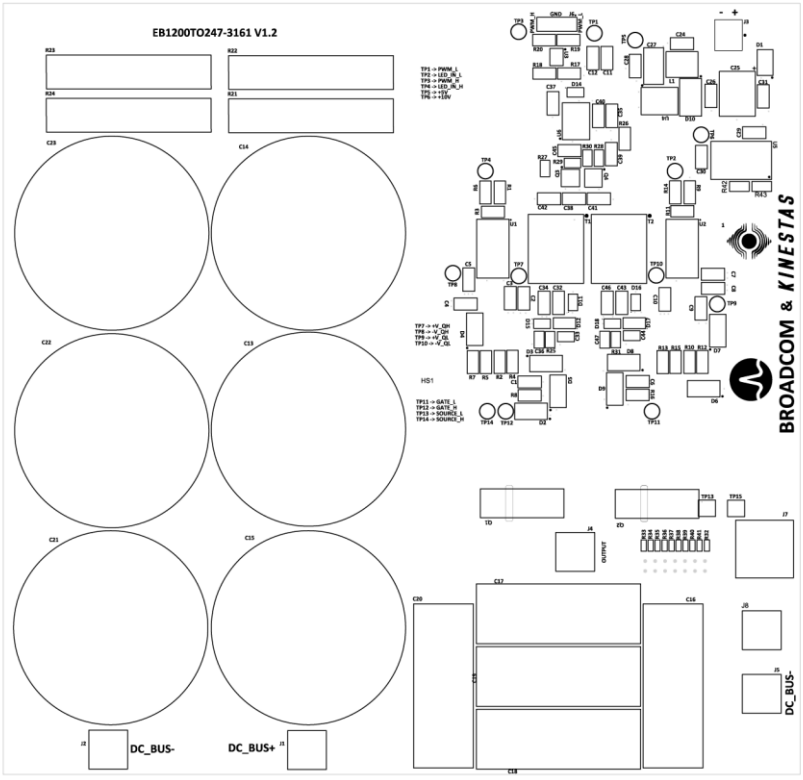


**Figure 28: EB1200-3161 – Top Layer**

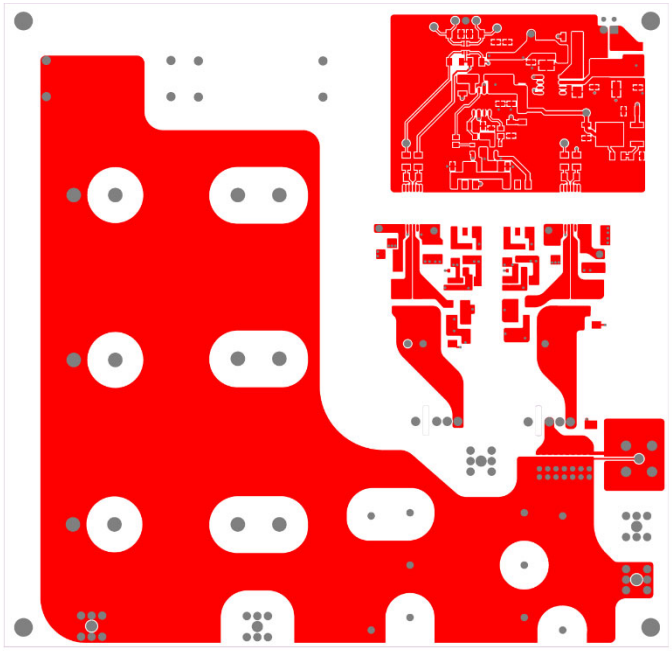


**Figure 29: EB1200-3161 – Signal Layer 1**

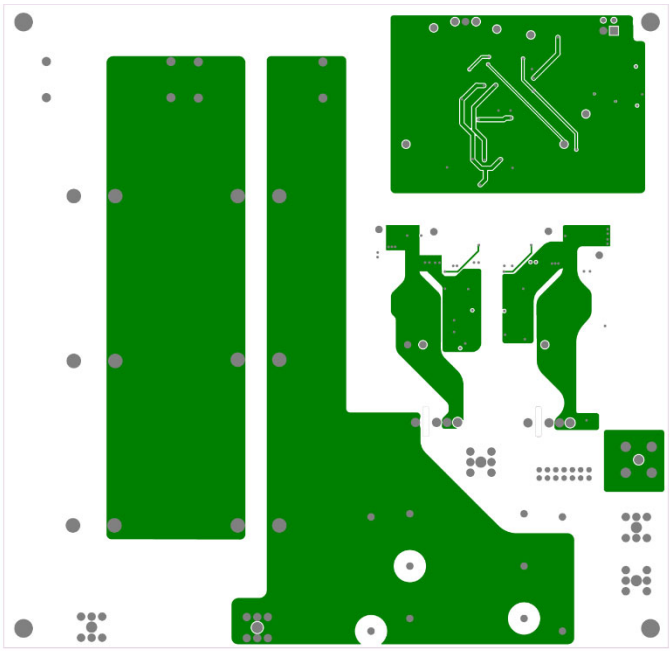


**Figure 30: EB1200-3161 – Signal Layer 2**

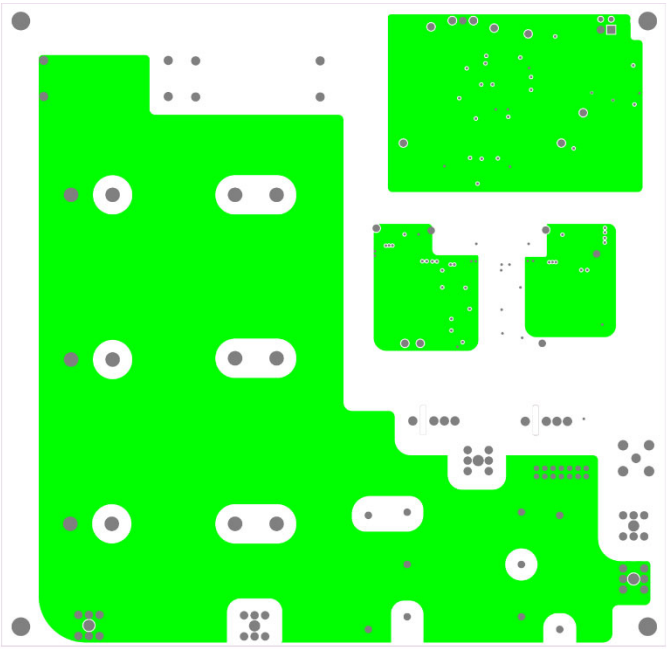
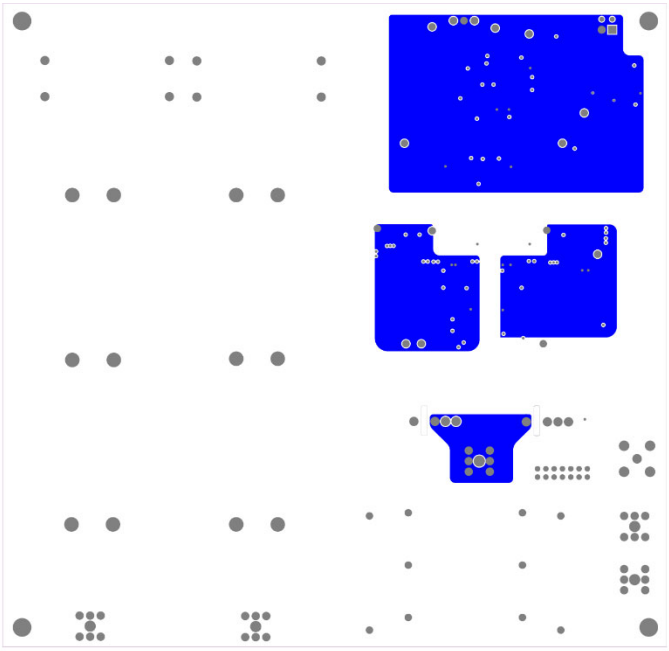


**Figure 31: EB1200-3161 – Bottom Layer**



## 6.3 Bill of Materials

Table 9 lists the bill of materials of EB1200-3161.

**Table 9: Bill of Materials for the Evaluation Board EB1200-3161**

| EB1200-3161 BOM | | |
|---|---|---|
| **Designator** | **MFPN** | **Quantity** |
| C1, C6 | DNP[a] | 2 |
| C2, C3, C4, C5, C7, C8, C9, C10, C26, C29, C37, C40 | SH31B105K500CT | 12 |
| C11, C28, C31 | 885012208058 | 3 |
| C12, C30, C32, C34, C35, C38, C41, C42, C43, C46 | GRT31CR61H106ME01L | 10 |
| C13, C14, C15, C21, C22, C23 | ALA7DA471DE500 | 6 |
| C16, C17, C18, C19, C20 | MKP1848C51012JK2 | 5 |
| C24 | VJ1206Y103JXAMC | 1 |
| C25 | EEE-FT1V101AP | 1 |
| C27 | TPSC107K010T0200 | 1 |
| C33, C36, C44, C47 | GRM21BR61E226ME44L | 4 |
| C39, C45 | 885012008043 | 2 |
| D1 | B240AE-13 | 1 |
| D2, D6 | ES1D | 2 |
| D3, D4, D5, D7, D8, D9 | MBRA340T3G | 6 |
| D10 | MBRS130LT3G | 1 |
| D11, D14, D15, D16, D18 | BAT165E6327HTSA1 | 5 |
| D12, D17 | PDZ18BGWX | 2 |
| D13, D19, D20 | BAS170WE6327HTSA1 | 3 |
| H1, H2 | M3-hole | 2 |
| J1, J2, J4, J5, J8 | 7461057 | 5 |
| J3 | 1725656 | 1 |
| J6 | 54101-T3003LF | 1 |
| J7 | 5-1634503-1 | 1 |
| L1 | VLS5045EX-680M | 1 |
| Q1, Q2 | SCTWA70N120G2V4 | 2 |
| Q3, Q4 | PMV130ENEAR | 2 |
| R1, R9 | CRCW1206330RFKEA | 2 |
| R2, R4, R5, R7, R10, R12, R13, R15 | CRCW12065R10FKEA | 8 |
| R3, R11 | CRCW12064K70FKEBC | 2 |
| R6, R14 | CR1206-JW-111ELF | 2 |
| R8, R16 | CRCW120620K0FKEAC | 2 |
| R17, R18, R19, R20 | RC1206JR-0710KL | 4 |
| R21, R22, R23, R24 | HPC2C563K | 4 |
| R25, R31 | RT0805FRE074K7L | 2 |
| R26 | ERJ-8ENF3302V | 1 |
| R27, R28 | CRCW080510R0FKEAC | 2 |
| R29 | RT0805FRE072K2L | 1 |
| R30 | ERJ-U6SJR15V | 1 |

**Table 9: Bill of Materials for the Evaluation Board EB1200-3161 (Continued)**

| EB1200-3161 BOM | | |
|---|---|---|
| **Designator** | **MFPN** | **Quantity** |
| R32, R33, R34, R35, R36, R37, R38, R39, R40, R41 | ESR03EZPJR0 / RCS06030000Z0EC[b] | 10 |
| T1, T2 | PH9185.012NLT | 2 |
| TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP14 | 5002 | 13 |
| TP13, TP15 | 5190TR | 2 |
| U1, U2 | ACFL-3161 | 2 |
| U3 | SN74LVC2G06DCKR | 1 |
| U4 | LM2674MX-5.0/NOPB | 1 |
| U5 | R1501J120B-T1-JE | 1 |
| U6 | IR2085STRPBF | 1 |

a. By placing capacitors C2 and C6, the overall gate capacitance of the MOSFET is raised.

b. Each of the resistors R32, R33, R34, R35, R36, R37, R38, R39, R40, and R41 of 1Ω is connected in parallel and forms a plain resistive shunt to enable appropriate low side switch current measurement. Replace these resistors with 0Ω if the board is used to drive a continuous load.

## 6.4 Test Points

Table 10 lists the available test points of the EB1200-3161.

**Table 10: Available Test Points for the Evaluation Board EB1200-3161**

| Test Point Designator | Signal |
|---|---|
| TP1 | PWM_L (before buffer) |
| TP2 | LED_IN.L (after buffer) |
| TP3 | PWM_H (before buffer) |
| TP4 | LED_IN.H (after buffer) |
| TP5 | +5V |
| TP6 | +10V… +12V |
| TP7 | +V_QH |
| TP8 | -V_QH |
| TP9 | +V_QL |
| TP10 | -V_QL |
| TP11 | GATE_L |
| TP12 | GATE_H |
| TP13 | SOURCE_L |
| TP14 | SOURCE_H |
| TP15 | POWER_SOURCE_L |

# 7 Disclaimer

This reference manual contains information that should serve only as a reference for initial evaluation and implementation of the Broadcom products. Broadcom does not take responsibility for using and implementing the products in other designs.

# Revision History

## Version 1.0, July 15, 2021

- Initial document release.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