Data Sheet

ACFJ-3540T

Automotive Gate Drive Optocoupler with Integrated Flyback DC-DC Controller, Emitter Sensing, UVLO Feedback, Active Miller Clamping, and Negative Bias

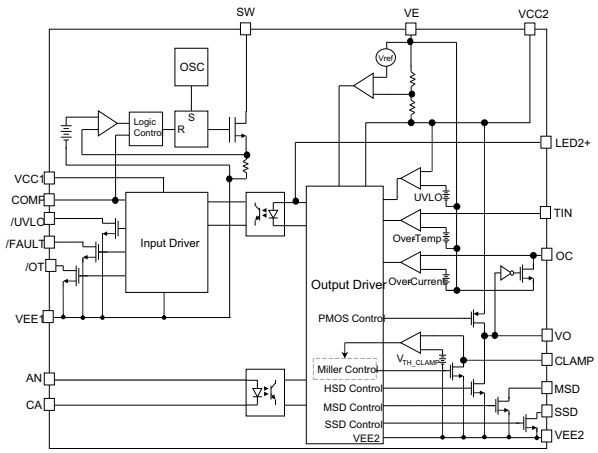
Description

The Broadcom® Automotive Optocoupler Smart Gate Driver features an integrated flyback controller for isolated DC-DC converter, IGBT emitter over-current sensing with soft-shutdown protection and fault feedback, under voltage lockout, IGBT over-temperature detection/shutdown and feedback, and active Miller current clamping. The fast propagation delay with excellent timing skew performance enables excellent timing control and efficiency. This full feature optocoupler, which comes in a compact, surface-mountable SO-24 package with 0.8-mm pitch for space savings, is suitable for HEV and EV applications.

Broadcom R^{2}Coupler® isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

Functional Diagram

Figure 1: ACFJ-3540T Functional Diagram



Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: –40ºC to +125ºC
- Integrated flyback controller for isolated DC-DC converter
- Regulated output supply voltage: 15V ± 5%
- Minimum peak output current: –1A/+2.5A
- Miller clamp sinking current: 2.5A
- Maximum propagation delay: 150 ns
- Common mode rejection (CMR): 50 kV/µs at V_{CM} = 1500V
- Integrated fail-safe IGBT protection
  - Emitter over-current sensing, "Soft" IGBT turn-off and fault feedback
  - Under Voltage Lock-Out protection (UVLO) with feedback
  - Over-temperature detection, with auto shutdown and feedback
- High noise immunity
  - Miller current clamping
  - Direct LED input with low input impedance and low noise sensitivity
  - Negative gate bias
- SO-24 package with 8-mm creepage and clearance
- Regulatory approvals:
  - UL1577, CSA
  - IEC 60747-5-5

Applications

- IGBT gate driver for traction inverter, charger, and HVAC

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACFJ-3540T	-000E	SO-24	X		X	45 per tube
	-500E		X	X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

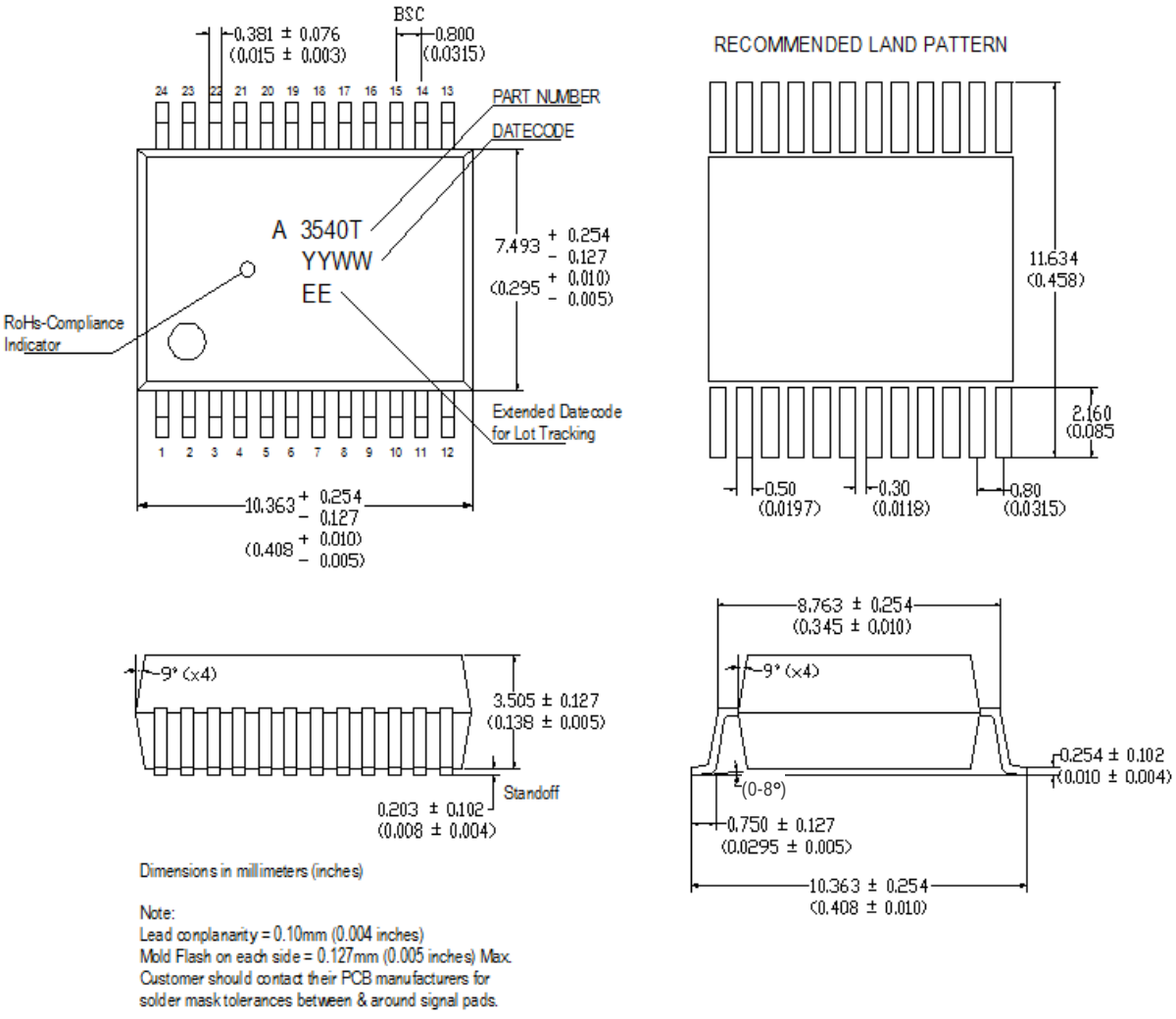
Example 1:

ACFJ-3540T-500E to order product of SO-24 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawing

Figure 2: 24-Lead Surface Mount



Dimensions in millimeters (inches)

Note:
Lead coplanarity = 0.10mm (0.004 inches)
Mold Flash on each side = 0.127mm (0.005 inches) Max.
Customer should contact their PCB manufacturers for solder mask tolerances between & around signal pads.

Recommended PB-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

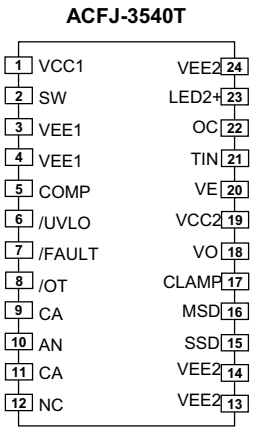
NOTE: Non-halide flux should be used.

Product Overview Description

The ACFJ-3540T (shown in Figure 1) is a highly integrated power control device that incorporates all the necessary components for a complete, isolated IGBT gate drive circuit. It features flyback controller for isolated DC-DC converter, a high current gate driver, Miller current clamping, IGBT over-current and under voltage lock-out protection and feedback in a SO-24 package. Direct LED input allows flexible logic configuration and differential current mode driving with low input impedance, greatly increased its noise immunity.

Package Pin Out

Figure 3: ACFJ-3540T Package Pin Out

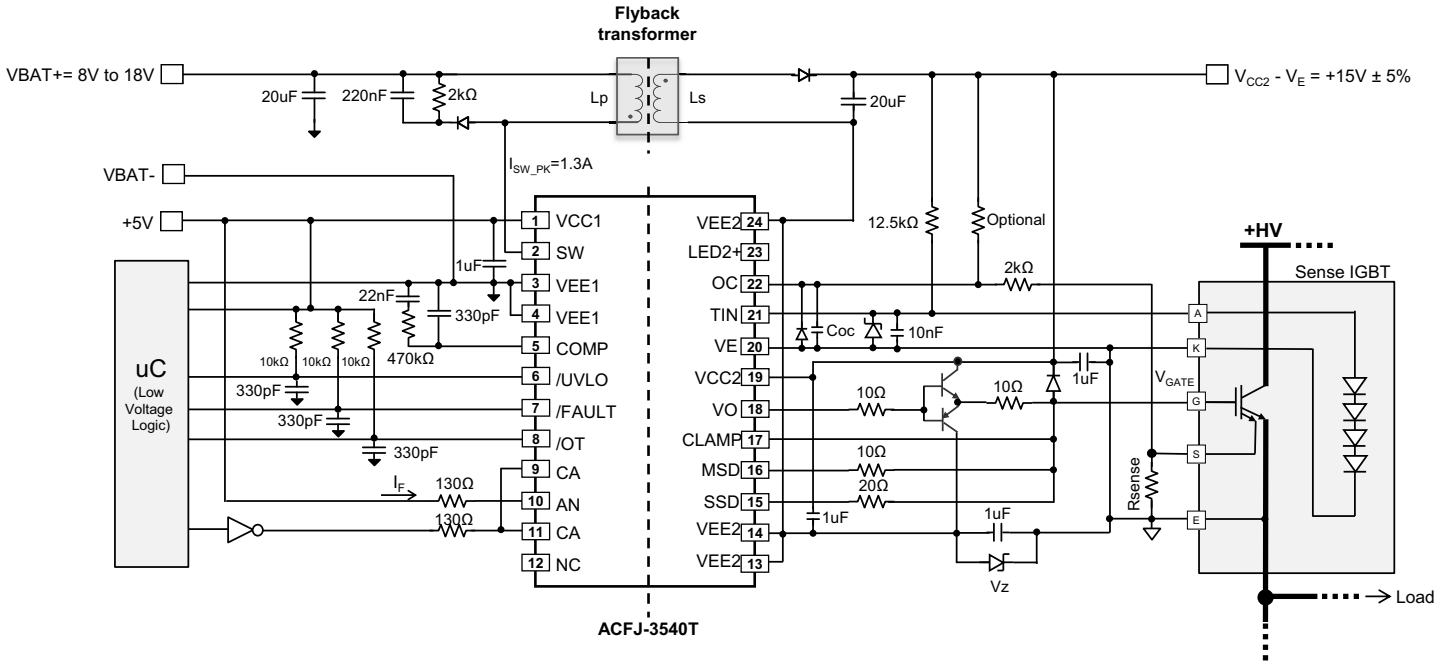


Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	VCC1	Input power supply	24	VEE2	Output ground
2	SW	Switch output to primary coil	23	LED2+	No connection, for testing only
3	VEE1	Input ground	22	OC	Current sense input
4	VEE1	Input ground	21	TIN	Temperature sense input
5	COMP	Compensation network for flyback controller	20	VE	IGBT emitter reference
6	/UVLO	VCC2 under voltage feedback	19	VCC2	Output power supply
7	/FAULT	Over current fault feedback	18	VO	Pull-up and hard shutdown driver
8	/OT	Over temperature fault feedback	17	CLAMP	Miller current clamping output
9	CA	Input LED cathode	16	MSD	Mild shutdown driver
10	AN	Input LED anode	15	SSD	Soft shutdown driver
11	CA	Input LED cathode	14	VEE2	Output ground
12	NC	No internal connection	13	VEE2	Output ground

Typical Gate Drive Circuit with Emitter Current Sensing

Figure 4: ACFJ-3540T Typical Gate Drive Circuit with Over-Current and Over-Temperature Sensing and Negative Bias Set by Vz



NOTE: Component value is subjected to change with varying application requirements.

Description of Operations and Functions

Operation of Integrated Flyback Controller

The primary control block implements direct duty cycle control logics for line and load regulation. Primary winding current is sensed and limited within 1.3A to prevent transformer short circuit failure from damaging the primary switch inside the chip. Secondary output voltage V_{CC2} is sensed and fed back to the primary control circuits. V_{CC2} over-voltage can be detected and primary switch (SW) is turned off to protect secondary over voltage failure.

The flyback controller maximum PWM duty cycle is designed to be around 50% to ensure discontinuous operation mode under high load condition. A discrete transformer should be connected to ACFJ-3540T according to Figure 4 for complete isolated DC-DC converter. Input LED should be kept off while powering up the VCC1. To ensure proper operation of the DC-DC converter, fast VCC1 rise time (<=5ms) is preferred for soft start function to control the inrush current. (The soft start function is explained in Application Note 5576). If V_{CC2} fails to rise above 6V at the end of the soft start period (about 17 ms), the primary switch is turned off to prevent a possible V_{CC2} short circuit event during start-up.

The average PWM switching frequency of primary switch (SW) is dithered in a range of ± 6% typically. Frequency dithering feature helps to achieve better EMI performance by spreading the switching and its harmonics over wider band.

Status Flags

The status flags at the input side reflect the state of the circuit operation.

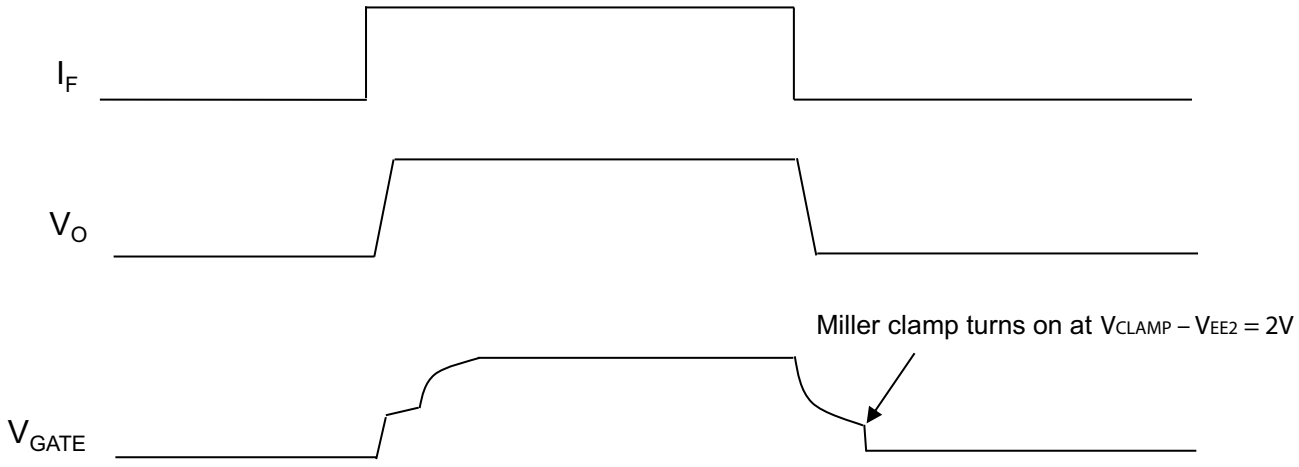
- Normal operation: All the status flags (/UVLO, /FAULT and /OT) are in Hi-Z state. These pins are pulled high through the external resistors.
- V_{CC2} UVLO (under-voltage lock out) fault: During operation, if the V_{CC2} falls below the UVLO threshold, only the /UVLO flag will be pulled low.
- Short circuit (SC) fault: If short circuit fault occurs, the IGBT gate will be soft-shutdown (pulled low by the SSD pin action). Only the /FAULT flag will be pulled low.
- Over-temperature fault: If over temperature fault occurs whereby TIN voltage crosses V_{TIN-} threshold level, the output driver VO will do hard shutdown. Only the /OT flag will be pulled low.
- LED2 fault: If the primary IC detects no signal from LED2 (LED2 is off), it is presumed that LED2 is faulty and all the status flags (/UVLO, /FAULT and /OT) will be pulled low. The driver IC's power will then need to be recycled for IC reset.

Conditions	Status Flags		
	/UVLO	/FAULT	/OT
Normal operation	Hi-Z	Hi-Z	Hi-Z
VCC2 UVLO fault	Low	Hi-Z	Hi-Z
Short circuit (SC) fault	Hi-Z	Low	Hi-Z
Over temperature fault	Hi-Z	Hi-Z	Low
LED2 fault	Low	Low	Low

Description of Gate Driver and Miller Clamping

The gate driver is directly controlled by the input LED current (I_F). When input LED current is driven high, the main output of ACFJ-3540T can then delivers a 1A sourcing current to drive the external buffer that drives the IGBT's gate. While the input LED is switched off, it provides 2.5A sinking current to external buffer to switch the gate off fast. An additional Miller clamping pull-down transistor is activated when gate voltage drops below V_{TH_CLAMP} voltage to provide low impedance path to Miller current as shown in Figure 5.

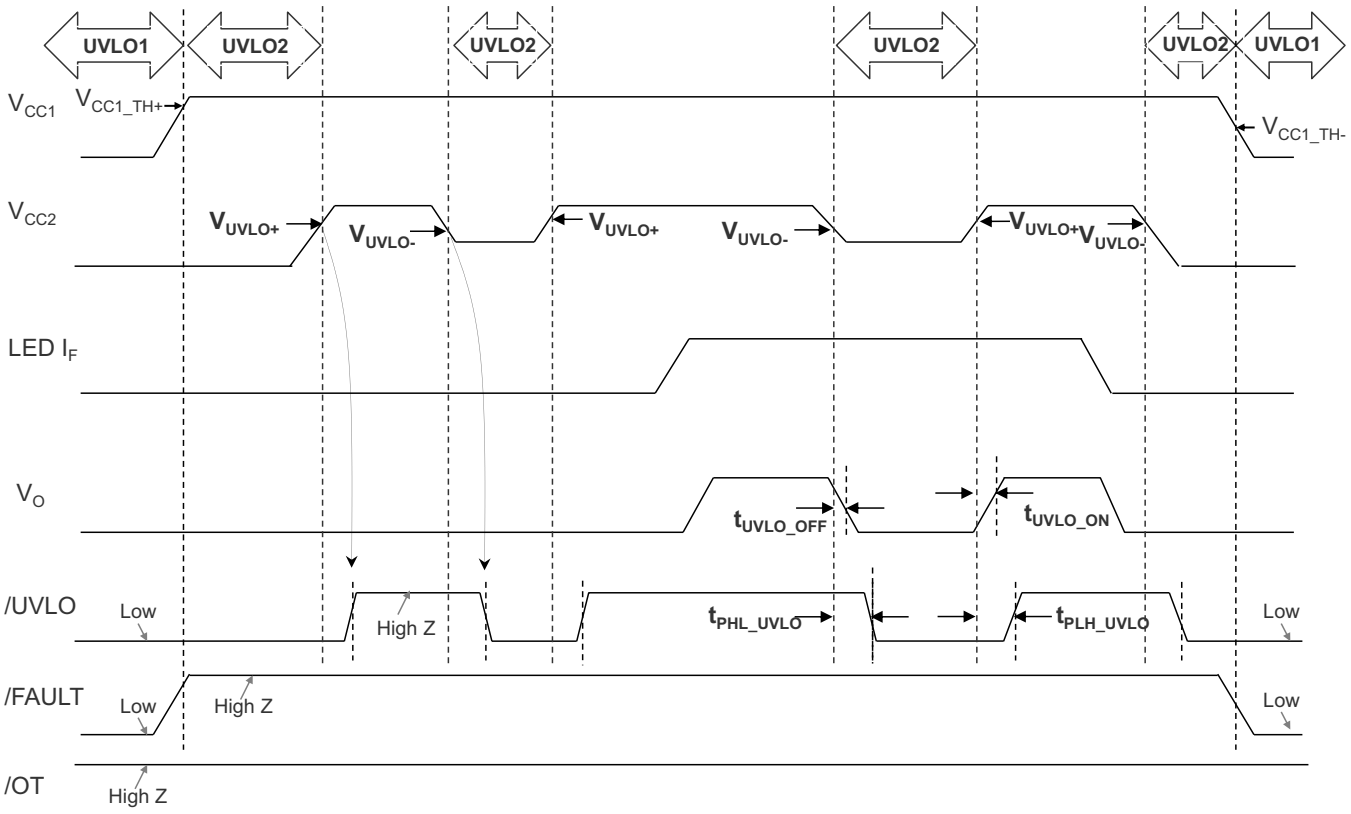
Figure 5: Gate Drive Signal Behavior



Description of Under-Voltage Lock Out

Insufficient gate voltage to IGBT can increase turn on resistance of IGBT, resulting in large power loss and IGBT damage due to high heat dissipation. ACFJ-3540T monitors the output power supply (V_{CC2}) constantly. When output power supply is lower than under-voltage lock out (UVLO) threshold, gate driver output will shut off to protect IGBT from low voltage bias. During power up, the UVLO feature forces the ACFJ-3540T's output low to prevent unwanted turn-on at lower voltage.

Figure 6: Circuit Behaviors at Power-Up, Power-Down and UVLO



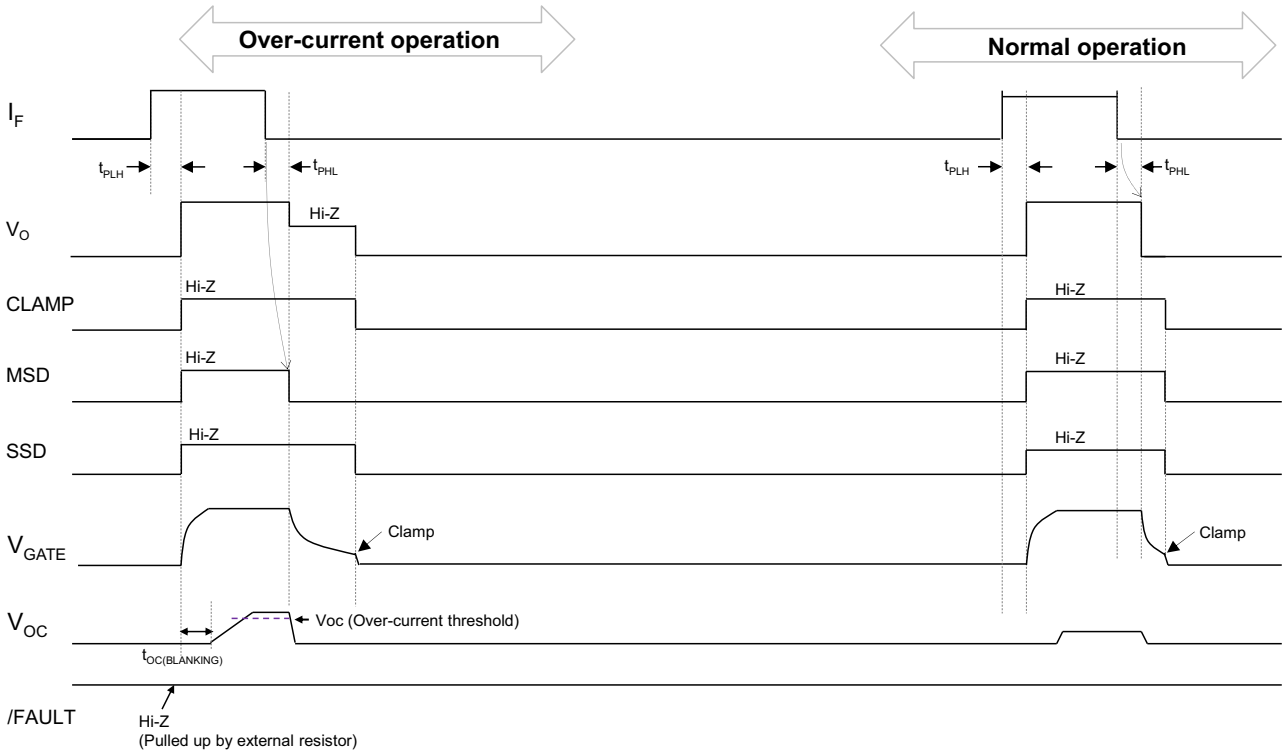
Description of Over-Voltage Protection

When V_{CC2} is greater than the specified V_{CC2} Over-Voltage Protection threshold, the transistor at the SW pin on the primary side will shut down and the DC/DC flyback conversion will cease.

Description of Operation during Over-Current Condition

1. OC terminal monitors IGBT's emitter current via the emitter sense resistor.
2. At the moment when LED turns off, the voltage at the OC terminal is assessed. If it is within V_{OC} threshold voltage, a hard-shutdown will be executed for this normal condition, where VO pin is used to lower the IGBT gate voltage (V_{GATE}) strongly.
3. If the voltage at the OC terminal is above V_{OC} threshold at the moment of turn-off, a mild-shutdown will be triggered for this over-current condition, where only MSD pin is used to lower the IGBT gate voltage (V_{GATE}) slowly.
4. When V_{GATE} falls across the V_{TH_CLAMP} voltage (approximately 2V), all driver pins (VO, MSD, SSD, and CLAMP) are activated to clamp the gate low.
5. In the Mild-shutdown state (over-current), /FAULT is not triggered (remains in Hi-Z state) and is pulled high by external resistor.
6. Driver output responds to LED input normally upon next PWM switching.

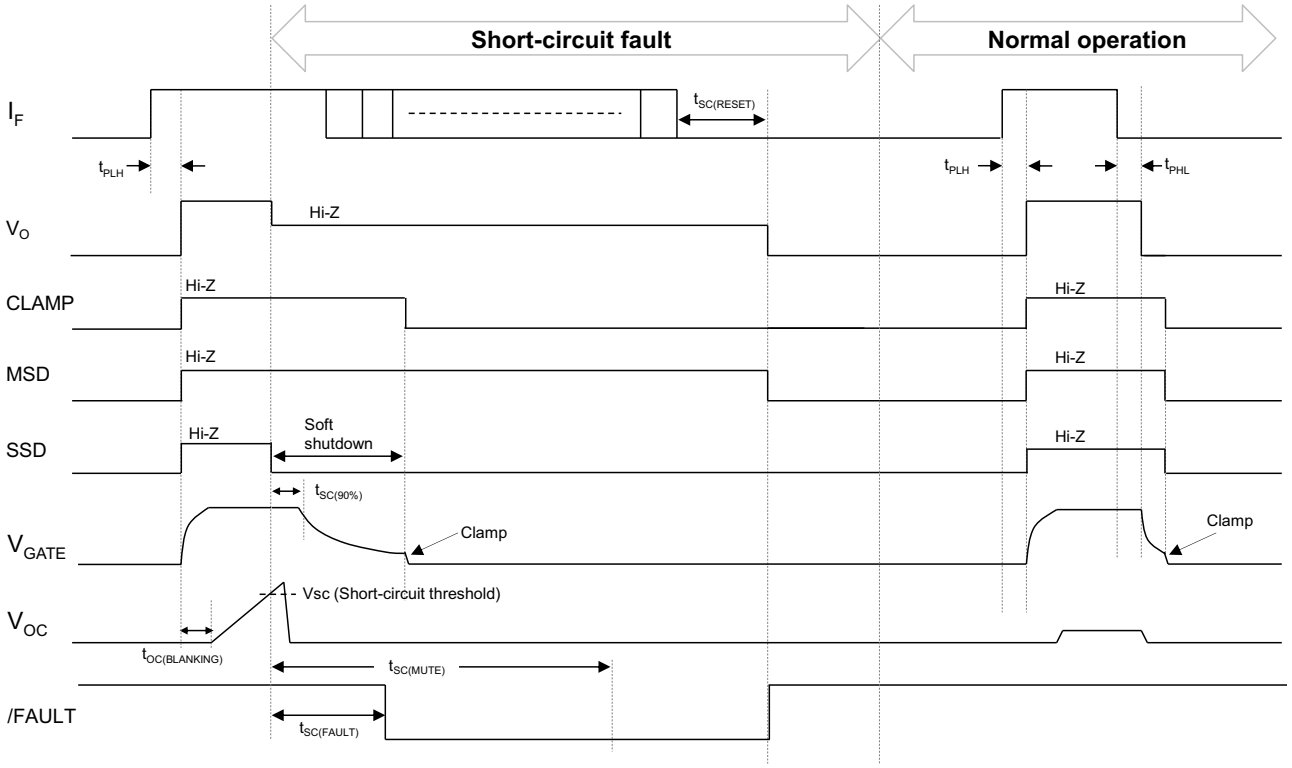
Figure 7: Circuit Behavior During an Over-Current Event



Description of Operation during Short-Circuit Condition

1. OC terminal monitors IGBT's emitter current via the emitter sense resistor.
2. When LED is on, the voltage at the OC terminal is constantly assessed. When it exceeds the V_{SC} threshold, gate driver IC recognized it as a short circuit event and a soft-shutdown will be triggered. The IGBT gate voltage (V_{GATE}) is lowered very slowly by SSD pin only.
3. /FAULT signal is pulled low, notifying the microcontroller of the short-circuit fault condition.
4. When V_{GATE} falls across the V_{TH_CLAMP} voltage (typically 2V above V_{EE2}), the CLAMP pin is activated to clamp the gate low, but VO and MSD remain in Hi-Z state.
5. All PWM commands will be ignored during mute time $t_{SC(MUTE)}$.
6. When $t_{SC(MUTE)}$ expires, LED input needs to be kept low for $t_{SC(RESET)}$ duration before fault condition can be cleared. VO and MSD will then be reset to low.
7. After fault condition is cleared, /FAULT flag will return to high, and output starts to respond to LED input.

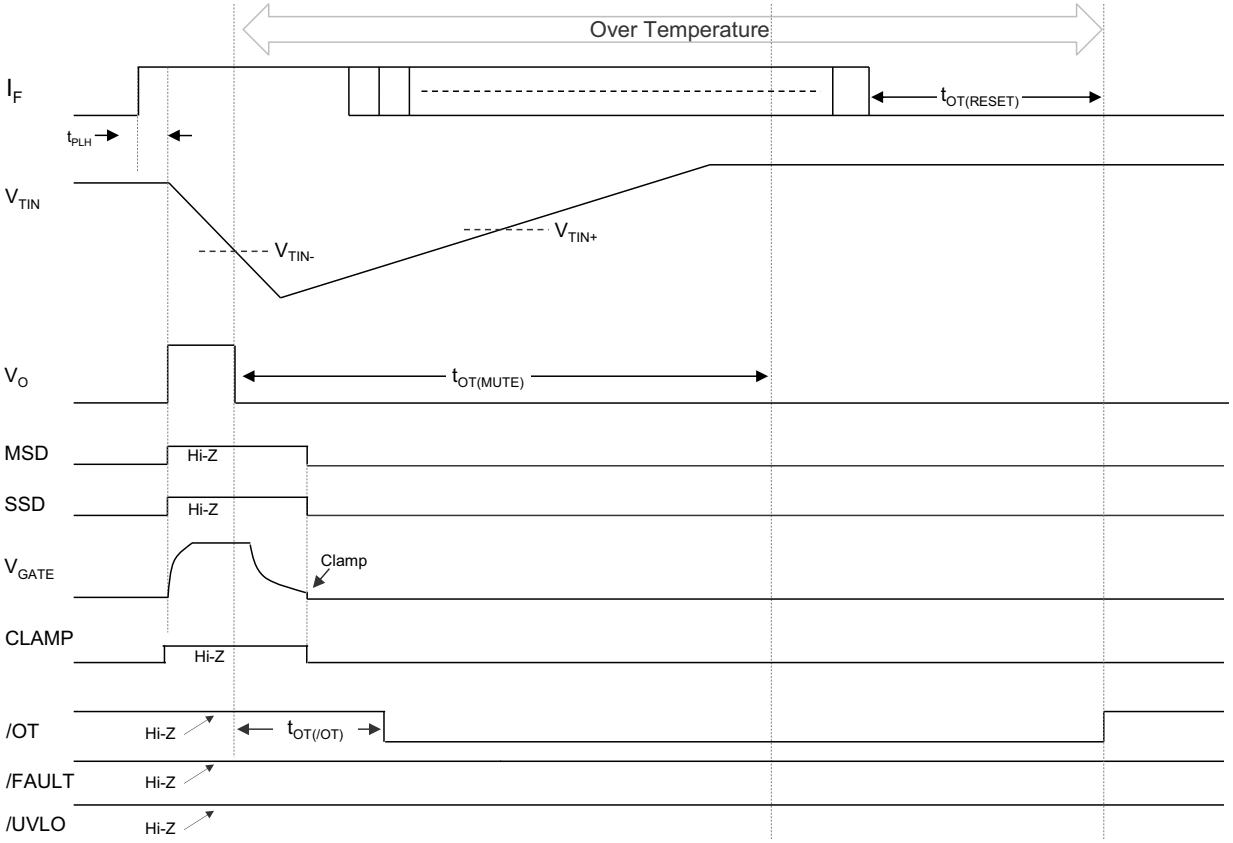
Figure 8: Circuit Behavior during Short-Circuit Event



Description of Operation during Over-Temperature Fault Condition

1. TIN terminal monitors temperature input by connecting to temperature sensor, such as IGBT on-chip diodes with external bias. If the TIN pin voltage crosses below V_{TIN-}, the VO will shut down to protect IGBT from over-heating if it is in the ON state.
2. The /OT status flag at the input IC will go low to notify the microcontroller of the over-temperature fault.
3. LED input is ignored after over-temperature fault is triggered for $t_{OT(MUTE)}$.
4. When $t_{OT(MUTE)}$ expires, the TIN pin voltage level must be higher than V_{TIN+} and LED input must be kept low for $t_{OT(RESET)}$ duration before the over-temperature fault condition is cleared.
5. After over-temperature fault condition is cleared, the /OT flag will then return to high, and driver output starts to respond to LED input.

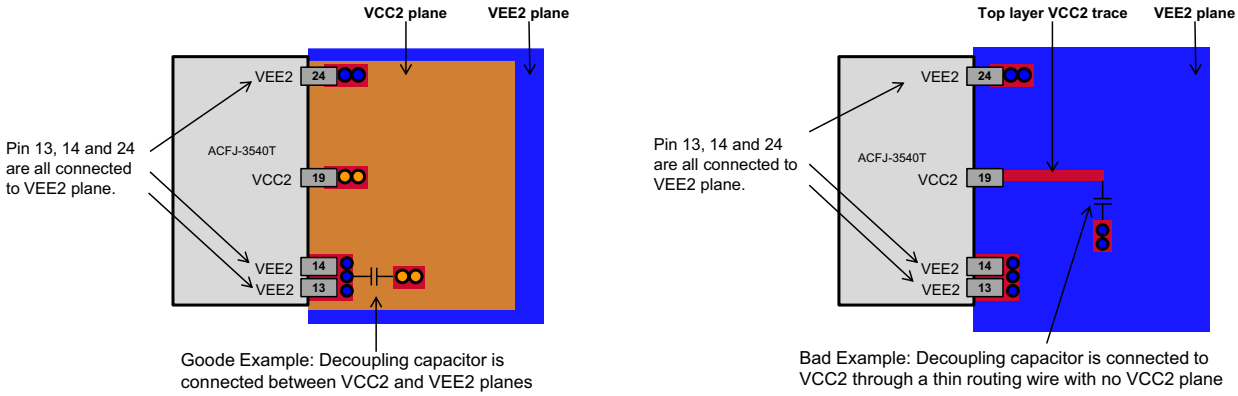
Figure 9: Circuit Behavior during an Over-Temperature Fault Event



Printed Circuit Board Layout

Design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, the use of power and ground planes, etc. It is recommended that VCC2 and VEE2 are connected to their respective planes by vias right next to the pins. Figure 9 shows a good example of PCB layout arrangement in comparison with a bad one.

Figure 10: PCB Layout Examples



Regulatory Approval

The ACFJ-3540T is approved by the following organizations.

UL	Approved under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}.
CSA	Approved under CSA Component Acceptance Notice #5, File CA 88324.
IEC/EN/DIN EN 60747-5-5	Approved under:IEC 60747-5-5EN 60747-5-5DIN EN 60747-5-5

IEC/EN/DIN EN60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Insulation Classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 Vrms		I - IV	
for rated mains voltage ≤ 300 Vrms		I - IV	
for rated mains voltage ≤ 600 Vrms		I - IV	
for rated mains voltage ≤ 1000 Vrms		I - III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1230	V_{PEAK}
Input to Output Test Voltage, Method b V_{IORM} × 1.875 = V_{PR}, 100% Production Test with tm = 1s, Partial discharge < 5 pC	V_{PR}	2306	V_{PEAK}
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, tm = 10s, Partial Discharge < 5 pC	V_{PR}	1968	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage tini = 60s)	V_{IOTM}	8000	V_{PEAK}
Safety-limiting values – maximum values allowed in the event of a failure			
Case Temperature	T_S	175	°C
Input Power	$P_{S,INPUT}$	400	mW
Output Power	$P_{S,OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	> 10^9	Ohm

NOTE:

1. Isolation characteristics are guaranteed only within the safety maximum ratings that must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.
2. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulation section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

Insulation and Safety-Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group	IIIa			Material Group (DIN VDE 0110)

Absolute Maximum Ratings

Unless otherwise specified, all voltages at input IC reference to V_{EE1}, all voltages at output IC reference to V_{EE2}.

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	150	°C	
Operating Temperature	T_A	–40	125	°C	
IC Junction Temperature	T_J	—	150	°C	
Average LED Input Current	$I_{F(AVG)}$	—	20	mA	
Peak Transient LED Input Current (< 1 µs pulse width, 300 pps)	$I_{F(TRAN)}$	—	1	A	
Reverse Input Voltage (VCA-VAN)	V_R	—	6	V	
Input Supply Voltage	V_{CC1}	–0.5	6	V	
Primary Switch Voltage	V_{SW}	—	36	V	
COMP Pin Voltage	V_{COMP}	–0.5	6	V	
/UVLO Pin Voltage	$V_{/UVLO}$	–0.5	6	V	
/FAULT Pin Voltage	$V_{/FAULT}$	–0.5	6	V	
/OT Pin Voltage	$V_{/OT}$	–0.5	6	V	
/UVLO Output Sinking Current	$I_{/UVLO}$	—	5	mA	
/FAULT Output Sinking Current	$I_{/FAULT}$	—	5	mA	
/OT Output Sinking Current	$I_{/OT}$	—	5	mA	
Total Output Supply Voltage	V_{CC2}	–0.5	30	V	
Positive Output Supply Voltage	$V_{CC2} – V_E$	–0.5	20	V	
Negative Output Supply Voltage	$V_{EE2} – V_E$	–15	+0.5	V	
Gate Driver Output Voltage, VO	V_O	–0.5	V_{CC2} + 0.5	V	
Gate Driver Output Voltage, MSD	V_{MSD}	–0.5	V_{CC2} + 0.5	V	
Gate Driver Output Voltage, SSD	V_{SSD}	–0.5	V_{CC2} + 0.5	V	
Gate Driver Output Voltage, CLAMP	V_{CLAMP}	–0.5	V_{CC2} + 0.5	V	
Over-current Pin Voltage, OC	$V_{OC} – V_E$	–0.5	6	V	
Temperature Input Pin Voltage	$V_{TIN} – V_E$	–0.5	6	V	
Output IC Power Dissipation	P_O	—	600	mW	a
Input IC Power Dissipation	P_I	—	280	mW	b

a. Output IC power dissipation is derated linearly above 100°C from 600 mW to 300 mW at 125°C.

b. Input IC power dissipation is derated linearly above 100°C from 280 mW to 200 mW at 125°C.

Recommended Operating Conditions

Unless otherwise specified, all voltages at input IC reference to V_{EE1}, all voltages at output IC reference to V_{EE2}.

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T_A	–40	125	°C	
Input IC Supply Voltage	V_{CC1}	4.7	5.5	V	a
Positive Output IC Supply Voltage	$V_{CC2} – V_E$	14.25	15.75	V	
Negative Output IC Supply Voltage	$V_{EE2} – V_E$	–10	0	V	b
Input LED Turn On Current	$I_{F(ON)}$	10	16	mA	
Input LED Turn Off Voltage ($V_{AN} – V_{CA}$)	$V_{F(OFF)}$	–5.5	0.8	V	
DC-DC Flyback Controller PWM Duty Cycle	D_{MAX}	—	50	%	
Peak SW Current	I_{SW_PK}	—	1.3	A	

a. Power-up sequence: Supply (V_{BAT+}) to the DC-DC flyback transformer must be ready before V_{CC1} power up.

b. This supply is optional. Required only when negative gate drive is implemented.

Electrical and Switching Specifications

Unless otherwise specified, all Minimum/Maximum specifications are at recommended operating conditions; all voltages at input IC reference to V_{EE1}, all voltages at output IC reference to V_{EE2}. All typical values at T_A = 25°C, V_{CC1} = 5V, $V_{CC2} – V_E$ = 15V, V_E = 0V.

Table 1: Electrical and Switching Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
DC-DC Flyback Converter								
PWM Switching Frequency	f_{PWM}	40	60	80	kHz			a
Maximum PWM Duty Cycle	D	50	55	60	%		11	
VCC1 Turn-on Threshold	V_{CC1_TH+}	2.5	—	4.6	V			
VCC1 Turn-off Threshold	V_{CC1_TH-}	—	—	4.1	V			
SW Turn-on Resistance	R_{ON_SW}	—	0.7	—	Ω	I_{SW} = 1.3A	12	
Regulated VCC2 Voltage	$V_{CC2} – V_E$	14.25	15	15.75	V	I_{COMP} = 0A	13	
SW Over Current Protection Threshold	I_{SW_TH}	—	2	—	A			
VCC2 Over Voltage Protection Threshold, Low to High	$V_{OV\_TH+} – V_E$	17	19	21	V			
VCC2 Over Voltage Protection Threshold, High to Low	$V_{OV\_TH-} – V_E$	16	18	20	V			
IC Supply Current								
Input Supply Current	I_{CC1}	—	4.7	8	mA		14	
Output High Supply Current	I_{CC2H}	—	12.5	17.5	mA	I_F = 10 mA, $V_E – V_{EE2}$ = 0V	15	
Output Low Supply Current	I_{CC2L}	—	12.5	17.5	mA	I_F = 0 mA, $V_E – V_{EE2}$ = 0V	15	
Output High VE Supply Current	I_{EH}	—	–1.5	—	mA	I_F = 10 mA	16	

Table 1: Electrical and Switching Specifications (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Output Low VE Supply Current	I_{EL}	—	–1.5	—	mA	I_F = 0 mA	16	
Logic Input and Output								
LED Forward Voltage (VAN - VCA)	V_F	1.25	1.55	1.85	V	I_F = 10 mA	17	
LED Reverse Breakdown Voltage (VCA - VAN)	V_{BR}	6	—	—	V	I_F = –10 µA		
LED Input Capacitance	C_{IN}	—	90		pF			
LED Turn On Current Threshold, Low to High	I_{TH+}	—	3.2	6	mA	V_O = 5V	18	
LED Turn On Current Threshold, High to Low	I_{TH-}	—	2.9	5.7	mA	V_O = 5V	18	
LED Turn On Current Hysteresis	I_{TH_HYS}	—	0.3	—	mA			
/UVLO Logic Low Output Current	$I_{/UVLO\_L}$	4	—	—	mA	$V_{/UVLO}$ = 0.4V		
/UVLO Logic High Output Current	$I_{/UVLO\_H}$	—	—	1	µA	$V_{/UVLO}$ = 5V		
/FAULT Logic Low Output Current	$I_{/FAULT\_L}$	4	—	—	mA	$V_{/FAULT}$ = 0.4V		
/FAULT Logic High Output Current	$I_{/FAULT\_H}$	—	—	1	µA	$V_{/FAULT}$ = 5V		
/OT Logic Low Output Current	$I_{/OT\_L}$	4	—	—	mA	$V_{/OT}$ = 0.4V		
/OT Logic Low Output Current	$I_{/OT\_H}$	—	—	1	µA	$V_{/OT}$ = 5V		
Gate Driver								
High Level VO Voltage	V_{O_H}	V_{CC2} – 0.5	V_{CC2} – 0.2	—	V	I_O = –20 mA		b, c, d
Low Level VO Voltage	V_{O_L}	—	0.2	0.5	V	I_O = 50 mA		
Low Level MSD Voltage	V_{MSD_L}	—	0.2	0.5	V	I_{MSD} = 32 mA		
Low Level SSD Voltage	V_{SSD_L}	—	0.2	0.5	V	I_{SSD} = 18 mA		
High Level VO Current	I_{O_H}	—	—	–1	A	$V_O = V_{CC2}$ – 5V	19	e
Low Level VO Current	I_{O_L}	2.5	—	—	A	V_O = 5V	20	e
Low Level MSD Current	I_{MSD_L}	1.6	—	—	A	V_{MSD} = 5V	21	e
Low Level SSD Current	I_{SSD_L}	0.9	—	—	A	V_{SSD} = 5V\	22	e
V_{IN} to High Level VO Propagation Delay Time	t_{PLH}	—	80	150	ns	Cload = 1 nF, f = 10 kHz, Duty cycle = 50%	23, 27	f
V_{IN} to Low Level VO Propagation Delay Time	t_{PHL}	—	80	150	ns		23, 27	g
Pulse Width Distortion	PWD	–70	0	70	ns			h, i
Dead Time Distortion ($t_{PLH} – t_{PHL}$)	DTD	–70	0	70	ns			j
VO 10% to 90% Rise Time	t_R	—	15	—	ns			
VO 90% to 10% Fall Time	t_F	—	11	—	ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	30	> 50	—	kV/µs	T_A = 25°C, I_F = 10 mA, V_{CM} = 1500V	28	k
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	30	> 50	—	kV/µs	T_A = 25°, I_F = 0 mA, V_{CM} = 1500V	29	l

Table 1: Electrical and Switching Specifications (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Active Miller Clamp								
Clamp Threshold Voltage	V_{TH_CLAMP}	—	2	—		V		
Clamp Low Level Sinking Current	I_{CLAMP}	1.2	2.5	—	A	$V_{CLAMP} = V_{EE2} + 2.5V$		
V_{CC2} UVLO Protection (UVLO Voltage V_{UVLO} reference to V_E)								
V_{CC2} UVLO Threshold Low to High	$V_{UVLO+} - V_E$	11.4	12.5	13.6	V	V_O > 5V		d, m
V_{CC2} UVLO Threshold High to Low	$V_{UVLO-} - V_E$	10.2	11.3	12.4	V	V_O < 5V		d, n
V_{CC2} UVLO Hysteresis	V_{UVLO_HYS}	—	1.2	—	V			
V_{CC2} to /UVLO High Delay	t_{PLH_UVLO}	—	20	—	µs			o
V_{CC2} to /UVLO Low Delay	t_{PHL_UVLO}	—	40	—	µs			p
V_{CC2} UVLO to VO High Delay	t_{UVLO_ON}	—	5.5	—	µs			q
V_{CC2} UVLO to VO Low Delay	t_{UVLO_OFF}	—	4.2	—	µs			r
Over-Current and Short-Circuit Protection (reference to V_E)								
Over-Current Sensing Threshold	$V_{OC} - V_E$	0.45	0.5	0.55	V		24	s
Short-Circuit Current Sensing Threshold	$V_{SC} - V_E$	0.67	0.715	0.76	V		25	t
V_{CC2} during Short-Circuit Fault Condition	$V_{CC2(FAULT)}$	—	14.85	—	V			
I_{CC2} during Short-Circuit Fault Condition	$I_{CC2(FAULT)}$	—	13.5	—	mA			
Over-Current Sense Blanking Time	$t_{OC(BLANKING)}$	0.7	1	1.3	µs			u
Short-Circuit Sense to 90% VGATE Delay	$t_{SC(90\%)}$	—		0.5	µs			v
Short-Circuit Sense to /FAULT Low Signal Delay	$t_{SC(/FAULT)}$	—	3.6	—	µs			w
Output Mute Time due to Short-Circuit Event	$t_{SC(MUTE)}$	—	3.8	—	ms			x
Time Input Kept Low Before /FAULT Reset to High	$t_{SC(RESET)}$	—	3.8	—	ms			y
Over-Temperature Protection (reference to V_E)								
Over-Temperature Threshold Low to High	$V_{TIN+} - V_E$	2.22	2.3	2.38	V		26	
Over-Temperature Threshold High to Low	$V_{TIN-} - V_E$	2.05	2.1	2.15	V		26	
Over-Temperature Sense to /OT Low Delay	$t_{OT(/OT)}$	—	0.6	1	ms			z
Output Mute Time due to Over-Temperature	$t_{OT(MUTE)}$	—	3.8	—	ms			aa
Time Input Kept Low Before /FAULT Reset to High	$t_{OT(RESET)}$	—	3.8	—	ms			ab

a. PWM switching frequency of SW is dithered in a range of ±6% typically over 3.3 ms.

b. For High Level Output Voltage testing, V_{O_H} is measured with a dc load current. When driving capacitive loads, V_{O_H} will approach V_{CC2} as I_{O_H} approaches zero.

c. Maximum pulse width = 1.0 ms, maximum duty cycle = 20%.

d. Once V_O of the ACFJ-3540T is allowed to go high ($V_{CC2} – V_E > V_{UVLO+}$), the OC (over current) detection feature of the ACFJ-3540T will be the primary source of IGBT protection. V_{CC2} must be greater than V_{UVLO+} threshold to ensure OC is functional. OC will remain functional until V_{CC2} is below V_{UVLO-} threshold. Thus, the OC detection and UVLO features of the ACFJ-3540T work in conjunction to ensure constant IGBT protection.

e. Maximum pulse width = 1 µs, maximum duty cycle = 1%.

f. t_{PLH} is defined as propagation delay from 50% of LED input V_F to 50% of High level output.

g. t_{PHL} is defined as propagation delay from 50% of LED input V_F to 50% of Low level output.

h. Pulse Width Distortion (PWD) is defined as ($t_{PHL} – t_{PLH}$) of any given unit.

i. As measured from V_F to output (VO).

j. Dead Time Distortion (DTD) is defined as ($t_{PLH} – t_{PHL}$) between any two parts under the same test conditions.

k. Common Mode Transient Immunity (CMTI) in the high state is the maximum tolerable dV_{CM}/d_t of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (that is, Output >13V). A 330-pF and a 10-kΩ pull-up resistor are needed in UVLO, OC, and OT faults detection mode.

l. Common Mode Transient Immunity (CMTI) in the low state is the maximum tolerable dV_{CM}/d_t of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (that is, Output < 1.0 V). A 330-pF and a 10-kΩ pull-up resistor are needed in UVLO, OC, and OT faults detection mode.

m. This is the "increasing" (that is, turn-on or "positive going" direction) of $V_{CC2} – V_E$.

n. This is the "decreasing" (that is, turn-off or "negative going" direction) of $V_{CC2} – V_E$.

o. The delay time when V_{CC2} exceeded UVLO+ threshold to 50% of /UVLO positive going edge.

p. The delay time when V_{CC2} exceeded UVLO- threshold to 50% of /UVLO negative going edge.

q. The delay time when V_{CC2} exceeded UVLO+ threshold to 50% of VO positive going edge (that is, VO turn-on).

r. The delay time when V_{CC2} exceeded UVLO- threshold to 50% of VO negative going edge (that is, VO turn-off).

s. See Description of Operation during Over-Current Condition for further details.

t. See Description of Operation during Short-Circuit Condition for further details.

u. The delay time for ACFJ-3540T to respond to an over current/ short circuit fault condition without any external blanking capacitor at OC pin.

v. The amount of time from when SC threshold is exceeded to 90% of Output negative going edge as mentioned test conditions.

w. The amount of time from when SC threshold is exceeded to 50% of /FAULT negative going edge.

x. The amount of time when SC threshold is exceeded, driver output VO is mute to LED input.

y. The amount of time when SC Mute time is expired, LED input must be kept Low for /FAULT status to return to High.

z. The amount of time from when TIN- threshold is crossed to 50% of /OT negative going edge.

aa. The amount of time when TIN- threshold is crossed, driver output is mute to LED input.

ab. The amount of time when OT Mute time is expired, LED input must be kept Low for /OT status to return to High.

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C	a, b, c
Resistance (Input – Output)	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500 Vdc	c
Capacitance (Input – Output)	C_{I-O}	—	1.3	—	pF	f = 1 MHz	
Thermal Coefficient between LED and Input IC	A_{EI}	—	28	—	°C/W		d
Thermal Coefficient between LED and Output IC	A_{EO}	—	32	—	°C/W		d
Thermal Coefficient between Input IC and Output IC	A_{IO}	—	29	—	°C/W		d
Thermal Coefficient between LED and Ambient	A_{EA}	—	148	—	°C/W		d
Thermal Coefficient between Input IC and Ambient	A_{IA}	—	76	—	°C/W		d
Thermal Coefficient between Output IC and Ambient	A_{OA}	—	52	—	°C/W		d

a. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 VRMS for 1 second.

b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.

c. The device is considered as a two terminal device: pins 1 to 12 shorted together and pins 13 to 24 shorted together.

d. The measurement is done using a PCB board according to JESD51-7.

Thermal Calculation

Application and environmental design for ACFJ-3540T must ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 150°C. The equations that follow are for the purposes of calculating the maximum power dissipation and corresponding effect on junction temperatures. This thermal calculation can only be used as a reference for thermal comparison between actual application board layout and PCB board according to JESD51-7.

LED Junction Temperature = $A_{EA} \times P_E + A_{EI} \times P_I + A_{EO} \times P_O + T_A$

Input IC Junction Temperature = $A_{EI} \times P_E + A_{IA} \times P_I + A_{IO} \times P_O + T_A$

Output IC Junction Temperature = $A_{EO} \times P_E + A_{IO} \times P_I + A_{OA} \times P_O + T_A$

where:

P_E: LED Power Dissipation

P_I: Input IC Power Dissipation

P_O: Output IC Power Dissipation

Calculation of LED Power Dissipation, P_E

LED Power Dissipation, $P_E = I_{F(LED)}$ (Recommended Max) × $V_{F(LED)}$ (125°C) × Duty Cycle

Example: P_E = 16 mA × 1.25V × 50% duty cycle = 10 mW

Calculation of Input IC Power Dissipation, P_I

Input IC Power Dissipation, $P_I = P_{I(Static)} + P_{I(SW)}$

$P_{I(Static)}$: Static power dissipated by the input IC

$P_{I(SW)}$: Power dissipated in the SW pin due to switching current of primary winding of transformer. It is calculated based on averaging switching current and turn-on resistance of SW.

where:

$P_{I(Static)} = I_{CC1}$ (Max) × V_{CC1} (Recommended Max)

$P_{I(SW)} = I_{sw(avg)}^2 \times R_{on\_sw}(125°C) = (I_{SW\_PK}/2 * D_{max})^2 \times R_{on\_sw}(125°C)$

The highest input power dissipation is at minimum V_{BAT+} where average current of SW pin is highest.

Example: Assuming maximum I_{SW_PK} = 1.3A at maximum duty cycle of 50%.

$P_{I(Static)}$ = 8 mA × 5.5V = 44 mW

$P_{I(SW)} = (1.3A / 2 \times 50\%)^2 \times 1\Omega$ = 106 mW

$P_I = P_{I(Static)} + P_{I(SW)}$ = 44 mW + 106 mW =150 mW

Calculation of Output IC Power Dissipation, P_O

Output IC Power Dissipation, $P_O = V_{CC2}$ (Recommended Max) × I_{CC2} (Max) + P_{HS} + P_{LS}

where:

P_{HS}: High Side Switching Power Dissipation

P_{LS}: Low Side Switching Power Dissipation

$P_{HS} = (V_{CC2} \times Q_G \times f_{PWM}) \times R_{OH(MAX)} / (R_{OH(MAX)} + R_{GH}) / 2$

$P_{LS} = (V_{CC2} \times Q_G \times f_{PWM}) \times R_{OL(MAX)} / (R_{OL(MAX)} + R_{GL}) / 2$

where:

Q_O: External Buffer Gate Charge (connector to VO) at Supply Voltage

f_{PWM}: LED Switching Frequency

$R_{OH(MAX)}$: Maximum High Side Output Impedance - VOH(MIN) / IOH(MIN)

R_{GH}: Gate Charging Resistance

$R_{OL(MAX)}$: Maximum Low Side Output Impedance - VOL(MIN) / IOL(MIN)

R_{GL}: Gate Discharging Resistance

Example:

$R_{OH(MAX)} = V_{OH(MIN)} / I_{OH(MIN)}$ = 5V / 1A = 5Ω

$R_{OL(MAX)} = V_{OL(MIN)} / I_{OL(MIN)}$ = 5V / 2.5A = 2Ω

P_{HS} = (15V * 100 nC * 10 kHz) * 5Ω / (5Ω + 10Ω) / 2 = 2.5 mW

P_{LS} = (15V * 100 nC * 10 kHz) * 2Ω / (2Ω + 10Ω) / 2 = 1.25 mW

P_O = 15V * 17.5 mA + 2.5 mW + 1.25 mW = 266 mW

Calculation of Junction Temperature

LED Junction Temperature = 148°C/W × 10 mW + 28°C/W × 150 mW + 32°C/W × 266 mW + T_A = 14.2°C + T_A

Input IC Junction Temperature = 28°C/W × 10 mW + 76°C/W × 150 mW + 29°C/W × 266 mW + T_A = 19.4°C + T_A

Output IC Junction Temperature = 32°C/W × 10 mW + 29°C/W × 150 mW + 52°C/W × 266 mW + T_A = 18.5°C + T_A

Typical Performance Plots

Figure 11: PWM Duty Cycle vs. V_{COMP}

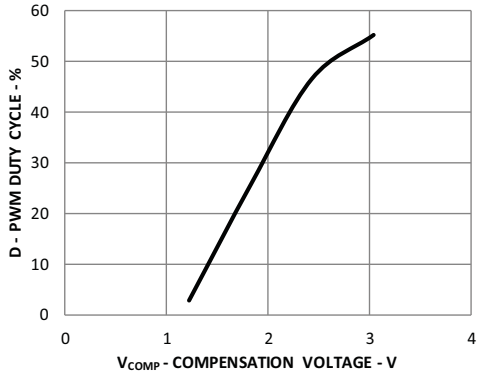


Figure 12: R_{ON_SW} vs. Temperature

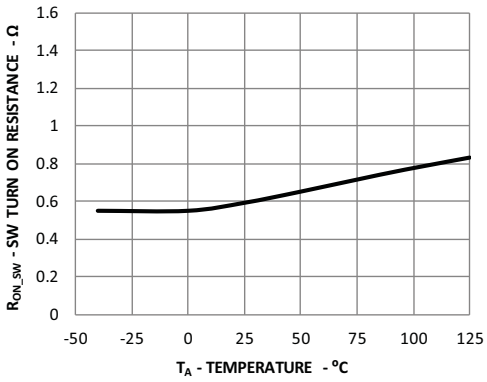


Figure 13: I_{COMP} vs. V_{CC2}

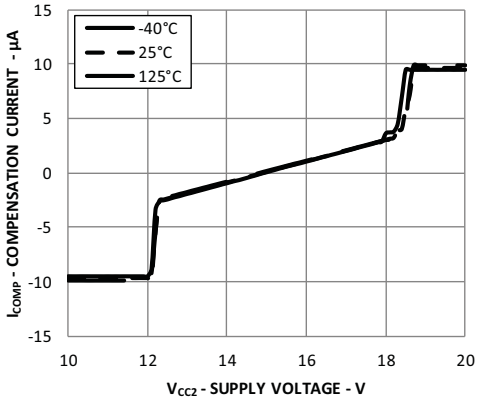


Figure 14: I_{CC1} vs. Temperature

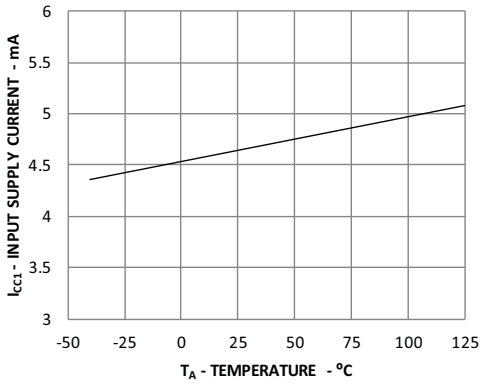


Figure 15: I_{CC2H}/I_{CC2L} vs. Temperature

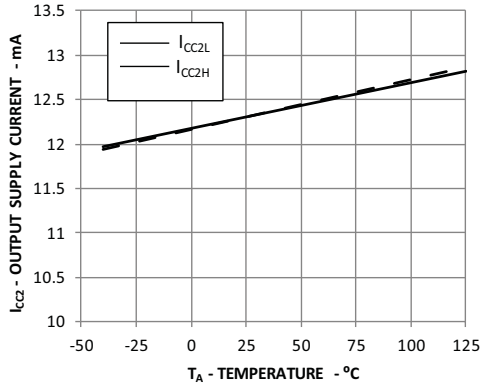


Figure 16: I_{EH}/I_{EL} vs. Temperature

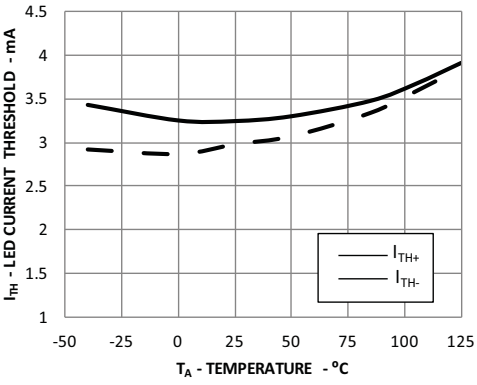


Figure 17: I_F vs. V_F

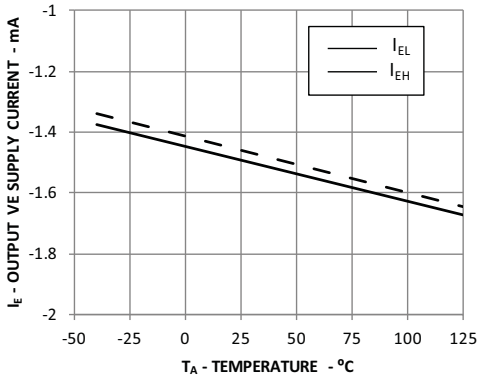


Figure 18: I_{TH+}/I_{TH-} vs. Temperature

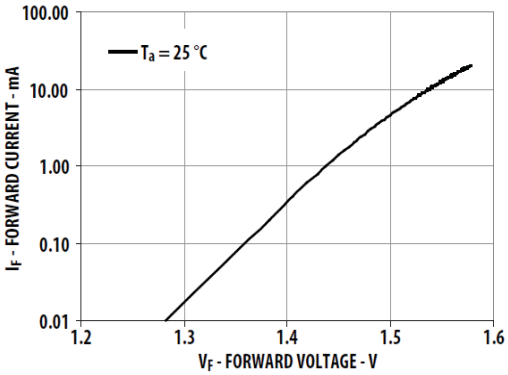


Figure 19: V_{OH} vs. I_{OH}

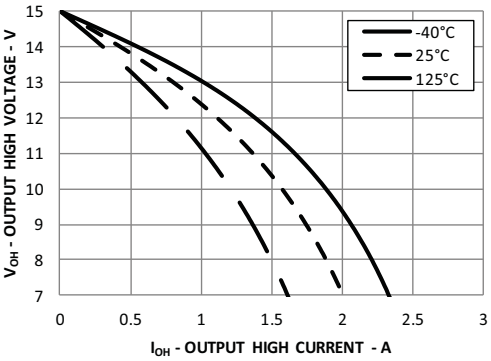


Figure 20: V_{OL} vs. I_{OL}

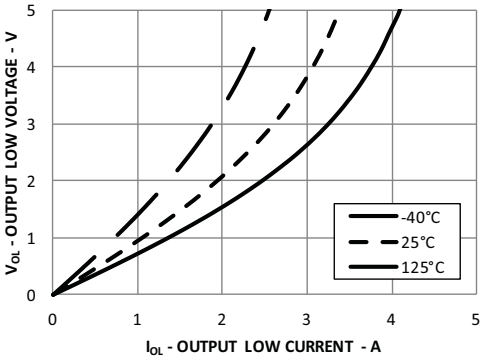


Figure 21: V_{MSDL} vs. I_{MSDL}

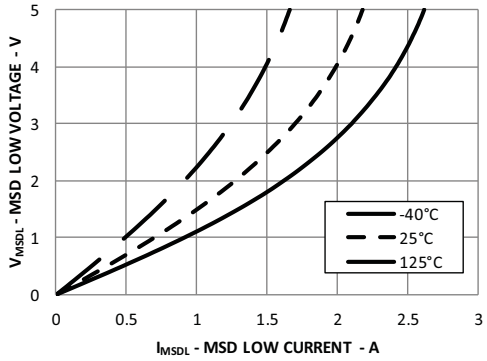


Figure 22: V_{SSDL} vs. I_{SSDL}

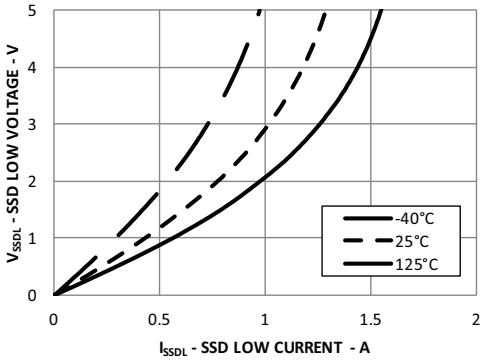


Figure 23: T_{PLH}/T_{PHL} vs. Temperature

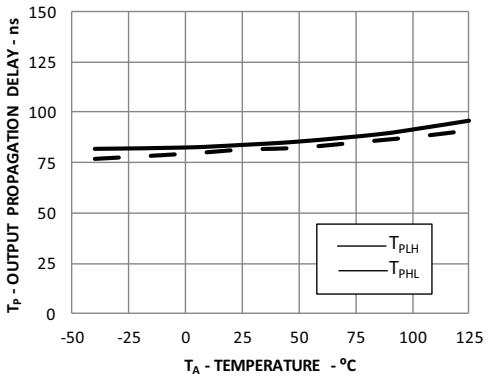


Figure 24: V_{OC} vs. Temperature

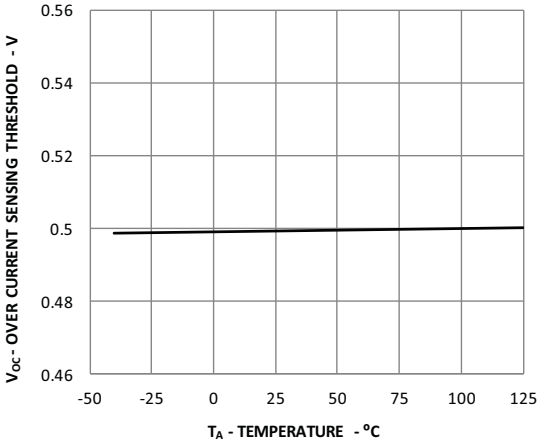


Figure 25: V_{SC} vs. Temperature

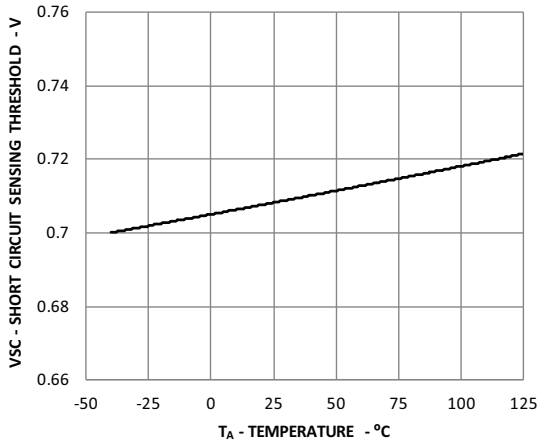


Figure 26: V_{TIN+}/ V_{TIN-} vs. Temperature

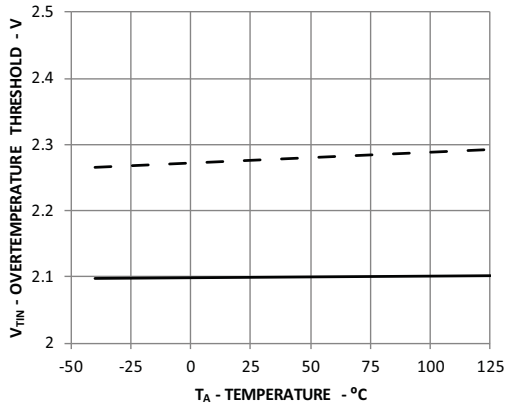


Figure 27: Propagation Delay Test Circuit

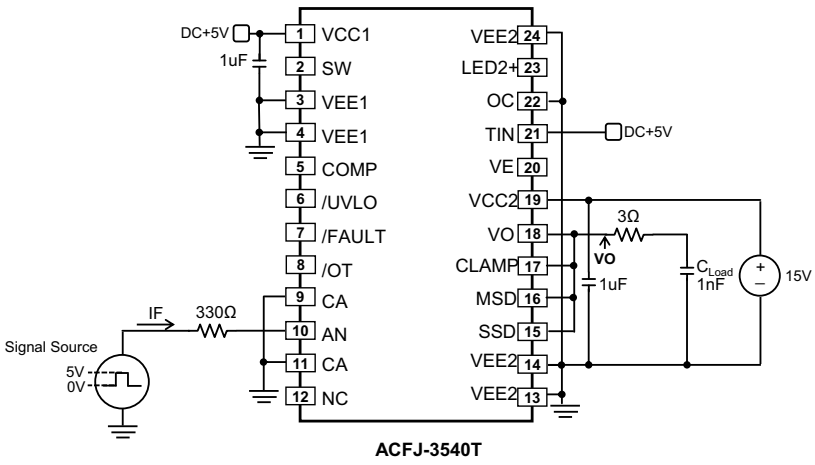


Figure 28: CMR V_O High Test Circuit

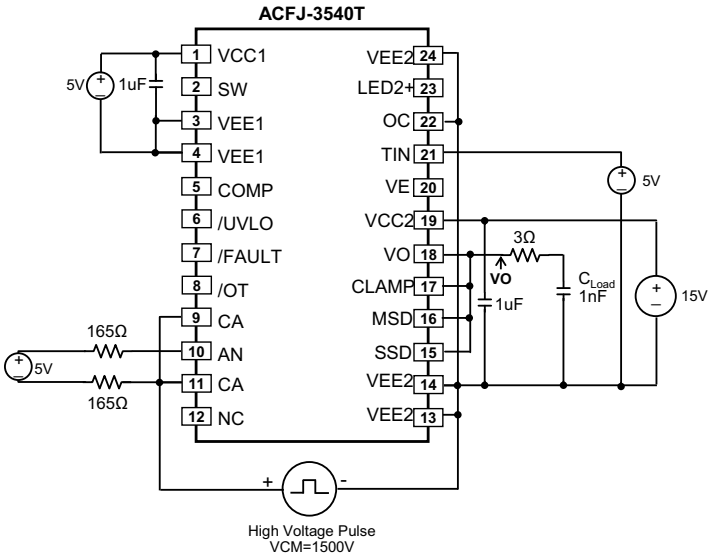


Figure 29: CMR V_O Low Test Circuit