Data Sheet

ACFJ-3531T

Automotive Gate Drive Optocoupler with Integrated Flyback DC-DC Controller, IGBT Desat Sensing, Active Miller Clamping, UVLO Feedback and Negative Bias

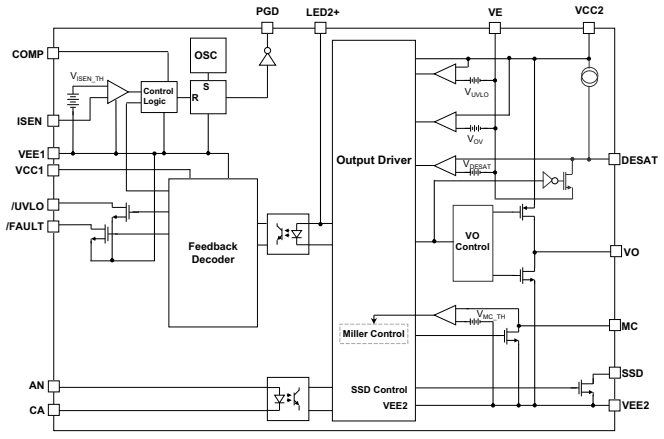
Description

The Broadcom® Automotive Optocoupler Smart Gate Driver features integrated flyback controller for isolated DC-DC converter, IGBT desaturation sensing with soft-shutdown protection and fault feedback, under voltage lockout with feedback, and active Miller current clamping. The fast propagation delay with excellent timing skew performance enables excellent timing control and efficiency. This full feature optocoupler comes in a compact, surface-mountable SO-24 package with 0.8-mm pitch for space-savings, is suitable for HEV and EV applications.

Broadcom R^{2}Coupler™ isolation products provide reinforced insulation and reliability that deliver safe signal isolation critical in automotive and high-temperature industrial applications.

Functional Diagram

Figure 1: ACFJ-3531T Functional Diagram



Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: –40°C to +125°C
- Integrated flyback controller for isolated DC-DC converter for power supply control and diagnostic
  - Regulated output supply voltage: 18.3V ± 5%
  - Programmable negative supply
  - Supply output over load protection
  - Supply output short circuit protection
  - External primary switch good for Load Dump test conditions and high power scaling
- Minimum peak output current: –1.5A/+1.5A
- Minimum Miller clamp sinking current: 2A
- Maximum propagation delay: 200 ns
- Integrated fail-safe IGBT protection
  - IGBT Desat over-current sensing, "Soft" IGBT turnoff and fault feedback
  - Under Voltage Lock-Out protection (UVLO) with feedback
- High noise immunity
  - Common Mode Rejection (CMR): 50 kV/µs at V_{CM} = 1500V
  - Miller current clamping
  - Direct LED input with low input impedance and low noise sensitivity
  - Negative gate bias
- SO-24 package with 8-mm creepage and clearance
- Regulatory approvals:
  - UL1577, CAN/CSA
  - IEC 60747-5-5

Applications

IGBT/SiC MOSFET gate driver for traction inverter, charger, and HVAC

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage, degradation, or both that might be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACFJ-3531T	-000E	SO-24	X		X	45 per tube
	-500E		X	X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

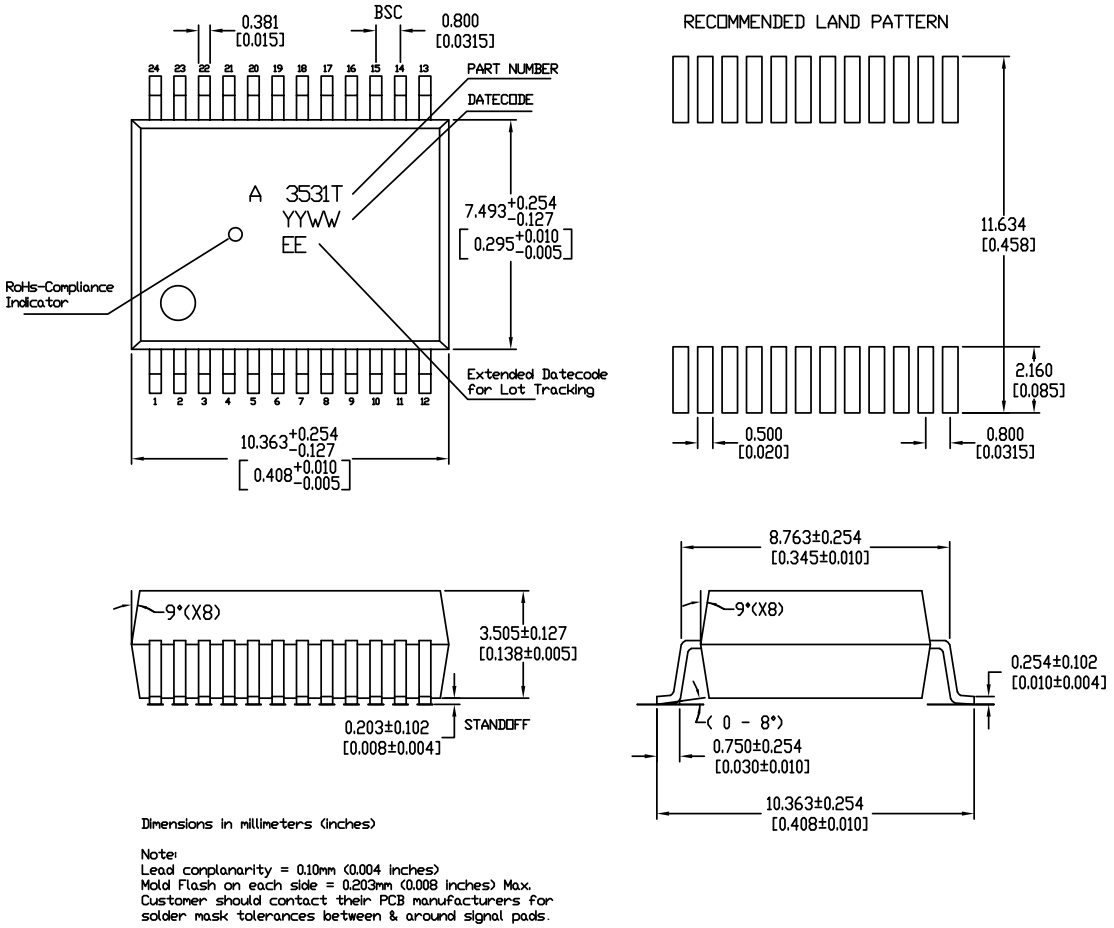
Example 1:

ACFJ-3531T-500E to order product of SO-24 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawing

Figure 2: Package Outline Drawing (24-Lead Surface Mount)



Recommended PB-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

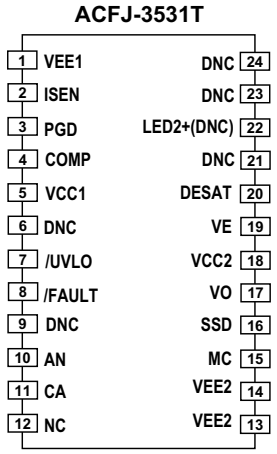
NOTE: Use non-halide flux.

Product Overview Description

The ACFJ-3531T (shown in Figure 1) is a highly integrated power control device that incorporates all the necessary components for a complete, isolated IGBT gate drive circuit. It features flyback controller for isolated DC-DC converter, a high-current gate driver, Miller current clamping, IGBT desaturation over-current protection, supply under voltage lock-out protection and feedback in a SO-24 package. Direct LED input allows flexible logic configuration and differential current mode driving with low input impedance, greatly increased its noise immunity.

Package Pin Out

Figure 3: ACFJ-3531T Pin Configuration



Pin Description

Pin Number	Pin Name	Description
1	VEE1	Input ground
2	ISEN	Current sense for flyback controller
3	PGD	Primary gate driver for external MOSFET
4	COMP	Compensation network for flyback controller
5	VCC1	Input power supply
6	DNC	Do not connect (internally connected to VEE1 lead frame)
7	/UVLO	Under-voltage feedback for VCC1; under-voltage lock out feedback for VCC2; over-voltage feedback for VCC2
8	/FAULT	Desaturation fault feedback
9	DNC	Do not connect (internally connected to input LED cathode lead frame)
10	AN	Input LED anode
11	CA	Input LED cathode
12	NC	No connection
13	VEE2	Output ground (connect decoupling capacitor to VCC2 and VEE2 planes through vias locally)
14	VEE2	Output ground (connect decoupling capacitor to VCC2 and VEE2 planes through vias locally)
15	MC	Miller current clamping output
16	SSD	Soft shutdown driver
17	VO	Output driver for IGBT/MOSFET gate
18	VCC2	Output power supply (connect decoupling capacitor to VCC2 and VEE2 planes through vias locally)
19	VE	IGBT emitter/MOSFET source reference
20	DESAT	Desaturation over-current sensing
21	DNC	Do not connect (internally connected to LED2+ lead frame)
22	LED2+(DNC)	Do not connect, for testing only
23	DNC	Do not connect (internally connected to VEE2 lead frame)
24	DNC	Do not connect (internally connected to VEE2 lead frame)

Approvals

The ACFJ-3531T is approved by the following organizations.

UL	CAN/CSA	IEC/EN/DIN EN 60747-5-5
Approved under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}	Approved under CAN/CSA-C22.2 No. 62368-1	Approved under: IEC 60747-5-5, EN 60747-5-5, DIN EN 60747-5-5

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Units
Insulation Classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 Vrms		I - IV	
for rated mains voltage ≤ 300 Vrms		I - IV	
for rated mains voltage ≤ 600 Vrms		I - IV	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1230	V_{PEAK}
Input to Output Test Voltage, Method b V_{IORM} × 1.875 = V_{PR}, 100% Production Test with tm = 1s, Partial Discharge < 5 pC	V_{PR}	2306	V_{PEAK}
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, tm = 10s, Partial Discharge < 5 pC	V_{PR}	1968	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60s)	V_{IOTM}	8000	V_{PEAK}
Safety-Limiting Values – maximum values allowed in the event of a failure			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	> 10^9	Ω

NOTE:

1. Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.
2. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulation section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from the input terminals to the output terminals, shortest distance through the air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from the input terminals to the output terminals, shortest distance path along the body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and the detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110)

ESD Ratings

Parameter	Classification	Note
Human Body Model	2	Per AEC Q100-002
Charge Device Model	C2a	Per AEC Q100-011

Absolute Maximum Ratings

Unless otherwise specified, all voltages at input IC reference to V_{EE1}, all voltages at output IC reference to V_{EE2}.

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	150	°C	
Operating Temperature	T_A	–40	125	°C	
IC Junction Temperature	T_J	—	150	°C	
Average LED Input Current	$I_{F(AVG)}$	—	20	mA	
Peak Transient LED Input Current (< 1-µs pulse width, 300 pps)	$I_{F(TRAN)}$	—	1	A	
LED Reverse Input Voltage (V_R)	$V_{CA} - V_{AN}$	—	6	V	
ISEN Pin Voltage	V_{ISEN}	–0.5	6	V	a
Primary Gate Driver Voltage	V_{PGD}	–0.5	6	V	a
COMP Pin Voltage	V_{COMP}	–0.5	6	V	a
Input Supply Voltage	V_{CC1}	–0.5	6	V	a
/UVLO Pin Voltage	$V_{/UVLO}$	–0.5	6	V	a
/FAULT Pin Voltage	$V_{/FAULT}$	–0.5	6	V	a
/UVLO Output Sinking Current	$I_{/UVLO}$	—	5	mA	
/FAULT Output Sinking Current	$I_{/FAULT}$	—	5	mA	
Total Output Supply Voltage	V_{CC2}	–0.5	30	V	b
Positive Output Supply Voltage	$V_{CC2} - V_E$	–0.5	24	V	
Negative Output Supply Voltage	$V_{EE2} - V_E$	–12	0.5	V	
DESAT Pin Voltage	$V_{DESAT} - V_E$	–0.5	V_{CC2} + 0.5	V	
Gate Driver Output Voltage, VO	V_O	–0.5	V_{CC2} + 0.5	V	b
Gate Driver Output Voltage, SSD	V_{SSD}	–0.5	V_{CC2} + 0.5	V	b
Gate Driver Output Voltage, MC	V_{MC}	–0.5	V_{CC2} + 0.5	V	b
Peak Output Current, VO	$\lvert I_{O(PEAK)} \rvert$	—	2.5	A	c
Output IC Power Dissipation	P_O	—	600	mW	d
Input IC Power Dissipation	P_I	—	150	mW	e

a. Reference to V_{EE1}.

b. Reference to V_{EE2}.

c. Maximum pulse width=1 µs, maximum duty cycle=1%.

d. Output IC power dissipation is derated linearly above 105°C from 600 mW to 550 mW at 125°C for high effective thermal conductivity board. For low effective thermal conductivity board, output IC power dissipation is derated linearly above 105°C from 600 mW to 400 mW at 125°C. PCB thermal resistance characteristic has to be considered so as not to exceed absolute maximum rating. See Thermal Resistance Model for ACFJ-3531T for details.

e. Input IC power dissipation is derated linearly above 105°C from 150 mW to 125 mW at 125°C for high effective thermal conductivity board. For low effective thermal conductivity board, input IC power dissipation is derated linearly above 105°C from 150 mW to 100 mW at 125°C. See Thermal Resistance Model for ACFJ-3531T for details.

Recommended Operating Conditions

Unless otherwise specified, all voltages at input IC reference to V_{EE1}, all voltages at output IC reference to V_{EE2}.

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T_A	–40	125	°C	
Input IC Supply Voltage	V_{CC1}	4.5	5.5	V	a
Positive Output IC Supply Voltage	$V_{CC2} – V_E$	17.4	19.2	V	
Negative Output IC Supply Voltage	$V_{EE2} – V_E$	–6	0	V	b
Input LED Turn On Current	$I_{F(ON)}$	10	16	mA	
Input LED Turn Off Voltage ($V_{AN} – V_{CA}$)	$V_{F(OFF)}$	–5.5	0.8	V	
DC-DC Flyback Controller PWM Duty Cycle	D_{MAX}	—	50	%	c

a. Power-up sequence: Battery supply (V_{BAT+}) to the DC-DC flyback transformer must be ready before V_{CC1} power up. When V_{CC1} is powered up from 0V to V_{UVLO1_TH+}, DC-DC soft start current will starts to charge the compensation network which is connected to COMP pin. Subsequently, V_{CC2} supply will be regulated to 18.3V. See Soft Start Operation for details.

b. This supply is optional. It is required only when negative gate drive is implemented. Negative gate drive voltage can be programmed easily by connecting a Zener diode from V_E to V_{EE2}. Connect V_E to V_{EE2} if negative gate drive bias is not required.

c. See Operation of Integrated DC-DC Flyback Controller for details.

Electrical and Switching Specifications

Unless otherwise specified, all minimum/maximum specifications are at recommended operating conditions; all voltages at input IC reference to V_{EE1}, all voltages at output IC reference to V_{EE2}. All typical values at T_A = 25°C, V_{CC1} = 5V, $V_{CC2} – V_E$ = 18.3V, $V_E = V_{EE2}$ = 0V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
DC-DC Flyback Converter								
V_{CC1} MOS Threshold	$V_{CC1\_MOS\_TH}$	0.5	1.3	1.5	V	$I_{/UVLO}$ = 2 mA	29	
V_{CC1} UVLO ON Threshold	V_{UVLO1_TH+}	3.7	4.0	4.3	V		29	
V_{CC1} UVLO Threshold Hysteresis	V_{UVLO1_HYS}	0.08	0.3	0.5	V			
PWM Switching Frequency	f_{PWM}	100	135	170	kHz			a
Primary Gate Drive Output High Level	V_{PGD_H}	V_{CC1} – 0.5	V_{CC1} – 0.25	V_{CC1} – 0.01	V	I_{PGD} = –50 mA		
Primary Gate Drive Output Low Level	V_{PGD_L}	0.01	0.2	0.4	V	I_{PGD} = 50 mA		
Primary Gate Drive Rise Time	t_{r_PGD}	10	22	40	ns	C_{PGD} = 1 nF		
Primary Gate Drive Fall Time	t_{f_PGD}	10	19	40	ns	C_{PGD} = 1 nF		
Maximum PWM Duty Cycle	D_{MAX}	55	62	69	%		7	b
I_{SEN} Threshold	$V_{ISEN\_TH} – V_{EE1}$	0.16	0.2	0.24	V			
Regulated V_{CC2} Voltage	$V_{CC2} – V_E$	17.4	18.3	19.2	V	I_{COMP} = 0A	8	

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
IC Supply Current								
Input Supply Current	I_{CC1}	3	4.5	6.7	mA	V_{COMP} = 2.3V	9	
Output High Supply Current	I_{CC2H}	9	13	17	mA	$V_{CC2} - V_E$ = 19.2V I_F = 10 mA, $V_E - V_{EE2}$ = 0V	10	
Output Low Supply Current	I_{CC2L}	8	12.5	16	mA	$V_{CC2} - V_E$ = 19.2V I_F = 0 mA, $V_E - V_{EE2}$ = 0V	10	
Output High V_E Supply Current	I_{EH}	–1	–1.6	–2.5	mA	$V_{CC2} - V_E$ = 19.2V I_F = 10 mA, $V_E - V_{EE2}$ = 6V	11	
Output Low V_E Supply Current	I_{EL}	–1	–1.6	–2.5	mA	$V_{CC2} - V_E$ = 19.2V I_F = 0 mA, $V_E - V_{EE2}$ = 6V	11	
Logic Input and Output								
LED Forward Voltage ($V_{AN} - V_{CA}$)	V_F	1.25	1.55	1.85	V	I_F = 10 mA	12	
LED Reverse Breakdown Voltage ($V_{CA} - V_{AN}$)	V_{BR}	6	—	—	V	I_F = –10 µA		
LED Input Capacitance	C_{IN}	—	90	—	pF			
LED Turn On Current Threshold, Low to High	I_{TH+}	—	3.1	7.5	mA	V_O > 5V	13	
LED Turn On Current Threshold, High to Low	I_{TH-}	0.3	2.4	—	mA	V_O < 5V	13	
LED Turn On Current Hysteresis	I_{TH_HYS}	—	0.6	—	mA			
/UVLO Logic Low Output Voltage	$V_{/UVLO\_L}$	—	—	0.4	V	$I_{/UVLO}$ = 3 mA		
/UVLO Logic High Output Current	$I_{/UVLO\_H}$	—	0.015	10	µA	$V_{/UVLO}$ = 5V		
/FAULT Logic Low Output Voltage	$V_{/FAULT\_L}$	—	—	0.4	V	$I_{/FAULT}$ = 3 mA		
/FAULT Logic High Output Current	$I_{/FAULT\_H}$	—	0.015	10	µA	$V_{/FAULT}$ = 5V		
Gate Driver								
High Level VO Voltage	V_{OH}	V_{CC2} – 0.25	V_{CC2} – 0.05	V_{CC2} – 0.01	V	I_O = –50 mA	14	c, d, e
Low Level VO Voltage	V_{OL}	0.01	0.05	0.25	V	I_O = 50 mA	15	
Low Level SSD Voltage	V_{SSD_L}	0.01	0.05	0.25	V	I_{SSD} = 40 mA		
High Level VO Current	I_{OH}	—	—	–1.5	A	$V_O = V_{CC2} - 5V$		f
Low Level VO Current	I_{OL}	1.5	—	—	A	V_O = 5V		f
Low Level SSD Current	I_{SSD_L}	2	—	—	A	V_{SSD} = 7V	16	f
V_{IN} to High Level VO Propagation Delay Time	t_{PLH}	—	110	200	ns	V_{Source} = 5V, RLED = 260Ω, Rg = 10Ω, Cload = 1 nF, f = 10 kHz, Duty cycle = 50%	17, 22	g
V_{IN} to Low Level VO Propagation Delay Time	t_{PHL}	—	128	200	ns		17, 22	h
Pulse Width Distortion	PWD	–50	18	100	ns			i, j
Dead Time Distortion ($t_{PLH} - t_{PHL}$)	DTD	–100	–18	50	ns			k
VO 10% to 90% Rise Time	t_R	—	15	—	ns		22	
VO 90% to 10% Fall Time	t_F	—	15	—	ns		22	

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	50	—	—	kV/µs	T_A = 25°C, I_F = 10 mA, V_{CM} = 1500V	23	l
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	50	—	—	kV/µs	T_A = 25°C, I_F = 0 mA, V_{CM} = 1500V	24	m
Active Miller Clamp								
Clamp Threshold Voltage	V_{TH_CLAMP}	1.5	2	2.5				
Clamp Low Level Sinking Current	I_{CLAMP}	2	3.5	—	A	V_{CLAMP} = V_{EE2} + 3.5V	18	
VCC2 UVLO Protection (UVLO Voltage V_{UVLO} reference to V_E)								
V_{CC2} UVLO Threshold Low to High	V_{UVLO2_TH+}	13.6	14.6	15.6	V	V_O > 5V		e, n
V_{CC2} UVLO Threshold High to Low	V_{UVLO2_TH-}	12.6	13.4	14.6	V	V_O < 5V		e, o
V_{CC2} UVLO Hysteresis	V_{UVLO2_HYS}	0.8	1.2	1.4	V			
V_{CC2} to /UVLO High Delay	t_{PLH_UVLO2}	—	15	35	µs			p
V_{CC2} to /UVLO Low Delay	t_{PHL_UVLO2}	—	38	100	µs			q
V_{CC2} UVLO to VO High Delay	t_{UVLO2_ON}	—	2.8	6	µs			r
V_{CC2} UVLO to VO Low Delay	t_{UVLO2_OFF}	—	1.9	6	µs			s
V_{CC2} Over-Voltage Protection (OV Voltage V_{OV} reference to V_E)								
V_{CC2} Over Voltage Protection Threshold, Low to High Reference to V_E	$V_{OV2\_TH+} - V_E$	21	22.3	23.3	V			
V_{CC2} Over Voltage Protection Threshold, High to Low Reference to V_E	$V_{OV2\_TH-} - V_E$	20	21.3	22.3	V			
V_{CC2} Over Voltage to /ULVO Flag High Delay	t_{PLH_OV2}	—	8	20	µs			t
V_{CC2} Over Voltage to /ULVO Flag Low Delay	t_{PHL_OV2}	—	14	35	µs			u
Short Circuit Protection (reference to V_E)								
Desat Sensing Threshold	$V_{DESAT\_TH} - V_E$	8.55	9.1	9.45	V		19	v
Desat Charging Current	I_{CHG}	0.925	1.0	1.075	mA	$V_{DESAT} - V_E$ = 2V	20	
Desat Discharging Current	I_{DSCHG}	19	60	—		$V_{DESAT} - V_E$ = 2V	21	
VCC2 during Short Circuit Fault Condition	$V_{CC2(FAULT)}$	—	18.3	—	V			
ICC2 during Short Circuit Fault Condition	$I_{CC2(FAULT)}$	—	14	—	mA			
Desat Blanking Time	$t_{DESAT(BLANKING)}$	0.1	0.3	0.5	µs			w
Desat Sense to 90% V_{GATE} Delay	$t_{DESAT(90\%)}$	0.05	0.10	0.20	µs	Rg = 15Ω, Cload = 1 nF		x
Desat Sense to V_{GATE} = (V_{EE2} + 2V) Delay	$t_{DESAT(2V)}$	0.1	0.17	0.3	µs			y
Desat Sense to /FAULT Low Signal Delay	$t_{DESAT(/FAULT)}$	2.1	4.2	8	µs			z
Output Mute Time Due to Desaturation Sense	$t_{DESAT(MUTE)}$	1.6	3	6	ms			aa
Time Input Kept Low Before /FAULT Reset to High	$t_{DESAT(RESET)}$	1.6	3	6	ms			ab

a. PWM switching frequency of PGD is dithered in a range of ± 6% typically over 3.3 ms.

b. Maximum PWM duty cycle, D_{MAX} is the hard limit set by IC for protection purpose. For discontinuous mode (DCM) operation, the maximum duty cycle for transformer design should be limited to 50% under system full load conditions.

c. For High Level Output Voltage testing, V_{O_H} is measured with a dc load current. When driving capacitive loads, V_{O_H} will approach V_{CC2} as I_{O_H} approaches zero.

d. Maximum pulse width = 1.0 ms, maximum duty cycle = 20%.

e. After V_O of the ACFJ-3531T is allowed to go high ($V_{CC2} – V_E > V_{UVLO2\_TH+}$), the DESAT detection feature of the ACFJ-3531T will be the primary source of IGBT protection. V_{CC2} must be greater than V_{UVLO2_TH+} threshold to ensure Desat is functional. Desat detection feature will remain functional until V_{CC2} is below V_{UVLO2_TH-} threshold. Thus, the Desat detection and UVLO features of the ACFJ-3531T work in conjunction to ensure constant IGBT protection.

f. Maximum pulse width = 1 µs, maximum duty cycle = 1%.

g. t_{PLH} is defined as propagation delay from 50% of input source voltage, V_{Source} to 50% of High level output.

h. t_{PHL} is defined as propagation delay from 50% of input source voltage, V_{Source} to 50% of Low level output.

i. Pulse Width Distortion (PWD) is defined as ($t_{PHL} – t_{PLH}$) of any given unit.

j. As measured from I_F to output (V_O).

k. Dead Time Distortion (DTD) is defined as ($t_{PLH} – t_{PHL}$) between any two parts under the same test conditions.

l. Common Mode Transient Immunity (CMTI) in the high state is the maximum tolerable dV_{CM}/d_t of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (that is, Output > 15V). A 330 pF and a 10-kΩ pull-up resistor are needed in UVLO and Desat faults detection mode.

m. Common Mode Transient Immunity (CMTI) in the low state is the maximum tolerable dV_{CM}/d_t of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (that is, Output < 1.0V). A 330 pF and a 10-kΩ pull-up resistor are needed in UVLO and Desat faults detection mode.

n. This is the "increasing" (that is, turn-on or "positive going" direction) of $V_{CC2} – V_E$.

o. This is the "decreasing" (that is, turn-off or "negative going" direction) of $V_{CC2} – V_E$.

p. The delay time when V_{CC2} exceeded V_{UVLO2_TH+} to 50% of /UVLO positive going edge.

q. The delay time when V_{CC2} exceeded V_{UVLO2_TH-} threshold to 50% of /UVLO negative going edge.

r. The delay time when V_{CC2} exceeded V_{UVLO2_TH+} to 50% of VO positive going edge (that is, VO turn-on).

s. The delay time when V_{CC2} exceeded V_{UVLO2_TH-} threshold to 50% of VO negative going edge (that is, VO turn-off).

t. The delay time when V_{CC2} exceeded V_{OV2_TH-} to 50% of /UVLO positive going edge.

u. The delay time when V_{CC2} exceeded V_{OV2_TH+} to 50% of /UVLO negative going edge.

v. See During IGBT Short Circuit Event for further details.

w. The delay time for ACFJ-3531T to respond to an over-current/short circuit fault condition without any external blanking capacitor at the DESAT pin.

x. The amount of time from when Desat threshold is exceeded to 90% of V_{GATE} negative going edge as mentioned test conditions.

y. The amount of time from when Desat threshold is exceeded to (V_{EE2} + 2V) of V_{GATE} negative going edge as mentioned test conditions.

z. The amount of time from when Desat threshold is exceeded to 50% of /FAULT negative going edge.

aa. The amount of time when Desat threshold is exceeded, driver output VO is mute to LED input.

ab. The amount of time when Desat Mute time is expired, LED input must be kept Low for /FAULT status to return to High.

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{RMS}	RH < 50%, t = 1 minute, T_A = 25°C	a, b, c
Resistance (Input – Output)	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500 Vdc	c
Capacitance (Input – Output)	C_{I-O}	—	1.3	—	pF	f = 1 MHz	

a. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 VRMS for 1 second.

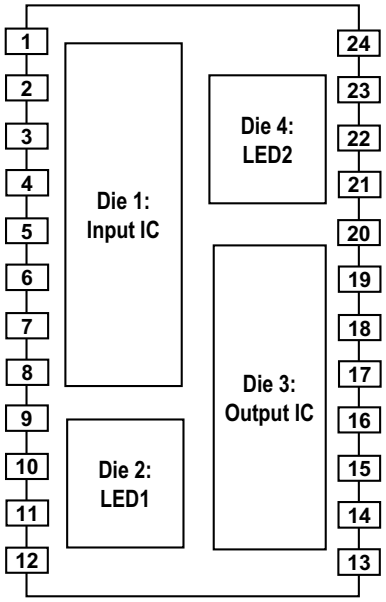
b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.

c. The device is considered as a two-terminal device: pins 1 to 12 are shorted together and pins 13 to 24 are shorted together.

Thermal Resistance Model for ACFJ-3531T

The diagram for measurement is shown in Figure 4. This is a multi-chip package with four heat sources, the effect of heating of one die due to the adjacent dice are considered by applying the theory of linear superposition. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated, and all the dice temperatures are recorded and so on until the fourth die is heated. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4 by 4 matrix for this case of four heat sources.

Figure 4: Diagram of ACFJ-3531T for Thermal Resistance Model



$$\begin{vmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{vmatrix} \cdot \begin{vmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{vmatrix}$$

Definitions

R_{11}: Thermal Resistance of Die1 due to heating of Die1 (°C/W)

R_{12}: Thermal Resistance of Die1 due to heating of Die2 (°C/W)

R_{13}: Thermal Resistance of Die1 due to heating of Die3 (°C/W)

R_{14}: Thermal Resistance of Die1 due to heating of Die4 (°C/W)

R_{21}: Thermal Resistance of Die2 due to heating of Die1 (°C/W)

R_{22}: Thermal Resistance of Die2 due to heating of Die2 (°C/W)

R_{23}: Thermal Resistance of Die2 due to heating of Die3 (°C/W)

R_{24}: Thermal Resistance of Die2 due to heating of Die4 (°C/W)

R_{31}: Thermal Resistance of Die3 due to heating of Die1 (°C/W)

R_{32}: Thermal Resistance of Die3 due to heating of Die2 (°C/W)

R_{33}: Thermal Resistance of Die3 due to heating of Die3 (°C/W)

R_{34}: Thermal Resistance of Die3 due to heating of Die4 (°C/W)

R_{41}: Thermal Resistance of Die4 due to heating of Die1 (°C/W)

R_{42}: Thermal Resistance of Die4 due to heating of Die2 (°C/W)

R_{43}: Thermal Resistance of Die4 due to heating of Die3 (°C/W)

R_{44}: Thermal Resistance of Die4 due to heating of Die4 (°C/W)

P_1: Power dissipation of Die1 (W)

P_2: Power dissipation of Die2 (W)

P_3: Power dissipation of Die3 (W)

P_4: Power dissipation of Die4 (W)

T_1: Junction temperature of Die1 due to heat from all dice (°C)

T_2: Junction temperature of Die2 due to heat from all dice (°C)

T_3: Junction temperature of Die3 due to heat from all dice (°C)

T_4: Junction temperature of Die4 due to heat from all dice (°C)

T_a: Ambient temperature (°C)

ΔT_1: Temperature difference between Die1 junction and ambient (°C)

ΔT_2: Temperature deference between Die2 junction and ambient (°C)

ΔT_3: Temperature difference between Die3 junction and ambient (°C)

ΔT_4: Temperature deference between Die4 junction and ambient (°C)

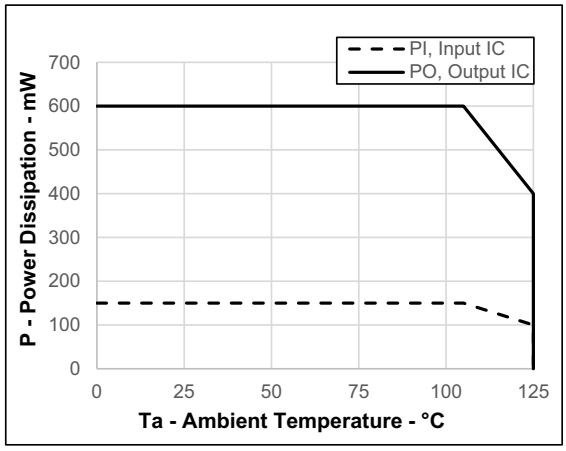
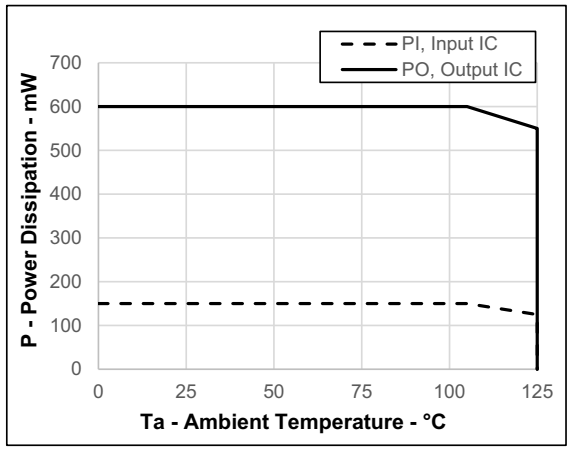
$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + Ta \quad \text{---------- (1)}$$

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + Ta \quad \text{---------- (2)}$$

$$T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + Ta \quad \text{---------- (3)}$$

$$T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + Ta \quad \text{---------- (4)}$$

Measurement is done on both low effective thermal conductivity test board (according to JESD51-3) and on high effective thermal conductivity test board (according to JESD51-7).

Test Board Type	Test Board Conditions	Thermal Resistance	Power Dissipation Derating Chart
Low effective thermal conductivity board	■ Single layer board for signal. ■ Outer layer copper thickness: 2 oz. ■ Board size: 76.2 mm × 76.2 mm.	R_{11}: 59.5°C/W R_{12}: 44.1°C/W R_{13}: 29.6°C/W R_{14}: 49.3°C/W R_{21}: 31.1°C/W R_{22}: 153.5°C/W R_{23}: 33.2°C/W R_{24}: 46.4°C/W R_{31}: 30.3°C/W R_{32}: 50.9°C/W R_{33}: 50.4°C/W R_{34}: 62.9°C/W R_{41}: 33.2°C/W R_{42}: 47°C/W R_{43}: 42°C/W R_{44}: 118.6°C/W	**Figure 5: Power Dissipation Derating Chart Using Low Effective Thermal Conductivity Board**  **NOTE:** ■ Input IC power dissipation is derated linearly above 105°C from 150mW to 100mW at 125°C. ■ Output IC power dissipation is derated linearly above 105°C from 600mW to 400mW at 125°C.
High effective thermal conductivity board	■ Four-layer board that embodies two signal layers, a power plane, and a ground plane. ■ Outer layer copper thickness: 2 oz. ■ Inner layers copper thickness: 1 oz. ■ Board size: 76.2 mm × 76.2 mm.	R_{11}: 37°C/W R_{12}: 18.8°C/W R_{13}: 12.4°C/W R_{14}: 22.9°C/W R_{21}: 15.5°C/W R_{22}: 129.2°C/W R_{23}: 16.1°C/W R_{24}: 21.5°C/W R_{31}: 14.6°C/W R_{32}: 23.9°C/W R_{33}: 28.6°C/W R_{34}: 31.8°C/W R_{41}: 18.4°C/W R_{42}: 22.8°C/W R_{43}: 22.8°C/W R_{44}: 90.5°C/W	**Figure 6: Power Dissipation Derating Chart Using High Effective Thermal Conductivity Board**  **NOTE:** ■ Input IC power dissipation is derated linearly above 105°C from 150 mW to 125 mW at 125°C. ■ Output IC power dissipation is derated linearly above 105°C from 600 mW to 550 mW at 125°C.

Application and environmental design for ACFJ-3531T needs to ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 150°C. The following examples are based on typical circuit shown in Figure 25 for estimation of maximum power dissipation and corresponding effect on junction temperatures. This thermal calculation can only be used as a reference for thermal comparison between actual application board layout and PCB board according to JESD51-7. The actual power dissipation achievable will depend on the application environment (PCB layout, air flow, part placement, and so on).

Calculation of Input IC Power Dissipation, P_1

Input IC Power Dissipation (P_1) = $P_{I(Static)} + P_{IH(PGD)} + P_{IL(PGD)}$

where:

$P_{I(Static)}$ – Static power dissipated by the input IC = $V_{CC1(MAX)} \times I_{CC1(MAX)}$

$P_{IH(PGD)}$ – High side switching power dissipation at PGD pin

= $(V_{CC1(MAX)} \times Q_{G\_ExtMOS} \times f_{PWM\_DCDC}) \times R_{OH\_PGD(MAX)} / (R_{OH\_PGD(MAX)} + R_{G\_PGD}) / 2$

PIL(PGD) – Low side switching power dissipated at PGD pin

= $(V_{CC1(MAX)} \times Q_{G\_ExtMOS} \times f_{PWM\_DCDC}) \times R_{OL\_PGD(MAX)} / (R_{OL\_PGD(MAX)} + R_{G\_PGD}) / 2$

Q_{G_ExtMOS} – Gate charge of external MOSFET connected to PGD pin at supply voltage

f_{PWM_DCDC} – DC-DC switching frequency

$R_{OH\_PGD(MAX)}$ – Maximum high side PGD pin output impedance = 0.5V / 50 mA = 10Ω

$R_{OL\_PGD(MAX)}$ – Maximum low side PGD pin output impedance = 0.4V / 50 mA = 8Ω

R_{G_PGD} – Gate resistance connected to PGD pin

Example:

$P_{I(Static)}$ = 5.5V × 6.7 mA = 36.85 mW

$P_{IH(PGD)}$ = (5.5V × 5 nC × 160 kHz) × 10Ω / (10Ω + 20Ω) / 2 = 0.73 mW

$P_{IL(PGD)}$ = (5.5V × 5 nC × 160 kHz) × 8Ω /(8Ω + 20Ω) / 2 = 0.63mW

P_1 = 36.85 mW + 0.73 mW + 0.63 mW = 38.21 mW

Calculation of Input LED Power Dissipation, P_2

Input LED Power Dissipation (P_2) = $I_{F(LED)}$ (Recommended Max) × $V_{F(LED)}$ (at 125°C) × Duty Cycle

Example:

P_2 = 16 mA × 1.25V × 50% = 10 mW

Calculation of Output IC Power Dissipation, P_3

Output IC Power Dissipation (P_3) = $P_{O(Static)}$ + P_{OH} + P_{OL}

where:

$P_{O(Static)}$ – Static power dissipated by the output IC = $(V_{CC2} – V_{EE2}) \times I_{CC2(MAX)}$

$(V_{CC2} – V_{EE2})$ – Total output power supply = Regulated $V_{CC2(MAX)}$ + Vz *(Vz can be 0V if negative supply is not used)*

P_{OH} – High side switching power dissipation at V_O pin

$= (V_{CC2} – V_{EE2}) \times Q_G \times f_{PWM} \times R_{OH(MAX)} / (R_{OH(MAX)} + R_{GH}) / 2$

P_{OL} – Low side switching power dissipation at VO pin

$= (V_{CC2} – V_{EE2}) \times Q_G \times f_{PWM} \times R_{OL(MAX)} / (R_{OL(MAX)} + R_{GL}) / 2$

Q_G – External buffer gate charge at supply voltage

f_{PWM} – Input LED switching frequency

$R_{OH(MAX)}$ – Maximum high side V_O pin output impedance at $I_{OH(MIN)}$ = 3.33Ω

R_{GH} – Gate charging resistance

$R_{OL(MAX)}$ – Maximum low side V_O pin output impedance $I_{OL(MIN)}$ = 3.33Ω

R_{GL} – Gate discharging resistance

Example:

$(V_{CC2} – V_{EE2})$ = 19.2V + 3.1V = 22.3V

$P_{O(Static)}$ = 22.3V × 17 mA = 379.1 mW

P_{OH} = (22.3V × 200 nC × 10 kHz) × 3.33Ω / (3.33Ω +10Ω) / 2 = 5.57 mW

P_{OL} = (22.3V × 200 nC × 10 kHz) × 3.33Ω / (3.33Ω +10Ω) / 2 = 5.57 mW

P_3 = 379.1 mW + 5.57 mW + 5.57 mW = 390.24 mW

Calculation of LED2 Power Dissipation, P_4

LED2 Power Dissipation (P_4) = $I_{F(LED2)}$ (Design Max) × $V_{F(LED2)}$ (at 125°C) × Duty Cycle

Example:

P_4 = 16 mA × 1.25V × 50% = 10 mW

Calculation of Junction Temperature using High Effective Thermal Conductivity Board:

Input IC Junction Temperature = $(37°C/W \times P_1 + 18.8°C/W \times P_2 + 12.4°C/W \times P_3 + 22.9°C/W \times P_4) + T_a$

Input LED Junction Temperature = $(15.5°C/W \times P_1 + 129.2°C/W \times P_2 + 16.1°C/W \times P_3 + 21.5°C/W \times P_4) + T_a$

Output IC Junction Temperature = $(14.6°C/W \times P_1 + 23.9°C/W \times P_2 + 28.6°C/W \times P_3 + 31.8°C/W \times P_4) + T_a$

LED2 Junction Temperature = $(18.4°C/W \times P_1 + 22.8°C/W \times P_2 + 22.8°C/W \times P_3 + 90.5°C/W \times P_4) + T_a$

Junction temperatures of the internal ICs and LEDs must not exceed 150°C.

Typical Performance Plots

Figure 7: PWM Duty Cycle vs. V_{COMP}

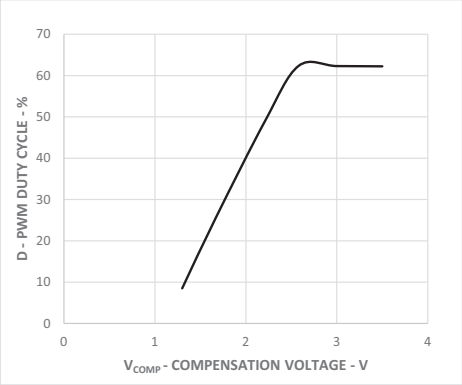


Figure 8: I_{COMP} vs. Supply Voltage

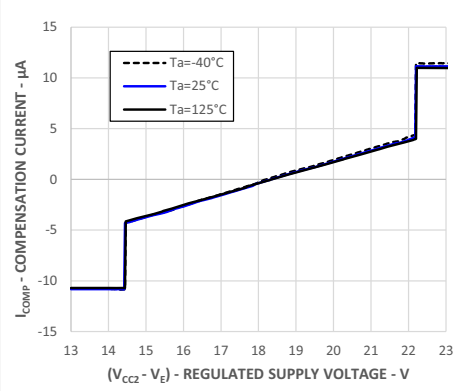


Figure 9: I_{CC1} vs. Temperature

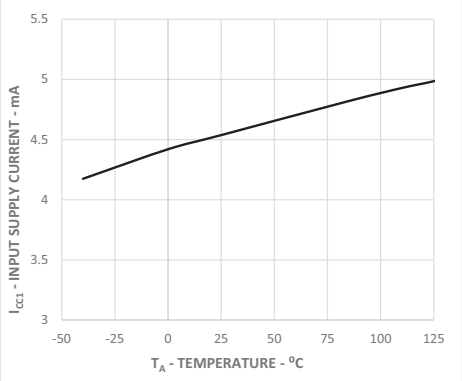


Figure 10: I_{CC2} vs. Temperature

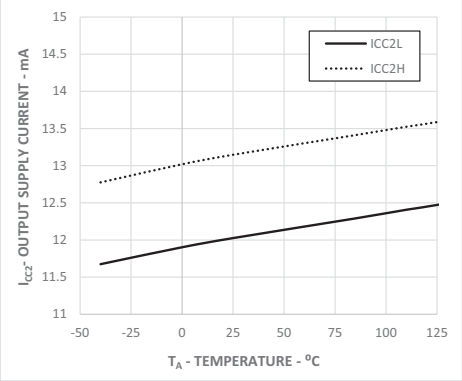


Figure 11: I_E vs. Temperature

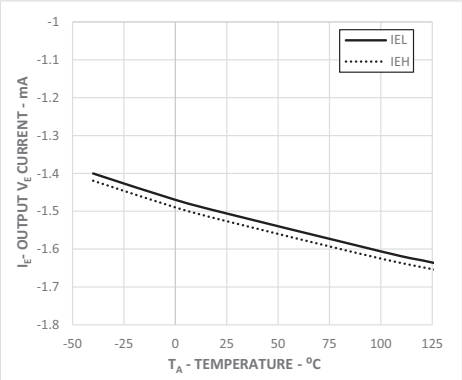


Figure 12: I_F vs. V_F

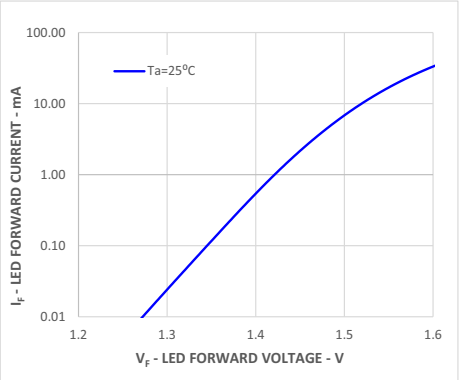


Figure 13: I_{TH} vs. Temperature

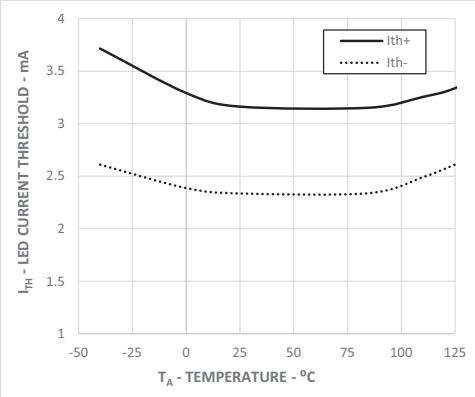


Figure 14: V_{OH} vs. I_{OH}

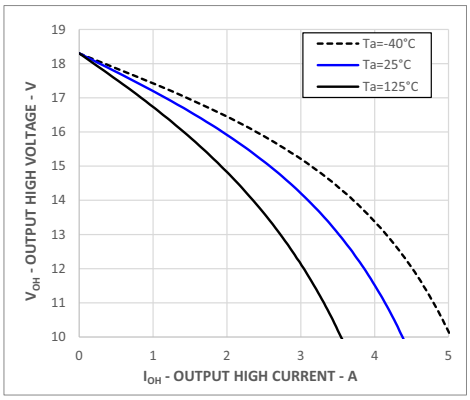


Figure 15: V_{OL} vs. I_{OL}

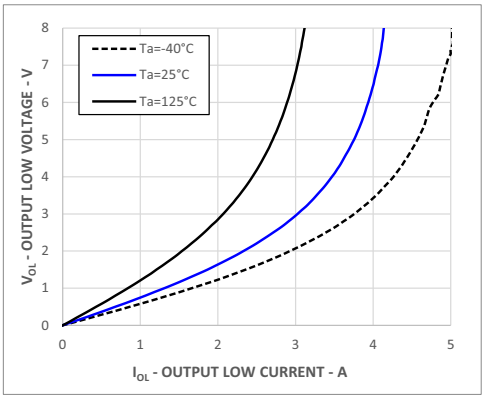


Figure 16: I_{SSD} vs. V_{SSD}

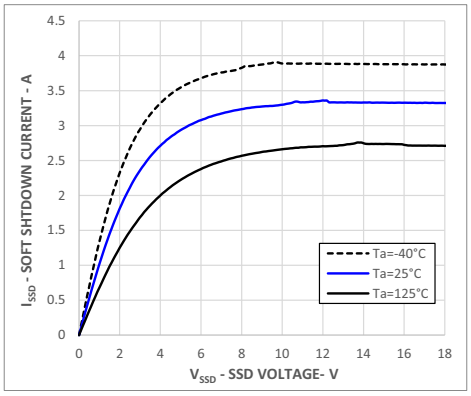


Figure 17: T_P vs. Temperature

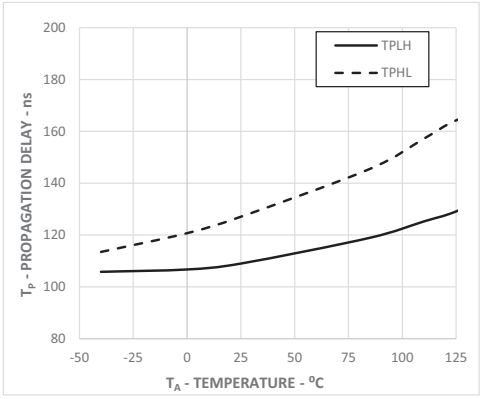


Figure 18: I_{CLAMP} vs. V_{CLAMP}

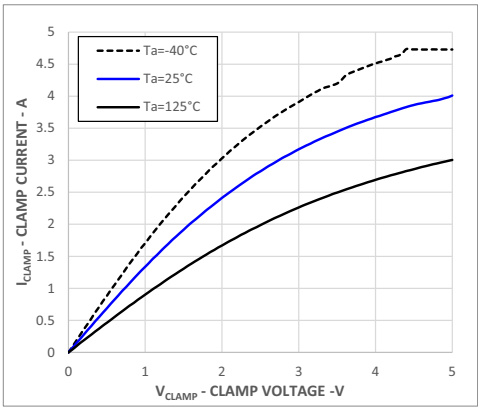


Figure 19: V_{DESAT} vs. Temperature

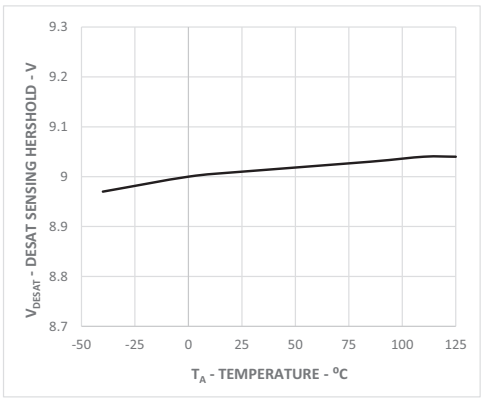


Figure 20: I_{CHG} vs. Temperature

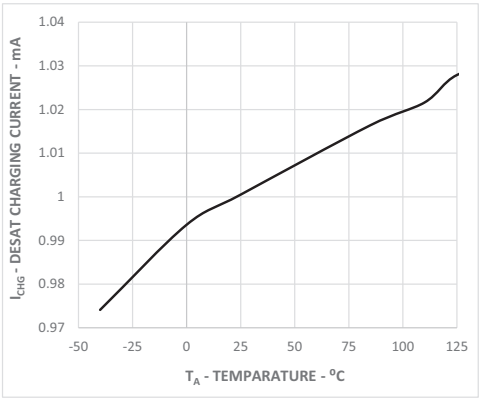


Figure 21: I_{DCHG} vs. Temperature

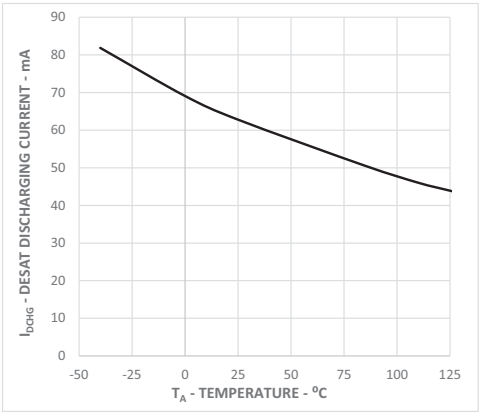


Figure 22: Propagation Delay Test Circuit

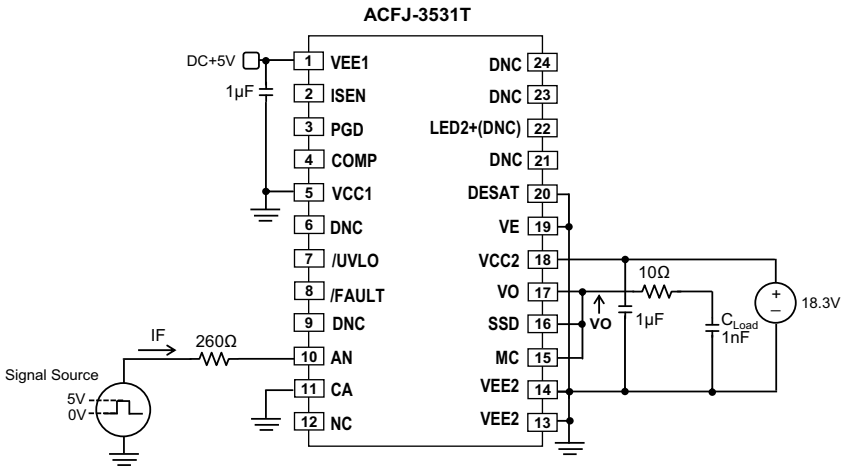


Figure 23: CMR VO High Test Circuit

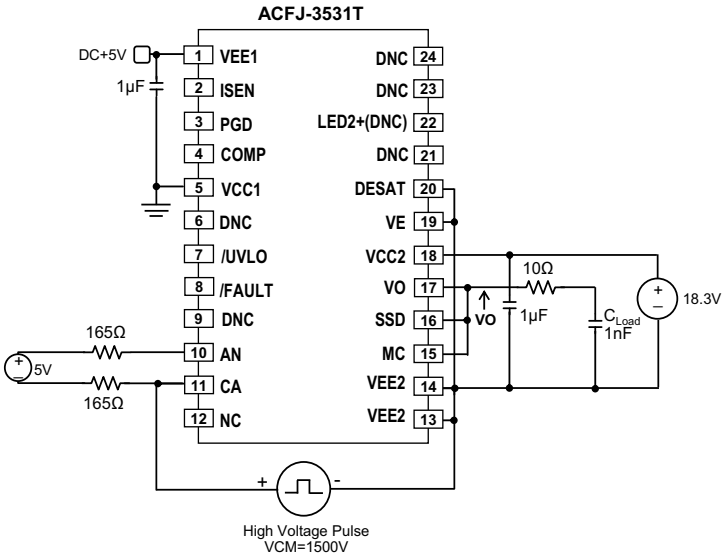
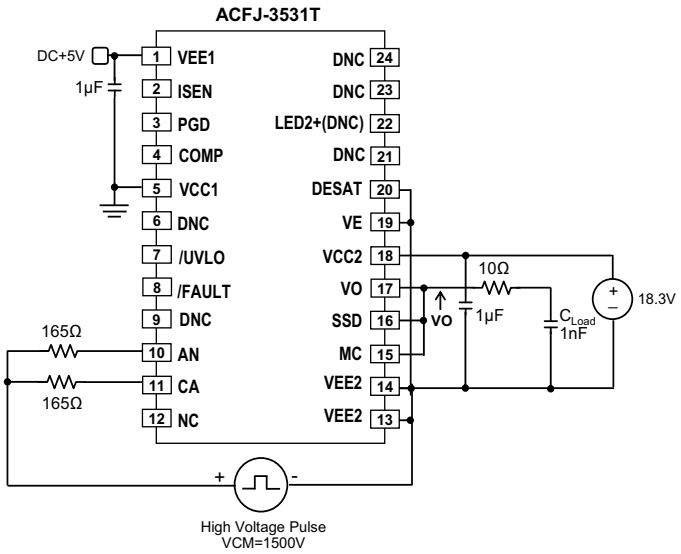
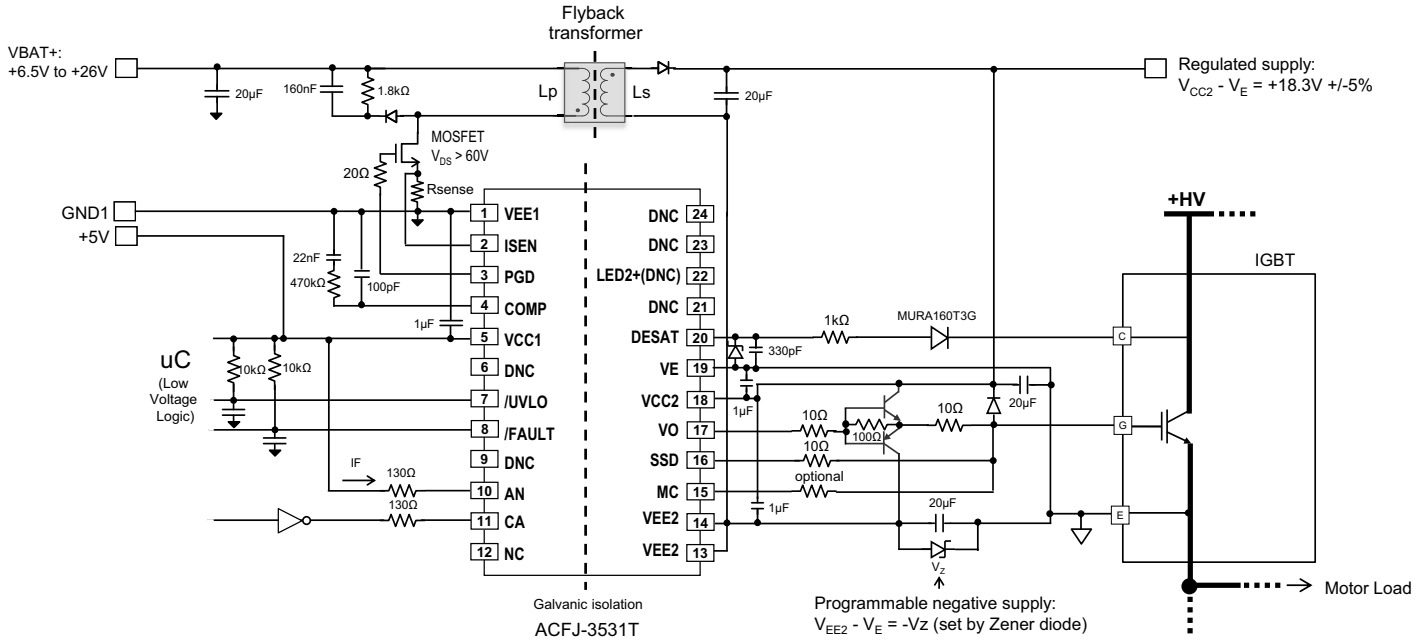


Figure 24: CMR VO Low Test Circuit



Typical Gate Drive Circuit with IGBT Desaturation Detection

Figure 25: ACFJ-3531T Typical Gate Drive Circuit with IGBT Desaturation Over-Current Sensing and Negative Bias Set by Vz



NOTE: Component values are subjected to change with various application requirements.

Description of Operations and Functions

Operation of Integrated DC-DC Flyback Controller

The ACFJ-3531T integrated DC-DC flyback controller operates in a discontinuous conduction mode (DCM) at a fixed average switching frequency of 135 kHz. It converts a wide 6.5V to 26V input range to 18.3V fixed positive output and programmable negative voltage of 0V to 6V. These voltage ranges are well suited for various automotive and industrial applications.

The primary control block implements direct duty cycle control logics for line and load regulation. Primary winding current is sensed and limited to V_{ISEN_TH} to prevent transformer short circuit failure from damaging the primary switch. The sense resistor (R_{sense}) is selected based on the maximum primary winding current limit and maximum power dissipation requirement. Secondary output voltage V_{CC2} is sensed and feedback to the primary control circuits. The closed loop control circuits always regulates V_{CC2} to 16V with respect to V_E. When V_{CC2} is greater than the specified V_{CC2} threshold (V_{OV2_TH+}), V_{CC2} over voltage protection is triggered. The PGD pin on the primary side of gate driver is shut down to protect secondary over voltage failure. When V_{CC2} reduces to V_{OV2_TH-}, the PGD pin is released and DC-DC regulation resumes its normal operations.

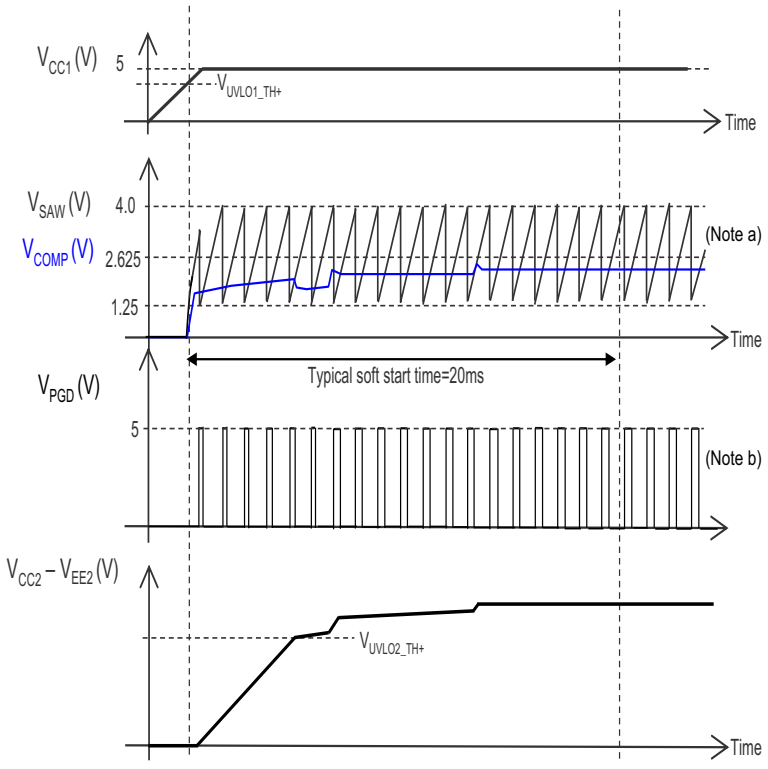
While designing the flyback transformer for DCM controller, the maximum PWM duty cycle must be limited to 50% or less at the minimum input voltage (for example, V_{BAT+} = 6.5V) under full load conditions. A flyback transformer should be connected to ACFJ-3531T according to Figure 25 for complete isolated DC-DC converter. The input LED should be kept off while powering up the V_{CC1}. To ensure proper operation of the DC-DC converter, fast V_{CC1} rise time (≤ 5 ms) is preferred for soft start function to control the inrush current. If V_{CC2} fails to rise above 6V at the end of the soft start period (about 20 ms), the primary switch is turned off to prevent a possible V_{CC2} short circuit event during start-up. The DC-DC controller can be restart by power reset V_{CC1}.

The average PWM switching frequency of primary gate drive (PGD) is dithered ± 6% typically from center frequency of 135 kHz. Frequency dithering feature helps to achieve better EMI performance by spreading the switching and its harmonics over wider band.

Soft Start Operation

ACFJ-3531T is designed with built-in soft start feature. When V_{CC1} is higher than V_{UVLO1_TH+}, the built-in soft start circuit starts to function. Typical soft start timing is 20 ms. Soft start current (I_{COMP}) charges up the compensation network through the V_{COMP} pin and gradually increases the V_{COMP} voltage to the correct working level. Figure 26 shows the typical DC-DC start up waveforms.

Figure 26: Typical DC-DC Start Up Waveforms



NOTE:

a. V_{SAW} is IC internal saw waveform and cannot be measured externally. V_{SAW} frequency is not drawn to scale.

b. Typical DC-DC switching frequency at PGD pin is 135 kHz. V_{PGD} frequency is not drawn to scale.

Status Flags

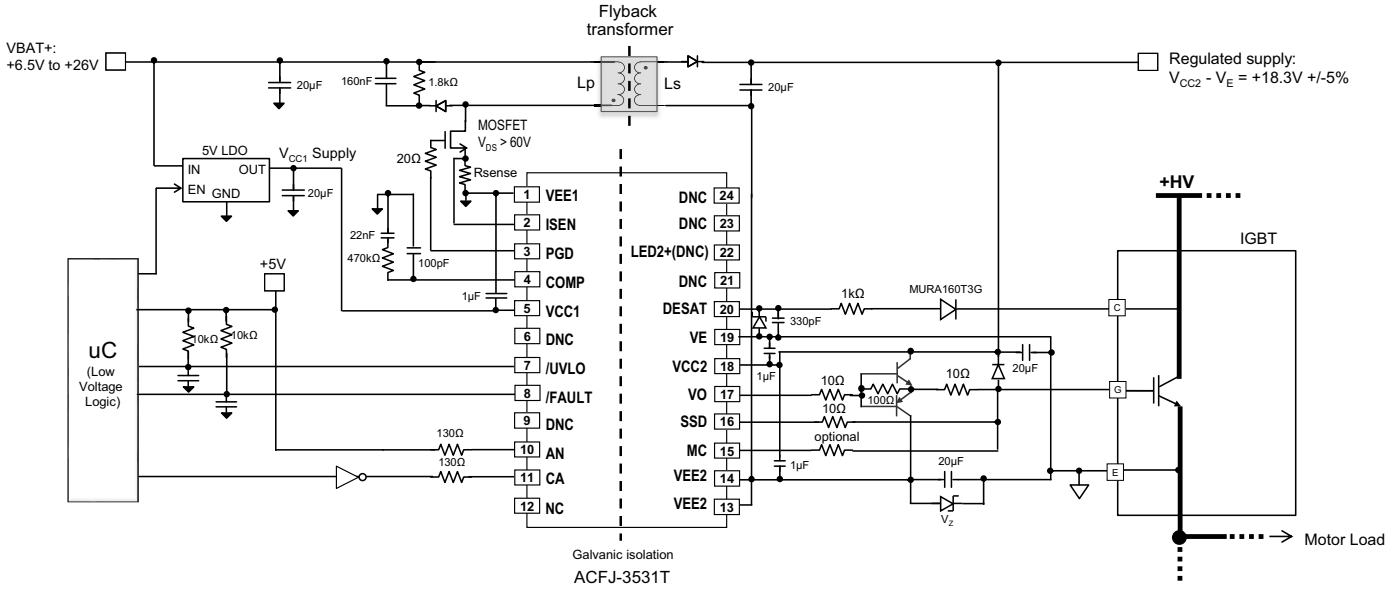
The status flags at the primary side reflect the state of the circuit operation. Figure 29 exemplifies how the status flags react when V_{CC2} ramps up and down when V_{CC1} is ready.

- Normal operation: All the status flags (/UVLO and /FAULT) are in Hi-Z state. These pins are pulled high through the external resistors.
- Under voltage lock out (UVLO) fault: During operation, if V_{CC1} falls below the V_{CC1} threshold (V_{UVLO1_TH-}) or V_{CC2} falls below the UVLO threshold (V_{UVLO2_TH-}), /UVLO flags will be pulled low.
- V_{CC2} over voltage (OV) fault: When V_{CC2} is over V_{CC2} over voltage protection threshold (V_{OV2_TH+}), /UVLO flags will be pulled low.
- IGBT short circuit (SC) fault: If a short circuit fault occurs, the IGBT gate will be soft shutdown (pulled low by the SSD pin action). /FAULT pin will be pulled low.
- LED2 Fault: When $V_{CC2} – V_{EE2}$ supply voltage is greater than typical 6V, secondary side LED2 starts to pulse to inform the primary IC that the feedback channel is working normally. If the primary IC detects no signal from LED2, it is diagnosed as LED2 is faulty. Primary IC will stop the DC-DC regulation by pulling the PGD pin and COMP pin low. Both status flags (/ULVO and /FAULT) will be pulled low to inform the microcontroller. The primary IC's power (V_{CC1}) is then needed to be rebooted for IC reset. Figure 27 shows a typical gate driver circuit with low-dropout linear regulator (LDO) for primary IC (V_{CC1}) reboot during LED2 fault condition.

Table 1: Status Flags

Conditions	Status Flags	
	/UVLO	/FAULT
Normal operation	Hi-Z	Hi-Z
VCC1 UVLO fault	Low	Hi-Z
VCC2 UVLO fault	Low	Hi-Z
VCC2 OV fault	Low	Hi-Z
Short circuit (SC) fault	Hi-Z	Low
LED2 fault	Low	Low

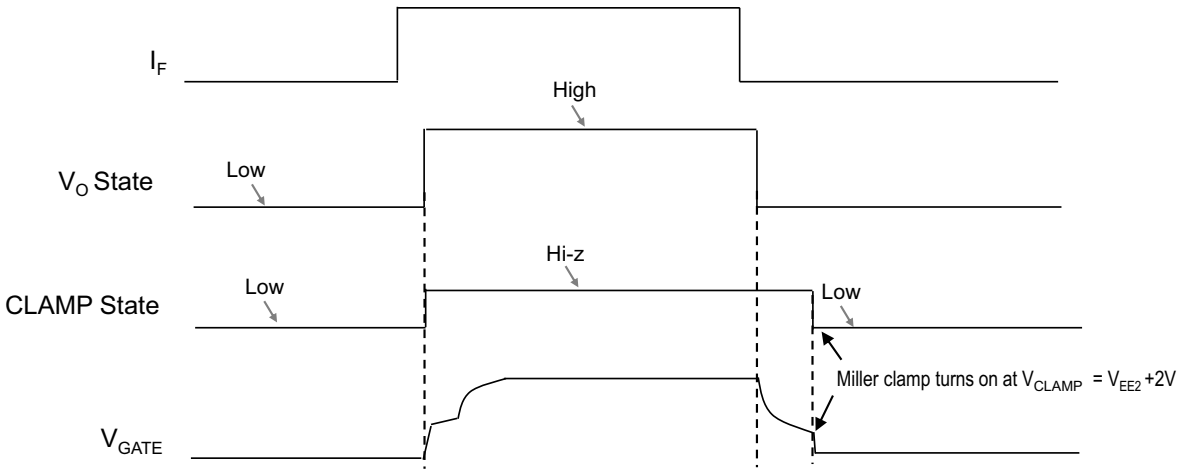
Figure 27: Typical Gate Driver Circuit with Low-Dropout Linear Regulator (LDO) for V_{CC1} Reboot



Description of Gate Driver and Miller Clamping

The gate driver is directly controlled by the input LED current (I_F). When input LED current is driven high, the main output of ACFJ-3531T can then delivers a 1.5A sourcing current to drive the external buffer that drives the IGBT's gate. While the input LED is switched off, V_O provides 1.5A sinking current to external buffer to switch the gate off fast. The Miller clamping pull-down MOSFET (MC pin) is activated when gate voltage drops below V_{TH_CLAMP} voltage to provide low impedance path to Miller current.

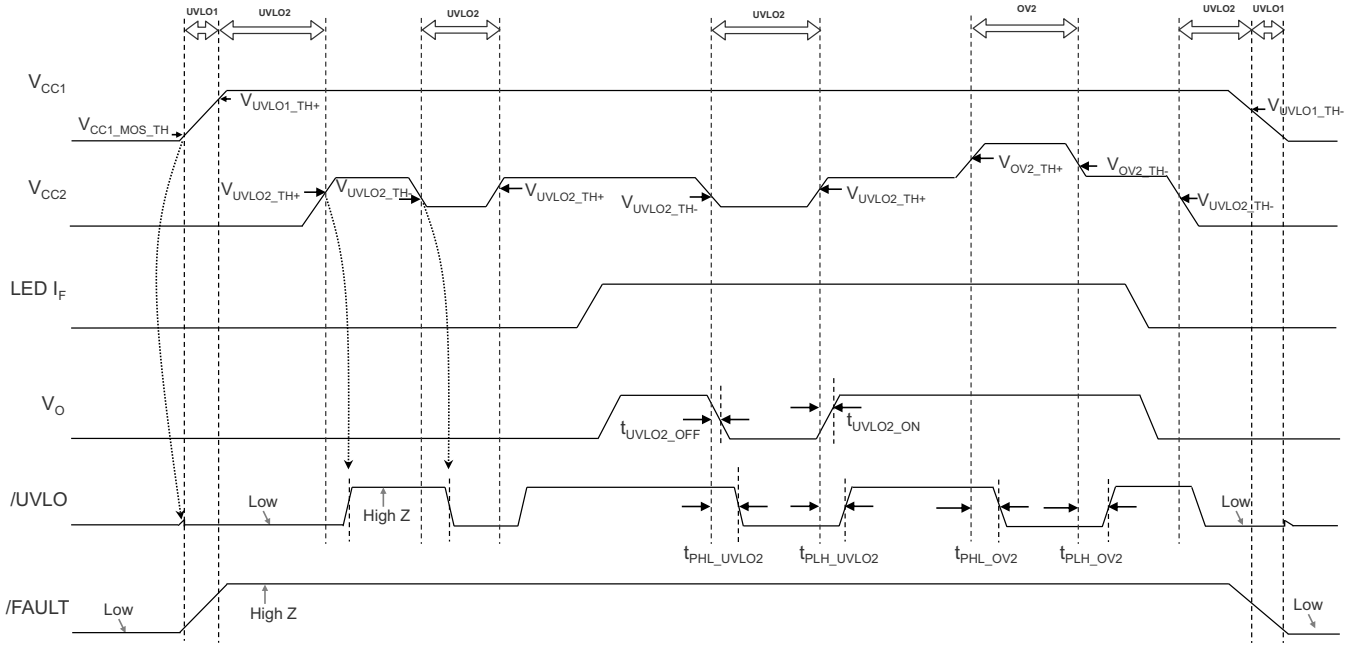
Figure 28: Gate Drive Signal Behavior



Description of Under Voltage Lock Out

Insufficient gate voltage to IGBT can increase turn on resistance of IGBT, resulting in large power loss and IGBT damage due to high heat dissipation. ACFJ-3531T monitors the output power supply (V_{CC2}) constantly. When output power supply is lower than under voltage lock out (UVLO) threshold, gate driver output will shut off to protect IGBT from low voltage bias. During power up, the UVLO feature forces the ACFJ-3531T's output low to prevent unwanted turn-on at lower voltage. When power supply (V_{CC2}) voltage increases more than V_{UVLO2_TH+} threshold, the /UVLO fault status will be cleared and the gate driver resumes its normal function automatically.

Figure 29: Circuit Behaviors during Power Up and Power Down



Description of Over Voltage Protection

When V_{CC2} is greater than the specified V_{CC2} over voltage protection threshold, the PGD pin on the primary side of gate driver is shut down to protect secondary over voltage failure. When V_{CC2} goes below the V_{CC2} over voltage protection threshold, PGD starts to regulate again. The V_{CC2} over voltage condition is feedback to microcontroller by pulling the /UVLO pin low. Output driver (V_O), Miller clamp, Desat protection and soft shutdown functions are not locked out by over voltage protection. See Status Flags for /UVLO and /FAULT feedback truth table.

DESAT Fault Detection Blanking Time

After the IGBT is turned on, the DESAT fault detection circuitry must remain disabled for a short period of time to allow the IGBT collector voltage to fall below the DESAT threshold. This time period, called the total DESAT blanking time, is the sum of both internal DESAT blanking time, $t_{DESAT(BLANKING)}$ and external blanking time. While the internal DESAT blanking time is preset within the device, the external blanking time is flexibly determined by selecting the blanking capacitor (C_{BLANK}) with preset DESAT sensing voltage (V_{DESAT_TH}) and Desat charge current (I_{CHG}).

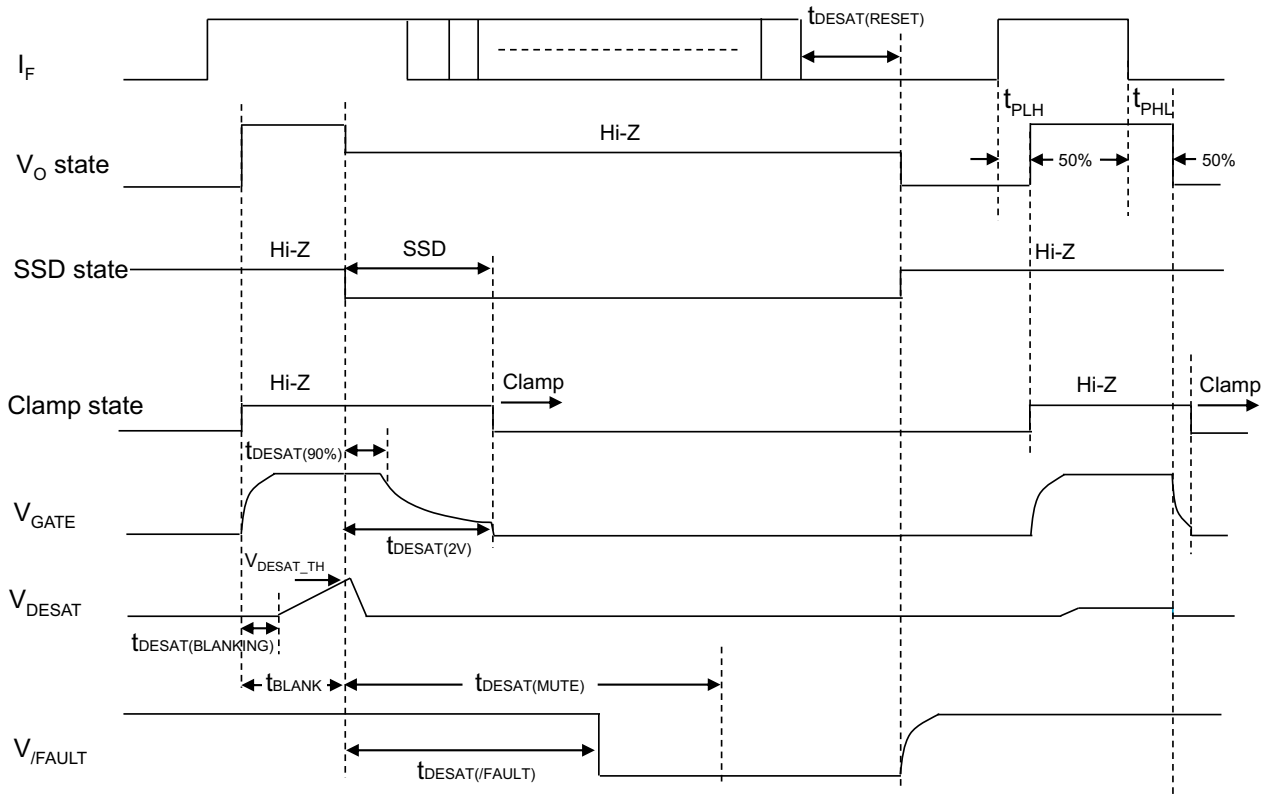
The total blanking time is calculated in terms of internal blanking time ($t_{DESAT(BLANKING)}$), external capacitance (C_{BLANK}), DESAT sensing voltage (V_{DESAT_TH}), and DESAT charge current (I_{CHG}) as follows:

Total DESAT blanking time, $t_{BLANK} = t_{DESAT(BLANKING)} + C_{BLANK} \times V_{DESAT\_TH} / I_{CHG}$

During IGBT Short Circuit Event

1. DESAT terminal monitors IGBT's VCE voltage.
2. When the voltage on the DESAT terminal exceeds 9.1V, the IGBT gate voltage (V_{GATE}) is slowly lowered by soft shutdown (SSD) pin. Output driver, VO enters into high impedance state.
3. Output driver VO ignores all PWM commands during mute time ($t_{DESAT(MUTE)}$) and remains in high impedance state.
4. /FAULT output goes low, notifying the microcontroller of the fault condition.
5. Microcontroller takes appropriate action.
6. When ($t_{DESAT(MUTE)}$) expires, the LED input must be kept low for $t_{DESAT(RESET)}$ before the fault condition can be cleared. /FAULT status will return to high, and SSD output will return to high impedance state.
7. Output (VO) starts to respond to LED input after fault condition is cleared.

Figure 30: Circuit Behaviors during IGBT Short Circuit Event



Printed Circuit Board Layout Considerations

Care must be taken while designing the layout of printed circuit board (PCB) for optimum performance.

Adequate spacing should always be maintained between the high voltage isolated circuitry and any input referenced circuitry. The same minimum spacing between two adjacent high-side isolated regions of the printed circuit board must be maintained as well. Insufficient spacing will reduce the effective isolation and increase parasitic coupling that will effect CMR performance.

The placement and routing of supply bypass capacitors requires special attention. During switching transients, the majority of the gate charge is supplied by the bypass capacitors. Maintaining short charging and discharging paths between capacitors and gate can help to achieve clean switching waveforms and low supply ripples. It is recommended to have supply and ground planes for V_{CC2} and V_{EE2}. It is also recommended to connect IC power pins, such as V_{CC2} (pin 18) and V_{EE2} (pins 13 and 14) and external output buffer directly to these planes using multiple via holes locally. Similar layout guidelines are applicable to input side circuitry, such as power supply V_{CC1} (pin 5), input side ground V_{EE1} (pin 1) and supply decoupling capacitors.

For thermal dissipation purposes, it is recommended to place large copper area for top layer V_{EE2} (pins 13 and 14) and connect the copper area with multiple via holes to V_{EE2} plane at the bottom layer of PCB as illustrated in Figure 31.

The compensation network circuitry which connected to COMP (pin 4) is to be placed next to IC with short traces.

Figure 31: Example of Recommended Layout