Data Sheet

ACFJ-332BT

Automotive Dual-Channel High-Speed 4A Peak Gate Drive Optocoupler for MOSFET/IGBT with Active Miller Clamp and Rail-to-Rail Output Voltage in SO-24 Package

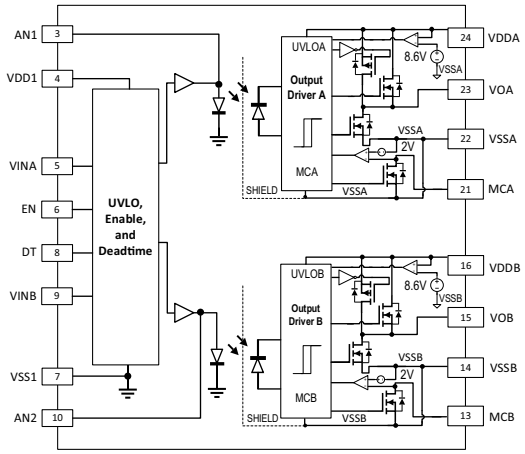
Overview

The Broadcom® ACFJ-332BT drivers are automotive-grade, dual-channel, high-speed, rail-to-rail output gate drive optocouplers, which come in a compact, surface-mountable SO-24 package with two independent isolated channels for space savings. It provides an isolation voltage of 5 kV_{RMS} between the input and the two output channels, with a minimum of 150 kV/µs common mode transient immunity (CMTI).

The ACFJ-332BT operates with a wide range of input voltage and driver output voltage. It also offers enhanced features such as an input buffer drive with TTL and CMOS compatible logics, an enable pin (EN) to support a system functional safety requirement, programmable dead time between two driver channels, and input power supply under-voltage lockout protection to drive MOSFET/ IGBT at high-frequency DC-DC and AC-DC converters.

The Broadcom R^2Coupler™ isolation products provide reinforced insulation and reliability that deliver safe signal isolation critical in automotive and high-temperature industrial applications.

Figure 1: ACFJ-332BT Functional Diagram



Features

- Qualified to AEC-Q100 Grade 1 test guidelines
- Automotive temperature range: –40°C to +125°C
- Wide operating supply range:
  - VDD1 range: 3.0V to 5.5V
  - VDDA and VDDB range: 10V to 25V
- Low supply current allows bootstrap half-bridge topology
- TTL and CMOS compatible inputs
- EN pin for enhanced safety feature
- Programmable dead time
- Under-voltage lockout (UVLO) protection with hysteresis:
  - VDD1 UVLO: 2.7V
  - VDDA and VDDB UVLO: 8.6V
- Rail-to-rail output driver voltage
- Minimum peak output current: ±2.4A
- Minimum Miller clamp sinking current: 1A
- Maximum propagation delay: 70 ns
- Maximum channel-to-channel skew: 15 ns
- High noise immunity
  - Common mode transient immunity (CMTI): 150 kV/µs at V_{CM} = 1500V
  - Active Miller clamp
- Dual isolated channels in an SO-24 package with 8.3-mm creepage and clearance
- 3.5-mm creepage between two output drivers
- Worldwide safety approvals:
  - UL/cUL approved, 5 kV_{RMS}
  - IEC/EN 60747-5-5

Applications

- Automotive power train DC-DC converter, EV/PHEV onboard charger, inverter, and HVAC

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage, degradation, or both that might be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	IEC 60747-5-5	Quantity
ACFJ-332BT	-000E	SO-24	X		X	45 per tube
	-500E		X	X	X	850 per reel

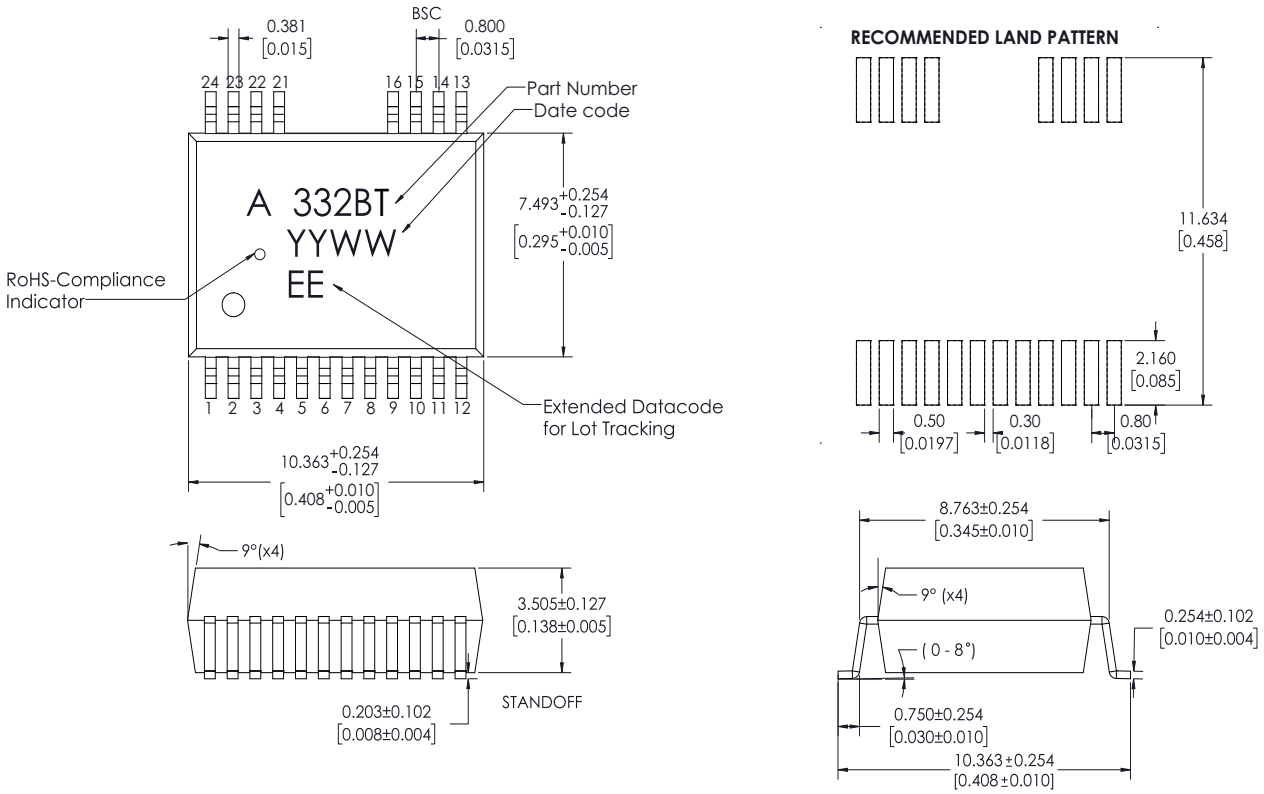
To order, choose a part number from the part number column and combine it with the desired option from the option column to form an order entry.

Example: Specify ACFJ-332BT-500E to order the product comprised of an SO-24 surface-mount package in tape and reel packaging with the IEC 60747-5-5 Safety Approval and RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawing

Figure 2: ACFJ-332BT Package Outline Drawing



NOTE:

- Dimensions are in millimeters (inches).
- Lead coplanarity = 0.10 mm (0.004 inches), Mold Flash on each side = 0.203 mm (0.008 inches) maximum. Customers should contact their PCB manufacturers for the solder-mask tolerance between and around signal pads.

Recommended PB-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Use non-halide flux.

Product Overview Description

The ACFJ-332BT (shown in Figure 1) is a dual-channel, high-speed, rail-to-rail output isolated MOSFET/IGBT gate driver in a compact SO-24 package. The ACFJ-332BT is designed with many enhanced features to enable seamless integration with control circuitry and support functional safety requirements.

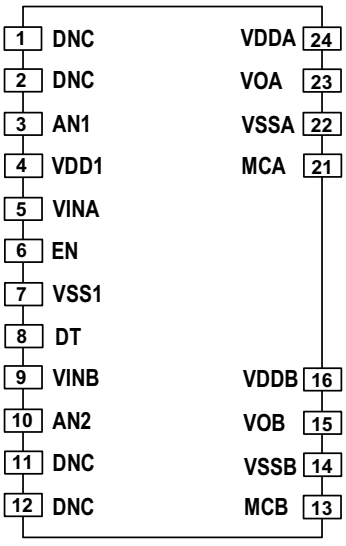
It can operate over a wide input supply VDD1 range of 3V to 5.5V and driver output supply VDDA and VDDB range of 10V to 25V. Both input and output supplies have under-voltage lockout protection, whereby when UVLO protection is triggered, both output drivers (VOA and VOB) are pulled to low state. With the dead time control disabled, its respective input pins (VINA and VINB) can control the dual isolated output drivers independently without an external buffer, since the two input pins (VINA and VINB) are TTL and CMOS logic levels compatible. By connecting an external resistor to the DT pin, the dead time control feature is functional. The output drivers are now configured as a pair of half-bridge drivers, with desired dead time interval inserted between the two channels.

An enable (EN) logic control is integrated inside the ACFJ-332BT to allow hard shut down of the output drivers when it is pulled to a low state. When the enable pin is not connected, the ACFJ-332BT is disabled via an internal 500-kΩ resistor pull down to VSS1.

With the enhanced features offered by the ACFJ-332BT, it is ideal for use in gate driver applications that require flexibility in system integration and control, high common-mode noise immunity, active Miller current clamping, and high input-to-output isolation as well as channel-to-channel isolation.

Package Pinout and Descriptions

Figure 3: ACFJ-332BT Pin Configuration



Pin No.	Pin Name	Description
1	DNC	Do not connect externally. This pin is connect to the IC lead frame.
2	DNC	Do not connect externally. This pin is connect to the IC lead frame.
3	AN1	Input LED1 anode. For testing purpose, do not connect to the external circuit.
4	VDD1	Input positive power supply.
5	VINA	Input control signal for A-channel driver. VINA input is compatible to TTL/CMOS logic levels. This pin has an internal pull-down 500-kΩ resistor. Tie this pin to ground if it is not used.
6	EN	Input enable pin. A logic high input for at least 50 ns enables both A channel and B channel drivers. This pin has an internal pull-down 500-kΩ resistor.
7	VSS1	Input ground.
8	DT	Dead time input control. Connects a resistor (R_{DT}) between the DT pin and the VSS1 pin to adjust dead time according to the equation: t_{DT} in (ns) = (8.9 × R_{DT}) + 18, R_{DT} in kΩ. Add a bypass ceramic capacitor of 0.1 µF to the DT pin for noise filtering. If the DT feature is not in use, it must be tied to VDD1.
9	VINB	Input control signal for B-channel driver. VINB input is compatible to TTL/CMOS logic. This pin has an internal pull-down 500-kΩ resistor. Tie this pin to ground if it is not in use.
10	AN2	Input LED2 anode. For testing purpose, do not connect to the external circuit.
11	DNC	Do not connect externally. This pin is connected to the IC lead frame.
12	DNC	Do not connect externally. This pin is connected to the IC lead frame.
13	MCB	Miller clamp output for the B-channel driver. Connect the MCB pin to the VSSB pin if it is not in use.
14	VSSB	B-channel output ground.
15	VOB	B channel Gate drive output.
16	VDDB	B-channel positive power supply.
21	MCA	Miller clamp output for the A-channel driver. Connect the MCA pin to the VSSA pin if it is not in use.
22	VSSA	A-channel output ground.
23	VOA	A-channel Gate drive output.
24	VDDA	A-channel positive power supply.

Regulatory Information

The ACFJ-332BT is approved by the following organizations:

UL/cUL	UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}
IEC/EN	IEC/EN 60747-5-5 Maximum working insulation voltage, V_{IORM} = 1414 V_{PEAK} Highest allowable overvoltage, V_{IOTM} = 8000 V_{PEAK}

IEC/EN 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Insulation Classification per DIN VDE 0110/1.89, Table 1 For Rated Mains Voltage ≤ 600 V_{RMS} For Rated Mains Voltage ≤ 1000 V_{RMS}		 I – IV I – III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{PEAK}
Input to Output Test Voltage, Method b[a] V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	2652	V_{PEAK}
Input to Output Test Voltage, Method a[a] V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	2262	V_{PEAK}
Highest Allowable Overvoltage[a] (Transient Overvoltage t_{ini} = 60 seconds)	V_{IOTM}	8000	V_{PEAK}
Safety-Limiting Values – maximum values allowed in the event of a failure[b] Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 400 1200	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	> 10^9	Ω

a. Refer to the optocoupler section of the *Isolation and Control Components Designer's Catalog*, under the Product Safety Regulation section IEC/EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

b. Isolation characteristics are guaranteed only within the safety maximum ratings that must be ensured by protective circuits in application. Surface-mount classification is Class A in accordance with CECCOO802.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight-line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	400	Volts	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		II		Material Group (DIN VDE 0110).

Absolute Maximum Ratings

Unless otherwise specified, all voltages at input IC reference to V_{SS1}, all voltages at A-channel output IC reference to V_{SSA}, and all voltages at B-channel output IC reference to V_{SSB}.

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	–55	150s	°C	
Operating Temperature	T_A	–40	125	°C	
IC junction Temperature	T_J	—	150	°C	
Input Supply Voltage	V_{DD1}	–0.3	6	V	
Input Control Signal Voltage	VIN_A, VIN_B	–0.3	6	V	
Input Enable Voltage	V_{EN}	–0.3	6	V	
Dead Time Control Input Voltage	V_{DT}	–0.3	6	V	
Output Supply Voltage	V_{DDA}, V_{DDB}	–0.3	30	V	
Output Driver Voltage	V_{OA}, V_{OB}	–0.3	30	V	
Miller Clamp Voltage	V_{MCA}, V_{MCB}	–0.3	30	V	
Peak Output Current	$\|I_{OA}\|$, $\|I_{OB}\|$	—	4	A	a
Peak Miller Clamp Current	$\|I_{MCA}\|$, $\|I_{MCB}\|$	—	4	A	a
Channel-to-Channel Internal Isolation Voltage	$\|V_{SSA} – V_{SSB}\|$	—	1414	V	
Input IC Power Dissipation	P_{IN}	—	150	mW	b
Output IC Power Dissipation (one channel)	P_{OUTA}, P_{OUTB}	—	400	mW	c
Total Power Dissipation	P_{TOTAL}	—	950	mW	d
ESD Immunity	$\|V_{ESD}\|$	—	4000	V	e
		—	2000	V	f

a. Maximum pulse width = 1 µs, maximum duty = 0.7%. Operation conditions must not exceed the maximum IC junction temperature of $T_{J(max)}$ = 150°C.

b. Input IC power dissipation is derated linearly above 105°C from 150 mW to 100 mW at 125°C for the high effective thermal conductivity board. For the low effective thermal conductivity board, input IC power dissipation is derated linearly above 105°C from 150 mW to 70 mW at 125°C. See Thermal Resistance Model for ACFJ-332BT for details.

c. Each channel output IC power dissipation is limited to 400 mW. Output IC power dissipation is derated linearly above 105°C from 400 mW to 320 mW at 125°C for the high effective thermal conductivity board. For the low effective thermal conductivity board, output IC power dissipation is derated linearly above 105°C from 400 mW to 240 mW at 125°C. The PCB thermal resistance characteristic has to be considered so as not to exceed absolute maximum rating. See Thermal Resistance Model for ACFJ-332BT for details.

d. Total power dissipation is derated linearly above 105°C from 950 mW to 740 mW at 125°C for the high effective thermal conductivity board. For the low effective thermal conductivity board, the total IC power dissipation is derated linearly above 105°C from 950 mW to 550 mW at 125°C. See Thermal Resistance Model for ACFJ-332BT for details.

e. Human Body Model (HBM) per AEC Q100-002. Class: C3A.

f. Charge Device Model (CDM) per AEC Q100-011, all pins. Class: C3.

Recommended Operating Conditions

Unless otherwise specified, all voltages at input IC reference to V_{SS1}, all voltages at A-channel output IC reference to V_{SSA} and all voltages at B-channel output IC reference to V_{SSB}.

Parameter	Symbol	Min.	Max.	Unit	Note
Operating Temperature	T_A	–40	125	°C	
Input Supply Voltage	V_{DD1}	3	5.5	V	
Output Supply Voltage	V_{DDA}, V_{DDB}	10	25	V	
Dead Time Resistor Range	R_{DT}	10	62	kΩ	a
Input IC Supply Decoupling Capacitor	C_{VDD1}	1	—	µF	b
Output IC Supply Decoupling Capacitor	C_{VDDA}, C_{VDDB}	10	—	µF	c
Minimum Input Pulse Width	$t_{ON(VINA)}$, $t_{ON(VINB)}$	50	—	ns	d

a. The dead time (t_{DT}) range is programmable from 110 ns to 572 ns using this formula: t_{DT} in (ns) = (8.9 × R_{DT}) + 18, R_{DT} in kΩ.

b. Connect the input supply decoupling capacitor between V_{DD1} to V_{SS1}.

c. Connect the output supply decoupling capacitor between V_{DDA} to V_{SSA} and V_{DDB} to V_{SSB}.

d. Minimum input pulse width for a guarantee output pulse under no load conditions.

Electrical and Switching Specifications

Unless otherwise specified, all minimum and maximum specifications are at recommended operating conditions; all voltages at input IC reference to V_{SS1}, all voltages at A-channel output IC reference to V_{SSA} and all voltages at B-channel output IC reference to V_{SSB}. All typical values at T_A = 25°C, V_{DD1} – V_{SS1} = 3.3V or 5V, V_{DDA} – V_{SSA} = 15V, V_{DDB} – V_{SSB} = 15V. The DT pin is tied to V_{DD1} (DT disabled), except for the t_{DT} test.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
DC Specifications								
Supply Current								
Input Supply Current (Quiescent)	I_{VDD1}	—	1.5	2.7	mA	VIN_A = 0V, VIN_B = 0V	24	
Input Supply Current at Operation (per channel)	I_{VDD1_SW}	—	6.3	—	mA	f = 200 kHz, Duty cycle = 50%		
Output Supply Current (Quiescent per channel)	I_{VDDA}, I_{VDDB}	—	4	5.9	mA	VIN_A = 0V, VIN_B = 0V	25	
Output Supply Current at Operation (per channel)	I_{VDDA_SW}, I_{VDDB_SW}	—	4.4	—	mA	f = 200 kHz, Duty cycle = 50%, No load		
V_{DD1} UVLO Threshold								
V_{DD1} UVLO Threshold Voltage, Low to High	V_{UV1_TH+}	2.4	2.7	2.95	V			
V_{DD1} UVLO Threshold Voltage, High to Low	$V_{UV1\_TH–}$	2.2	2.5	2.75	V			
V_{DD1} UVLO Hysteresis	V_{UV1_HYS}	—	0.2	—	V			

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
V_{DDA} and V_{DDB} UVLO Threshold (8V UVLO Version)								
V_{DDA} and V_{DDB} UVLO Threshold Voltage, Low to High	V_{UVLOA_TH+}, V_{UVLOB_TH+}	8.1	8.6	9.1	V		16	
V_{DDA} and V_{DDB} UVLO Threshold Voltage, High to Low	$V_{UVLOA\_TH–}$, $V_{UVLOB\_TH–}$	7.1	7.6	8.1	V		16	
V_{DDA} and V_{DDB} UVLO Hysteresis	V_{UVLOA_HYS}, V_{UVLOB_HYS}	—	1.0	—	V		17	
Input Control Threshold (VIN_A, VIN_B, EN)								
Input Control High Threshold Voltage	VIN_{AH}, VIN_{BH}	2	—	—	V		18	
Input Control Low Threshold Voltage	VIN_{AL}, VIN_{BL}	—	—	0.8	V		19	
Enable High Threshold Voltage	V_{ENH}	2	—	—	V		22	
Enable Low Threshold Voltage	V_{ENL}	—	—	0.8	V		23	
Gate Driver Output (V_{OA}, V_{OB})								
Output High Peak Sourcing Current	I_{OAH}, I_{OBH}	—	–4.0	–2.5	A	$V_{DDA} – V_{OA}$ = 15V, $V_{DDB} – V_{OB}$ = 15V		a
Output Low Peak Sinking Current	I_{OAL}, I_{OBL}	2.4	4.0	—	A	$V_{OA} – V_{SSA}$ = 15V, $V_{OB} – V_{SSB}$ = 15V		a
Output High Transistor on Resistance, $R_{DS(ON)}$	R_{OAH}, R_{OBH}	—	15	—	Ω	I_{OA} = –10 mA, I_{OB} = –10 mA		
Output Low Transistor on Resistance, $R_{DS(ON)}$	R_{OAL}, R_{OBL}	—	1.2	—	Ω	I_{OA} = 10 mA, I_{OB} = 10 mA		
High Level Output Voltage	V_{OAH}, V_{OBH}	—	$V_{DDA,B}$ − 0.15	—	V	I_{OA} = –10 mA, I_{OB} = –10 mA		
Low Level Output Voltage	V_{OAL}, V_{OBL}	—	0.01	—	V	I_{OA} = 10 mA, I_{OB} = 10 mA		
Clamp Parameters								
Clamp Threshold Voltage	V_{MCA_TH}, V_{MCB_TH}	1.5	1.8	2.1	V			
Clamp Low Peak Sinking Current	I_{MCAL}, I_{MCBL}	1.0	2.2	—	A	$V_{MCA} = V_{SSA}$ + 3.5V, $V_{MCB} = V_{SSB}$ + 3.5V		

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
AC Specifications								
V_{DD1} – V_{SS1} = 5V						Rg(external) = 4.7Ω, Cload = 2.2 nF, f = 200 kHz, Duty cycle = 50%, $VDD_{A,B}$ = 15V		
Propagation Delay Time from $VIN_{A,B}$ to $V_{OA,B}$, Low to High (per channel)	t_{PLH}	—	35	65	ns			
Propagation Delay Time from $VIN_{A,B}$ to $V_{OA,B}$, High to Low (per channel)	t_{PHL}	—	40	65	ns			
V_{DD1} – V_{SS1} = 3.3V								
Propagation Delay Time from $VIN_{A,B}$ to $V_{OA,B}$, Low to High (per channel)	t_{PLH}	—	40	70	ns			
Propagation Delay Time from $VIN_{A,B}$ to $V_{OA,B}$, High to Low (per channel)	t_{PHL}	—	43	70	ns			
V_{DD1} – V_{SS1} = 3.3V or 5V								
Pulse Width Distortion (t_{PHL} – t_{PLH})	PWD	–22	—	22	ns			b
Dead Time Distortion Caused by Any Two Parts (t_{PLH} – t_{PHL})	DTD	–26	—	26	ns			c
Channel-to-Channel Skew	t_{CSK}	–15	—	15	ns			d
Output 20% to 80% Rise Time (per channel)	t_R	—	10	17	ns			
Output 80% to 20% Fall Time (per channel)	t_F	—	10	18	ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	150	—	—	kV/µs	VIN_A = VIN_B = 5V V_{CM} = 1500V T_A = 25°C, $VDD_{A,B}$ = 15V		e
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	150	—	—	kV/µs	VIN_A = VIN_B = 0V V_{CM} = 1500V, T_A = 25°C $VDD_{A,B}$ = 15V		f
Dead Time Programming (Design Value Set by R_{DT})								
Dead Time	t_{DT}	Overlap Determined by VIN_A and VIN_B				DT Pin Tied to V_{DD1}		
		—	110	—	ns	R_{DT} = 10 kΩ		g
		—	572	—	ns	R_{DT} = 62 kΩ		g

a. Short circuit pulsed current at V_{DD} – V_{SS} = 15V and pulse duration less than 1 µs.

b. Pulse width distortion (PWD) is defined as t_{PHL} – t_{PLH} for any given device.

c. Dead time distortion (DTD) is defined as t_{PLH} – t_{PHL} between any two parts under the same test condition. A negative DTD reduces original system dead time, while a positive DTD increases original system dead time.

d. Channel-to-channel skew (t_{CSK}) is defined as propagation delay difference between two channels under the same test conditions.

e. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in the high state (that is, V_O > 12V).

f. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in a low state (that is, V_O < 1.0V).

g. Dead time is measured at the gate driver outputs, V_{OA} and V_{OB}. The measured dead time value includes the effect of dead time distortion (DTD): t_{DT} in (ns) = (8.9 × R_{DT}) + 18, R_{DT} in kΩ.

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{RMS}	RH < 50%, t = 1 minute T_A = 25°C	a, b, c
Resistance (Input-Output)	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500 Vdc	c
Capacitance (Input-Output)	C_{I-O}	—	0.9	—	pF	f = 1 MHz	

a. In accordance with UL1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second.

b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage, ratings refer to your equipment level safety specification or the IEC/EN 60747-5-5 Insulation Characteristics table.

c. Device is consider as a two-terminal device: pins 1 to 12 shorted together and pins 13 to 24 shorted together.

Parameter Measurements

Figure 4 depicts the test setup to measure the gate driver's propagation delay. These settings correlate to the loading effects found in most automotive applications.

Figure 4: Propagation Delay Measurement Test Setup

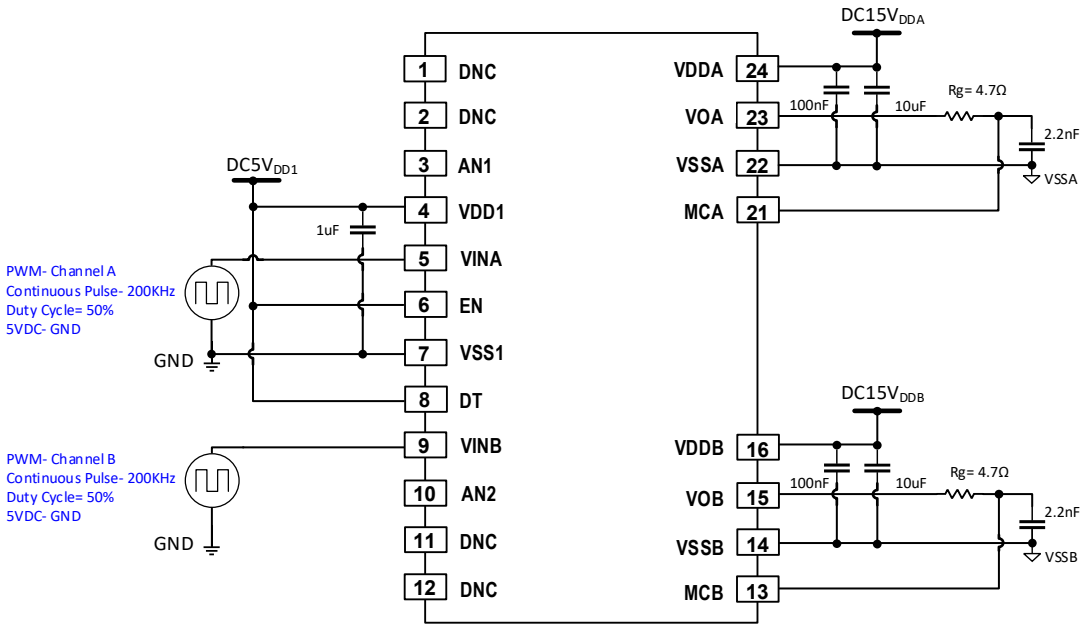


Figure 5 shows the propagation delay measurements and reference waveforms with dead time feature disabled from the test setup shown in Figure 4.

Figure 5: Propagation Delay Waveforms with Dead Time Disabled (DT Is Tied to VDD1)

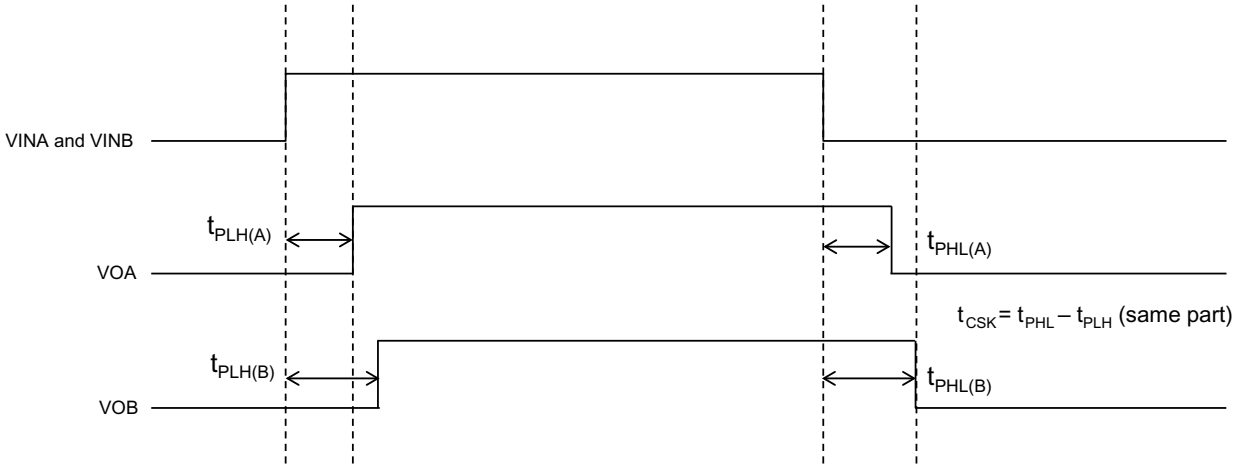


Figure 6 shows the 20% to 80% rise and fall time measurement.

Figure 6: Rise and Fall Time Measurement

The common mode rejection test circuitries are shown in the following figures. Both CMR High (Figure 7) and Low (Figure 8) V_O are probed in the presence of V_{CM} at 1500V.

Figure 7: CMR V_O High Test Circuit

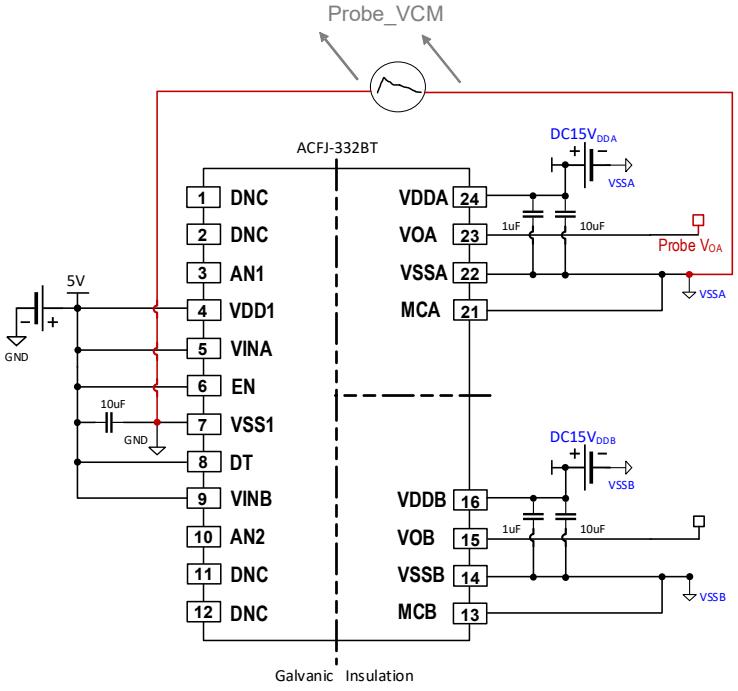
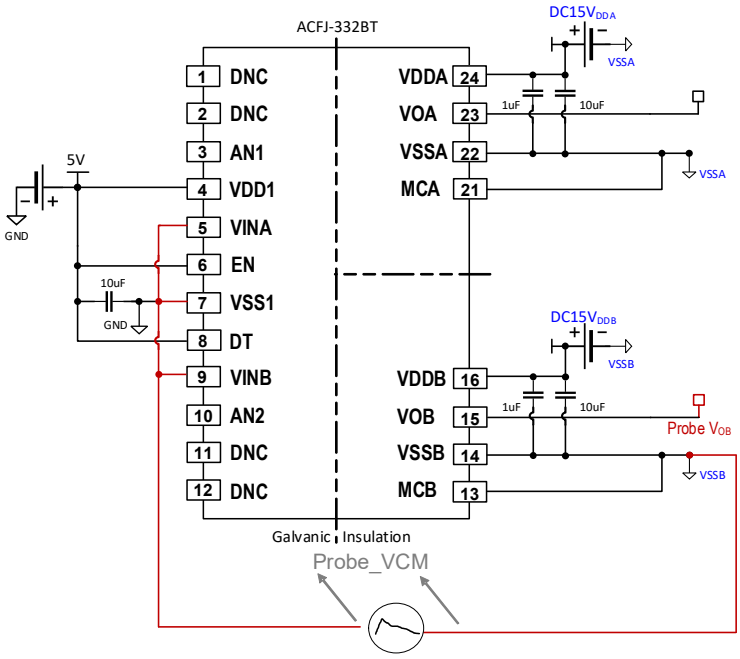


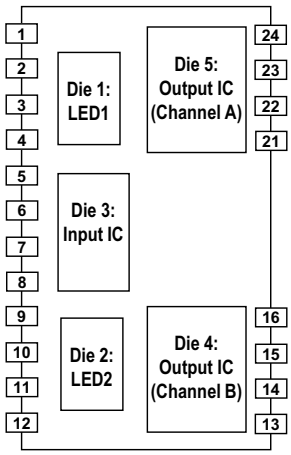
Figure 8: CMR V_O Low Test Circuit



Thermal Resistance Model for ACFJ-332BT

The diagram for measurement is shown in Figure 9. This is a multichip package with five heat sources. The effect of heating of one die due to the adjacent dice are considered by applying the theory of linear superposition. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated and all the dice temperatures are recorded and so on, until the fifth die is heated. With the known ambient temperature, die junction temperature, and power dissipation, the resultant thermal resistance can then be determined. The thermal resistance calculation can be casted into a 5-by-5 matrix form from the five heat sources.

Figure 9: Diagram of ACFJ-332BT for Thermal Resistance Model



$$\begin{vmatrix} R_{11} & R_{12} & R_{13} & R_{14} & R_{15} \\ R_{21} & R_{22} & R_{23} & R_{24} & R_{25} \\ R_{31} & R_{32} & R_{33} & R_{34} & R_{35} \\ R_{41} & R_{42} & R_{43} & R_{44} & R_{45} \\ R_{51} & R_{52} & R_{53} & R_{54} & R_{55} \end{vmatrix} \bullet \begin{vmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \\ P_5 \end{vmatrix} = \begin{vmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \end{vmatrix}$$

Definitions

R11: Thermal Resistance of Die1 due to heating of Die1 (°C/W)
R12: Thermal Resistance of Die1 due to heating of Die2 (°C/W)
R13: Thermal Resistance of Die1 due to heating of Die3 (°C/W)
R14: Thermal Resistance of Die1 due to heating of Die4 (°C/W)
R15: Thermal Resistance of Die1 due to heating of Die5 (°C/W)

R21: Thermal Resistance of Die2 due to heating of Die1 (°C/W)
R22: Thermal Resistance of Die2 due to heating of Die2 (°C/W)
R23: Thermal Resistance of Die2 due to heating of Die3 (°C/W)
R24: Thermal Resistance of Die2 due to heating of Die4 (°C/W)
R25: Thermal Resistance of Die2 due to heating of Die5 (°C/W)

R31: Thermal Resistance of Die3 due to heating of Die1 (°C/W)
R32: Thermal Resistance of Die3 due to heating of Die2 (°C/W)
R33: Thermal Resistance of Die3 due to heating of Die3 (°C/W)
R34: Thermal Resistance of Die3 due to heating of Die4 (°C/W)
R35: Thermal Resistance of Die3 due to heating of Die5 (°C/W)

R41: Thermal Resistance of Die4 due to heating of Die1 (°C/W)
R42: Thermal Resistance of Die4 due to heating of Die2 (°C/W)
R43: Thermal Resistance of Die4 due to heating of Die3 (°C/W)
R44: Thermal Resistance of Die4 due to heating of Die4 (°C/W)
R45: Thermal Resistance of Die4 due to heating of Die5 (°C/W)

R51: Thermal Resistance of Die5 due to heating of Die1 (°C/W)
R52: Thermal Resistance of Die5 due to heating of Die2 (°C/W)
R53: Thermal Resistance of Die5 due to heating of Die3 (°C/W)
R54: Thermal Resistance of Die5 due to heating of Die4 (°C/W)
R55: Thermal Resistance of Die5 due to heating of Die5 (°C/W)

P1: Power dissipation of Die1 (W)
P2: Power dissipation of Die2 (W)
P3: Power dissipation of Die3 (W)
P4: Power dissipation of Die4 (W)
P5: Power dissipation of Die5 (W)

T1: Junction temperature of Die1 due to heat from all dice (°C)
T2: Junction temperature of Die2 due to heat from all dice (°C)
T3: Junction temperature of Die3 due to heat from all dice (°C)
T4: Junction temperature of Die4 due to heat from all dice (°C)
T5: Junction temperature of Die5 due to heat from all dice (°C)
T_A: Ambient temperature (°C)
ΔT1: Temperature difference between Die1 junction and ambient (°C)
ΔT2: Temperature deference between Die2 junction and ambient (°C)
ΔT3: Temperature difference between Die3 junction and ambient (°C)
ΔT4: Temperature deference between Die4 junction and ambient (°C)
ΔT5: Temperature deference between Die5 junction and ambient (°C)

Equation 1:

$$T1 = (R11 \times P1 + R12 \times P2 + R13 \times P3 + R14 \times P4 + R15 \times P5) + T_A$$

Equation 2:

$$T2 = (R21 \times P1 + R22 \times P2 + R23 \times P3 + R24 \times P4 + R25 \times P5) + T_A$$

Equation 3:

$$T3 = (R31 \times P1 + R32 \times P2 + R33 \times P3 + R34 \times P4 + R35 \times P5) + T_A$$

Equation 4:

$$T4 = (R41 \times P1 + R42 \times P2 + R43 \times P3 + R44 \times P4 + R45 \times P5) + T_A$$

Equation 5:

$$T5 = (R51 \times P1 + R52 \times P2 + R53 \times P3 + R54 \times P4 + R55 \times P5) + T_A$$

Measurement Data

Measurement is done on both Low effective thermal conductivity test board (according to JESD51-3) and on High effective thermal conductivity test board (according to JESD51-7).

Table 1: Test Board Thermal Conductivity Measurement Data

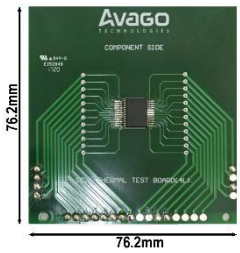
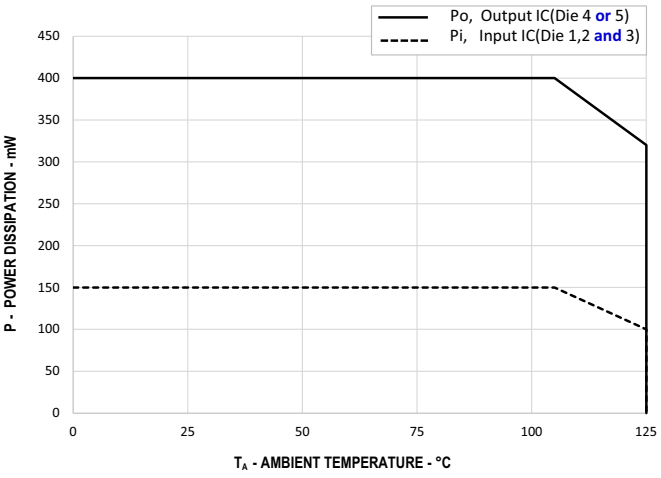
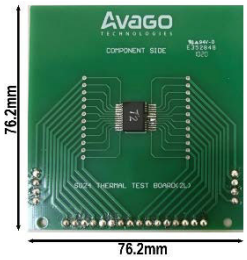
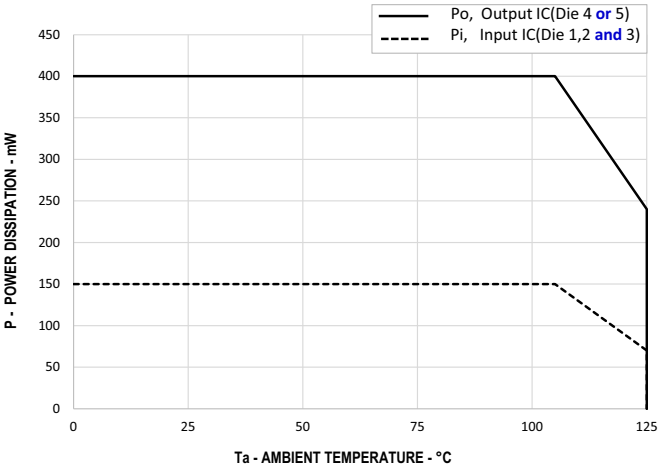
Test Board Type	Test Board Conditions	Thermal Resistance	Power Dissipation Derating Chart
High Effective Thermal Conductivity Board 	Four-layer board that embodies two signal layers, a power plane, and a ground plane. Outer layer copper thickness: 2 oz. Inner layers copper thickness: 1 oz. Board size: 76.2mm × 76.2mm	R11: 191.5˚C/W R12: 39.3˚C/W R13: 38.8˚C/W R14: 16.5˚C/W R15: 22.3˚C/W R21: 40.9˚C/W R22: 202.7˚C/W R23: 48.5˚C/W R24: 23.8˚C/W R25: 18.6˚C/W R31: 38.8˚C/W R32: 48.5˚C/W R33: 46.1˚C/W R34: 16.2˚C/W R35: 17.0˚C/W R41: 20.5˚C/W R42: 29.1˚C/W R43: 18.8˚C/W R44: 57.1˚C/W R45: 14.3˚C/W R51: 28.8˚C/W R52: 21.8˚C/W R53: 19.9˚C/W R54: 14.3˚C/W R55: 56.4˚C/W	**Figure 10: Power Derating Chart Based on High Effective Thermal Conductivity**  **NOTE:** ■ Output IC power dissipation is derated linearly 4 mW/°C above 105°C from 400 mW to 320 mW at 125°C. ■ Input ICs power dissipation is derated linearly 2.5 mW/°C above 105°C from 150 mW to 100 mW at 125°C.

Table 1: Test Board Thermal Conductivity Measurement Data (Continued)

Test Board Type	Test Board Conditions	Thermal Resistance	Power Dissipation Derating Chart
Low Effective Thermal Conductivity Board 	Single-layer board for signal. Outer layer copper thickness: 2 oz. Board size: 76.2mm × 76.2mm	R11: 224.9°C/W R12: 73.24°C/W R13: 64.15°C/W R14: 37.9°C/W R15: 47.49°C/W R21: 82.28°C/W R22: 239.8°C/W R23: 64.38°C/W R24: 47.15°C/W R25: 40.8°C/W R31: 64.15°C/W R32: 64.38°C/W R33: 70.91°C/W R34: 36.56°C/W R35: 38.56°C/W R41: 50.49°C/W R42: 60.8°C/W R43: 39.19°C/W R44: 91.58°C/W R45: 34.8°C/W R51: 62.22°C/W R52: 48.62°C/W R53: 48.38°C/W R54: 33.75°C/W R55: 86.64°C/W	**Figure 11: Power Derating Chart Based on Low Effective Thermal Conductivity**  **NOTE:** ■ Output IC power dissipation is derated linearly 8 mW/°C above 105°C from 400 mW to 240 mW at 125°C. ■ Input ICs' power dissipation is derated linearly 4 mW/°C above 105°C from 150 mW to 70 mW at 125°C.

Notes on Thermal Calculation

The application and environmental design for the ACFJ-332BT must ensure that the junction temperature of the internal ICs and LEDs within the gate driver's optocoupler do not exceed 150°C. The following examples are based on a typical circuit shown in Figure 33 for the estimation of maximum power dissipation and the corresponding effect on junction temperatures. This thermal calculation can be used as a reference for thermal comparison only between the actual application board layout and the PCB board according to JESD51-7. The actual power dissipation achievable will depend on the application environment (PCB layout, airflow, part placement, and so on). The following examples can be used as a reference for thermal performance comparison under the specified PCB layout as shown in Table 1.

Calculation of Input LED Power Dissipation, P1 and P2

Input LED Power Dissipation (P1) = $^{1}I_{F(LED,\ Recommended\ Max.)} \times {}^{1}V_{F(LED,\ 125°C)} \times$ Duty Cycle

Example:

P1 = 10 mA × 1.85V × 50% duty cycle = 9 mW
P2 = P_1 = 9 mW

Calculation of Input IC Power Dissipation, P3

Example:

Input IC Power Dissipation, P3 = $I_{VDD1(Max.)} \times V_{DD1\ (Recommended\ Max.)}$
= 2.7 mA × 5.5V
= 15 mW

1. By design.

Calculation of Output IC Power Dissipation, P4 or P5

Example:

Output IC Power Dissipation:

$P_{4,5} = P_{O\ (Static)} + P_{HS} + P_{LS} + P_{MC}$

- $Q_{G|21V}$: MOSFET gate charge at 21V supply voltage (0.15 µC)
- $Q_{G|2.5V}$: MOSFET gate charge at 2.5V supply voltage (0.04 µC)
- f_{PWM}: Input LED switching frequency (150 kHz)
- R_G: External gate charging resistance (6Ω)
- $R_{DS,OL(MAX)}$: By design, maximum low side output impedance (2Ω)
- $R_{DS,OH(MAX)}$: By design, maximum high side output impedance (2Ω)
- $V_{THCLAMP(MAX)}$: Maximum Clamp Threshold Voltage (2.1V)
- $R_{DS\_MC(MAX)}$: By design, maximum internal clamp resistance (2Ω)
- R_{MC}: External clamp resistance (1Ω)

$P_{O\ (Static)}$: Static power dissipated by the output IC
$= I_{VDD} \times V_{DD}$
$= 5.9\ mA_{(Data\ Sheet\ Max.)} \times 21V)$
$= 124$ mW

P_{HS}: High Side PMOS Switching Power Dissipation at V_O pin
$= (V_{DD} \times Q_{G|21V} \times f_{PWM}) \times R_{DS,OH(MAX)} / (R_{DS,OH(MAX)} + R_G) / 2$
$= (21V \times 0.15\ µC \times 150\ kHz) \times 2/(2 + 6) / 2$
$= 59$ mW

P_{LS}: Low Side Switching Power Dissipation at V_O pin
$= (V_{DD} \times Q_{G|21V} \times f_{PWM}) \times R_{DS,OL(MAX)} / (R_{DS,OL(MAX)} + R_G) / 2$
$= (21V \times 0.15\ µC \times 150\ kHz) \times 2/(2 + 6) / 2$
$= 59$ mW

P_{MC}: Miller Clamp NMOS Switching Power Dissipation
$= (V_{THCLAMP(MAX)} \times Q_{G|2.5V} \times f_{PWM}) \times R_{DS\_MC(MAX)} / (R_{DS\_MC(MAX)} + R_{MC}) / 2$
$= (2.1V \times 0.04\ µC \times 150\ kHz) \times 2/(2 + 1) / 2$
$= 4.2$ mW

$P_{4,5}$: Output IC Power Dissipation
$= P_{O\ (Static)} + P_{HS} + P_{LS} + P_{MC}$
$= 124\ mW + 59\ mW + 59\ mW + 4.2\ mW$
$= 246$ mW

Junction Temperature Calculation for High Thermal Conductivity Board, T_A = 125°C

Example:

- Input LED1 Junction Temperature, **T1**
  $= (R11 \times P1 + R12 \times P2 + R13 \times P3 + R14 \times P4 + R15 \times P5) + 125°C$
  $= (191.5°C/W \times 9\ mW) + (39.3°C/W \times 9\ mW) + (38.8°C/W \times 15\ mW) + (16.5°C/W \times 246\ mW) + (22.3°C/W \times 246\ mW) + 125°C$
  $= 137°C < T_J$ (absolute max.) of 150°C
- Input LED2 Junction Temperature, **T2**
  $= (R21 \times P1 + R22 \times P2 + R23 \times P3 + R24 \times P4 + R25 \times P5) + 125°C$
  $= (40.9°C/W \times 9\ mW) + (202.7°C/W \times 9\ mW) + (48.5°C/W \times 15\ mW) + (23.8°C/W \times 246\ mW) + (18.6°C/W \times 246\ mW) + 125°C$
  $= 138°C < T_J$ (absolute max.) of 150°C
- Input IC Junction Temperature, **T3**
  $= (R21 \times P1 + R22 \times P2 + R23 \times P3 + R24 \times P4 + R25 \times P5) + 125°C$
  $= (38.8°C/W \times 9\ mW) + (48.5°C/W \times 9\ mW) + (46.1°C/W \times 15\ mW) + (16.2°C/W \times 246\ mW) + (17°C/W \times 246\ mW) + 125°C$
  $= 135°C < T_J$ (absolute max.) of 150°C
- Output IC Junction Temperature, **T4**
  $= (R41 \times P1 + R42 \times P2 + R43 \times P3 + R44 \times P4 + R45 \times P5) + 125°C$
  $= (20.5°C/W \times 9\ mW) + (29.1°C/W \times 9\ mW) + (18.8°C/W \times 15\ mW) + (57.1°C/W \times 246\ mW) + (14.3°C/W \times 246\ mW) + 125°C$
  $= 143°C < T_J$ (absolute max.) of 150°C
- Output IC Junction Temperature, **T5**
  $= (R41 \times P1 + R42 \times P2 + R43 \times P3 + R44 \times P4 + R45 \times P5) + 125°C$
  $= (28.8°C/W \times 9\ mW) + (21.8°C/W \times 9\ mW) + (19.9°C/W \times 15\ mW) + (14.3°C/W \times 246\ mW) + (56.4°C/W \times 246\ mW) + 125°C$
  $= 143°C < T_J$ (absolute max.) of 150°C

NOTE: Junction temperature of **T1**, **T2**, **T3**, **T4**, and **T5** must not exceed 150°C at any given ambient temperature T_A.

Typical Performance Plots

T_A = 25°C, $VDD_{A,B}$ – $VSS_{A,B}$ = 15V. With capacitance load of 2.2 nF, unless otherwise noted.

Figure 12: t_{PLH} vs Temperature

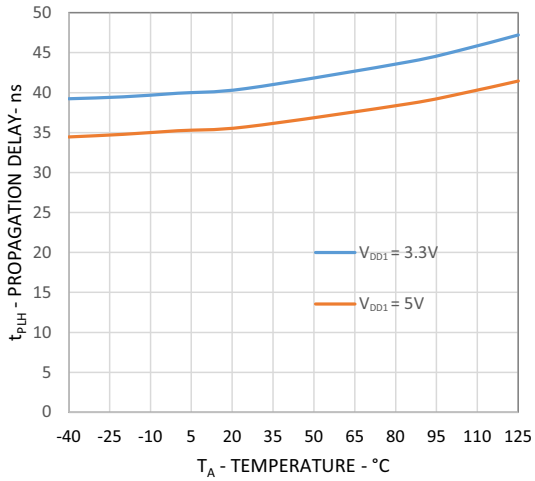


Figure 13: t_{PHL} vs Temperature

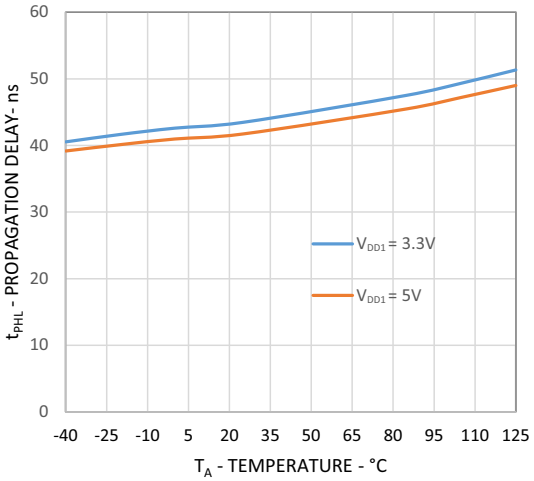


Figure 14: Pulse Width Distortion vs Temperature

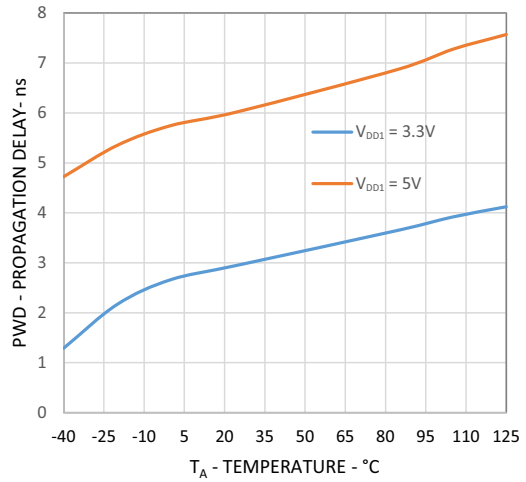


Figure 15: Channel-to-Channel Skew vs Temperature

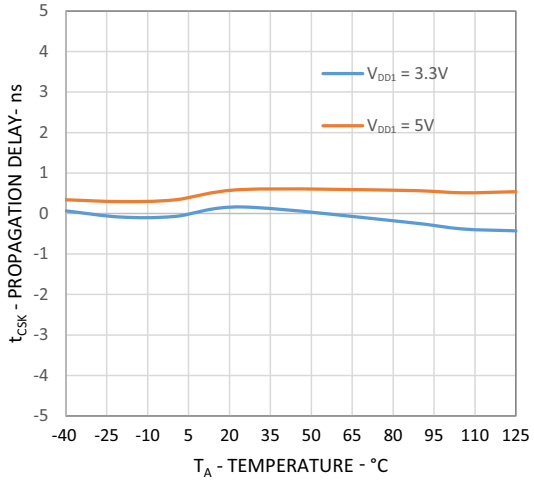


Figure 16: $UVLO_{A,B}$ Threshold vs Temperature

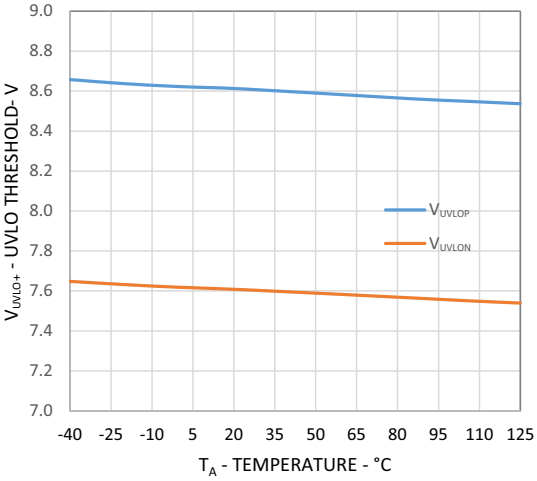


Figure 17: $UVLO_{A,B}$ Hysteresis vs Temperature

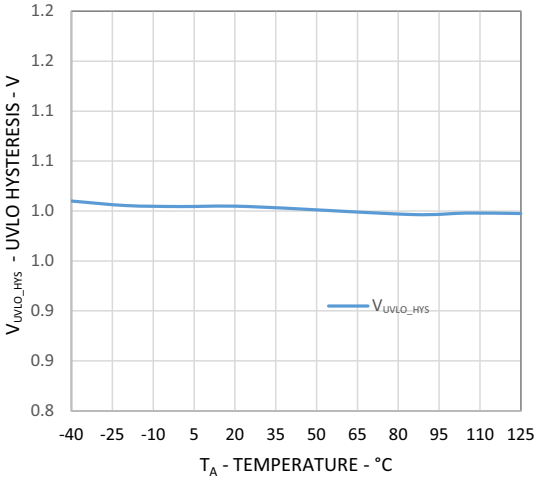


Figure 18: VIN High Threshold vs Temperature

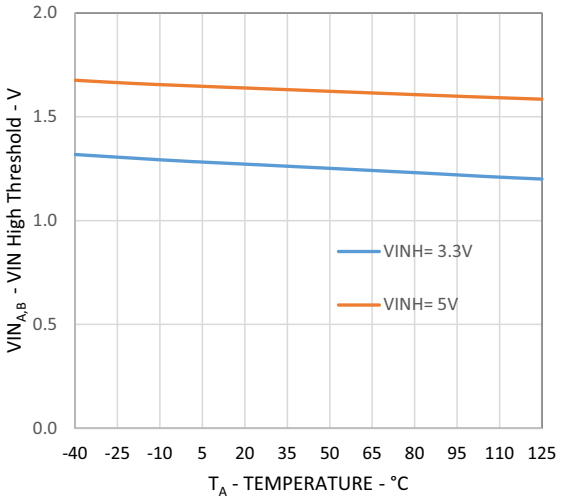


Figure 19: VIN Low Threshold vs Temperature

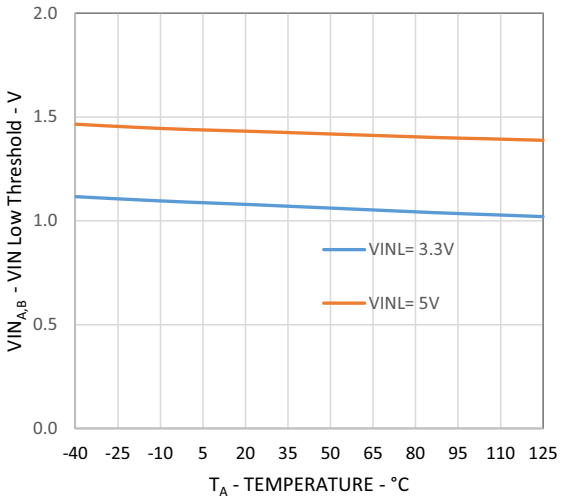


Figure 20: VIN Hysteresis vs Temperature

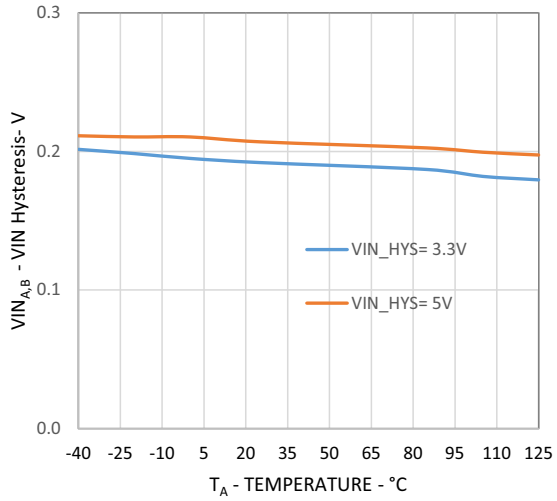


Figure 21: Enable Low Threshold vs Temperature

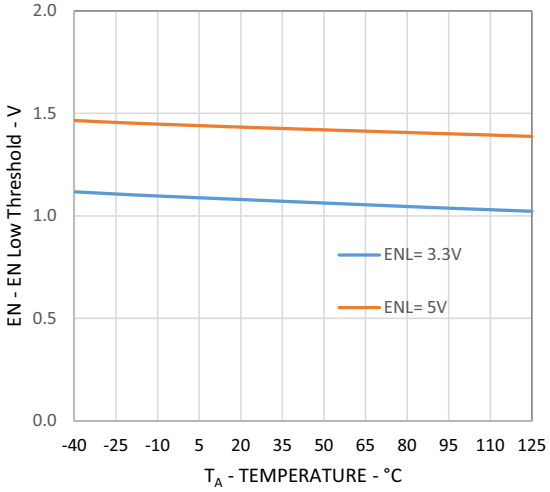


Figure 22: Enable High Threshold vs Temperature

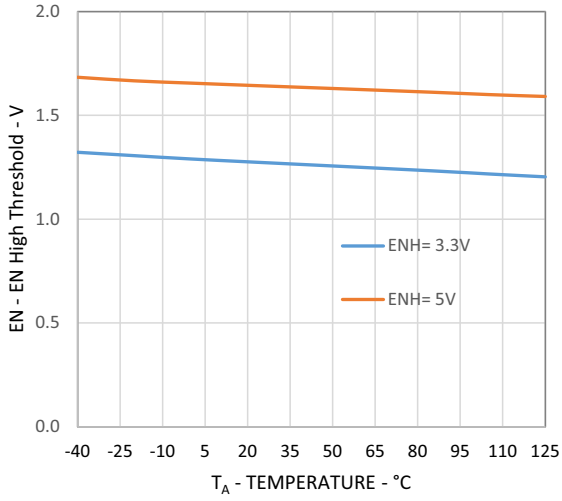


Figure 23: Enable Hysteresis vs Temperature

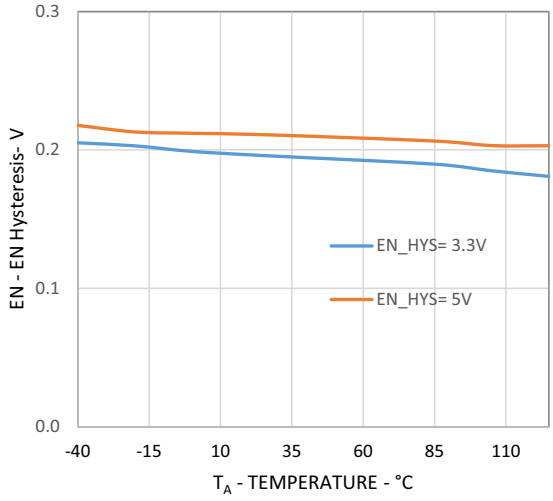


Figure 24: I_{VDD1} Quiescent Current vs Temperature

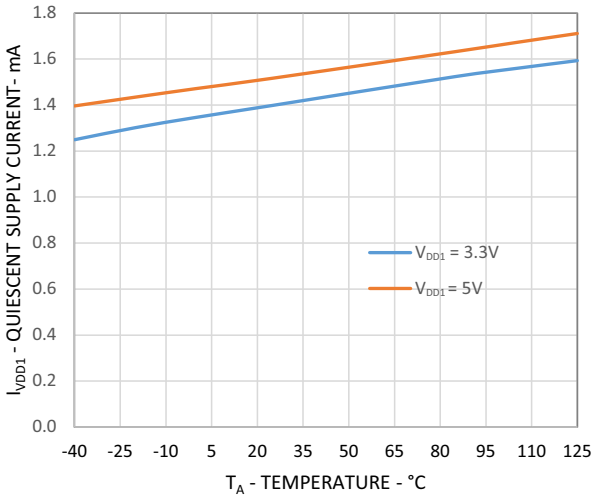


Figure 25: $I_{VDDA,B}$ Quiescent Current vs Temperature

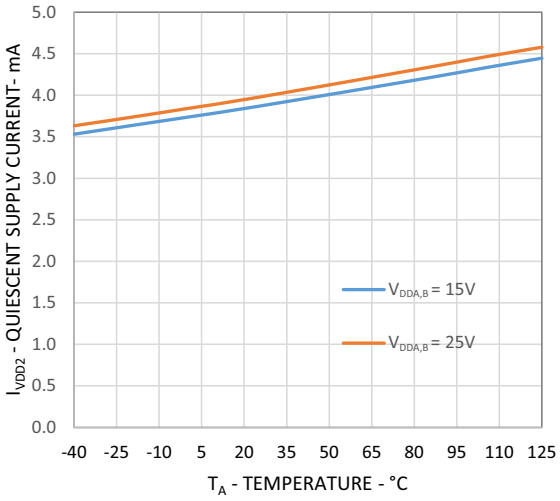


Figure 26: I_{VDD1} vs VIN_A & VIN_B Input Switching Frequency

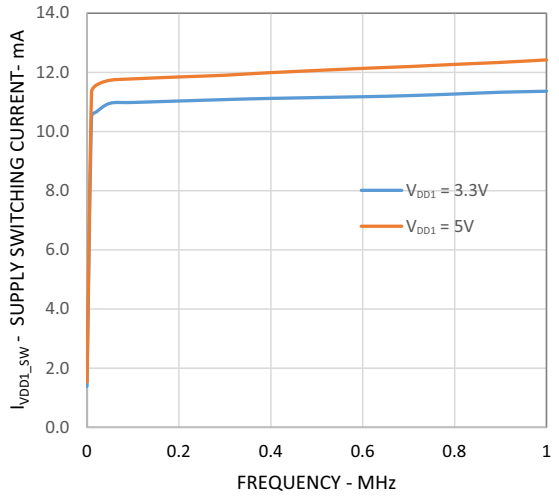


Figure 27: $I_{VDDA,B}$ vs VIN_A & VIN_B Input Switching Frequency

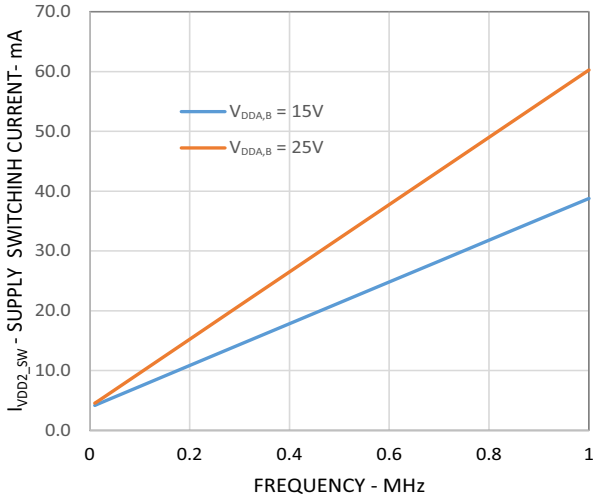


Figure 28: I_{OL} vs V_O

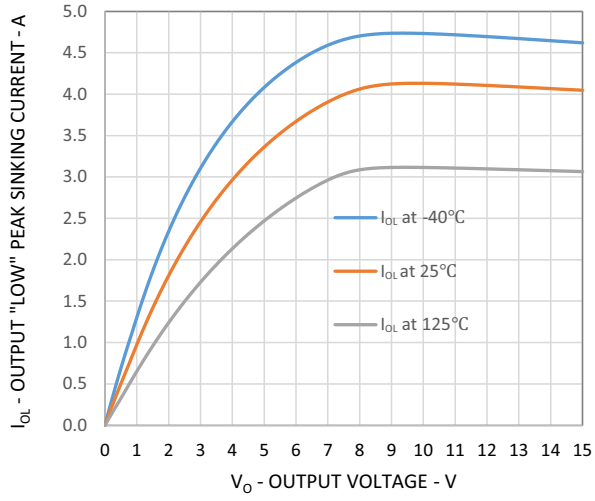


Figure 29: I_{OH} vs (V_{DD} – V_O)

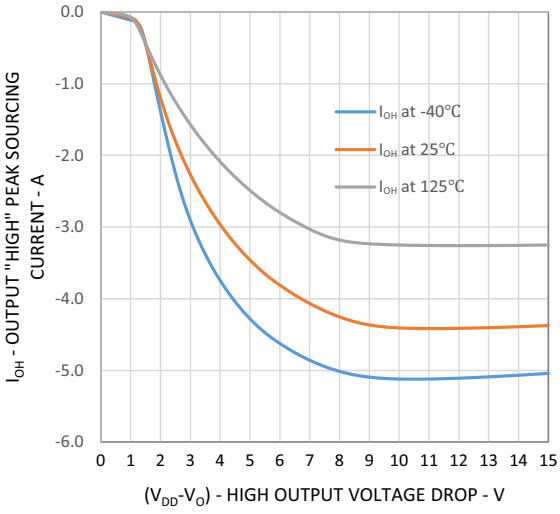


Figure 30: Channel A Dead Time vs. Temperature

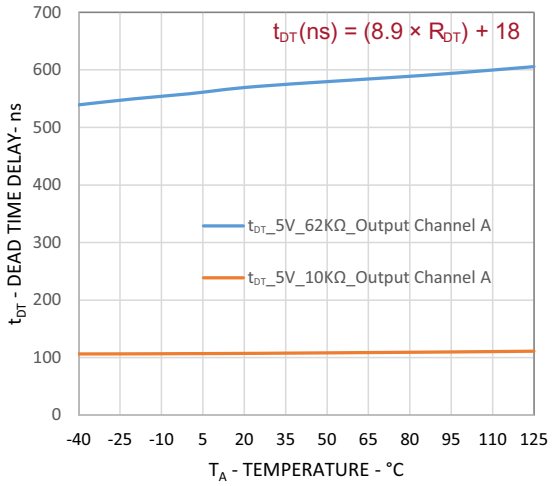
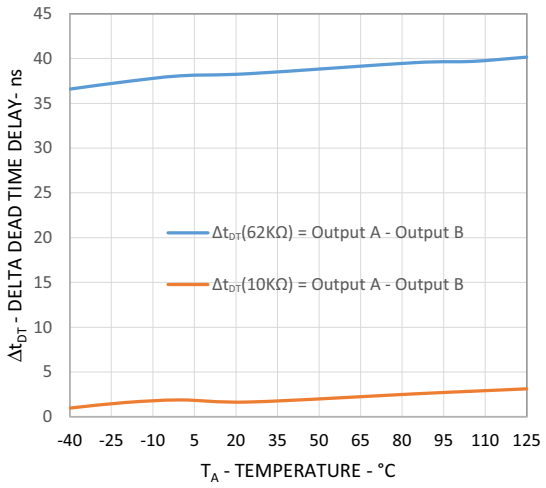
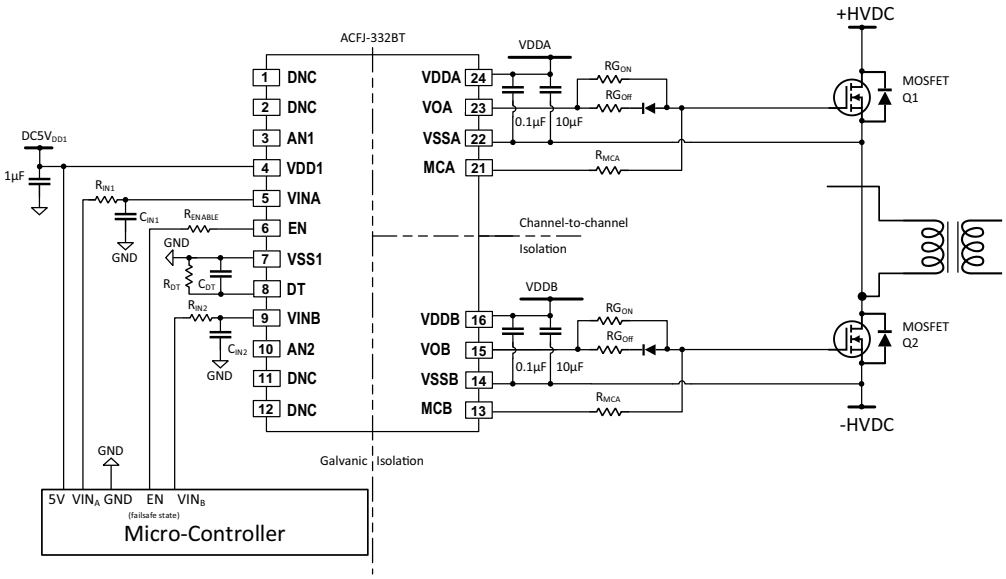


Figure 31: Dead Time Matching vs. Temperature



Typical Application Circuit

Figure 32: ACFJ-332BT Typical Application Circuit



NOTE: Component value is subject to change based on applications conditions.

VDD1, VDDA, and VDDB Supply Pins

A low ESR 1-µF ceramic capacitor with minimum voltage ratings of 6.5V is recommend for VDD1 to VSS1 decoupling capacitors.

For VDDA to VSSA and VDDB to VSSB, a pair of ceramic decoupling capacitors with low ESR of 100 nF and 10 µF are connected in parallel. During the dynamic load switching transition, a large transient charge from ACFJ-332BT is drawn from the decoupling capacitors to drive the output capacitive load. Depending on the load gate charge and ripple voltage tolerance during load switching, the minimum capacitance values can be adjusted accordingly.

EN Input Pin

Direct connection to TTL/CMOS compatible logic level devices or connect with a current-limiting resistor.

DT Pin

A pair of fixed resistor (R_{DT}) and a bypass ceramic capacitor (C_{DT}) of 0.1 µF are recommended to connect close to the DT and VSS1 pin.

The C_{DT} is for noise filtering, while the R_{DT} will insert dead time into the dual output channels, according to the following equation: t_{DT} in (ns) = (8.9 × R_{DT}) + 18, R_{DT} in kΩ.

Connect the DT pin to VDD1 if dead time is not in use.

VINA and VINB Input Pins

Direct connection to TTL/CMOS compatible logic level devices to a pair of PWM input. A first-order RC filter between PWM input and VIN, with $R_{INA,B}$ in the range of 0Ω to 100Ω, and C_{INA} and C_{INB} in the range of 33 pF to 100 pF is recommended for noise filtering.

VOA, VOB, MCA, and MCB Output Pins

External gate resistors are connected to the $VO_{A,B}$ pins to limit the peak gate current, skew the IGBT/MOSFET rise/fall times, and dissipate the gate driver's output power. The designer should size the external gate resistor so that the output peak current does not exceed the absolute maximum ratings.

Example:

Given VDDA – VSSA = 12V:

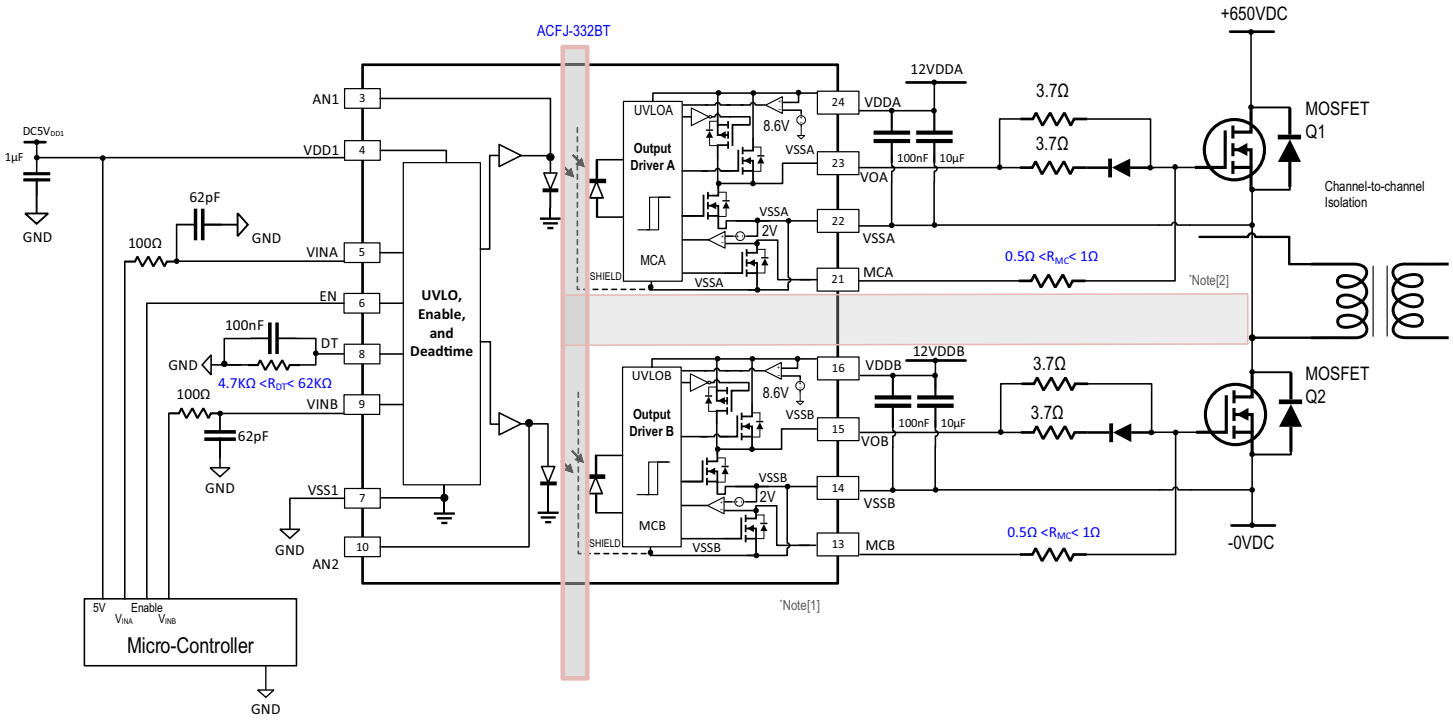
- Assume sourcing –2.5A out from ACFJ-332BT.
- Assume sinking 4A into ACFJ-332BT.

R_{OAH} = 1.2Ω(R_{NMOS})|| 15Ω, R_{OAL}= 1.2Ω, wherein R_{NMOS} is equal to R_{OAL}

- Minimum external gate turn-on resistor = (VDDA – VSSA)/$I_{OAH(PEAK)}$ – R_{OAH} = (12V/2.5A) – 1.1Ω = 3.7Ω
- Minimum external gate turn-off resistor = (VDDA – VSSA)/$I_{OAL(PEAK)}$ – R_{OAL} = (12V/4A) – 1.2Ω = 1.8Ω
- This example excludes the IGBT/MOSFET internal gate resistance.
- Similar calculation applies to channel B.

For MCA and MCB pins, use an external resistor value in the range of 0.5Ω to less than 1Ω.

Figure 33: Example ACFJ-332BT Gate Driver Circuit with Silicon MOSFET Application Circuit Diagram



NOTE:

1. 8.3-mm creepage and 400V CTI SO-24 can address basic insulation of 650 V_{RMS} with pollution degree 2.
2. 3.5-mm separation between two live parts of the SO-24 can address functional isolation up to 650 V_{RMS} with pollution degree 2.

Description of Operations and Functions

Input Control and Output Truth Table

Table 2 depicts all the possible input state transitions and the resultant outputs.

NOTE: 'x' – do not care state; 'H' – High; 'L' – Low; 'A' – Active[1]; and 'I' – Inactive[2].

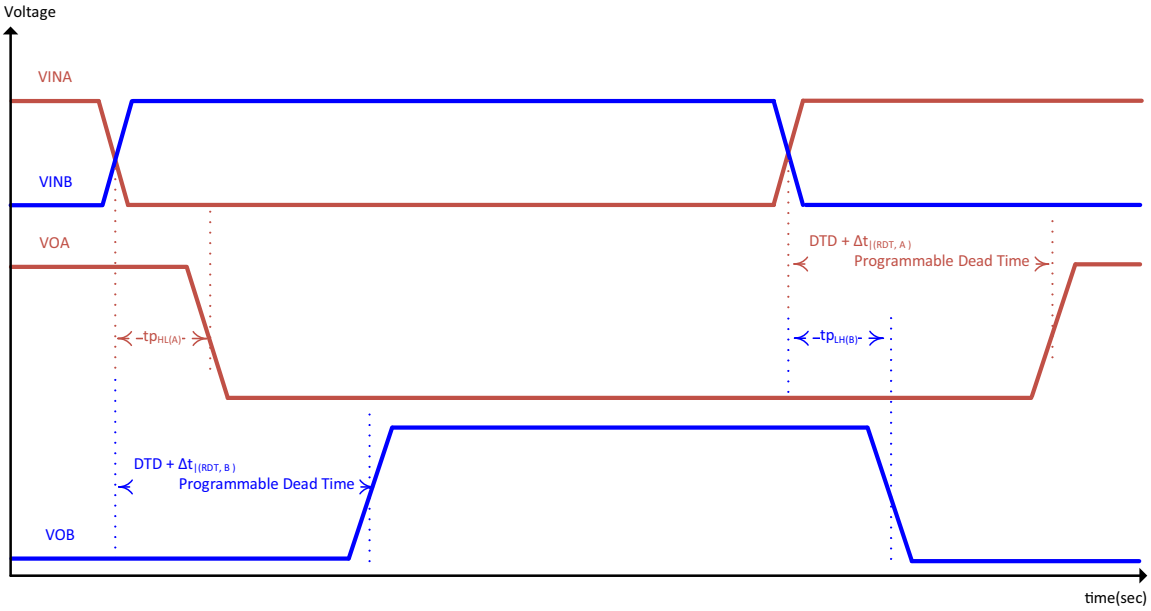
1. The Dead Time insertion function is enabled, and the DT pin is connected to an external R_{DT} referenced to VSS1. The DT pin *cannot* be connected to VSS1 directly.
2. The Dead Time is inactive by the connected DT pin to a high state (tied to VDD1). When DT is inactive, overlap of both output drivers' logic is allowed.

Table 2: Input and Output Control Truth Table

Input							Gate Input		Notes
VDD1	EN	DT	VINA	VINB	VDDA	VDDB	VOA	VOB	
> 2.5V	H	A	L	L	> V_{UVLOA_TH+}	> V_{UVLOB_TH+}	L	L	Output transition – High to Low occurs after internal dead time expires.
> 2.5V	H	A	L	H	> V_{UVLOA_TH+}	> V_{UVLOB_TH+}	L	H	Output transition – Low to High occurs after internal dead time expires.
> 2.5V	H	A	H	L	> V_{UVLOA_TH+}	> V_{UVLOB_TH+}	H	L	Output transition – Low to High occurs after internal dead time expires.
> 2.5V	H	A	H	H	> V_{UVLOA_TH+}	> V_{UVLOB_TH+}	L	L	Invalid state. Both outputs are pulled to low state.
> 2.5V	H	I	L	L	> V_{UVLOA_TH+}	> V_{UVLOB_TH+}	L	L	DT is disabled. Immediate Output transition.
> 2.5V	H	I	L	H	> V_{UVLOA_TH+}	> V_{UVLOB_TH+}	L	H	
> 2.5V	H	I	H	L	> V_{UVLOA_TH+}	> V_{UVLOB_TH+}	H	L	
> 2.5V	H	I	H	H	> V_{UVLOA_TH+}	> V_{UVLOB_TH+}	H	H	
> 2.5V	L	x	x	x	> V_{UVLOA_TH+}	> V_{UVLOB_TH+}	L	L	Driver is disabled. Both outputs are pulled to low state.
< 2.5V	x	x	x	x	> V_{UVLOA_TH+}	> V_{UVLOB_TH+}	L	L	VDD1 under-voltage lockout.
x	x	x	x	x	< V_{UVLOA_TH+}	< V_{UVLOB_TH+}	L	L	VDDA and VDDB under-voltage lockout during *power-up.*
x	x	x	x	x	< V_{UVLOA_TH-}	< V_{UVLOB_TH-}	L	L	VDDA and VDDB under-voltage lockout during *power-down*.

Programmable Dead Time

Figure 34: Timing Diagram with Programmable Dead Time



Programmable dead time is set according to the equation t_{DT} in (ns) = (8.9 × R_{DT}) + 18, R_{DT} in kΩ. The measured dead time at both the gate driver outputs V_{OA} and V_{OB} are the total of the programmable dead time plus the dead time distortion (DTD).

Dead time distortion (DTD) is defined as ($t_{PLH} - t_{PHL}$) between any two parts under the same test condition. A negative DTD value will decrease the programmable dead time set by R_{DT}; a positive DTD value will add to the programmable dead time set by R_{DT}.

Timing Response Enable and $VIN_{A,B}$

Figure 35: Enable Response Time

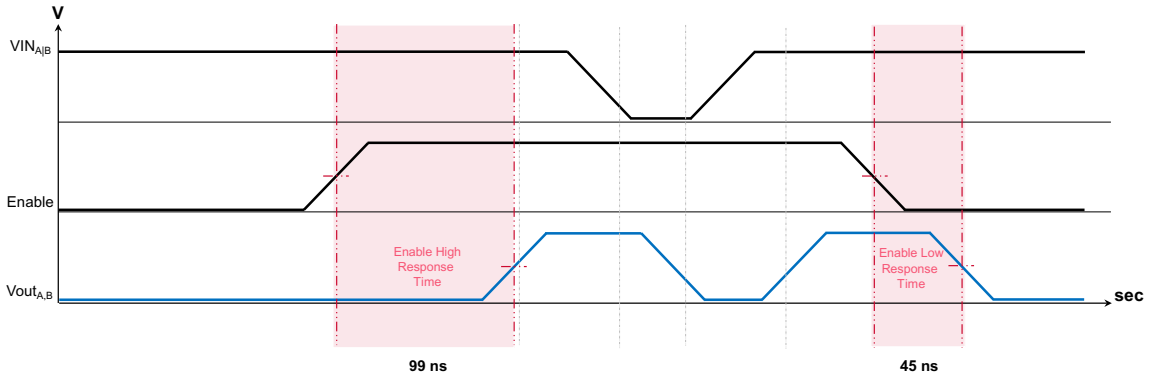


Figure 35 shows the response time that the enable function has on the dual-channel outputs. The enable function adds on a 50-ns delay on the rising edge of the output, but not on the falling edge.

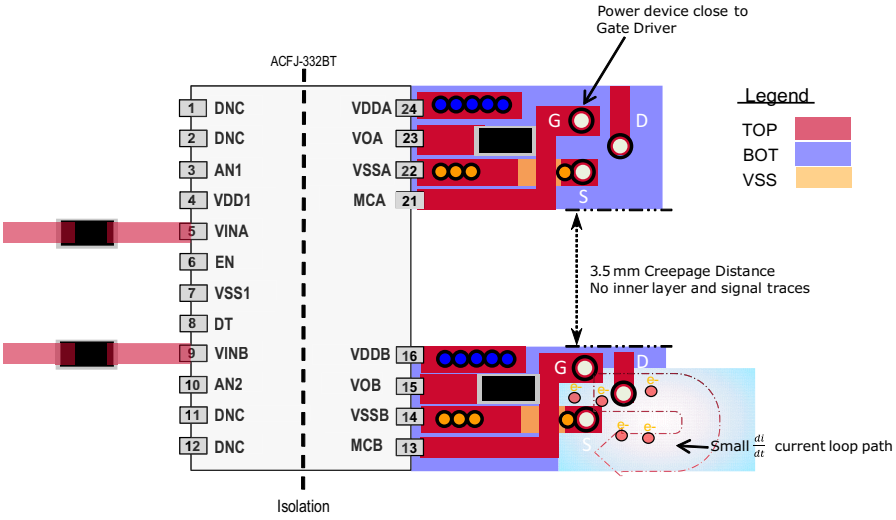
The measured propagation delay on the rising edge output is the total of enable 50-ns delay plus the gate driver's propagation delay.

Layout Guidelines

The gate driver's output sinks about 4A(typical), which the return current path of minimum inductance must be implemented during printed circuit board layout design to alleviate the effect of ground bounce.

Adequate spacing must be maintained between the high voltage isolated circuitry and any input reference circuitry. The minimum spacing between two adjacent high-side isolated channels (that is, top and bottom channels) must be taken into consideration as well. Insufficient spacing will reduce the effective isolation and might increase parasitic coupling that will degrade part performance. Figure 36 shows the recommended PCB layout guidelines.

Figure 36: PCB Layout Guidelines



The placement and routing of supply bypass capacitors require special attention. During switching transients, the majority of gate charge is supplied by bypass capacitors. Maintaining short bypass capacitor trace lengths will ensure low supply ripple and clean switching waveforms. It is recommended to connect the bypass capacitors to the power plane and ground plane with multiple via holes. The planes can provide better heat dissipation and, at the same time, serve as a natural decoupling capacitor to the IC. Figure 37 shows the bypass capacitors placement and PCB planes stack-up.

Figure 37: PCB Planes Stack-Up and Bypass Capacitors Placement