Reference Manual

ACFJ-332B

Transphorm GaN TP65H035G4QS Half-Bridge Evaluation Board

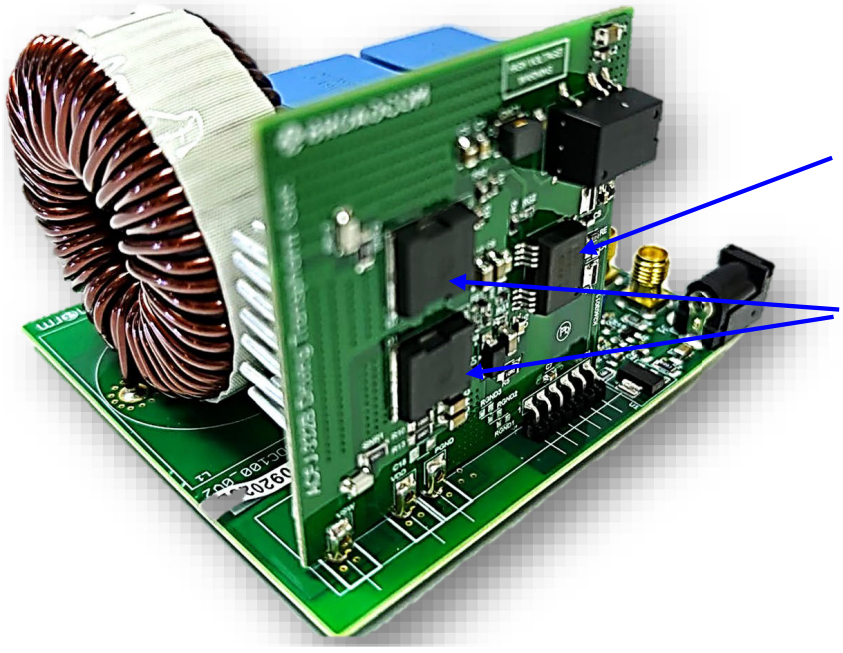
GaN Power Semiconductor

The gallium nitride (GaN) power semiconductor is rapidly emerging into the commercial market, delivering huge benefits over conventional silicon-based power semiconductors. GaN can improve overall system efficiency with lower on-resistance, and the higher switching capability can reduce the overall system size and cost. The technical benefits, coupled with lower costs, have increased the fast adoption of GaN power semiconductors in applications such as industrial power supplies and renewable energy inverters.

Broadcom gate drive optocouplers have been used extensively in driving silicon-based semiconductors, such as IGBT. This document describes how the gate drive optocoupler, ACFJ-332B, can also be used to drive GaN FET.

The half-bridge evaluation board features the ACFJ-332B, 4A dual-channel gate drive optocoupler, and Transphorm's GaN FET TP65H035G4QS. The half-bridge evaluation board enables the basic study of the switching characteristics and efficiency, after plugging on to the main board. The high-voltage input and output operate at up to 400 V_{DC}, with the current limit of the inductor at 40A, depending upon cooling, ambient temperature, and switching frequency.

Figure 1: ACFJ-332B Driving Transphorm GaN TP65H035G4QS Half-Bridge Evaluation Board



Design Features

The ACFJ-332B Transphorm GaN TP65H035G4QS half-bridge evaluation board features one ACFJ-332B gate drive optocoupler and two TP65H035G4QS GaN FETs.

Broadcom ACFJ-332B Gate Drive Optocoupler

- Dual channel in an SO-24 package
- 4A peak (absolute maximum), rail-to-rail output
- Single output for source and sink
- 65-ns maximum propagation delay (at 5V isolated low-side supply)
- 150-kV/µs minimum common mode rejection (CMR) at V_{CM} = 1500V
- 8.6V UVLO with hysteresis
- Wide operating V_{DD} range: 10V to 25V
- Wide industrial temperature range: –40°C to 125°C
- CTI > 400V
- 3.5-mm creepage between two output drivers
- Minimum Miller clamp current of 1A in each channel
- Programmable dead time
- Safety approvals:
  - UL recognized 5000 V_{RMS} for 1 minute
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 1414 V_{PEAK}

Transphorm GaN FET TP65H035G4QS

- Simplified driver design because standard-level MOSFET gate drivers can be used:
  - 0V to 12V drive voltage
  - Gate threshold voltage, $V_{GSth,}$ of 4V
- High gate threshold voltage of 4V for gate bounce immunity
- Low body diode V_f for reduced losses and simplified dead-time adjustments
- Transient overvoltage capability for increased robustness
- TOLL package technology:
  - Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
  - Increased efficiency in both hard- and soft-switched circuits
  - Easy to drive with commonly used gate drivers
  - GSD pin layout improves high-speed design
  - Pin-to-pin drop-in with e-mode GaN

Board Description

Functional Block Diagram

The evaluation board has a half-bridge topology as shown in Figure 2. A pair of high voltage ports, J2/J3 and J5/J7, serve as either high-voltage input or output, depending on whether a buck or boost configuration is used. In either case, one GaN FET acts as the active power switch, while the other carries the freewheeling current. The latter device may be enhanced as a synchronous rectifier as well. With GaN FETs, the reverse recovery charge is low, and there is no need for additional freewheeling diodes.

The high-side and low-side PWM signals are connected to connector P1, which is used to directly drive the LEDs of the ACFJ-332B.

An inductor is provided as a starting point for investigation. This is a 330-µH toroid intended to demonstrate a reasonable compromise between size and efficiency with the current limited at 40A and at a switching frequency of 100 kHz.

Figure 2: Half-Bridge Evaluation Board Functional Block Diagram

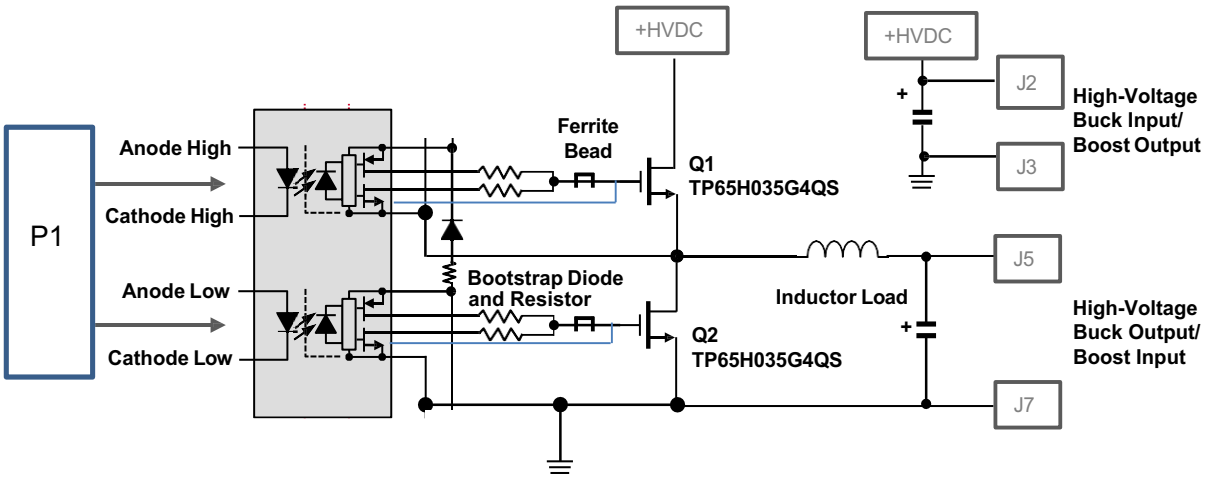
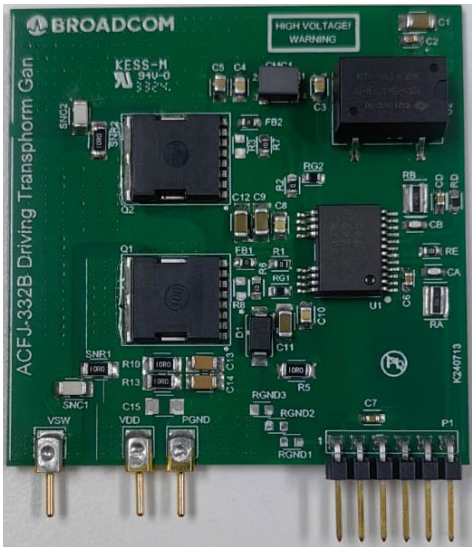


Figure 3: PCB Assembly Layout of the Actual Daughterboard



Pin Assignment

Table 1 shows the pin assignments for the low-voltage side P1 connector. See Figure 4 for more details.

Table 1: Pin Assignments for the Low-Voltage Side P1 Connector (User Interface Connector)

Label	Designation	Function	Direction
1	AGND	This is the analog supply Gnd for +5V.	Input
2	+12V	No connection, not needed.	N/A
3	+5V	5V power supply. To be supplied externally. This is needed to power up the low-voltage side operations of the ACFJ-332B. Other operations needed for the 5V supply are for the programmable dead time.	Input
4	EN	Enable pin; a positive +5V will enable the ACFJ-332B.	Input
5	GaN2_Gate	Connected to the VINB pin of the ACFJ-332B. This PWM input signal is used to drive the gate of Q2 GaN from Transphorm.	Input
6	GaN1_Gate	Connected to the VINA pin of the ACFJ-332B. This PWM input signal is used to drive the gate of Q1 GaN from Transphorm.	Input

Table 2 shows the pin assignments for the high-voltage side. See Figure 4 for more details.

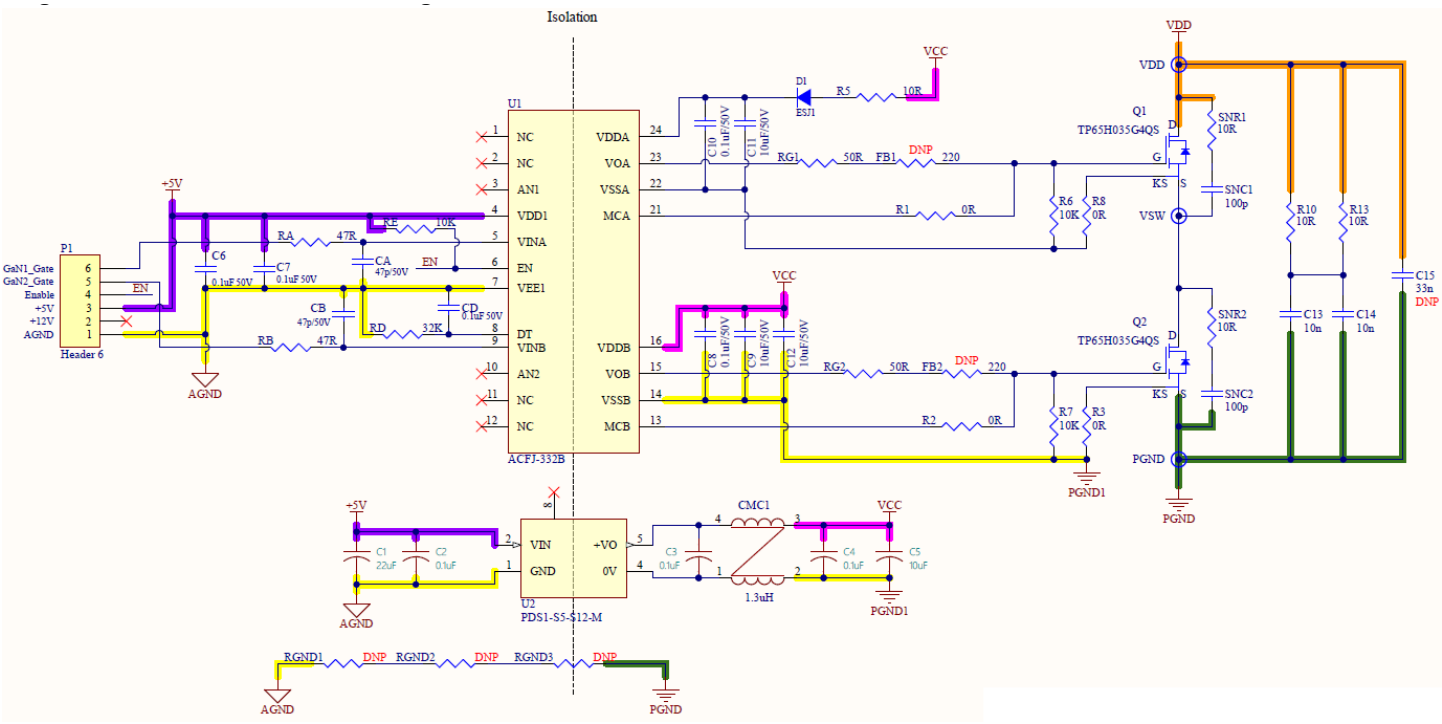
Table 2: Pin Assignments for the High-Voltage Bus and Load Connection (External Connection)

Label	Designation	Function	Direction
VSW	Vsw	This is the HV output terminal to drive an external inductor.	Output
VDD	Vdd	This is the HV DC supply (400 Vdc).	Input
PGND	PGnd	This is the HV supply Gnd (0V).	Input

Circuit Description

Figure 4 shows the schematic of the half-bridge evaluation board.

Figure 4: Schematic of the Half-Bridge Evaluation Board



Input Connector and Power Supply Circuit

P1 is the six-pin input connector that interfaces to the 5V supply and PWM signals.

Under normal operations, a +5V supply must be supplied externally to power up both the low-side logic circuit of U1 (ACFJ-332B) and the DC/DC switching converter U2 (PDS1-S5-S12-M). The Vcc output voltage of U2 is +12 Vdc. This is used to power up the low-side half bridge VDDB of U1. The high-side half bridge +12V power supply can be derived by the bootstrap operation of D1.

Once the +5V supply is turned on, the EN pin of U1 is activated through enable pin 4 by exerting high. Users can also deactivate U1 externally by pulling the pin 4 signal voltage low (0V).

U1's dead time (t_{DT}) control between high- and low-side PWM signal channels can be programmed by setting the values of R_D. t_{DT} is related to R_D under the formula as follows:

t_{DT} in (ns) = (8.9 × R_D) + 18, R_D in (kΩ), C_D = 0.1 µF

NOTE: For the actual value of R_D, see the Bill of Materials.

The PWM outputs of U1, namely VOA and VOB, are controlled by the isolated low-voltage side PWM input signals at pin 6 and pin 5 respectively.

Gate Driver Circuit

The half-bridge evaluation board uses a dual-channel gate drive optocoupler U1 (ACFJ-332B) to drive the GaN FETs directly. The ACFJ-332B is a dual-channel basic gate driver optocoupler used to isolate and drive the GaN FETs. It has two rail-to-rail outputs with 4A of peak output current each to provide fast switching high voltage and driving current to turn on and off the GaN efficiently.

The ACFJ-332B has a propagation delay of less than 65 ns at 5V isolated supply. The very high common mode rejection (CMR) of 150 kV/µs (minimum) is required to isolate high transient noise during the high-frequency operation from causing erroneous outputs. It is certified by UL1577 for V_{ISO} up to 5000V_{RMS}/1 minute and by IEC 60747-5-5 for working voltage V_{IORM} up to 1414 V_{PEAK}.

The ACFJ-332B has a UVLO threshold voltage of 8.6V, suitable for 10V to 12V gate operation of the GaN FET TP65H035G4QS. It has dual outputs, VOA and VOB, to control the turning on and off of dual GaN FETs Q1 and Q2 separately using a 50Ω external gate resistor on RG1 and RG2 respectively. With the 12V supply, this translates to an approximate 0.4A peak current to the gate of the GaN FET.

Ferrite beads, FBL and FBH, might need to be fitted in series with the gate of the GaN FET and should be located as close as possible to the gate pin without an active Miller clamp to prevent false turn-on when the GaN FET is turned off and to keep the gate-source loop as compact as possible to minimize the gate loop inductance. The ferrite beads damp the resonant circuit made up of the gate-source loop inductance and the GaN FET input capacitance. But the ferrite beads are not needed when the active Miller clamp functions of the ACFJ-332B are implemented. The MCA and MCB pins can be connected to the gate of Q1 and Q2 respectively via a 1Ω clamp resistor each (at R1 & R2) to implement the active Miller clamp functions. Each active Miller clamp function is activated when its gate voltage drops below 2.1V and sinks a current of around 0.8A with the gate driver internal Rds(on) of 1.5Ω.

An RC snubber network can be used across VDD and PGND to suppress EMI noise and lower the Q factor resonance in the HVDC bus.

GaN FET Circuit

The half-bridge evaluation board uses two GaN FETs, Q1 for the high-side switch and Q2 for the low-side switch. The TP65H035G4QS is a 650V, 33-mΩ normally off GaN FET that combines Transphorm's latest high-voltage GaN and low-voltage silicon MOSFET technologies in a cascode TOLL package.

Use a DC-link snubber, which consists of R10/R13 and C13/C14, to lower the Q factor of any resonance in the HVDC bus. That resonance acts as a load on the high-gain amplifier, which is the GaN FET, and can lead to instability.

The built evaluation board forms as a daughterboard, which can be plugged directly into the main board to form a buck and boost configuration for evaluation test purposes.

Buck and Boost Configurations

Figure 5 and Figure 6 show the buck and boost configurations. For buck mode, the HVDC input, J2/J3, is connected to the high-voltage input supply, and the output is taken from J5/J7. For boost mode, the high-voltage input supply is connected to J5/J7, and the output is taken from J2/J3.

Note that in boost mode, a load must be connected. The load current affects the output voltage up to the transition from discontinuous conduction mode (DCM) to continuous conduction mode (CCM). In buck mode, the load may be an open circuit. In the case of buck mode with no load, the ripple current in the inductor is symmetrical along the zero crossing current, and the soft switching behavior of the GaN FETs may be studied.

Figure 5: Schematic of the Half-Bridge Evaluation Board for Buck Mode

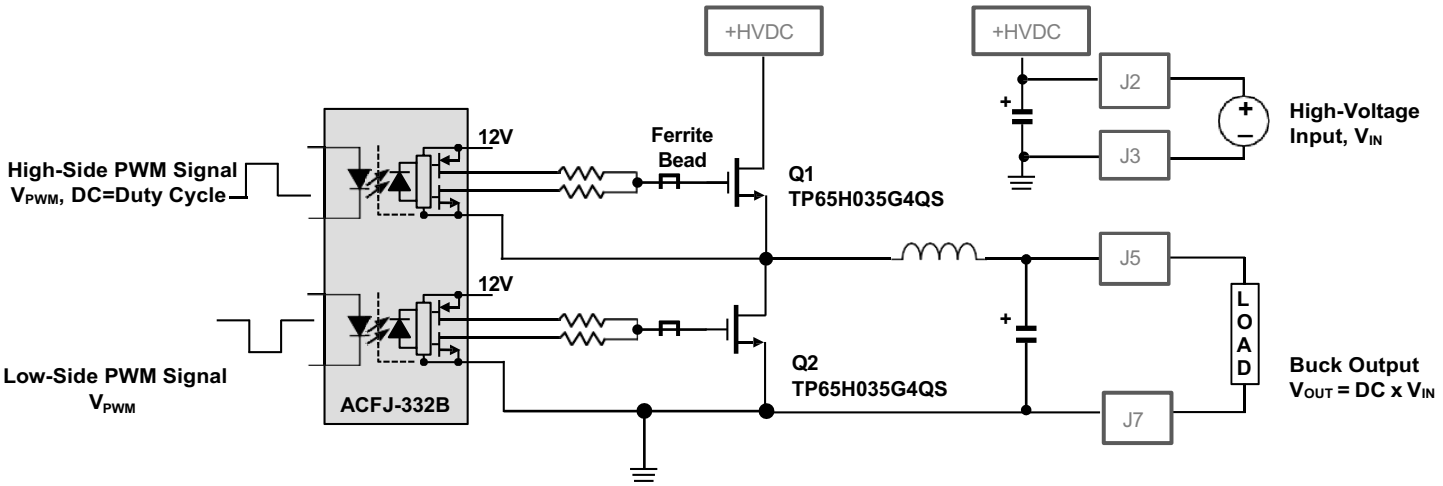
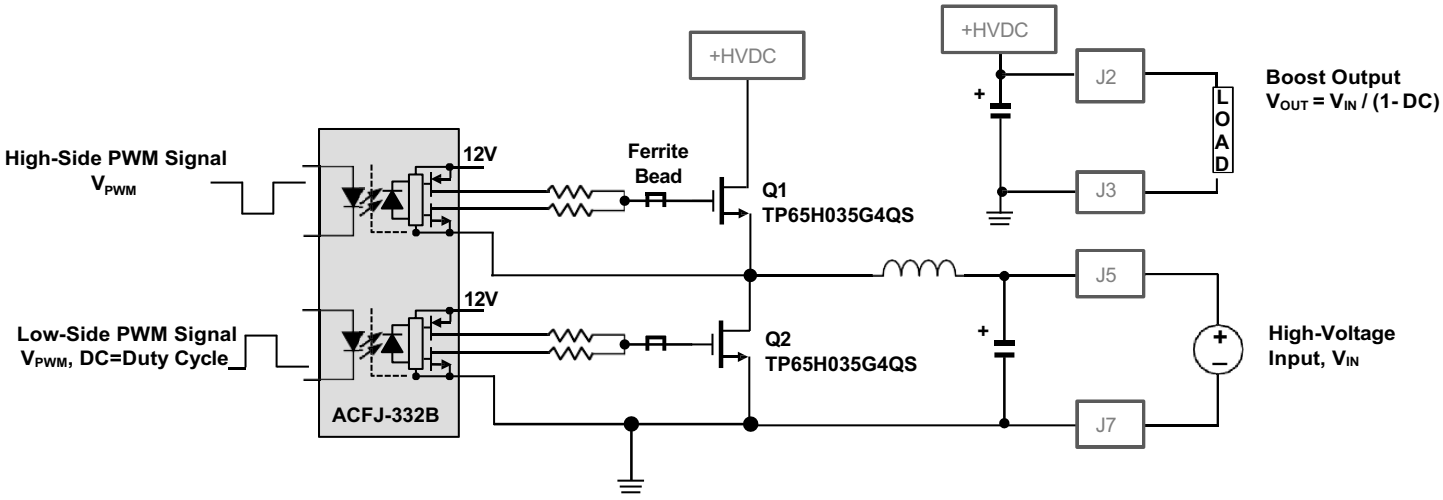


Figure 6: Schematic of the Half-Bridge Evaluation Board for Boost Mode



Switching Waveforms and Efficiency Test

Figure 7: Multiple Pulse Tests at 400V Bus Voltage and Drain Current Stepped to 40A

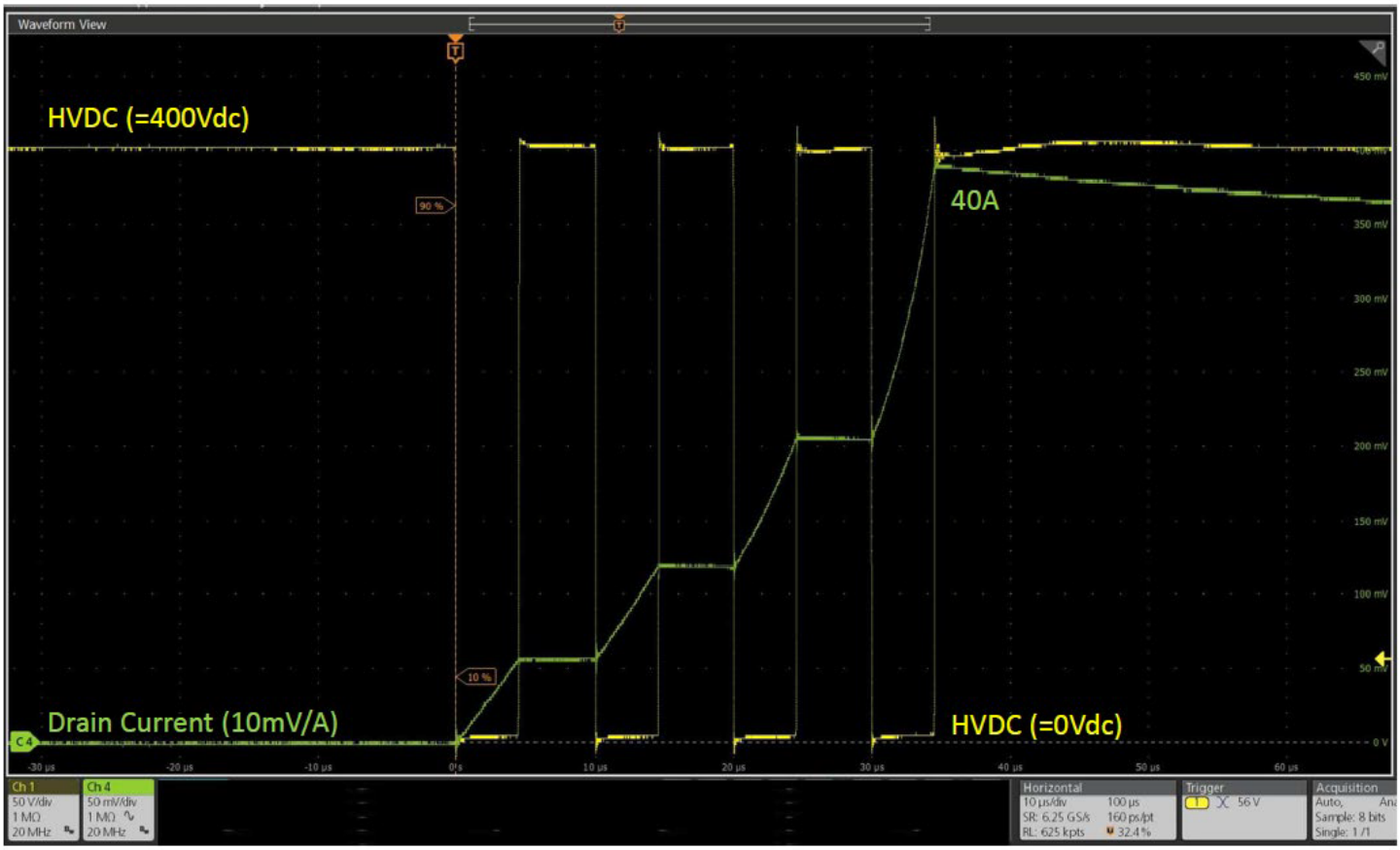


Figure 8: Switching Off at 39A

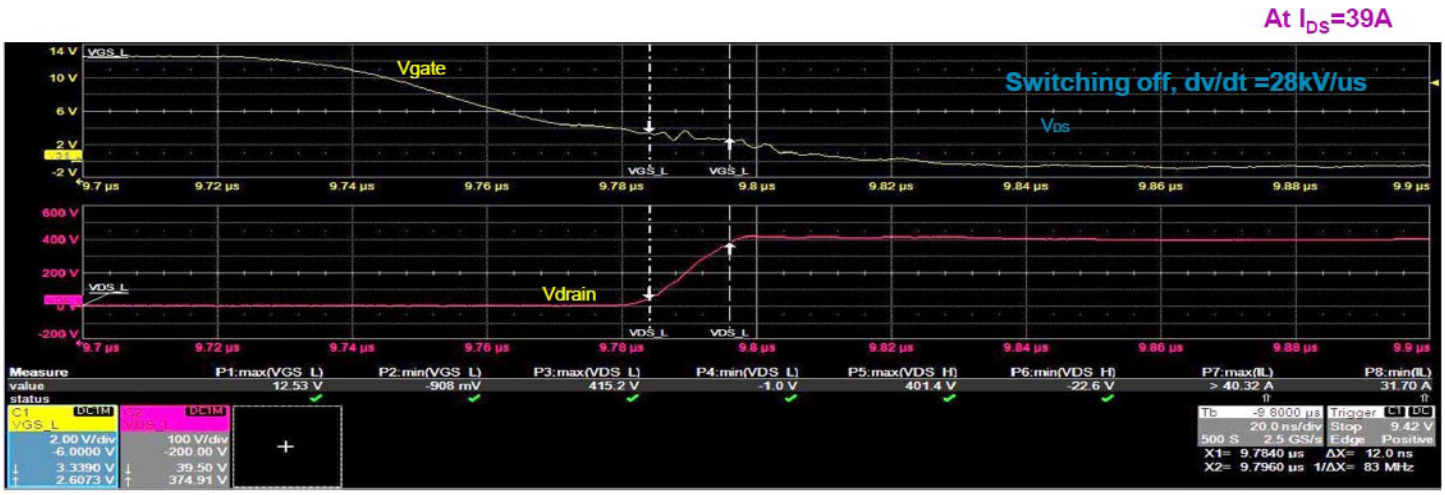


Figure 9: Switching On at 39A

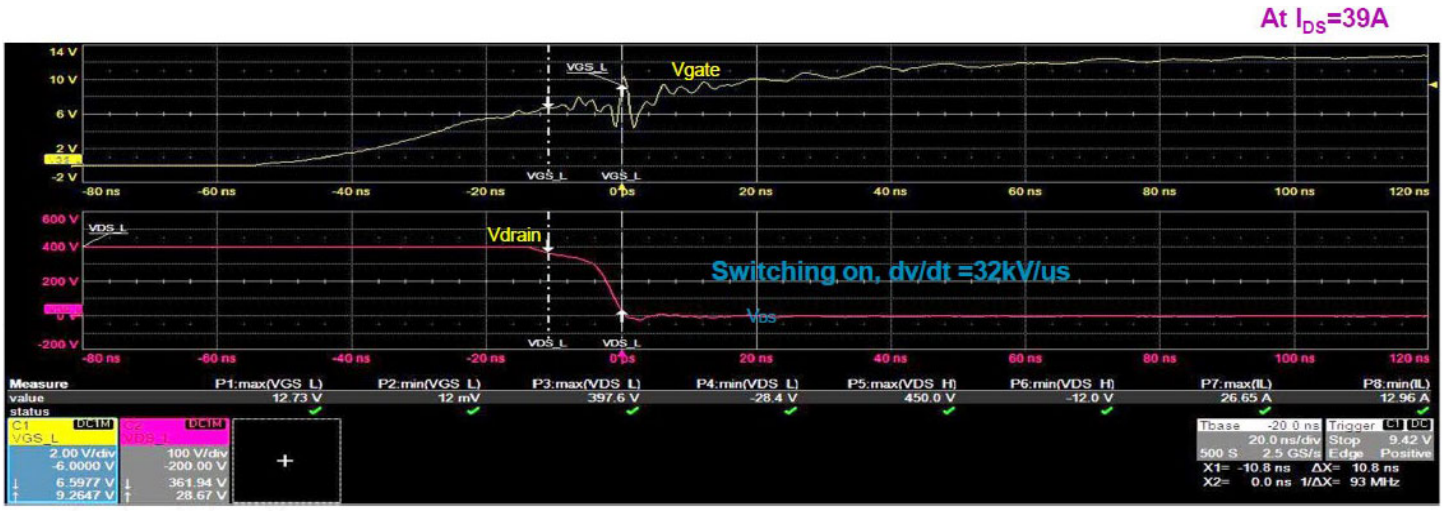
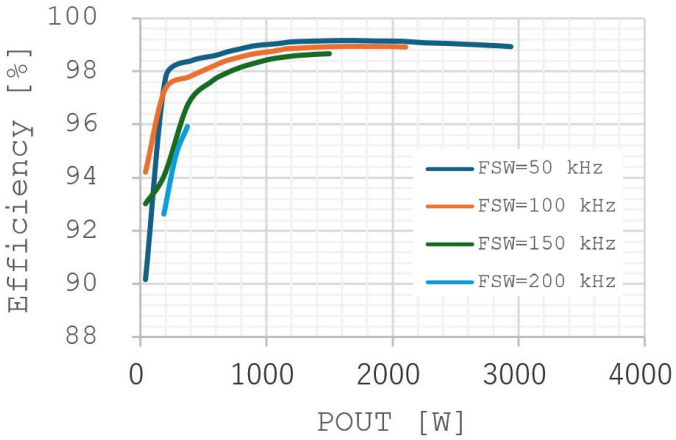


Figure 10: Efficiency at Different Switching Frequencies



Schematics, Layout, and BOM

This section provides the full schematics, layout, and bill of materials of the half-bridge evaluation board. This information enables customers to modify the design according to specific requirements.

Figure 11: Schematic of the Half-Bridge Evaluation Board

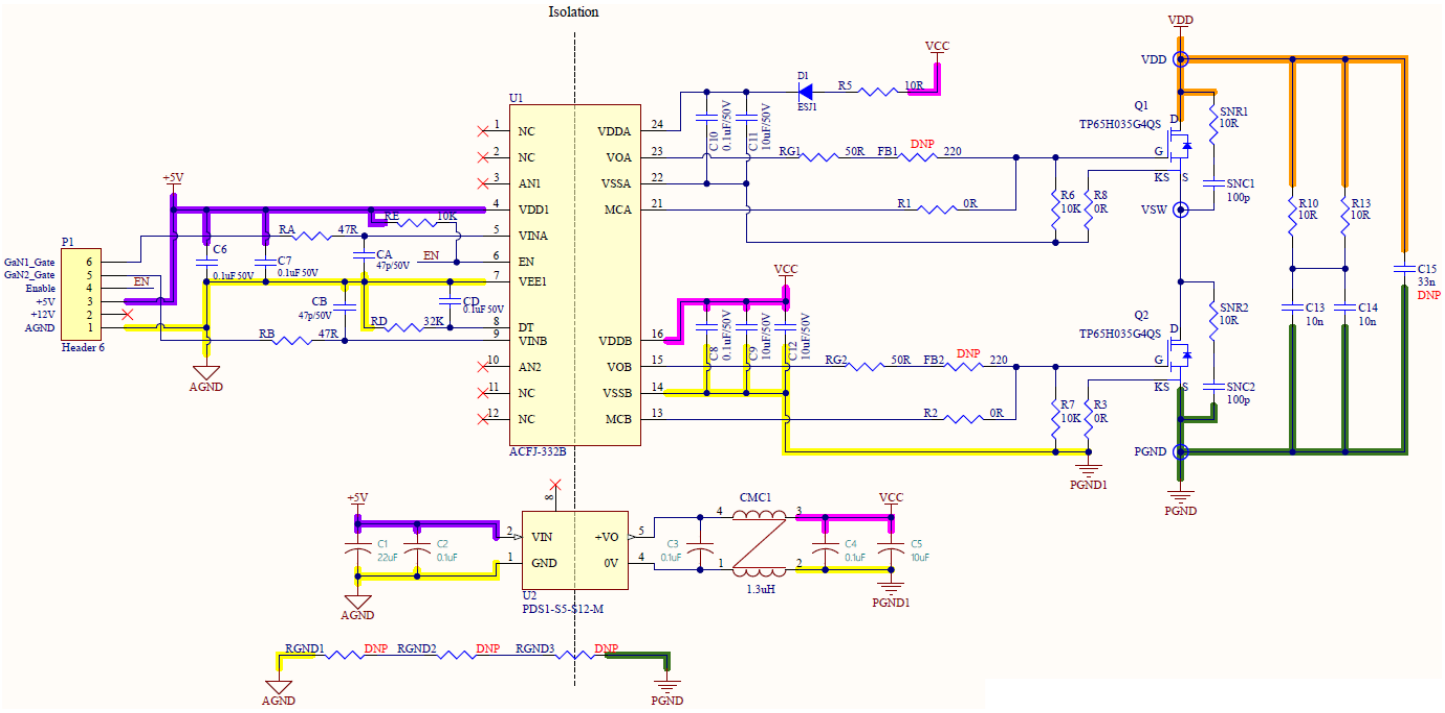


Figure 12: Top Layer with Assembly Drawing

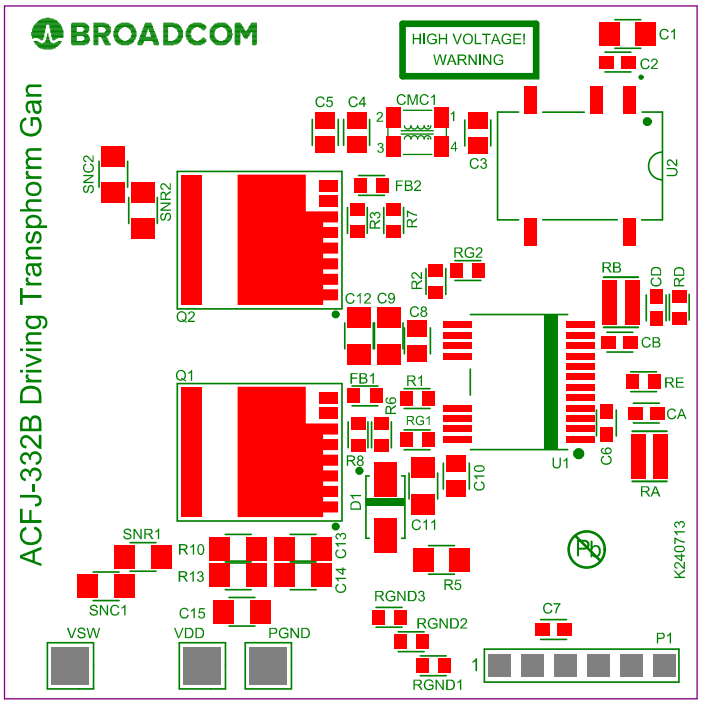


Figure 13: Bottom Layer

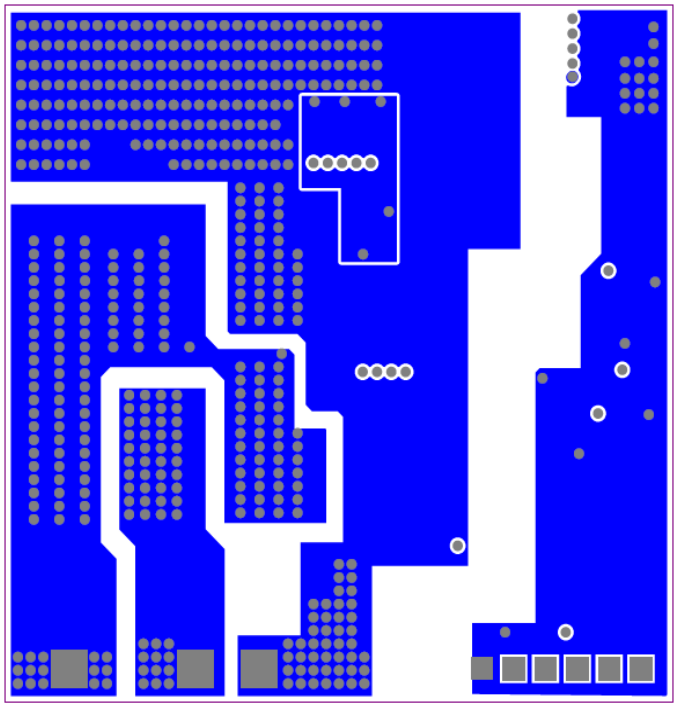


Figure 14: Internal Layer 1

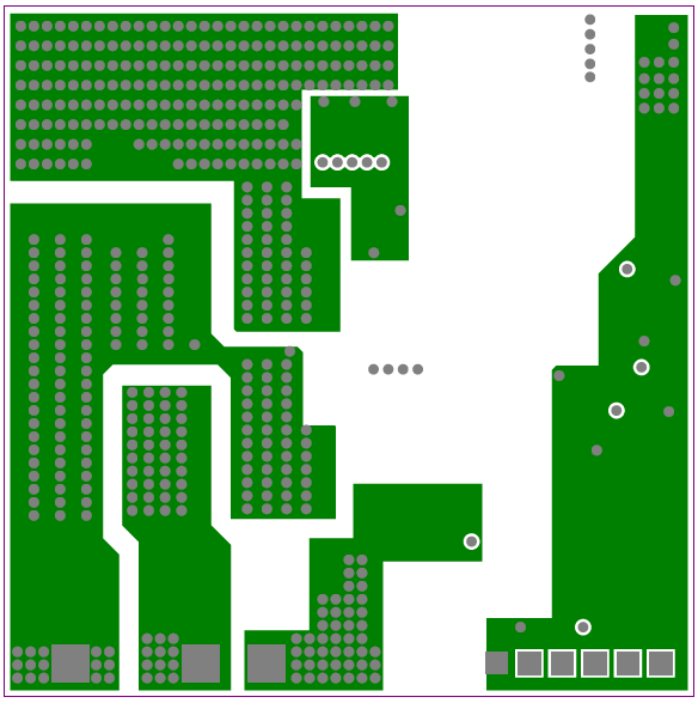


Figure 15: Internal Layer 2

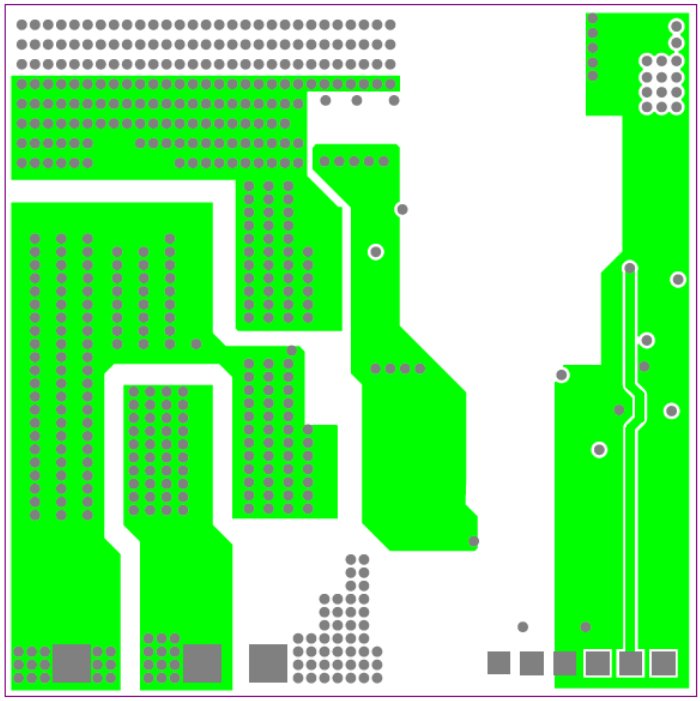


Table 3: Bill of Materials

Parts	Value	Device	Digikey/Mouser/Element14 PN	Qty	Remarks
C2, C6, C7, CD	0.1uF	C-USC0603	399-1282-1-ND	4	
C3, C4, C8, C10	0.1uF	C-USC0805	3372-0805B104K500BDTR-ND / 3013476 / 7569564	4	
SNC1, SNC2	100pF	C-USC1206	CC1206JKNPOZBN101	2	
CA, CB	47pF	C-USC0603	06033C470KAT2A	2	
CMC1	1.3uH	CMC_74423580	732-4222-1-ND / 2249867	1	
P1	6PINCONN	6PINCONN	WM8112-ND	1	
R5, R10, R13	10	R-US_R1206	408-1869-1-ND	3	
SNR1, SNR2	10	R-US_R1206	408-1869-1-ND	2	
R6, R7, RE	10k	R-US_R0603	A126331CT-ND	3	
R1, R2	0	R-US_R0603	RMCF0603ZT0R00CT-ND	2	
RA, RB	47	R-1206 WIDE	LTR18EZPF47R0	2	
C13, C14	10nF	C-USC1206	399-16678-1-ND	2	
C5	10uF	C-USC0805	490-5523-1-ND	1	
C9, C11, C12	10uF	C-USC1206	587-2259-1-ND	3	
RD	32k	R-US_R0603	RT0603BRD0732KL	1	
C1	22uF	C-USC1206	1276-1803-1-ND	1	
RG1, RG2	50	R-US_R0603	541-2655-1-ND	2	
FB1, FB2	0	R-US_R0603	RMCF0603ZT0R00CT-ND	2	
D1	ESJ1	DIODE-DO214AC	ES1JFSCT-ND	1	
U2	PDS1-S5-S12	PDS1-S12-S12-M-TR	102-2686-1-ND	1	
U1	ACFJ-332B	ACFJ-332B	ACFJ-332B	1	
Q1, Q2	TP65H035G4QS	LSG	TP65H035G4QS	2	
R3, R8	0	R-US_R0603	RMCF0603ZT0R00CT-ND	2	
C15	dnp	C-USC1206	DNP: Do not populate	1	DNP
RGND1, RGND2, RGND3	dnp		DNP: Do not populate	3	DNP
VSW, VDD, PGND		CONN PC PIN CIRC 0.040DIA GOLD	ED1278-ND	3	
HS - coolinnovations		HEATSINK	3-101006U	1	
Thermalpad for heatsink			BP100-0.008-00-1010	1