ACFJ-3262

Nexperia GAN039-650NBB Half-Bridge Evaluation Board

Reference Manual
Version 1.0

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1 Introduction

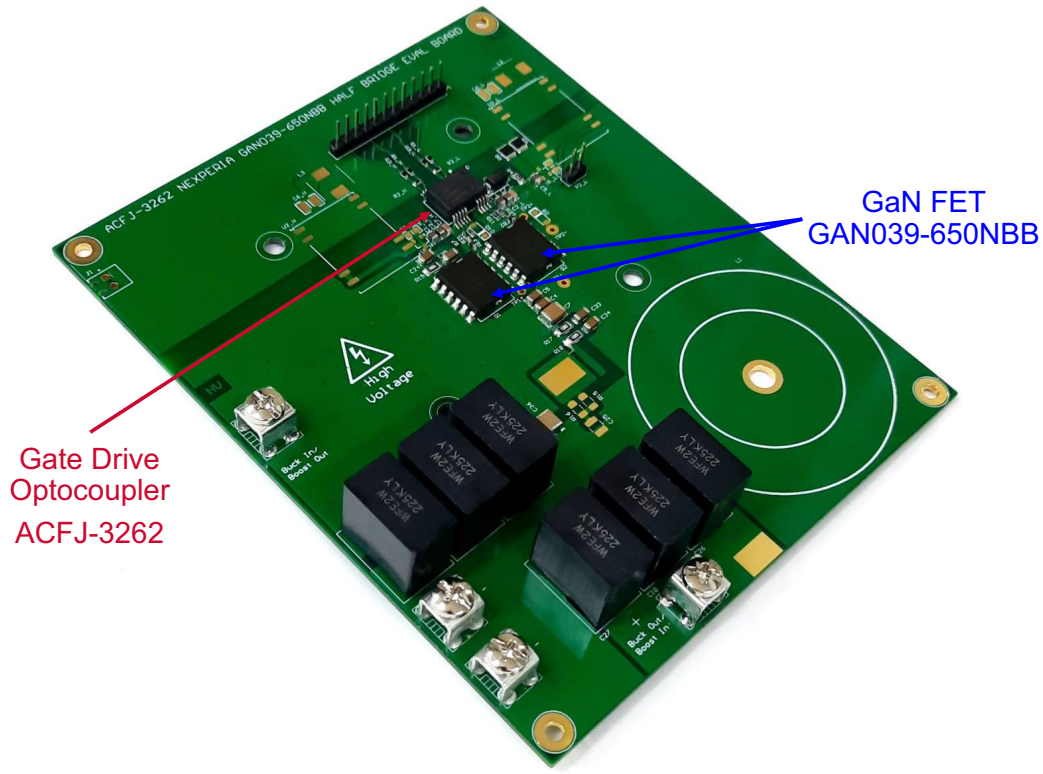
1.1 GaN Power Semiconductor

The Gallium Nitride (GaN) power semiconductor is rapidly emerging into the commercial market delivering huge benefits over conventional Silicon-based power semiconductors. GaN can improve overall system efficiency with lower on-resistance and the higher switching capability can reduce the overall system size and costs. The technical benefits coupled with lower costs have increased the fast adoption of GaN power semiconductors in applications, such as industrial power supplies and renewable energy inverters.

Broadcom gate drive optocouplers have been used extensively in driving Silicon-based semiconductors, such as IGBT. This document describes how the gate drive optocoupler, ACFJ-3262, can be used to drive GaN FET.

The half-bridge evaluation board features ACFJ-3262, 10A dual-channel gate drive optocoupler, and Nexperia's GAN039-650NBB FET. The half-bridge evaluation board enables the basic study of the switching characteristics and efficiency, by means of configuring for synchronous rectification, in either buck or boost mode. The high-voltage input and output operates at up to 400 V_{DC}, with the current limit of the inductor at 15A to 16A, depending upon cooling, ambient temperature, and switching frequency.

Figure 1: ACFJ-3262 Nexperia GAN039-650NBB Half-Bridge Evaluation Board



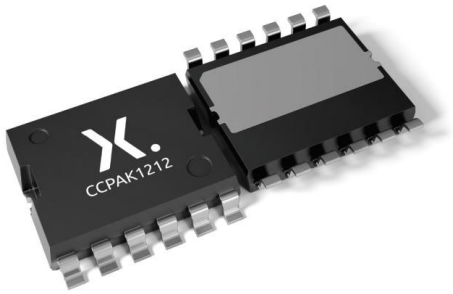
1.2 Design Features

The ACFJ-3262 Nexperia GAN039-650NBB half-bridge evaluation features one ACFJ-3262 gate drive optocoupler and two Two GAN039-650NBB GaN FETs.

One ACFJ-3262 gate drive optocoupler

- 10A peak (typical), rail-to-rail output
- Separate source and sink outputs
- 95-ns max. propagation delay
- 100-kV/µs min. common mode rejection (CMR) at V_{CM} = 1000 V
- 8.6V UVLO with hysteresis
- Wide operating V_{DD} Range: 10V to 25 V
- Wide automotive temperature range: –40°C to 125°C
- Dual channel in SO-24 package
- CTI > 600V
- Greater than 2.8-mm channel-to-channel separation
- Safety approvals:
  - UL Recognized 5000 V_{RMS} for 1 minute
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 1230 V_{PEAK}

Two GAN039-650NBB GaN FETs



- Simplified driver design as standard level MOSFET gate drivers can be used:
  - 0V to 12V drive voltage
  - Gate threshold voltage V_{GSth} of 4V
- Robust gate oxide with ±20V V_{GS} rating
- High gate threshold voltage of 4V for gate bounce immunity
- Low body diode V_f for reduced losses and simplified dead-time adjustments
- Transient over-voltage capability for increased robustness
- CCPAK package technology:
  - Improved reliability, with reduced $R_{th(j\text{-}mb)}$ for optimal cooling
  - Lower inductances for lower switching losses and EMI
  - 175°C maximum junction temperature
  - High board-level reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive X-ray equipment
  - Easy solder wetting for good mechanical solder joints

2 Board Description

2.1 Functional Block Diagram

The evaluation board has a half-bridge topology as shown in Figure 2. Two pairs of high voltage ports, J2/J3 and J5/J7 serve as either high-voltage input or output, depending on whether it is buck or boost configuration. In either case, one GaN FET acts as the active power switch while the other carries the freewheeling current. The latter device may be enhanced as a synchronous rectifier as well. With GaN FETs, the reverse recovery charge is low, and there is no need for additional freewheeling diodes.

The high-side and low-side PWM signals are connected to connector P1, which is used to drive the LEDs of ACFJ-3262 directly.

An inductor is provided as a starting point for investigation. This is a 330-µH toroid intended to demonstrate a reasonable compromise between size and efficiency with the current limited at 15A to 16A and at a switching frequency of 100 kHz.

Figure 2: Half-Bridge Evaluation Board Functional Block Diagram

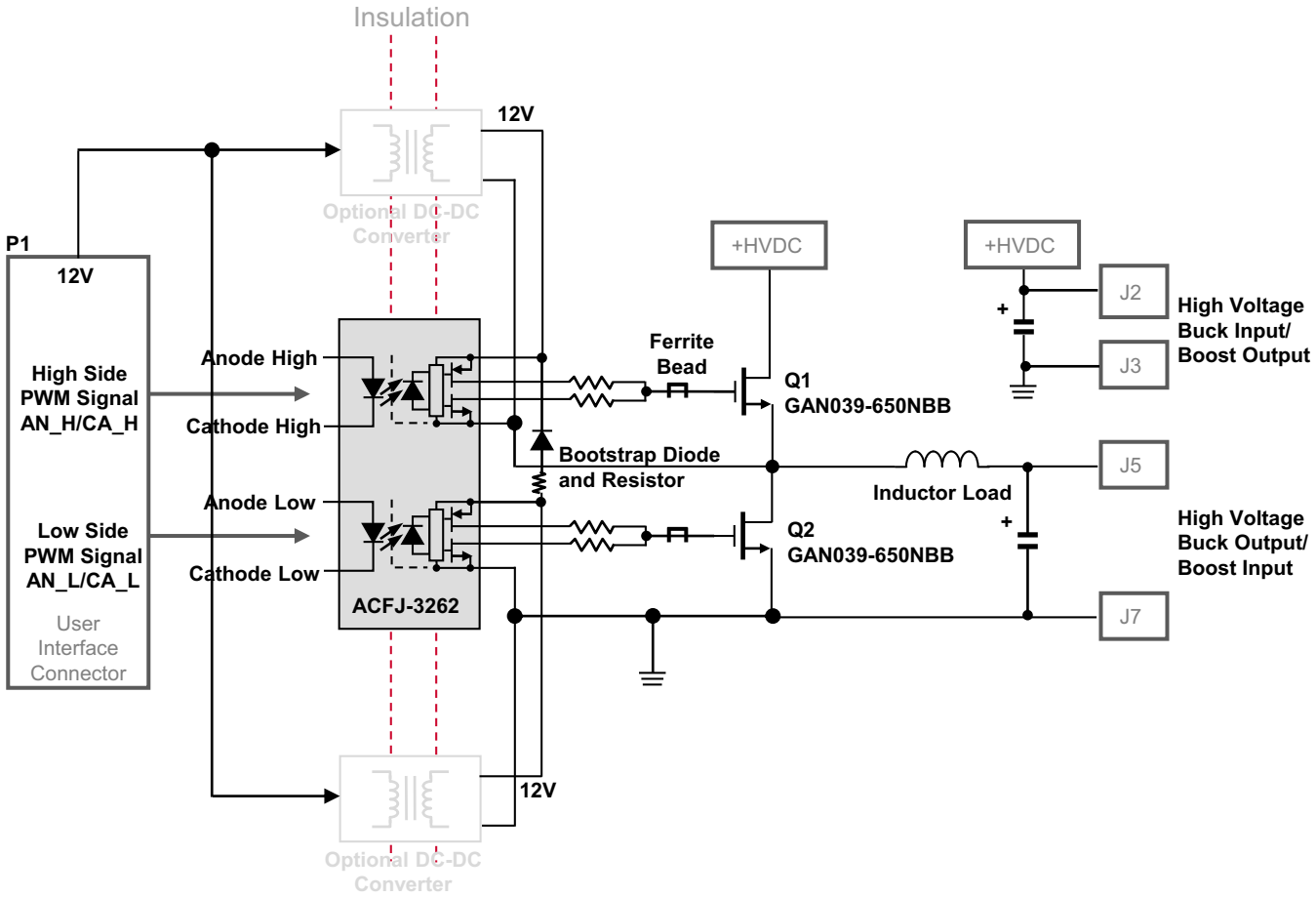
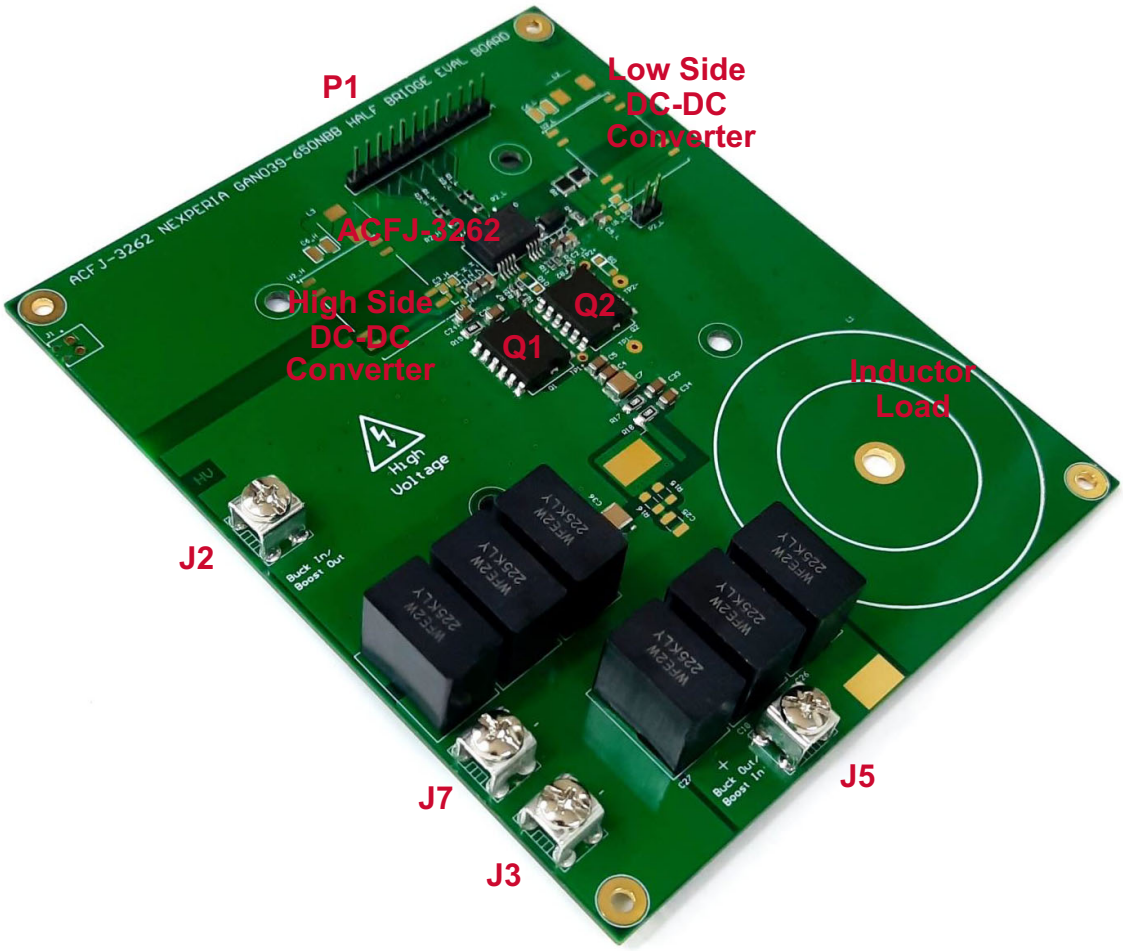


Figure 3: Functional Block Disposition on the Evaluation Board



2.2 Pin Assignment

Pin assignment for P1 connector is shown in Table 1.

Table 1: Pin Assignment of Connector P1 (User Interface Connector)

Label	Function	Direction
DC12VIN	12V power supply. If the DC-DC converter is not used, the 12V input can be applied either at P1 or J1, and R8 and R9 populated with 0Ω for the low side supply. The high side supply can then be derived from the bootstrap circuit, D1 and R4. Alternatively, the 12V can also be used with DC-DC converter MGJ1D121505MPC-R7 to provide isolated power supply.	Input
NC	No connection.	N/A
GND	Reference ground for the 12V power supply.	Input
NC	No connection.	N/A
AN_L	5V PWM input signal for the low side driver. Connects to the anode of the low side gate driver.	Input
NC	No connection.	N/A
CA_L	Reference ground for the low side driver PWM input signal. Connects to the cathode of the low side gate driver.	Input

Table 1: Pin Assignment of Connector P1 (User Interface Connector) (Continued)

Label	Function	Direction
NC	No connection.	N/A
AN_H	5V PWM input signal for the high side driver. Connects to the anode of the high side gate driver.	Input
NC	No connection.	N/A
CA_H	Reference ground for the high side driver PWM input signal. Connects to the cathode of the high side gate driver.	Input
NC	No connection.	N/A

Pin assignment for P2, gate driver power supply connector is shown in Table 2. There is no connection needed if DC-DC converters are used.

Table 2: Pin Assignment of Connector P2_L for Gate Driver, ACFJ-3262 Power Supply

Label	Function	Direction
P2_L, VDDL	Output stage low side power supply. Recommended 10V to 12V for the V_{GS} of the GaN FET. The high side supply can then be derived from the bootstrap circuit, D1 and R4. DC-DC converters MGJ1D121505MPC-R7 are not needed if this power supply scheme is used.	Input
P2_L, PGND	Reference ground for the output stage low side power supply.	Input

High voltage BUS and Load connections are shown in Table 3.

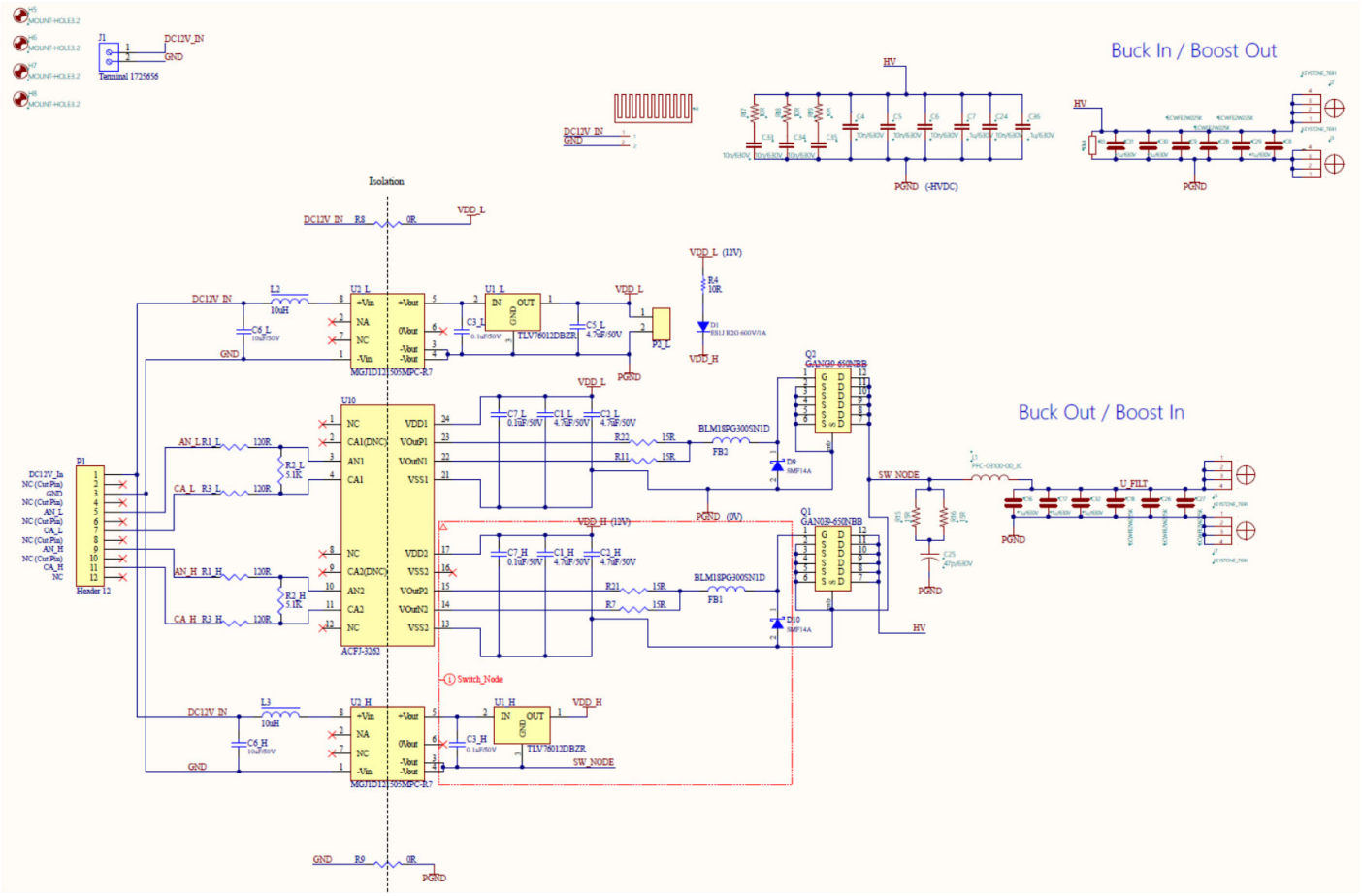
Table 3: High Voltage BUS (+HVDC and –HVDC) and Load Connection

Label	Function	Direction
J2(+HVDC), J5	High voltage input for Buck mode or high voltage output for Boost mode. The high voltage input and output can operate at up to 400VDC.	Input/Output
J3, J7	Reference ground for the high voltage input or output.	Input/Output

3 Circuit Description

The schematic of the half-bridge evaluation board is shown in Figure 4.

Figure 4: Schematic of the Half-Bridge Evaluation Board



3.1 Input Connector and Power Supply Circuit

P1 is the 12 pins input connector that interfaces to the 12V supply and PWM signals.

In the standard setup where the DC-DC converter is not used, the 12V input can be applied either at P1 or J1, and R8 and R9 populated with 0Ω for the low side supply. The high side supply can then be derived from the bootstrap circuit, D1 and R4. Alternatively, the external isolated 12V supply can also be connected to P2_L. In this case, there is no connection needed for DC12V_In at P1, and R8 and R9 should not be populated. Bootstrap power supply can then be used for the high side gate driver using bootstrap diode D1 and resistor R4.

For DC-DC converter setup, the 12V DC power supply can be connected to DC12V_In (Pin1) and GND (Pin 3) to provide isolated power supply to the secondary side through U2_L and U2_H. The Murata MGJ1D121505MPC-R7 is a 12V to +15V/–5V DC-DC converter and TLV76012DBZR is a 12V linear voltage regulator. They are used to provide 12V isolated supply to the high and low side gate driver optocoupler, U1.

3.2 Gate Driver Circuit

The half-bridge evaluation board uses a dual-channel gate drive optocoupler U10, ACFJ-3262 to drive the GaN FETs directly. The ACFJ-3262 is a basic gate driver optocoupler used to isolate and drive the GaN FETs. It has a rail-to-rail output with 10A maximum output current to provide fast switching high voltage and driving current to turn-on and off the GaN efficiently.

The ACFJ-3262 has a propagation delay of less than 95 ns. The very high CMR, common mode rejection of 100 kV/µs(min.) is required to isolate high transient noise during the high frequency operation from causing erroneous outputs. It is certified by UL1577 for up to V_{ISO} 5000V_{RMS}/min and IEC 60747-5-5 for working voltage, V_{IORM} up to 1230V_{PEAK}.

The LED inputs of the gate driver use a split resistor network of 120Ω at the anode and cathode. This is to balance the input impedance of the LEDs to achieve the high CMR of 100 kV/µs.

The ACFJ-3262 has a UVLO threshold voltage of 8.6V, suitable for 10V to 12V gate operation of the GaN FET GAN039-650NBB. It has dual output, VOutP1 and VOutP2 to control the turning on and off of the GaN FET using external 15Ω gate resistors, Rgon and Rgoff. With the 12V supply, this translates to approximate 0.8A peak current to the gate of the GaN FET.

Ferrite beads, FBL and FBH must be fitted in series with the gate of the GaN FET and should be located as close as possible to the gate pin. Keep the gate-source loop as compact as possible to minimize the gate loop inductance. The Ferrite bead damps the resonant circuit made up of the gate source loop inductance and the GaN FET input capacitance, thus providing fast switching stability. Use BLM18PG300SN1D with an impedance of 30Ω at 100 MHz.

14V TVS diodes D9 and D10, can be used to clamp and protect the gate of the GaN FET and gate driver output. However, the GaN FET does not require this diode for normal operation. The TVS diode must be selected carefully to prevent adverse effect to the switching performance.

3.3 GaN FET Circuit

The half-bridge evaluation board uses two GaN FETs, Q1 for the high side switch and Q2 for the low side switch. The GAN039-650NBB is a 650V, 33-mΩ normally-off GaN FET that combines Nexperia’s latest high-voltage GaN HEMT H2 technology and low-voltage silicon MOSFET technologies in a CCPAK1212 package.

Use a DC-link snubber, which consists of R17/R18/R19 and C33/C34/C35 to lower the Q factor of any resonance in the HVDC bus. That resonance acts as a load on the high-gain amplifier, which is the GaN FET and can lead to instability. The remaining capacitors, C4-6/C17/C24.C36–16 are high-frequency DC-link components, placed very close to the GaN FETs for fast switching half-bridge operations.

4 Buck and Boost Configurations

The buck and boost configurations are shown in Figure 5 and Figure 6. For buck mode, the HVDC input, J2/J3, is connected to the high-voltage input supply, and the output is taken from J5/J7. For boost mode, the high-voltage input supply is connected to J5/J7, and the output is taken from J2/J3.

Note that in boost mode, a load must be connected. The load current affects the output voltage up to the transition from discontinuous conduction mode (DCM) to continuous conduction mode (CCM). In buck mode, the load may be an open circuit. In the case of buck mode with no load, the ripple current in the inductor is symmetric about zero, and the soft switching behavior of the GaN FETs may be studied.

Figure 5: Schematic of the Half-Bridge Evaluation Board for Buck Mode

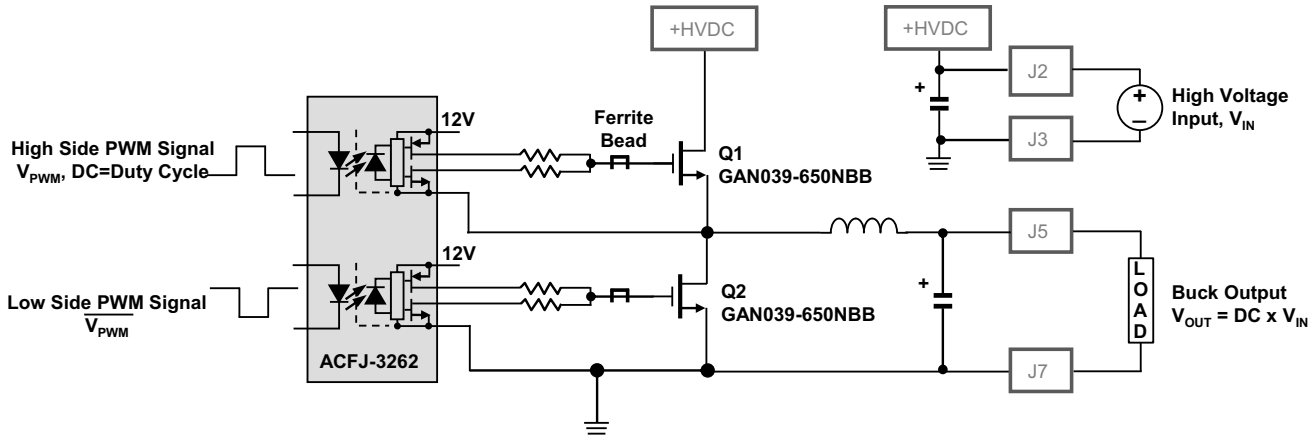
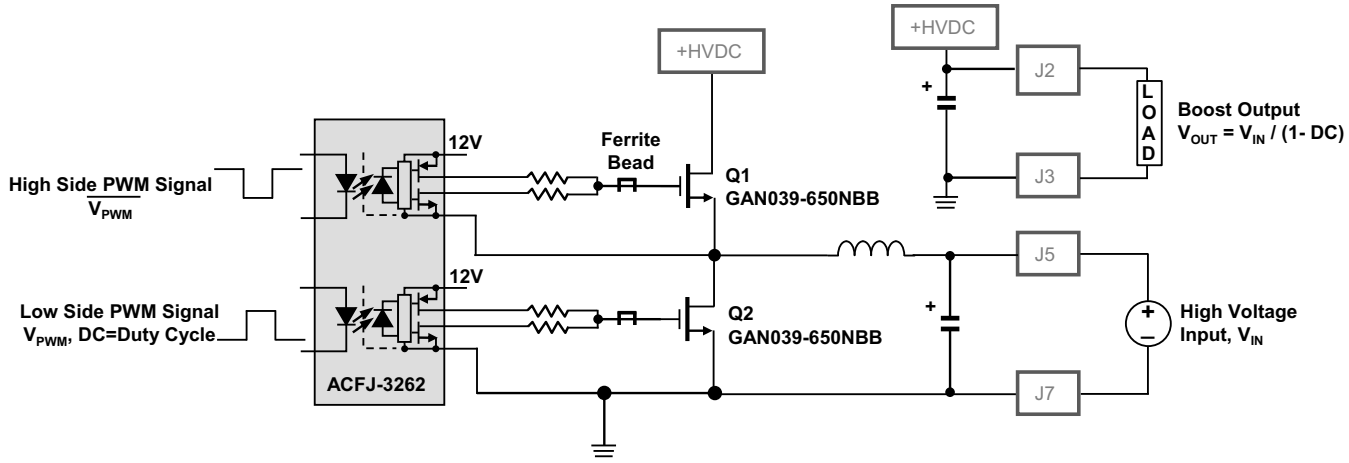


Figure 6: Schematic of the Half-Bridge Evaluation Board Boost Mode



5 Switching Waveforms and Efficiency Test

Figure 7: Multiple Pulse Tests at 400V BUS Voltage and Drain Current Stepped to 60A

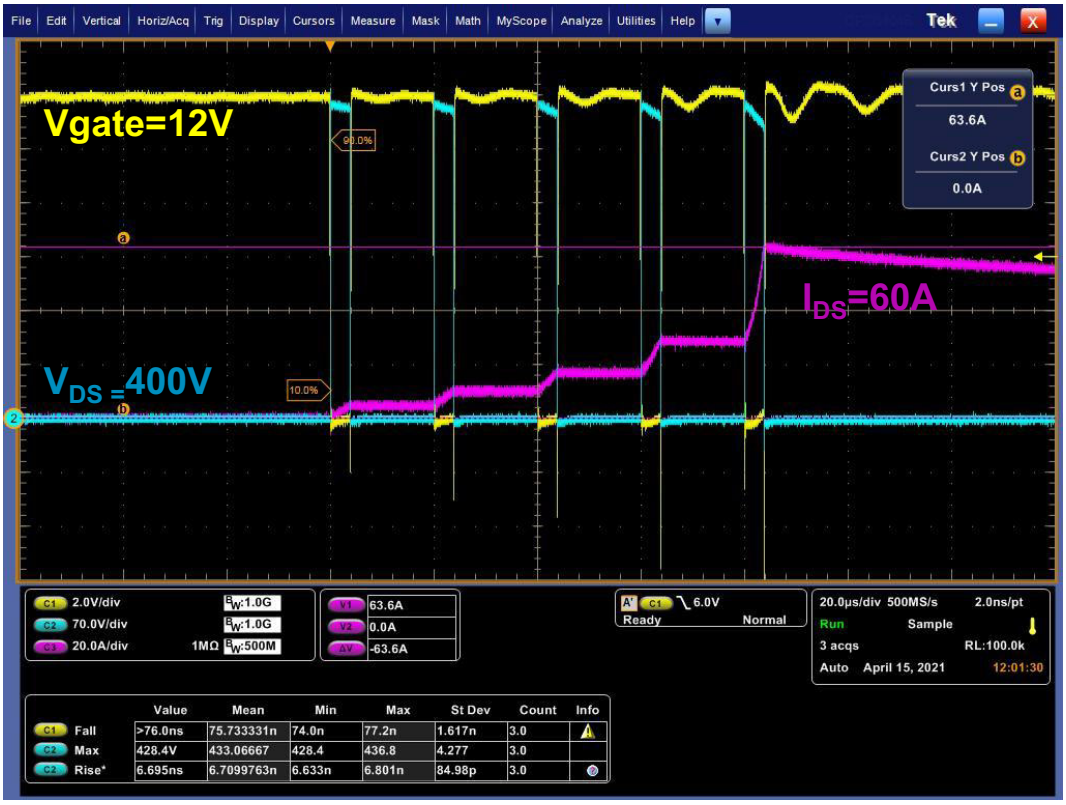


Figure 8: Switching Off at 28A

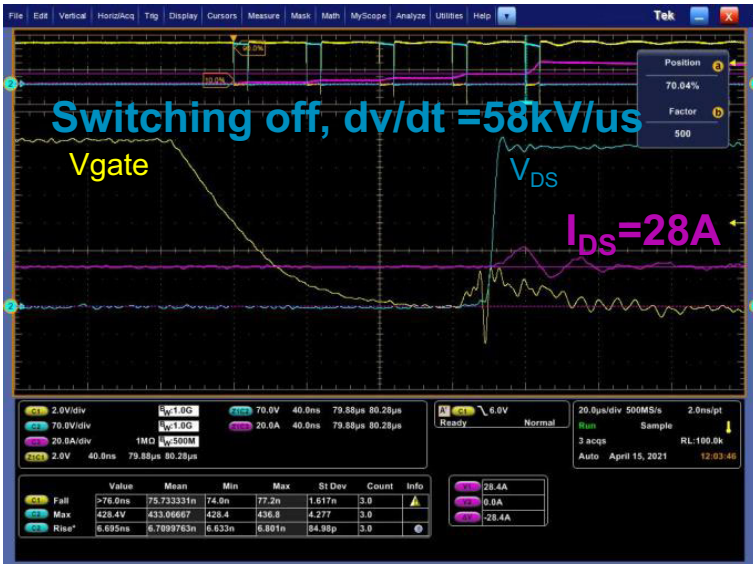
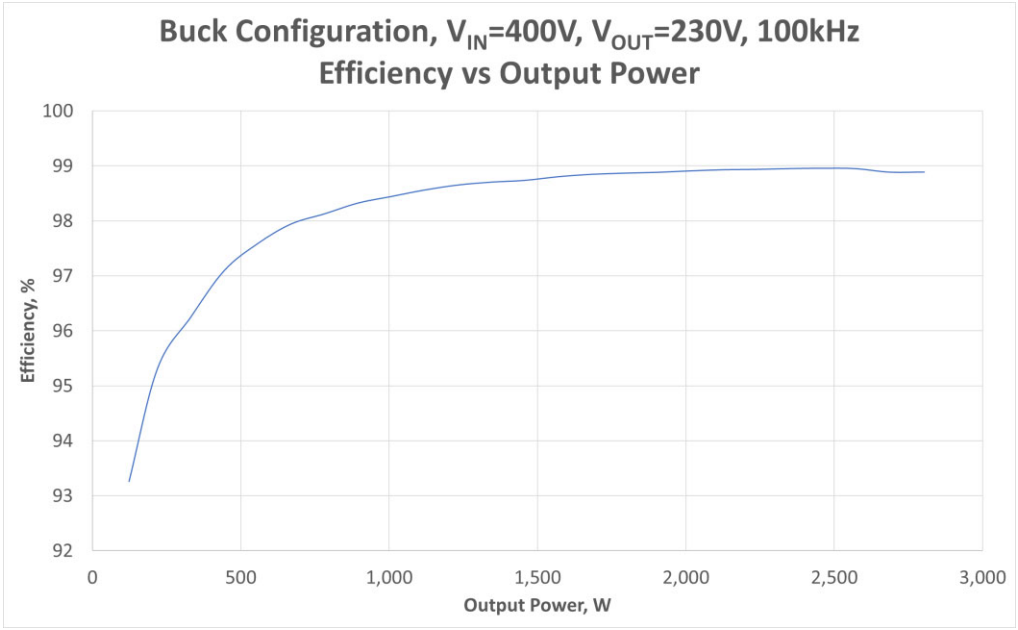


Figure 9: Switching On at 60A

Figure 10: Efficiency Sweep for Buck Conversion from 400V to 230V



6 Schematics, Layout, and BOM

This section provides full schematics, layout, and bill of materials of the half-bridge evaluation board. This information enables customers to modify the design according to specific requirements.

Figure 11: Schematic of the Half-Bridge Evaluation Board

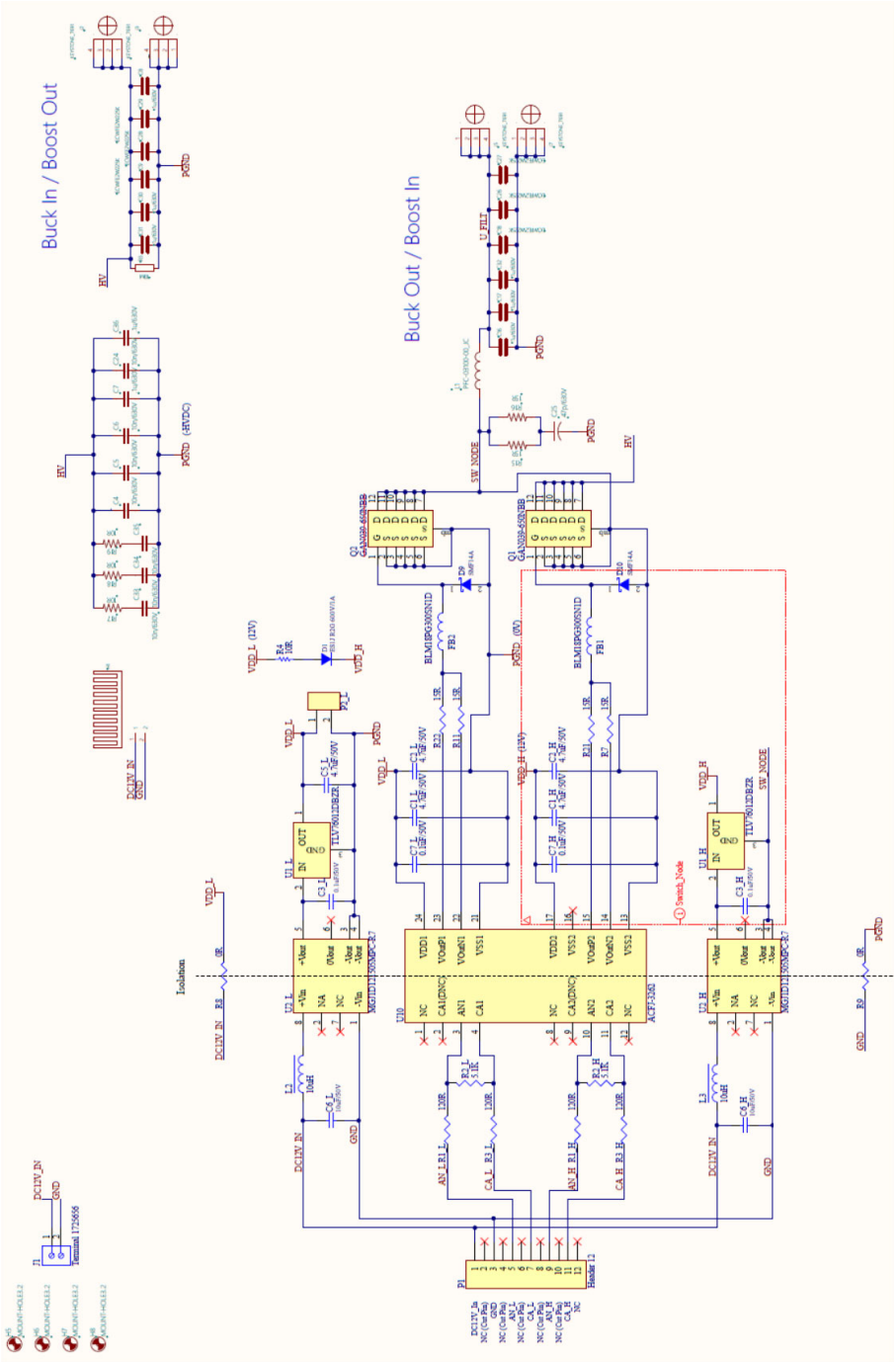


Figure 12: Top Level and Assembly Drawing

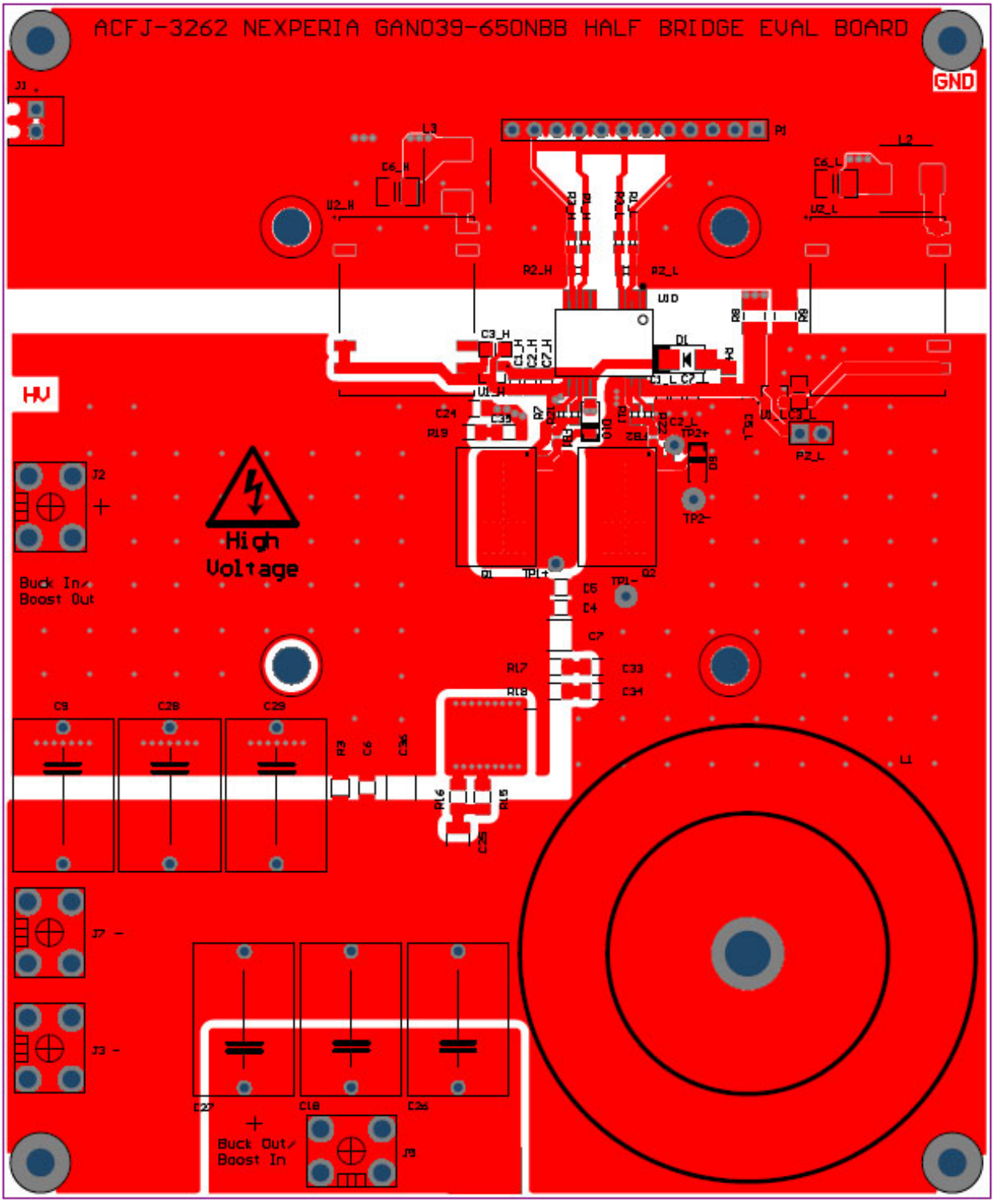


Figure 13: Signal Layer 1

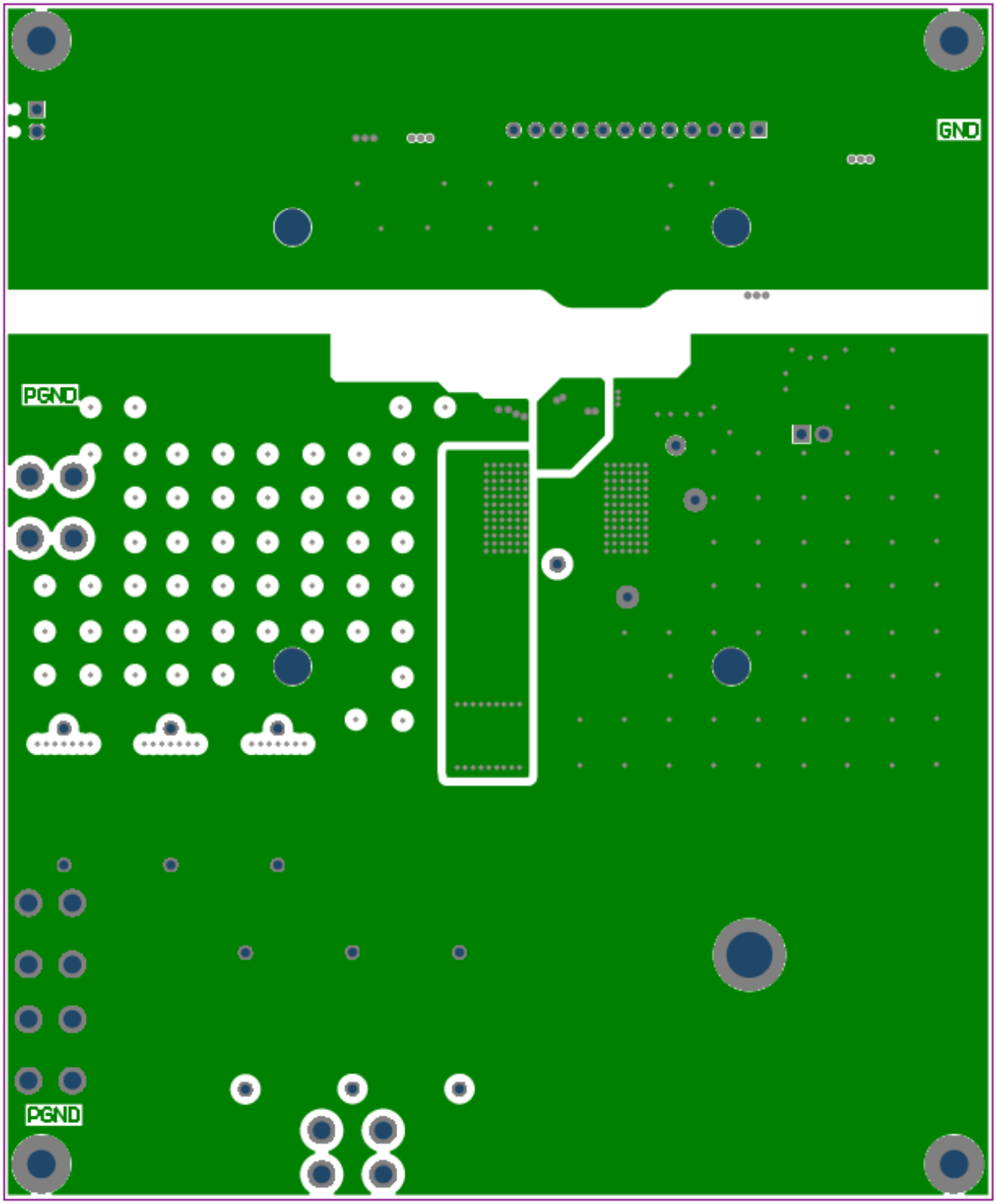


Figure 14: Signal Layer 2

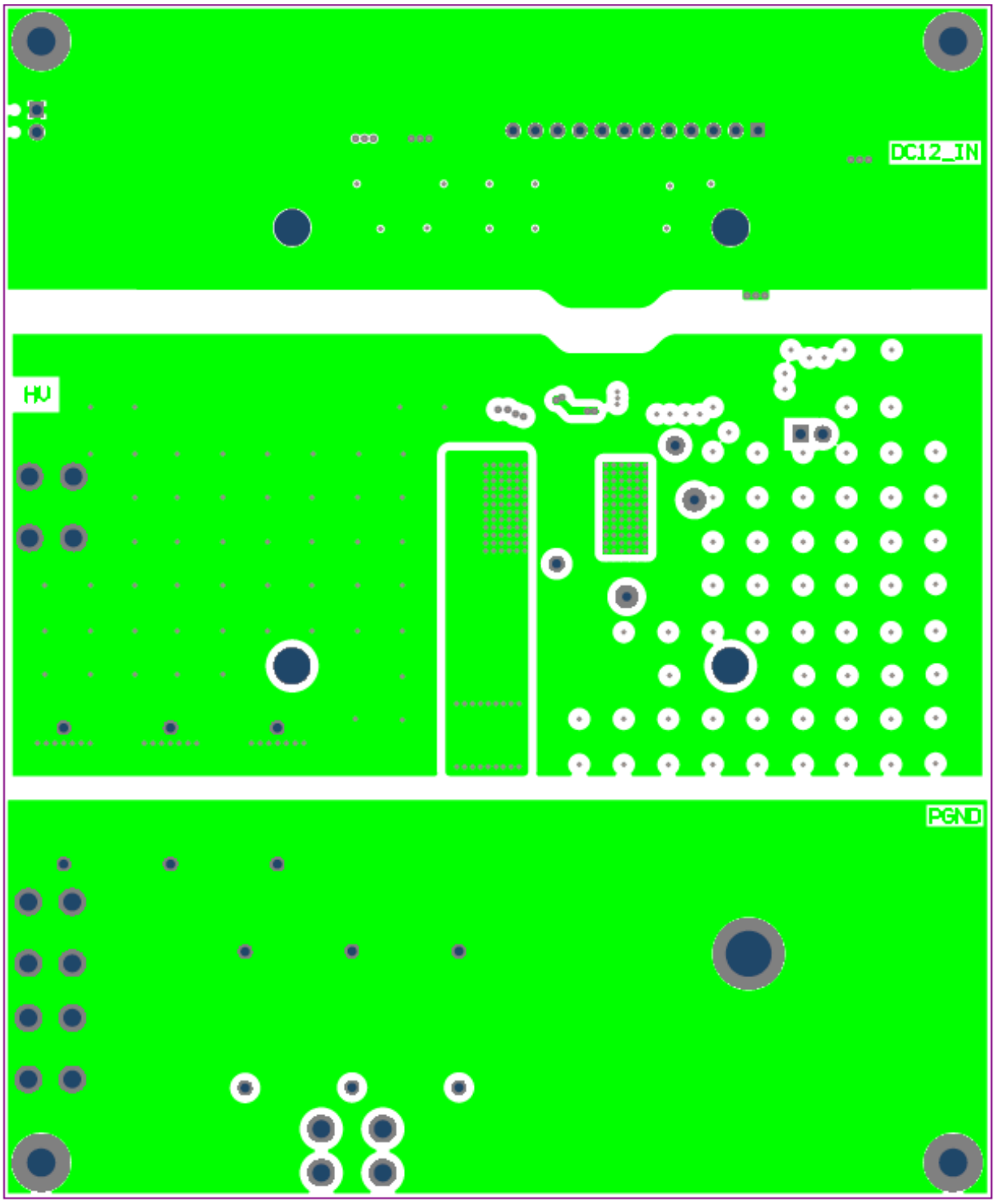
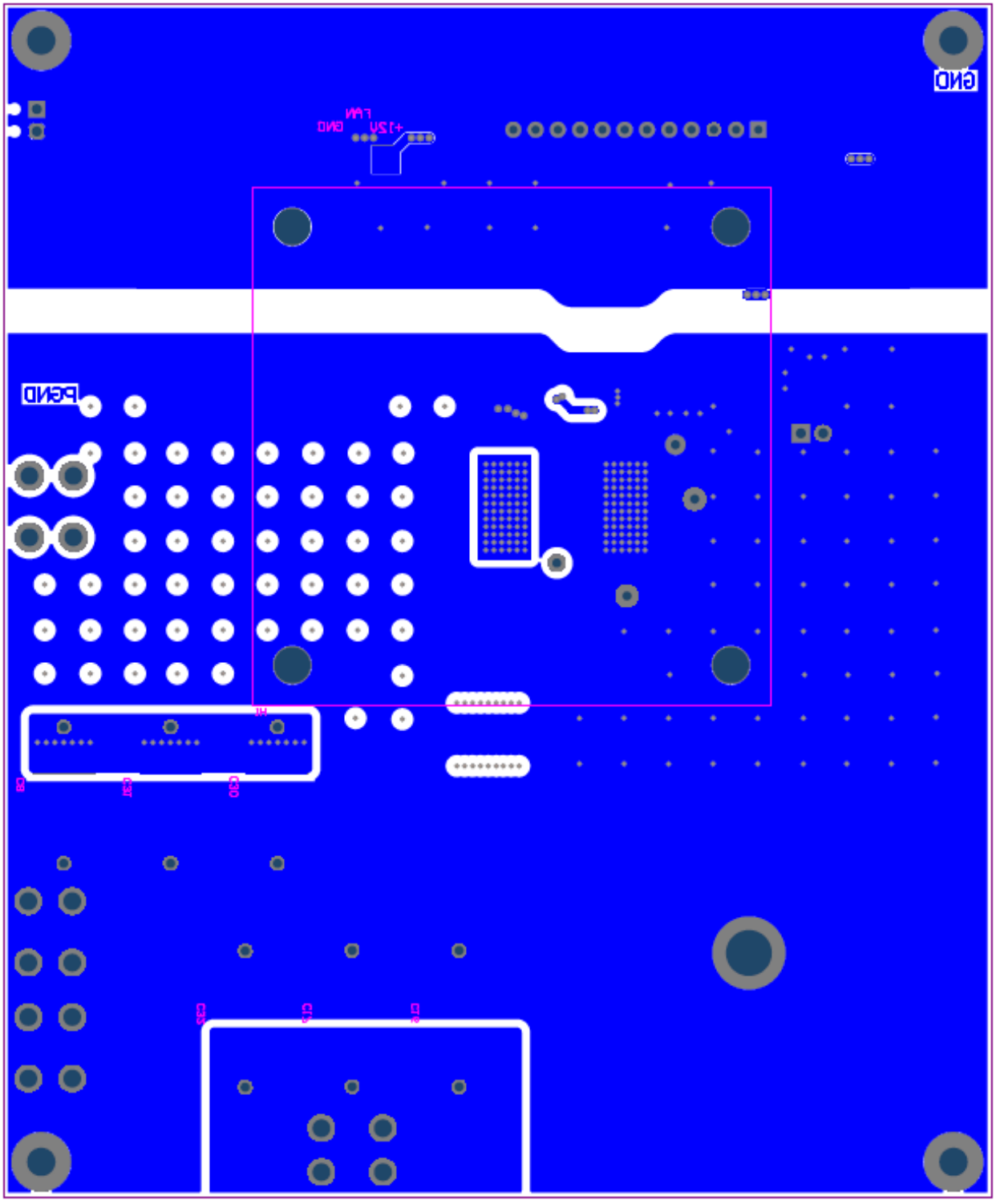


Figure 15: Bottom Layer



Revision History

Version 1.0, June 9, 2021

- Initial document release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