PRELIMINARY DATA SHEET

AC101

AC101QF/TF Ultra Low Power 10/100 Ethernet Transceiver

GENERAL DESCRIPTION

The AC101QF/TF is a highly integrated, 3.3V, low power, 10BASE-T/100BASE-TX/FX, Ethernet transceiver implemented in 0.35 µm CMOS technology. Multiple modes of operation, including normal operation, test mode and power saving mode, are available through either hardware or software control.

Features include MAC interfaces, encoder/decoders (ENDECs), Scrambler/Descrambler, and Auto-Negotiation (ANeg) with support for parallel detection. The transmitter includes a dual-speed clock synthesizer that only needs one external clock source (crystal or clock oscillator). The chip has built-in wave shaping driver circuit for both 10 Mbps and 100 Mbps, eliminating the need for an external hybrid filter. The receiver has an adaptive equalizer/DC restoration circuit for accurate clock and data recovery for the 100BASE-TX signal. It also provides an on-chip low pass filer/Squelch circuit for the 10BASE-T signal.

MAC interfaces to support 10/100 MII, 100M only Symbol Mode, 10M only Symbol Mode and 10M only 7 wire interface are included.

The AC101TF and the AC101QF are the same product in different packages.

FEATURES

- MII MAC connection
  - 5 Volt tolerant and 2.5 Volt capable
- 10/100 TX/FX
  - Full-duplex or half-duplex
  - FEFI on 100FX
- Two packages: 80TQFP and 100PQFP
- Industrial temperature: -40°C to +85°C
- Very low power – TYP < 280 mW (Total)
  - Cable Detect mode – TYP < 40 mW (Total)
  - Power Down mode – TYP < 3.3 mW (Total)
  - Selectable TX drivers for 1:1 or 1.25:1 transformers for additional power reduction
- 3.3 Volt .35 micron CMOS
- Fully compliant with
  - IEEE 802.3/802.3u
  - MII
- Baseline Wander Compensation
- Multi-Function LED outputs
- Legacy 10BASE-T 7 wire interface
- 100M Symbol Mode/10M Symbol Mode
- Cable length indicator
- Reverse polarity detection and correction with register bit indication – automatic or forced
- 8 programmable interrupts
- Diagnostic registers

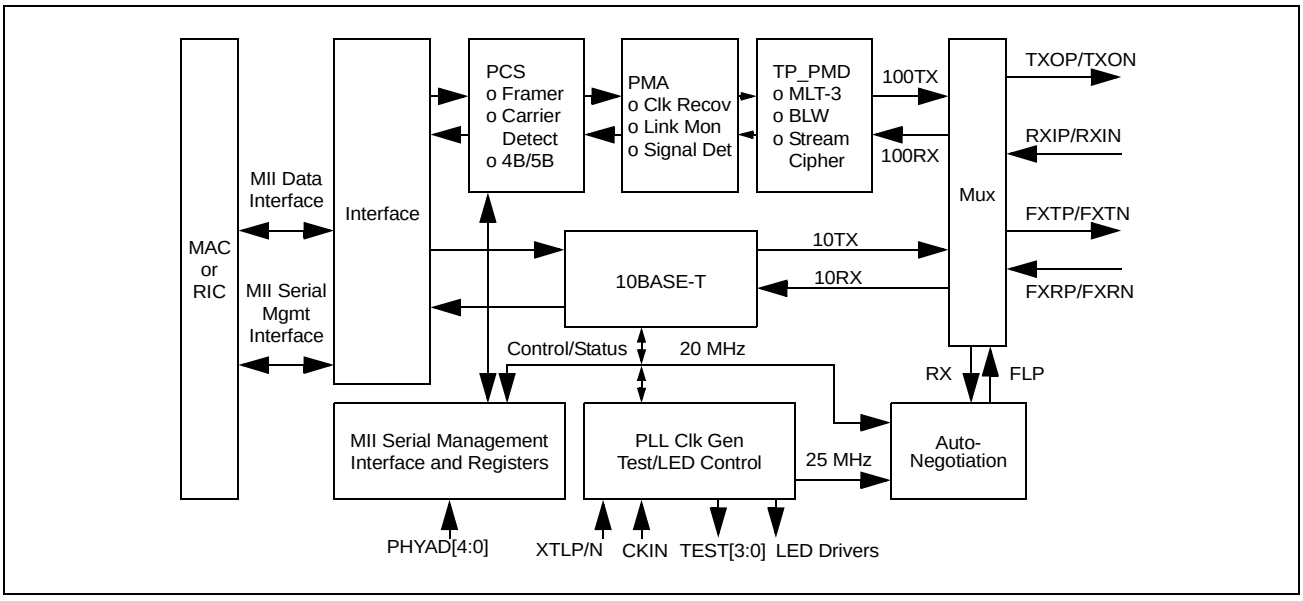

Figure 1: Functional Block Diagram

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Revision History

Revision	*Date*	*Change Description*
AC101-DS00-R	5/22/01	Initial release.
AC101-DS01-R		Changed signal names: FX_DIS, FXRP/FXRN, FXTP/FXTN, RXIP/RX-IN, and TXOP/TXON.

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OVERVIEW

The AC101TF/QF PHYsical layer device (PHY) integrates the 100BASE-X and 10BASE-T functions in a single chip that is used in Fast Ethernet 10/100 Mbps applications. The 100BASE-X section consists of physical coding sublayer (PCS), physical media attachment (PMA), and physical media dependent (PMD) functions and the 10BASE-T section consists of Manchester encoder/decoder (ENDEC) and transceiver functions. The device performs the following functions:

- 4B/5B
- MLT3
- NRZI
- Manchester Encoding and Decoding
- Clock and Data Recovery
- Stream Cipher Scrambling/De-Scrambling
- Adaptive Equalization
- Line Transmission
- Carrier Sense
- Link Integrity Monitor
- Auto-Negotiation (ANeg)
- MII MAC connectivity
- MII Management Function

It also provides an IEEE802.3u compatible Media Independent Interface (MII) to communicate with an Ethernet Media Access Controller (MAC). Selection of 10 or 100 Mbps operation is based on the settings of internal Serial Management Interface registers or determined by the on-chip ANeg logic. The device can operate in 10 or 100 Mbps with full-duplex or half-duplex mode.

MAC INTERFACE

MEDIA INDEPENDENT INTERFACE (MII)

The Media Independent Interface (MII) is an 18 wire MAC/PHY interface (see ”MII (Media Independent Interface) 100 PCS Bypass Pins” on page 12) described in 802.3u. The purpose of the interface is to allow MAC layer devices to attach to a variety of Physical Layer devices through a common interface. MII operates at either 100 Mbps or 10 Mbps, dependant on the speed of the Physical Layer. With clocks running at either 25 MHz or 2.5 MHz, 4 bit data is clocked between the MAC and PHY, synchronous with Enable and Error signals.

At the time of PLL lock on an incoming signal from the wire interface, the PHY will generate RX_CLK at either 2.5 MHz for 10 Mbps or 25 MHz for 100 Mpbs.

On receipt of valid data from the wire interface, RX_DV will go active signaling to the MAC that the valid data will be presented on the RXD[3:0] pins at the speed of the RX_CLK.

On transmission of data from the MAC, TX_EN is presented to the PHY indicating the presence of valid data on TXD[3:0]. TXD[3:0] are sampled by the PHY synchronous to TX_CLK during the time that TX_EN is valid.

Serial Management Interface (SMI)

The PHY’s internal registers are accessible only through the MII 2-wire Serial Management Interface (SMI. see ”MII (Media

Independent Interface) 100 PCS Bypass Pins" on page 12). MDC is a clock input to the PHY which is used to latch in or out data and instructions for the PHY. The clock can run at any speed from DC to 25 MHz. MDIO is a bi-directional connection used to write instructions to, write data to, or read data from the PHY. Each data bit is latched either in or out on the rising edge of MDC. MDC is not required to maintain any speed or duty cycle, provided no half cycle is less than 20ns and that data is presented synchronous to MDC.

MDC/MDIO are a common signal pair to all PHYs on a design. Therefore, each PHY needs to have its own unique Physical Address. The Physical Address of the PHY is set using the pins defined as PHYAD[4:0] (see "PHY Address Pins" on page 11). These input signals are strapped externally and sampled as reset is negated. At idle, the PHY is responsible to pull MDIO line to a high state. Therefore, a 1.5K Ohms resistor is required to connect MDIO line to Vcc. The PHYAD can be reprogrammed via software. A detailed definition of the Serial Management registers follows.

At the beginning of a read or write cycle, the MAC will send a continuous 32 bits of one at the MDC clock rate to indicate preamble. A zero and a one will follow to indicate start of frame. A read OP code is a one and a zero, while a write OP code is a zero and a one. These will be followed by 5 bits to indicate PHY address and 5 bits to indicate register address. Then 2 bits follow to allow for turn around time. For read operation, the first bit will be high impedance. Neither the PHY nor the station will assert this bit. During the second bit time, the PHY will assert this bit to a zero. For write operation, the station will drive a one for the first bit time, and a zero for the second bit time. The 16 bits data field is then presented. The first bit that is transmitted is bit 15 of the register content.

Interrupts

The INTR pin (see "MII (Media Independent Interface) 100 PCS Bypass Pins" on page 12) on the PHY will be asserted whenever one of 8 selectable interrupt events occur. Assertion state is programmable to either high or low through the INTR_LEVL register bit (see "Register 16: Polarity and Interrupt Level Register" on page 29). Selection is made by setting the appropriate bit in the upper half of the Interrupt Control/Status register (see "Register 17: Interrupt Control/Status Register" on page 30). When the INTR bit goes active, the MAC interface is required to read the Interrupt Control/Status register to determine which event caused the interrupt. The Status bits are read only and clear on read. When INTR is not asserted, the pin is held in a high impedance state.

Carrier Sense/RX_DV

Carrier sense is asserted asynchronously on the CRS pins as soon as activity is detected on the receive data stream. RX_DV is asserted as soon as a valid SSD (Start-of-Stream Delimiter) is detected. Carrier sense and RX_DV are de-asserted synchronously upon detection of a valid end of stream delimiter or two consecutive idle code groups in the receive data stream. However, if the carrier sense is asserted and a valid SSD is not detected immediately, RX_ER is asserted instead of RX_DV. See "MII (Media Independent Interface) 100 PCS Bypass Pins" on page 12.)

In 10BASE-T mode, CRS is asserted asynchronously when the valid preamble and data activity is detected on the RXIP and RXIN pins.

In the half-duplex mode, the CRS is activated during the transmit and receiving of data. In the full-duplex mode, the CRS is activated during data reception only.

7-WIRE SERIAL INTERFACE

To allow the PHY to run in legacy 10 Mbps only designs, the 7-wire serial interface, referred to as General Purpose Serial Interface (GPSI, see "10 Mbps 7-Wire Interface Pins" on page 13) has been included. GPSI is an industry standard interface which has been implemented in many micro-controllers and micro-processors, as well as the majority of the 10 Mpbs MACs.

The interface consists of 10 Mbps transmit and receive clocks, 10 Mbps serial transmit and receive data, transmit enable, receive enable and collision.

When running the GPSI mode, the PHY must be forced to 10 Mbps only mode through hardware configuration.

The 10BASE-T 7-wire interface is enabled when the GPIO[0] (see "Control and Status Pins" on page 14) is pull low by 1 KΩ during reset.

PCS BYPASS

The AC101TF/QF is put into PCS bypass mode when the PCSBP pin is pull high (see ”Control and Status Pins” on page 14).

100 Mbps PCS Bypass

In MII designs, the encoding/decoding functions are performed in the PHY, thereby allowing 4-bit data exchange. Certain designs, however, require MAC/PHY data transfer to be in the form of 5-bit symbols. By selecting PCS Bypass mode of operation, the PHY will present data to, and accept data from the MAC layer as 5-bit symbols. In PCS Bypass mode the RX_ER and TX_ER pins are used as the RXD4 and TXD4 (see ”MII (Media Independent Interface) 100 PCS Bypass Pins” on page 12).

10 Mbps PCS Bypass

When using PCS Bypass at 10 Mbps, the standard MAC/PHY interface is no longer valid. Differential drivers and receivers carry data serially between the MAC and PHY (see ”10 Mbps PCS Bypass Pins” on page 13).

MEDIA INTERFACE

The AC101TF/QF can be media-configured using any of the following three methods:

- Hardware configuration: see ”Control and Status Pins” on page 14.
- Software configuration: see ”Register 21: Mode Control Register” on page 32.
- Auto-Negotiation (ANeg): see ”Control and Status Pins” on page 14 and ”MII-Specified Registers” on page 24.

10BASE-T INTERFACE

When configured to run in 10BASE-T mode, either through hardware configuration, software configuration, or ANeg, the PHY will support all the features and parameters of the industry standards.

Transmit Function

If the MII interface is used, Parallel to Serial logic is used to convert the 4-bit data into the serial stream. If the 7-Wire interface is used (see ”10 Mbps 7-Wire Interface Pins” on page 13), the serial data goes directly to the Manchester encoder where it is synthesized through the output waveshaping driver. The waveshaper reduces any EMI emission by filtering out the harmonics, therefore eliminating the need for an external filter.

Receive Function

The received signal passes through a low-pass filter, which filters out the noise from the cable, board, and transformer. This eliminates the need for a 10BASE-T external filter. A Manchester decoder converts the incoming serial stream. If the 7-wire 10BASE-T interface is enabled (see ”10 Mbps 7-Wire Interface Pins” on page 13), the decoded serial data is presented to the MAC. If the MII interface is used (see ”MII (Media Independent Interface) 100 PCS Bypass Pins” on page 12), Serial to Parallel logic is used to generate the 4-bit data.

Link Monitor

The 10-BASE-T link-pulse detection circuit will constantly monitor the RXIP/RXIN pins (see ”MDI (Media Dependent Interface) Pins” on page 11) for the presence of valid link pulses. In the absence of valid link pules, the Link Status bit will be cleared and the Link LED will de-assert.

100BASE-TX INTERFACE

When configured to run in 100BASE-TX mode, either through hardware configuration, software configuration, or ANeg, the PHY will support all the features and parameters of the industry standards.

Transmit Function

In 100BASE-TX mode, the PHY transmit function converts synchronous 4-bit data nibbles from the MII to a pair of 125 Mbps differential serial data streams. The serial data is transmitted over network twisted pair cables via an isolation transformer. Data conversion includes 4B/5B encoding, scrambling, parallel to serial, NRZ to NRZI, and MLT-3 encoding. The entire operation is synchronous to 25 MHz and 125 MHz clock. Both clocks are generated by an on-chip PLL clock synthesizer that is locked on to an external 25 MHz clock source.

The transmit data, in 4-bit nibbles at 25 MHz rate, is transmitted from the MAC to the PHY via the MII TXD[3:0] signals. The 4B/5B encoder replaces the first two nibbles of the preamble from the MAC frame with a /J/K/ code-group pair Start-of-Stream Delimiter (SSD), following the onset of TX_EN signal. The 4B/5B encoder appends a /T/R/ code-group pair End-of-Stream Delimiter (ESD) to the end of transmission in place of the first two IDLE code-groups that follow the negation of the TX_EN signal. The encapsulated data stream is converted from 4-bit nibbles to 5-bit code-groups. During the inter-packet gap, when there is no data present, a continuous stream of IDLE code-groups are transmitted. When TX_ER is asserted while TX_EN is active, the Transmit Error code-group /H/ is substituted for the translated 5B code word. The 4B/5B encoding is bypassed when Reg. 21.1 is set to “1”, or the PCSBP pin is strapped high. See ”MII (Media Independent Interface) 100 PCS Bypass Pins” on page 12.

In 100BASE-TX mode, the 5-bit transmit data stream is scrambled as defined by the TP-PMD Stream Cipher function in order to reduce radiated emissions on the twisted pair cable. The scrambler encodes a plain text NRZ bit stream using a key stream periodic sequence of 2047 bits generated by the recursive linear function:

```
X[n] = X[n-11] + X[n-9] (modulo 2)
```

The scrambler reduces peak emissions by randomly spreading the signal energy over the transmitted frequency range, thus eliminating peaks at any single frequency. For repeater applications, where all ports transmit the same data simultaneously, signal energy is spread further by using a non-repeating sequence for each PHY (i.e., the scrambled seed is unique for each different PHY based on the PHY address).

When Dis_Scrm (see ”Register 21: Mode Control Register” on page 32) is set to “0” the data scrambling function is disabled, the 5-bit data stream is clocked directly to the device’s PMA sublayer.

Parallel to Serial, NRZ to NRZI, and MLT3 Conversion

The 5-bit NRZ data is clocked into PHY’s shift register with a 25 MHz clock and clocked out with a 125 MHz clock to convert it into a serial bit stream. The serial data is converted from NRZ to NRZI format, which produces a transition on Logic 1 and no transition on Logic 0. To further reduce EMI emissions, the NRZI data is converted to an MLT-3 signal. The conversion offers a 3dB to 6dB reduction in EMI emissions. This allows system designers to meet the FCC Class B limit. Whenever there is a transition occurring in NRZI data, there is a corresponding transition occurring in the MLT-3 data. For NRZI data, it changes the count up/down direction after every single transition. For MLT-3 data, it changes the count up/down direction after every two transitions. The NRZI to MLT-3 data conversion is implemented without reference to the bit timing or clock information. The conversion requires detecting the transitions of the incoming NRZI data and setting the count up/down direction for the MLT-3 data. Asserting FX_SEL high will disable this encoding.

The slew rate of the transmitted MLT-3 signal can be controlled to reduce EMI emissions. The MLT-3 signal after the magnetic has a typical rise/fall time of approximately 4 ns, which is within the target range specified in the ANSI TP- PMD standard. This is guaranteed with either 1:1 or 1.25:1 transformer.

Receive Function

The 100BASE-TX receive path functions as the inverse of the transmit path. The receive path includes a receiver with adaptive equalization and DC restoration in the front end. It also includes a MLT-3 to NRZI converter, 125 MHz data and clock recovery, NRZI/NRZ conversion, Serial-to-Parallel conversion, de-scrambler, and 5B/4B decoder. The receiver circuit starts with a DC bias for the differential RX+/- inputs, followed with a low-pass filter to filter out high frequency noise from the transmission channel media. An energy detect circuit is also added to determine whether there is any signal energy on the media. This is useful in the power-saving mode. The amplification ratio and slicer’s threshold is set by the on-chip bandgap reference.

Baseline Wander Compensation

The 100BASE-TX data stream is not always DC balanced. The transformer blocks the DC components of the incoming signal, thus the DC offset of the differential receive inputs can drift. The shifting of the signal level, coupled with non-zero rise and fall times of the serial stream can cause pulse-width distortion. This creates jitter and possible increase in the bit error rates. Therefore, a DC restoration circuit is needed to compensate for the attenuation of the DC component. This PHY implements a patent-pending DC restoration circuit. Unlike the traditional implementation, the circuit does not need the feedback information from the slicer or the clock recovery circuit. This design simplifies the circuit design and eliminates any random/systematic offset on the receive path. In the 10BaseT and the 100BASE-FX modes, the baseline wander correction circuit is not required, and therefore is disabled.

Clock/Data Recovery

The equalized MLT-3 signal passes through the slicer circuit, and gets converted to NRZI format. The PHY uses a proprietary mixed-signal phase locked loop (PLL) to extract clock information from the incoming NRZI data. The extracted clock is used to re-time the data stream and set the data boundaries. The transmit clock is locked to the 25 MHz clock input while the receive clock is locked to the incoming data streams. When initial lock is achieved, the PLL switches to the data stream, extracts the 125 MHz clock, and uses it for the bit framing for the recovered data. The recovered 125 MHz clock is also used to generate the 25 MHz RX_CLK signal. The PLL requires no external components for its operation and has high noise immunity and low jitter. It provides fast phase alignment and locks to data in one transition. Its data/clock acquisition time after power-on is less than 60 transitions. The PLL can maintain lock on run-lengths of up to 60 data bits in the absence of signal transitions. When no valid data is present, i.e. when the SD is de-asserted, the PLL will switch and lock on to TX_CLK. This provides a continuously running RX_CLK. At the PCS interface, the 5 bit data RXD[4:0] is synchronized to the 25 MHz RX_CLK. See ”MII (Media Independent Interface) 100 PCS Bypass Pins” on page 12.

Decoder/De-scrambler

The de-scrambler detects the state of the transmit Linear Feedback Shift Register (LFSR) by looking for a sequence representing consecutive idle codes. The de-scrambler acquires lock on the data stream by recognizing IDLE bursts of 30 or more bits and locks its frequency to its de-ciphering LFSR.

Once lock is acquired, the device can operate with an inter-packet-gap (IPG) as low as 40 nS. However, before lock is acquired, the de-scrambler needs a minimum of 270 nS of consecutive idles in between packets in order to acquire lock.

The de-ciphering logic also tracks the number of consecutive errors received while the RX_DV (see ”MII (Media Independent Interface) 100 PCS Bypass Pins” on page 12) is asserted. Once the error counter exceeds its limit currently set to 64 consecutive errors, the logic assumes that the lock has been lost, and the de-cipher circuit resets itself. The process of regaining lock will start again.

Stream cipher de-scrambler is not used in the 100BASE-FX and the 10BASE-T modes.

Link Monitor

Signal level is detected through a squelch detection circuitry. A signal detect (SD) circuit allows the equalizer to assert high whenever the peak detector detects a post-equalized signal with peak to ground voltage greater than 400 mV. This is approximately 40% of a normal signal voltage level. In addition, the energy level must be sustained for longer than 2~3 µS in order for the signal detect signal to stay on. The SD gets de-asserted approximately 1~2 µs after the energy level drops consistently below 300 mV from peak to ground.

The link signal is forced low during a local loopback operation (Loopback register bit is set) and forced to high when a remote loopback is taking place (EN_RPBK is set, see ”Register 21: Mode Control Register” on page 32).

In forced 100BASE-TX mode, when a cable is unplugged or no valid signal is detected on the receive pair, the link monitor enters in the “link fail” state and NLP's are transmitted. When a valid signal is detected for a minimum period of time, the link monitor enters Link Pass State and transmits MLT-3 signal.

100BASE-FX INTERFACE

When configured to run in 100BASE-FX mode, either through hardware configuration or software configuration (100BASE-FX does not support ANeg) the PHY will support all the features and parameters of the industry standards.

Transmit Function

The serialized data bypasses the scrambler and 4B/5B encoder in FX mode. The output data is NRZI PECL signals. The PECL level signals are used to drive the Fiber-transmitter.

Receive Function

In 100BASE-FX mode, signal is received through the PECL receiver inputs, and directly passed to the clock recovery circuit for data/clock extraction. In FX mode, the scrambler/de-scrambler cipher function is bypassed.

Link Monitor

In 100BASE-FX mode, the external fiber-optic receiver performs the signal energy detection function and communicates this information directly to the PHY's SDP pin (see "MDI (Media Dependent Interface) Pins" on page 11).

Far-End-Fault-Insertion (FEFI)

ANeg provides the mechanism to inform the link partner that a remote fault has occurred. However, ANeg is disabled in the 100BASE-FX applications. An alternative in-band signaling function (FEFI) is used to signal a remote fault condition. FEFI is a stream of 84 consecutive ones followed by one logic zero. This pattern is repeated 3 times. A FEFI will signal under 3 conditions:

1 When no activity is received from the link partner.

2 When the clock recovery circuit detects a signal error or PLL lock error.

3 When management entity sets the transmit Far-End-Fault bit.

The FEFI mechanism is enabled by default in the 100BASE-FX mode, and is disabled in 100BASE-TX or 10BASE-T modes. The register setting can be changed by software after reset.

10BASE-T/100BASE-TX/FX INTERFACE

Multi-Mode Transmit Driver

The multi-mode driver transmits the MLT-3 coded signal in 100BASE-TX mode, NRZI coded signal in 100BASE-FX mode, and Manchester coded signal in 10BASE-T mode.

In 100BASE-FX mode, no filtering is performed. The transmit driver utilizes a current drive output which is well balanced and produces a low noise PECL signal. PECL voltage levels are produced with resistive terminations. (See section 16.)

In 10BaseT mode, high frequency pre-emphasis is performed to extend the cable-driving distance without the external filter. The FLP and NLP pulses are also drive out through the 10BaseT driver.

The 10BaseT and 100BaseTX transmit signals are multiplexed to the transmit output driver. This arrangement results in using the same external transformer for both the 10BaseT and the 100BaseTX. The driver output level is set by a built-in band-gap reference and an external resistor connected to the RIBB pin (see "Special/Test Pins" on page 14). The resistor sets the output current for all modes of operation. The TXOP/N outputs (see "MDI (Media Dependent Interface) Pins" on page 11) are open drain devices with serial source to I/O pad resistance of 10 Ω maximum. When the 1:1 transformer is used, the current rating is 40 mA for the $2V_{p-p}$ MLT-3 signal, and 100 mA for the $5V_{p-p}$ Manchester signal. One can use a 1.25:1 transmit transformer for a 20% output driver power reduction. This will decrease the drive current to 32 mA for 100BASE-TX operation, and 80 mA for 10BASE-T operation.

Adaptive Equalizer

The PHY is designed to accommodate a maximum of 150 meters UTP CAT-5 cable. An AT&T 1061 CAT-5 cable of this length typically has an attenuation of 31 dB at 100 MHz. A typical attenuation of 100-meter cable is 21 dB. The worst case cable attenuation is around 24-26 dB as defined by TP-PMD specification.

The amplitude and phase distortion from the cable cause inter-symbol interference (ISI) which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pair cable. The equalizer has the ability to changes its equalizer frequency response according to the cable length. The equalizer will tune itself automatically for any cable, compensating for the amplitude and phase distortion introduced by the cable.

PLL Clock Synthesizer

The PHY includes an on-chip PLL clock synthesizer that generate 25 MHz and 125 MHz clocks for the 100BASE-TX circuitry. It also generates 20 MHz and 100 MHz clocks for the 10BaseT and ANeg circuitry. The PLL clock generator uses a fully differential VCO cell that introduces very low jitter. The Zero Dead Zone Phase Detection method implemented in the PHY design provides excellent phase tracking. A charge pump with charge sharing compensation is also included to further reduce jitter at different loop filter voltages. The on-chip loop filter eliminates the need for external components and minimizes the external noise sensitivity. Only one external 25 MHz crystal or clock source is required as a reference clock.

After power-on or reset, the PLL clock synthesizer generates the 20 MHz clock output until the 100BASE-X operation mode is selected.

Jabber and SQE (Heartbeat)

After the MAC transmitter exceeds the jabber timer (46mS), the transmit and loopback functions will be disabled and COL signal get asserted. After TX_EN goes low for more than 500 ms, the TP transmitter will reactivate and COL gets de-asserted. Setting Jabber Disable will disable the jabber function.

When the SQE test is enabled, a COL pulse with 5-15BT is asserted after each transmitted packet. SQE is enabled in 10BASE-T by default, and can be disabled via SQE Test Inhibit.

Reverse Polarity Detection and Correction

Certain cable plants have crossed wiring on the twisted pairs; the reversal of TXIN and TXIP. Under normal circumstances this would cause the receive circuitry to reject all data. When the Auto Polarity Disable bit (see ”Register 16: Polarity and Interrupt Level Register” on page 29) is cleared, the PHY has the ability to detect the fact that either 8 NLPs or a burst of FLPs are inverted and automatically reverse the receiver’s polarity. The polarity state is stored in the Reverse Polarity bit.

If the Auto Polarity Disable bit is set, then the Reverse Polarity bit (see ”Register 16: Polarity and Interrupt Level Register” on page 29) can be written to force the polarity reversal of the receiver.Initialization and Setup

HARDWARE CONFIGURATION

Several different states of operation can be chosen through hardware configuration. External pins may be pulled either high or low at reset time (see ”Control and Status Pins” on page 14). The combination of high and low values determines the power on state of the device.

Many of these pins are multi-function pins which change their meaning when reset ends.

SOFTWARE CONFIGURATION

Several different states of operation can be chosen through software configuration. Please refer to ”Serial Management Interface (SMI)” on page 1 and Section 4 ”Register Descriptions” on page 23.

LED Outputs

Individual LED outputs are available to indicate Speed, Duplex, Collision, Receive, Transmit, and Link. These multi-function pins are inputs during reset and LED output pins thereafter. The level of these pins during reset determines their active out-

put states. If a multi-function pin is pulled up during reset to select a particular function, then that LED output would become active low, and the LED circuit must be designed accordingly, and vice versa.

In addition to the individual LED configurations, an advanced LED circuit has been implemented, as illustrated in ”Advanced LED Selections” on page 19.

AUTO-NEGOTIATION

By definition the 10/100 Transceiver is able to run at either 10 Mbps over Twisted Pair Copper (10BASE-T), 100 Mpbs over Twisted Pair Copper (100BASE-TX) or 100 Mpbs over Fiber Optics (100BASE-FX). In addition the PHY is able to run in either half-duplex (repeater mode) or full-duplex. To determine the operational state, the PHY has hardware selects and software selects while also supporting Auto- Negotiation and Parallel Detection. To run in 100BASE-FX mode, the selection must be done through hardware configuration. There is no support for Auto-Negotiation of the FX interface.

Not all of the above combinations are possible due to limitations of the environment and the 802.3 standards. Legitimate operating states are:

- 10BASE-T Half-duplex
- 10BASE-T Full-duplex
- 100BASE-TX Half-duplex
- 100BASE-TX Full-duplex
- 100BASE-FX Half-duplex
- 100BASE-FX Full-duplex

The PHY can be hardware configured to force any one of the above mentioned modes (see ”Control and Status Pins” on page 14). By forcing the mode, the PHY will only run in that mode, hence limiting the locations where the product will operate.

The PHY is able to negotiate its mode of operation in the twisted pair environment using the Auto-Negotiation mechanism defined in the clause 28 of IEEE 802.3u specification. ANeg can be enabled or disabled by hardware (ANEGA pin) or software (Reg. 0.12) control. When the ANeg is enabled, the PHY chooses its mode of operation by advertising its abilities and comparing them with the ability received from its link partner. It can be configured to advertise 100BASE-TX or 10BASE-T operating in either full or half-duplex.

Register 4 (see ”Register 4: Auto-Negotiation Advertisement Register” on page 26) contains the current capabilities, speed and duplex, of the PHY, determined through hardware selects (TECH[2:0], see ”Control and Status Pins” on page 14) or chip defaults. The contents of Reg. 4 is sent to its link partner during the ANeg process using Fast Link Pulses (FLPs). An FLP is a string of 1s and 0s, each of which has a particular meaning, the total of which is called a Link Code Word. After reset, software can change any of these bits from 1 to 0 and back to 1, but not from 0 to 1. Therefore, the hardware has priority over software.

When ANeg is enabled, the PHY sends out FLPs during the following conditions:

- Power on
- Link loss
- Restart command

During this period, the PHY continually sends out FLPs while monitoring the incoming FLPs from the link partner to determine their optimal mode of operation. If FLPs are not detected during this phase of operation, Parallel Detection mode is entered (see ”Parallel Detection” on page 9).

When the PHY receives 3 identical link code words (ignoring acknowledge bit) from its link partner, it stores these code words in Reg. 5 (see ”Register 5: Auto-Negotiation Link Partner Ability Register” on page 27), sets the acknowledge bit it the generated FLPs, and waits to receive 3 identical code word with the acknowledge bit set from the link partner. Once this occurs the PHY configures itself to the highest technology that is common to both ends.

The technology priorities are:

1 100BASE-TX, full-duplex

2 100BASE-TX, half-duplex

3 10BASE-T, full-duplex

4 10BASE-T half-duplex

Once the ANeg is complete, Reg. 1.5 is set, Reg. 1.[14:11] reflects negotiated speed and duplex mode, and the PHY enters the negotiated transmission and reception state. This state will not change until link is lost or the PHY is reset through either hardware or software, or the restart negotiation bit (Reg. 0.9) is set. See ”Register 0: Control Register” on page 24 and ”Register 1: Status Register” on page 25.

PARALLEL DETECTION

Because there are many devices in the field that do not support the ANeg process, but must still be communicated with, it is necessary to detect and link through the Parallel Detection process.

The parallel detection circuit is enabled in the absence of FLPs. The circuit is able to detect:

- Normal Link Pulse (NLP)
- 10BASE-T receive data
- 100BASE-TX idle

The mode of operation gets configured based on the technology of the incoming signal. If any of the above is detected, the device automatically configures to match the detected operating speed in the half-duplex mode. This ability allows the device to communicate with the legacy 10BASE-T and 100BASE-TX systems, while maintaining the flexibility of Auto-Negotiation.

DIAGNOSTICS

Loopback Operation

Local Loopback and Remote Loopback are provided for testing purpose. They can be enabled by write to either Reg. 0.14 (LPBK) or Reg. 21.3 (EN_RPBK). See ”Register 0: Control Register” on page 24 and ”Register 21: Mode Control Register” on page 32.

The Local Loopback routes transmitted data through the transmit path back to the receiving path’s clock and data recovery module. The loopback data are presented to the PCS in 5 bits symbol format. This loopback is used to check the operation of the 5-bit symbol decoder and the phase locked loop circuitry. In Local Loopback, the SD output is forced to logic one and TXOP/N outputs are tri-stated.

In Remote Loopback, incoming data is passed through the equalizer and clock recovery, then looped back to the NRZI/MLT3 converter and then to the transmit driver. This loopback is used to ensure the device’s connection on the media side. It also checks the operation of the device's internal adaptive equalizer, phase locked loop circuit, and wave-shaper synthesizer. During Remote Loopback, signal detect (SD) output is forced to logic zero.

Cable Length Indicator

The PHY can detect the length of the cable it’s attached and display the result in Reg. 20.[7:4] (see ”Register 20: Cable Measurement Register” on page 31). A reading of [0000] translates to < 10m cable used, [0001] translates to ~ 10 meter of cable, and [1111] translates to 150 meter cable. The cable length value can be used by the network manage to determine the proper connectivity of the cable and to manage the cable plant distribution

RESET AND POWER

The PHY can be reset in three ways:

1 During initial power on.

2 Hardware Reset: (See pin descriptions).

3 Software Reset: (See register descriptions).

The power consumption of the device is significantly reduced due to its built-in power management features. Separate power supply lines are used to power the 10BaseT circuitry and the 100BaseTX circuitry. Therefore, the two circuits can be turned-on and turned-off independently. When the PHY is set to operate in 100BASE-TX mode, the 10BASE-T circuitry is powered down, and vice versa.

The following power management features are supported:

1 Power down mode: (See Section 2 ”Signal Definitions and Pin Assignments” on page 11 and Section 4 ”Register Descriptions” on page 23). During power down mode, the device is still be able to interface through the management interface.

2 Energy detect/power saving mode: Energy detect mode turns off the power to select internal circuitry when there is no live network connected. Energy Detect (ED) circuit is always turned on to monitor if there is a signal energy present on the media. The management circuitry is also powered on and ready to respond to any management transaction. The transmit circuit still send out link pulses with minimum power consumption. If a valid signal is received from the media, the device will power up and resume normal transmit/receive operation.

3 Valid data detection mode: This can be achieved by writing to the Receive Clock Register Control Bit. During this mode, if there is no data other than idles coming in, the receive clock (RX_CLK, see ”MII (Media Independent Interface) 100 PCS Bypass Pins” on page 12) will turn off. This could save the power of the attached media access controller. RX_CLK will resume operation one clock period prior to the assertion of RX_DV. The receive clock will again shut off 64 clock cycles after RX_DV gets de-asserted.

4 Reduced Transmit Drive Strength mode: Additional power saving can be gained at the PHY level by designing with 1.25:1 turns ration magnetic (see pin and register descriptions).

CLOCK INPUT

The clock input (see ”Special/Test Pins” on page 14) can be either a TTL clock oscillator or a crystal measured at 25 MHz-100PPM.

Section 2: Signal Definitions and Pin Assignments

Many of the pins of these devices have multiple functions. The multi-function pins will be designated by **bolding** of the pin number. The separate descriptions of these pins will be listed in the proper sections. Designers must assure that they have identified all modes of operation prior to final design.

The signal types in this section are designated as follows:

- I = inputs
- O = outputs
- Z = high impedance
- U = pull up
- D = pull down
- A = analog signal
- * = Active Low Signal
- NC = No Connect pin
- P = Power
- G = Ground

PIN DESCRIPTIONS

PHY ADDRESS PINS

Table 1: PHY Address Pins

Pin Name	*101TF*	*101QF*	*Type*	*Description*
PHYAD [4]	**14**	**19**	I/O, U	PHY Address. Allows 31 configurable PHY addresses. The PHYAD will also determine the scramble seed; this will help reduce EMI emission when there are multiple ports switching at the same time (repeater/ switch applications).
PHYAD [3]	**15**	**20**	I/O, U	
PHYAD [2]	**16**	**21**	I, U	
PHYAD [1]	**17**	**22**	I, U	
PHYAD [0]	**18**	**23**	I, U	

MDI (MEDIA DEPENDENT INTERFACE) PINS

Table 2: MDI (Media Dependent) Pins

Pin Name	*101TF*	*101QF*	*Type*	*Description*
RXIN	63	83	AI	Receiver input positive and negative for both 10BASE-T and 100BASE-TX.
RXIP	64	84		
TXOP	77	97	AO	Transmitter output positive and negative for both 10BASE-T and 100BASE-TX.
TXON	78	98		

Table 2: MDI (Media Dependent) Pins (Cont.)

Pin Name	101TF	101QF	Type	Description
FXRN	**66**	**86**	AO/AI	Receive input positive and negative for 100BASE-FX when FX_DIS pin is pulled low.
FXRP	**67**	**87**	AO/AI	
FXTP	69	89	AO	Transmit output positive and negative for 100BASE-FX when FX_DIS pin is pulled low.
FXTN	70	90	AO	
SDP	**62**	**82**	AO/AI	Signal Detect input from Fiber-optic transceiver when FX_DIS pin is pulled low

MII (MEDIA INDEPENDENT INTERFACE) 100 PCS BYPASS PINS

Outputs tri-state during MII isolation.

Table 3: MII (Media Independent Interface) 100 PCS Bypass Pins

Pin Name	101TF	101QF	Type	Description
MDIO	21	31	I/O, U	Management Data Input/Output. Bi-directional data interface. A 1.5K pull up resistor is required (as specified in IEEE-802.3).
MDC	22	32	I	Management Data Clock. 0 to 25 MHz clock sourced by the MAC for transfer of MDIO data.
RXD [3]	23	33	O, Z	MII received data. The data is synchronous with RX_CLK when RX_DV is active.
RXD [2]	24	34		
RXD [1]	25	35		
RXD [0]	**26**	**36**		PCS Bypass RXD[3:0]
RX_DV	29	39	O, Z	Receive Data Valid. Asserted high when valid data is present on the RX[3:0]. In 100Base mode, it is asserted with the first nibble of preamble and is de-asserted when the last data nibble has been received. In 10Base mode, it is asserted when the SFD (Start-of-Frame) delimiter is detected and de-asserted at end of data.
RX_CLK	**30**	**40**	O, Z	Receive Clock. A continuous clock which provides timing reference for RX_DV, RX_ER and RXD[3:0] signals. 25 MHz in 100Base and 2.5 MHz in 10Base. To reduce system power consumption RX_CLK is held inactive (low) when no data is received and Reg. 16.0 is enabled.
RX_ER	31	41	O, Z	MII Receive Error. Active high to indicate an error has been detected during frame reception during 100Base mode.
RXD[4]				PCS Bypass RXD[4]
TX_ER	32	42	I	MII Transmit Error. When TX_ER is asserted, it will cause the 4B/5B encoding process to substitute the transmit error code-group /H/ for the encoded data word during 100Base mode.
TXD[4]				PCS Bypass TXD[4]
TX_CLK	**33**	**43**	O, Z	Transmit Clock. A continuous clock which provides timing reference for TX_EN, TX_ER and TXD[3:0] signals. It is 25 MHz in 100Base and 2.5 MHz in 10Base.
TX_EN	**34**	**44**	I	Transmit Enable. TX_EN is asserted by the MAC to indicate that valid data is present on TXD[3:0].

Table 3: MII (Media Independent Interface) 100 PCS Bypass Pins (Cont.)

Pin Name	101TF	101QF	Type	Description
TXD [3]	40	50	I	Transmit Data. The MAC will source TXD[3:0] synchronous with TX_CLK when TX_EN is asserted.
TXD [2]	39	49		
TXD [1]	38	48		PCS Bypass TXD[3:0]
TXD [0]	**37**	**47**		
COL	**41**	**56**	O, Z	Collision. COL is asserted high when a collision is detected on the media.
CRS	**42**	**57**	O, Z	Carrier Sense. CRS is asserted high when twisted pair media is non-idle.
INTR	43	58	O, Z	Interrupt. See Registers 16 and 17 for polarity and sources. The INTR pin has a high impedance output, a 1K Ω pull-up or pull-down resistor is needed.

10 MBPS PCS BYPASS PINS

Table 4: 10 Mbps PCS Bypass Pins

Pin Name	101TF	101QF	Type	Description
TP_RD-	**14**	**19**	I/O, U	10BASE-T serial input and output. The ANeg function is disabled, therefore, the MAC is responsible for generating FLP and performing media arbitration.
TP_RD+	**15**	**20**	I/O, U	
TP_TD++	**16**	**21**	I, U	
TP_TD--	**19**	**24**	I, U	
TP_TD+	**17**	**22**	I, U	
TP_TD-	**18**	**23**	I, U	

10 MBPS 7-WIRE INTERFACE PINS

Table 5: 10 Mbps 7-Wire Interface Pins

Pin Name	101TF	101QF	Type	Description
10RD	**26**	**36**	O, Z	Receive Data. 10 MHz serial data output.
10RCLK	**30**	**40**	O, Z	10 MHz receive clock.
10TCLK	**33**	**43**	O, Z	10 MHz transmit clock. (10TCLK goes idle 5 seconds after link drop.)
10TXEN	**34**	**44**	I	Transmit enable.
10TD	**37**	**47**	I	Transmit Data. 10 MHz serial data input.
10COL	**41**	**56**	O, Z	Collision. COL is asserted high when a collision is detected on the media
10CRS	**42**	**57**	O, Z	Carrier Sense. CRS is asserted high when twisted pair media is active.

SPECIAL/TEST PINS

Table 6: Special/Test Pins

Pin Name	101TF	101QF	Type	Description
CLK25	6	11	O	CLK25 provides a continuous 25 MHz clock if CLK25EN is asserted during reset.
Reserved	7	12	I, D	
TEST0 **TEST1** TEST2 **TEST3**	**66** **67** 68 **62**	**86** **87** 88 **82**	AO/AI AO/AI AO AO/AI	TEST [3:0] pins are used as the test-mode output monitor pin. Internal pull-down in normal 100BASE-TX or 10BASE-T mode.
RST*	8	13	I, U	Reset. An active low input will force a known initialization state. The reset pulse duration must be > 150 us. Setting MII Reg. 0.15 (see "Register 0: Control Register" on page 24) will assert software reset, which has the same functionality as the hardware reset.
PWRDN	9	14	I, D	Power Down. Driving this pin high will power down the device's analog modules and reset the device's digital circuits. The device still responds to the management MDC/MDIO data. Power-down mode can also be achieved by setting MII Reg. 0.11 (see "Register 0: Control Register" on page 24).
RIBB	72	92	A	Reference Bias Resistor. To be tied to analog ground through an external 10.0 K (1%) resistor.
CKIN	5	10	I, D	Clock Input. Connects to a 25 MHz clock source. When a crystal input is used, this pin should be tied low to ground via 1K Ω.
XTLN XTLP	74 75	94 95	AI	Crystal inputs. To be connected to a 25 MHz crystal. CKIN should be tied low when the crystal is used as a clock source.

CONTROL AND STATUS PINS

Table 7: Control and Status Pins

Pin Name	101TF	101QF	Type	Description
ISODEF	2	7	I, D	Isolate Default. If pulled high during reset, the MII interface will be tri-stated for use with multiple PHYs in a single MAC. The status of this pin will be latched in to Register 0.10 (see "Register 0: Control Register" on page 24).
ISO	3	8	I, D	Isolate. The MII output pins assume high impedance state when ISO is asserted high. However, the MII input pins still respond to data. This allows multiple PHYs to be attached to the same MII interface. The same isolate condition can also be achieved by setting MII Reg. 0.10 (see "Register 0: Control Register" on page 24). In repeater mode, ISO will not tri-state CRS pin (see "MII (Media Independent Interface) 100 PCS Bypass Pins" on page 12).

Table 7: Control and Status Pins (Cont.)

Pin Name	101TF	101QF	Type	Description
TECH [2] /DUPLEX TECH[1] /SPDSEL TECH[0] /LINK_BT	53 54 55	68 69 70	I, U I, U I, U	Technology Select. • When ANEGA pin is set to high, TECH[2:0] will then set the negotiable capabilities. (See "Technology Selections" on page 18.) • When ANEGA is set to low, TECH[2:0] will then set the forced capabilities. (See "Technology Selections" on page 18.) When the PHY is in PCS bypass mode (PCSBP pin pull high), TECH[2:0] are as follows: • TECH[0] is 10BaseT Link input (High Active). The MAC is responsible for ANeg, and creates 10BaseT Link signal. • TECH[1] is SPDSEL for the SYMBOL interface. When it is de-asserted, only the 10BaseT driver is used to transmit 10BASE-T signals, NLP and FLP. • TECH[2] is DUPLEX. The MAC is responsible for indicating the duplex operation mode. The input values of TECH[2] and TECH[0] in this mode are used for LED display only.
ANEGA	**56**	**71**	I, U	Auto-Negotiation Ability. ANeg is enabled when this pin is pulled high. When this pin is pulled low, mode of operation is depended on TECH[2:0]. This pin also controls the ANEGA bit in MII Reg.1.3.
ACTIVITY	**56**	**71**	I, U	Activity. In PCS bypass mode (PCSBP pin pull high), the MAC provides the activity signal to generate the activity LED signal.
RPTR	61	81	I	Repeater Mode. When this pin is asserted high via 1 K Ω, repeater mode will be enabled. In repeater mode, CRS becomes receive activity. SQE test function is disabled in 10BASE-T mode. Repeater mode can also enabled via MII Reg. 16.15. Requires a pull down of 1 K Ω resistor when used in NIC applications.
PCSBP	1	6	I, D	PCS Bypass. 100BASE-TX or 10BASE-T enter PCS bypass if PCSBP is asserted high at reset.
GPIO[0] **7W***	**19**	**24**	I/O, U	General Purpose I/O. These pins can be configured as either an input or output by the management Reg. 16.[6]. 7W - If the GPIO[0] is pull low by 1 KΩ during reset, the 10BASE-T 7-wire interface is enabled.
GPIO[1] TP125	20	25	I/O, D	General Purpose I/O. These pins can be configured as either an input or output by the management Reg. 16.[8]. In MII mode, GPIO[1] is used to select the 10BASE-T operation mode. With internal pull down, the device defaults to standard MII interface for 10BASE-T after reset. TP125 - If the GPIO[1] pin is pulled high by a 1 KΩ resistor during Reset, the 1.25:1 transformer ratio transmitter is enabled. A 1:1 type transformer is selected by default.

LED INDICATORS PINS

Table 8: LED Indicator Pins

Pin Name	*101TF*	*101QF*	*Type*	*Description*
LEDBTX*	**44**	**59**	I/O, U	LEDBTX - 100BASE-X LED. Active low indicates 100BASE-TX, active high indicates 10BaseT.
LEDBTA				LEDBTA **-** This pin is to be used in conjunction with LEDBTB pin that drives a 10BASE-T status LED. The LEDBTA/B pins are enabled if LED-SEL pin is pulled low during reset. (See ”Advanced LED Selections” on page 19.)
FX_DIS				FX_DIS - FX mode De-select. 100BASE-FX mode is selected if this pin is pulled low via 1K Ω resistor. This pin has an internal pull up, and is defaulted to have the FX mode not selected after reset.
LEDCOL	**45**	**60**	I/O, U	LEDCOL - Collision LED. This pin will toggle between high and low when there is a collision in half-duplex mode. It is inactive in full-duplex mode.
SCRAM_EN*				SCRAM_EN - When this pin is pulled low via 1 K Ω during reset the scrambler/de-scrambler function will be disabled.
LEDRX*	**46**	**61**	I/O, U	LEDRX - Receive LED. This pin will toggle between high and low when data is received.
LEDSEL				LEDSEL - When this pin is pulled down by a 1 K Ω during reset the LEDBTA, LEDBTB, LEDTXA, and LEDTXB can be used to drive dual-color LEDs. (See ”Advanced LED Selections” on page 19.)
LEDTX*	**47**	**62**	O	LEDTX - Transmit LED. This pin will toggle between high and low when data is transmitted.
LEDBTB				LEDBTB - This pin is to be used in conjunction with the LEDBTA pin that drives a 10B-T status LED. The LEDBTA/B pins are enabled if the LED-SEL pin is pulled low during reset. (See ”Advanced LED Selections” on page 19.)
LEDL*	**48**	**63**	O	LEDL - Link LED. Active low when link is established.
10LSTA				10LSTA - When operating in 10BASE-T 7-wire serial mode, this pin indicates Link Status (Active High).
SD				SD - When the PHY is in PCS bypass mode, this pin is used to indicate Signal Detect (Active High) for symbol interface. This pin is also active high when link is established in PCSBP 100B-TX operation.

Table 8: LED Indicator Pins (Cont.)

Pin Name	101TF	101QF	Type	Description
LEDBT*	**57**	**72**	I/O, U	LEDBT - 100BASE-X LED output. Active low indicates 10BaseT, high indicates 100BASE-TX.
LEDTXA				LEDTXA - This pin is to be used in conjunction with LEDTXB pin that drives a 100B-T status LED. The LEDTXA/B pin is enabled if the LEDSEL pin is pulled low during reset. (See ”Advanced LED Selections” on page 19.)
CLK25EN*				CLK25EN* - To enable the CLK25 output, pull this pin low with 1 KΩ.
LEDFDX*	**58**	**73**	O	LEDFDX - Full-duplex LED. Active low indicates full-duplex, high indicates half-duplex.
LEDTXB				LEDTXB - This pin is to be used in conjunction with the LEDTXA pin that drives a 100B-T status LED. The LEDTXA/B pin is enabled if the LEDSEL pin is pulled low during reset. (See ”Advanced LED Selections” on page 19.)

POWER AND GROUND PINS

Table 9: Power and Ground Pins

	101TF	101QF	Type	Description
Power Pins				
VAAPLL	10	15	P	3.3V power supply for PLL.
OVDD	13, 49	18, 64	P	3.3V power supply for I/O.
CVDD	27, 36	37, 46	P	3.3V power supply for digital logic.
VAACRV	52	67	P	3.3V power supply for clock recovery.
VAAEQ	59, 60	74, 75	P	3.3V power supply for Equalizer.
VAAREF	73	93	P	3.3V power supply for Bandgap reference.
VAAT	79, 80	99, 100	P	3.3V power supply for transmit driver.
Ground Pins				
GNDPLL	11	16	G	Ground for VAAPLL.
OGND	12, 50	17, 65	G	Ground for OVDD.
CGND	28, 35	38, 45	G	Ground for CVDD.
GNDCRV	51	66	G	Ground for VAACRV.
GNDEQ	65	85	G	Ground for VAAEQ.
GNDREF	71	91	G	Ground for VCCREF.
GNDT	4, 76	9, 96	G	Ground for VCCT.

NO CONNECT PINS

Table 10: No Connect Pins

Pin Name	101TF	101QF	Type	Description
NC		1, 2, 3, 4, 5, 26, 27, 28, 29, 30, 51, 52, 53, 54, 55, 76, 77, 78, 79, 80	NC	No Connect pin

TECHNOLOGY SELECTIONS

Table 11: Technology Solutions

ANEGEN	TECH[2:0]	Reg1[14:11]	Reg4[8:5]	Reg0.13	Reg0.8
0	x00	1111	1111	Decide by SMI input (Write-able)	Decide by SMI input (Writeable)
0	001	0001	0001	0 (Not Write-able)	0 (Not Write-able)
0	01x	0100	0100	1 (Not Write-able)	0 (Not Write-able)
0	101	0010	0010	0 (Not Write-able)	1 (Not Write-able)
0	11x	1000	1000	1(Not Write-able)	1 (Not Write-able)
1	x00	0000	0000	1 (writable, ignored)	0 (writable, ignored)
1	001	0001	0001	1 (writable, ignored)	0 (writable, ignored)
1	010	0100	0100	1 (writable, ignored)	0 (writable, ignored)
1	011	0101	0101	1 (writable, ignored)	0 (writable, ignored)
1	101	0011	0011	1 (writable, ignored)	0 (writable, ignored)
1	110	1100	1100	1 (writable, ignored)	0 (writable, ignored)
1	111	1111	1111	1 (writable, ignored)	0 (writable, ignored)

ADVANCED LED SELECTIONS

Table 12: Advanced LED Selections

Condition	10BASE-T LED			100BASE-TX LED		
	LEDBTA	LEDBTB	LED color	LEDTXA	LEDTXB	LED color
No Link	0	0	Off	0	0	Off
10B-T HDX Link	1	0	Yellow	0	0	Off
10B-T HDX RX	**Flashing**	0	**Yellow**	0	0	Off
10B-T FDX DX Link	0	1	Green	0	0	Off
10B-T FDX RX	0	**Flashing**	**Green**	0	0	Off
100B-TX HDX Link	0	0	Off	1	0	Yellow
100B-TX HDX RX/TX	0	0	Off	**Flashing**	0	**Yellow**
100B-TX FDX Link	0	0	Off	0	1	Green
100B-TX FDX RX	0	0	Off	0	**Flashing**	**Green**

Note **In HDX mode, the 'A'LED may blink off if RX and TX occur simultaneously.**

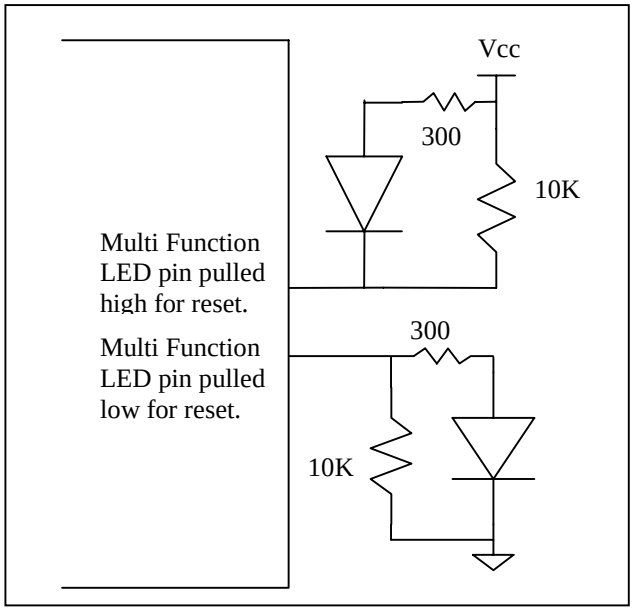

Figure 2: Multifunction LED Pin Connection

A suggested LED connection diagram is shown in Figure 3 that could simplify the board design.

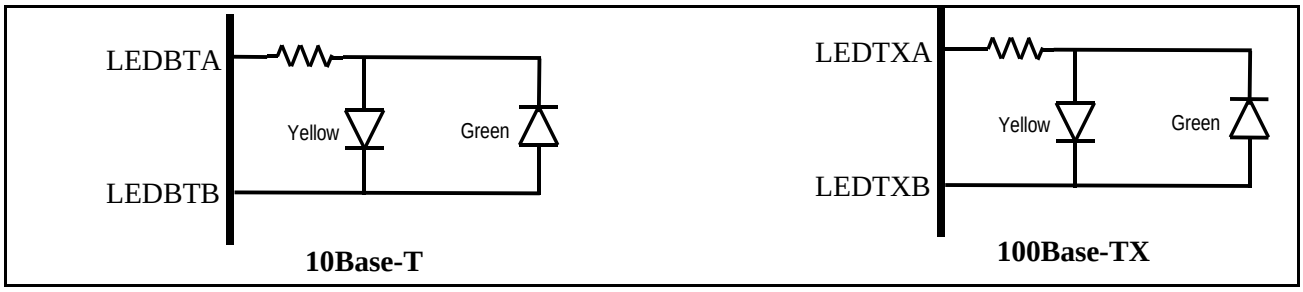

Figure 3: Dual-color LED Indicator for Link, Duplex, and Activity Status

Section 3: Pinout Diagrams

AC101QF PINOUT DIAGRAM

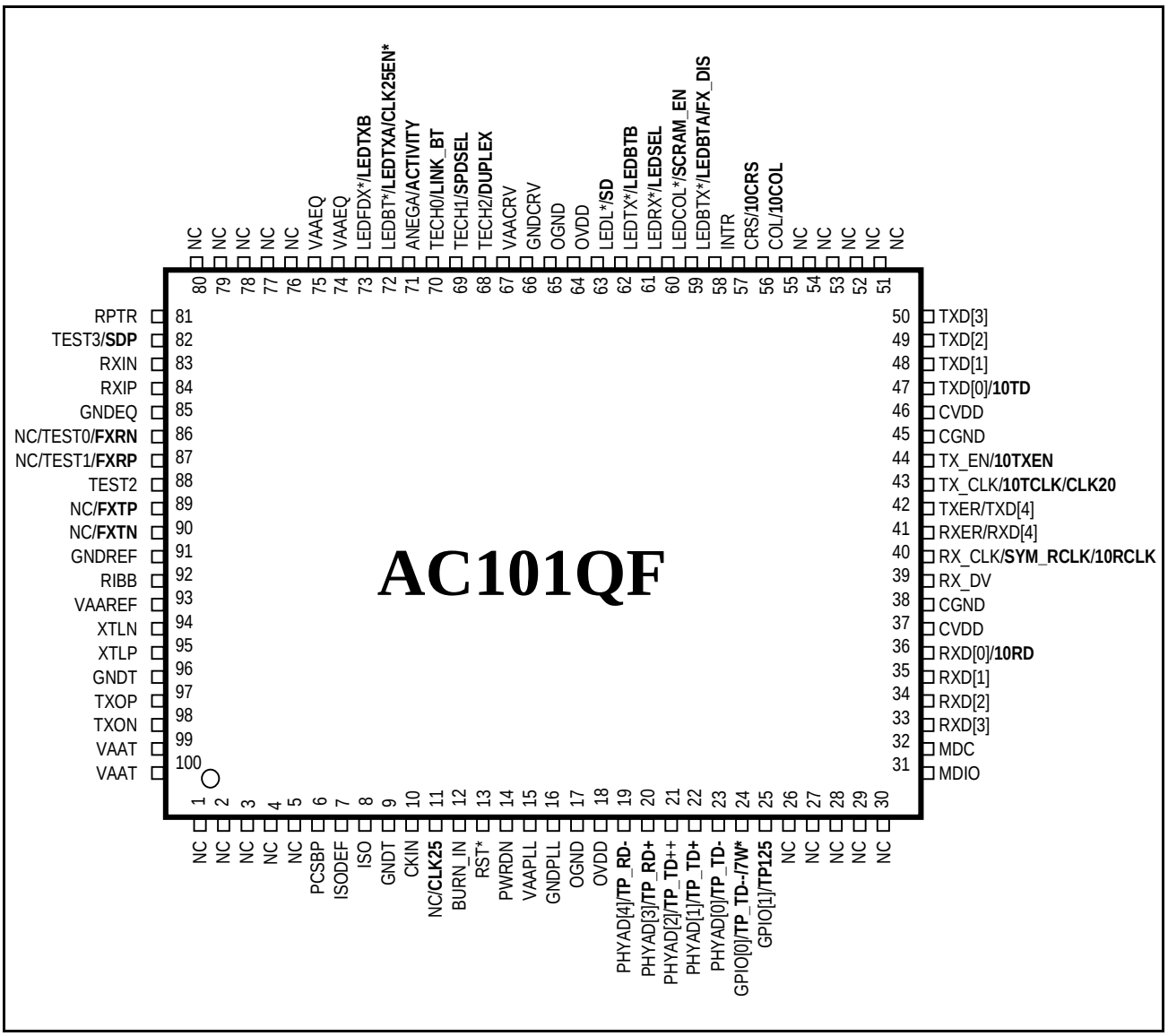

Figure 4: AC101QF Pinout Diagram

AC101TF PINOUT DIAGRAM

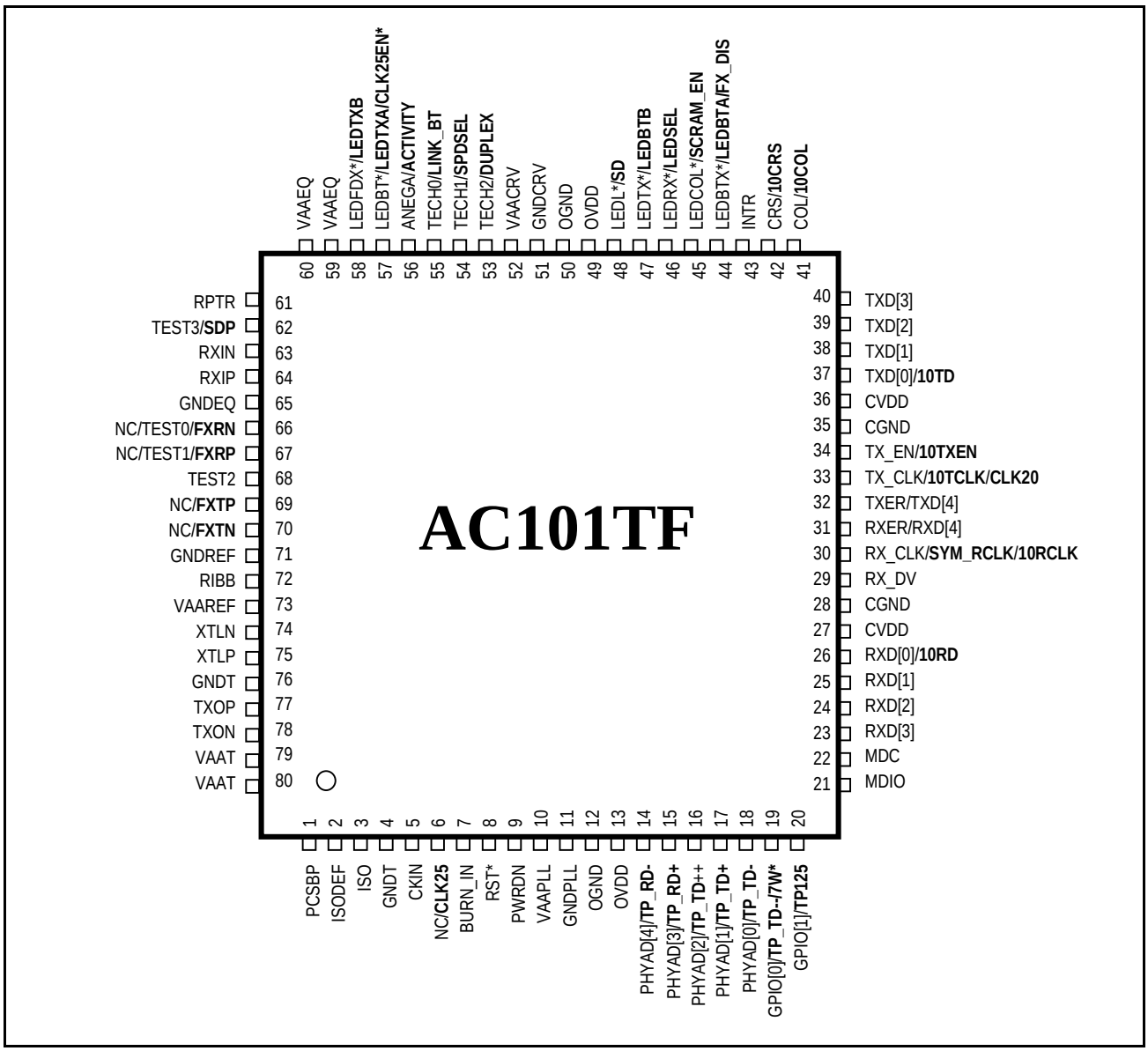

Figure 5: AC101TF Pinout Diagram

Section 4: Register Descriptions

REGISTER SUMMARY

The first eight registers of the MII register set are defined by the MII specification. In addition to these required registers are several Altima-specific registers. There are reserved registers and/or bits that are for Altima internal use only. (Register numbers are in Decimal format, the values are in Hex format).

Note **When writing to registers it is recommended that a read/modify/write operation be performed, as unintended bits may get set to unwanted states. This applies to all registers, including those with reserved bits.**

Legend:

- RW Read and Write Access
- SC Self Clearing
- LL Latch Low until cleared by reading
- RO Read Only
- RC Cleared on Read
- LH Latch High until Cleared by reading

Table 13: Register Summary

Register	*Description*	*Default*
MII-Specified Registers		
0	Control Register	3000
1	Status Register	7849
2	PHY Identifier 1 Register	0022
3	PHY Identifier 2 Register	561B
4	Auto-Negotiation Advertisement Register	01E1
5	Auto-Negotiation Link Partner Ability Register	0001
6	Auto-Negotiation Expansion Register	0004
7	Next Page Advertisement Register	2001
Altima-Specified Registers		
8-15	Reserved	XXXX
16	Polarity and Interrupt Register	03C0
17	Interrupt Control/Status Register	0000
18	Diagnostic Register	5020
19	Power Management & Loopback Register	8060
20	Cable Measurement Register	XXXX
21	Mode Control Register	0304

Table 13: Register Summary (Cont.)

Register	Description	Default
22	Reserved	XXXX
23	Reserved	0000
24	Receive Error Counter Register	0000
25-31	Reserved	XXXX

MII-SPECIFIED REGISTERS

REGISTER 0: CONTROL REGISTER

Table 14: Register 0: Control Register

Reg.bit	Name	Description	Mode	Default
0.15	Reset	1 = PHY reset. This bit is self-clearing.	RW/SC	0
0.14	Loopback	• 1 = Enable loopback mode. This will loopback TXD to RXD (see ”MII (Media Independent Interface) 100 PCS Bypass Pins” on page 12) and ignore all the activity on the cable media. • 0 = Normal operation.	RW	0
0.13	Speed Select	• 1 = 100 Mbps • 0 = 10 Mbps. See ”Technology Selections” on page 18.	RW	Set by TECH[2:0]
0.12	ANeg Enable	• 1 = Enable Auto-Negotiate process (overrides 0.13 and 0.8) • 0 = Disable Auto-Negotiate process. Mode selection is controlled via bit 0.8, 0.13 or through TECH[2:0] pins (see ”Control and Status Pins” on page 14).	RW	Set by ANEGA
0.11	Power Down	• 1 = Power down. All blocks except for SMI will be turned off. Setting PWRDN pin (see ”Special/Test Pins” on page 14) to high will achieve the same result. • 0 = Normal operation.	RW	0
0.10	Isolate	• 1 = Electrically isolate the PHY from MII. PHY is still able to response to SMI. The default value of this bit depends on ISODEF pin (see ”Control and Status Pins” on page 14). • 0 = Normal operation.	RW	Set by ISODEF
0.9	Restart ANeg	• 1 = Restart Auto-Negotiation process. • 0 = Normal operation.	RW/SC	0
0.8	Duplex Mode	• 1 = Full-duplex. • 0 = Half-duplex. See ”Technology Selections” on page 18.	RW	Set by TECH[2:0]

Table 14: Register 0: Control Register (Cont.)

Reg.bit	Name	Description	Mode	Default
0.7	Collision Test	• 1 = Enable collision test, which issues the COL signal in response to the assertion of TX_EN signal (see "MII (Media Independent Interface) 100 PCS Bypass Pins" on page 12). Collision test is disabled if PCSBP pin (see "Control and Status Pins" on page 14) is high. Collision test is enabled regardless of the duplex mode. • 0 = Disable COL test.	RW	0
0.[6:0]	Reserved		RW	0000000

REGISTER 1: STATUS REGISTER

Table 15: Register 1: Status Register

Reg.bit	Name	Description	Mode	Default
1.15	100BASE-T4	Permanently tied to zero indicates no 100BaseT4 capability.	RO	0
1.14	100BASE-TX Full-duplex	• 1 = 100BaseTX full-duplex capable. • 0 = Not 100BaseTX full-duplex capable.	RO	TECH[2:0]
1.13	100BASE-TX Half-duplex	• 1 = 100BaseTX half-duplex capable. • 0 = Not TX half-duplex capable.	RO	TECH[2:0]
1.12	10BASE-T Full-duplex	• 1 = 10BaseT full-duplex capable. • 0 = Not 10BaseT full-duplex capable.	RO	TECH[2:0]
1.11	10BASE-T Half-duplex	• 1 = 10BaseT half-duplex capable. • 0 = Not 10BaseT half-duplex capable.	RO	TECH[2:0]
1.[10:7]	Reserved		RO	0000
1.6	MF Preamble Suppression	The PHY is able to perform management transaction without MDIO preamble. The management interface needs minimum of 32 bits of preamble after reset.	RO	1
1.5	ANeg Complete	• 1 = Auto-Negotiate process completed. Reg. 4, 5, 6 are valid after this bit is set. • 0 = Auto-negotiate process not completed.	RO	0
1.4	Remote Fault	• 1 = Remote fault condition detected. • 0 = No remote fault. This bit will remain set until it is cleared by reading register 1.	RO/LH	0
1.3	Aneg. Ability	• 1 = Able to perform Auto-Negotiation function, default value determined by ANEGA pin (see "Control and Status Pins" on page 14). • 0 = Unable to perform Auto-Negotiation function.	RO	ANEGA
1.2	Link Status	• 1 = Link is established. If link fails, this bit will be cleared and remain at 0 until register is read again. • 0 = Link has gone down.	RO/LL	0
1.1	Jabber Detect	• 1 = Jabber condition detect. • 0 = No Jabber condition detected.	RO/LH	0

Table 15: Register 1: Status Register (Cont.)

Reg.bit	Name	Description	Mode	Default
1.0	Extended Capability	1 = Extended register capable. This bit is tied permanently to one.	RO	1

REGISTER 2: PHY IDENTIFIER 1 REGISTER

Table 16: Register 2: PHY Identifier 1 Register

Reg.bit	Name	Description	Mode	Default
2.[15:0]	OUI[a]	Composed of the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0022(H)

a. Based on an OUI of 0010A9 (Hex).

REGISTER 3: PHY IDENTIFIER 2 REGISTER

Table 17: Register 3: PHY Identifier 2 Register

Reg.bit	Name	Description	Mode	Default
3.[15:10]	OUI[a]	Assigned to the 19th through 24th bits of the OUI.	RO	010101
3.[9:4]	Model Number	Six bit manufacturer's model number. 101 is encoded as 100001.	RO	100001
3.[3:0]	Revision Number	Four-bit manufacturer's revision number. 0011 stands for Rev. C, etc.	RO	1011

a. Based on an OUI of 0010A9 (Hex).

REGISTER 4: AUTO-NEGOTIATION ADVERTISEMENT REGISTER

The ANeg Complete bit of Register 1: Status Register (see "Register 1: Status Register" on page 25) must be set for this register to be valid.

Table 18: Register 4: Auto-Negotiation Advertisement Register

Reg.bit	Name	Description	Mode	Default
4.15	Next Page	• 1 = Next Page enabled. • 0 = Next Page disabled.	RW	0
4.14	Acknowledge	This bit will be set internally after receiving 3 consecutive and consistent FLP bursts.	RO	0
4.13	Remote Fault	• 1 = Advertises that this device has detected a Remote Fault. • 0 = No remote fault detected.	RW	0
4.[12:10]	Reserved	For future technology.	RW	000
4.9	100BASE-T4	Technology not supported. This bit always 0	RO	0

Table 18: Register 4: Auto-Negotiation Advertisement Register (Cont.)

Reg.bit	Name	Description	Mode	Default
4.8	100BASE-TX Full-duplex	• 1 = 100BaseTX full-duplex capable. • 0 = Not 100BaseTX full-duplex capable.	RW	TECH [2:0]
4.7	100BASE-TX	• 1 = 100BaseTX half-duplex capable. • 0 = Not TX half-duplex capable.	RW	TECH [2:0]
4.6	10BASE-T Full-duplex	• 1 = 10BaseT full-duplex capable. • 0 = Not 10BaseT full-duplex capable.	RW	TECH [2:0]
4.5	10BASE-T	• 1 = 10BaseT half-duplex capable. • 0 = Not 10BaseT half-duplex capable.	RW	TECH [2:0]
4.[4:0]	Selector Field	Protocol Selection [00001] = IEEE 802.3.	RO	00001

REGISTER 5: AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER

The ANeg Complete bit of Register 1: Status Register (see ”Register 1: Status Register” on page 25) must be set for this register to be valid.

Table 19: Register 5: Auto-Negotiation Link Partner Ability Register

Reg.bit	Name	Description	Mode	Default
5.15	Next Page	• 1 = Link partner desires Next Page transfer. • 0 = Link partner does not desire Next Page transfer.	RO	0
5.14	Acknowledge	• 1 = Link Partner acknowledges reception of FLP words. • 0 = Not acknowledged by Link Partner.	RO	0
5.13	Remote Fault	• 1 = Remote Fault indicated by Link Partner. • 0 = No remote fault indicated by Link Partner.	RO	0
5.[12:10]	Reserved	For future technology.	RO	000
5.9	100BASE-T4	• 1 = 100BaseT4 supported by Link Partner. • 0 = 100BaseT4 not supported by Link Partner.	RO	0
5.8	100BASE-TX Full-duplex	• 1 = 100BaseTX full-duplex supported by Link Partner. • 0 = 100BaseTX full-duplex not supported by Link Partner.	RO	0
5.7	100BASE-TX	• 1 = 100BaseTX half-duplex supported by Link Partner. • 0 = 100BaseTX half-duplex not supported by Link Partner.	RO	0
5.6	10BASE-T Full-duplex	• 1 = 10 Mbps full-duplex supported by Link Partner. • 0 = 10 Mbps full-duplex not supported by Link Partner.	RO	0
5.5	10BASE-T	• 1 = 10 Mbps half-duplex supported by Link Partner. • 0 = 10 Mbps half-duplex not supported by Link Partner.	RO	0
5.[4:0]	Selector Field	Protocol Selection [00001] = IEEE 802.3.	RO	00001

REGISTER 6: AUTO-NEGOTIATION EXPANSION REGISTER

The ANeg Complete bit of Register 1: Status Register (see ”Register 1: Status Register” on page 25) must be set for this register to be valid.

Table 20: Register 6: Auto-Negotiation Expansion Register

Reg.bit	Name	Description	Mode	Default
6.[15:5]	Reserved		RO	0
6.4	Parallel Detection Fault	• 1 = Fault detected by parallel detection logic, this fault is due to more than one technology detecting concurrent link up condition. This bit can only be cleared by reading Register 6 using the management interface. • 0 = No fault detected by parallel detection logic.	RO/LH	0
6.3	Link Partner Next Page Able	• 1 = Link partner supports next page function. • 0 = Link partner does not support next page function.	RO	0
6.2	Next Page Able	Next page is supported.	RO	1
6.1	Page Received	This bit is set when a new link code word has been received into the Auto-Negotiation Link Partner Ability Register. This bit is cleared upon a read of this register.	RC	0
6.0	Link Partner ANeg-Able	• 1 = Link partner is Auto-Negotiation capable. • 0 = Link partner is not Auto-Negotiation capable.	RO	0

REGISTER 7: AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER

The ANeg Complete bit of Register 1: Status Register (see ”Register 1: Status Register” on page 25) must be set for this register to be valid.

Table 21: Register 7: Auto-Negotiation Next Page Transmit Register

Reg.bit	Name	Description	Mode	Default
7.15	NP	• 1 = Another Next Page desired. • 0 = No other Next Page Transfer desired.	RW	0
7.14	Reserved		RO	0
7.13	MP	• 1 = Message page. • 0 = Unformatted page.	RW	1
7.12	ACK2	• 1 = Will comply with message. • 0 = Can not comply with message.	RW	0
7.11	TOG_TX	• 1 = Previous value of transmitted link code word equals to 0. • 0 = Previous value of transmitted link code word equals to 1.	RW	0
17.[10:0]	CODE	Message/Un-formatted Code Field.	RW	001

ALTIMA-SPECIFIED REGISTERS

REGISTER 16: POLARITY AND INTERRUPT LEVEL REGISTER

Table 22: Register 16: Polarity and Interrupt Level Register

Reg.bit	*Name*	*Description*	*Mode*	*Default*
16.15	Repeater	• 1= Repeater mode, full-duplex will be inactive, and CRS only responses to receive activity. SQE test function is disabled.	RW	Set by RPTR
16.14	INTR_LEVL	• 1=INTR pin will be active high. • 0=INTR pin will be active low.	RW	0
16.[13:12]	Reserved		RW	00
16.11	SQE Test Inhibit	• 1 = Disable 10BaseT SQE testing. • 0 = Enable 10BaseT SQE testing, which will generate a COL pulse following the completion of a packet transmission**.**	RW	0
16.10	10BaseT Loopback	• 1 = Enable normal loopback in 10BaseT mode. • 0 = Disable normal loopback in 10BaseT mode.	RW	1
16.9	GPIO[1] Data	• When GPIO[1] DIR bit (Reg. 16.8) is set to one, this bit value reflects the signal of GPIO[1] pin. • When GPIO[1] DIR bit is set to 0, the value of this bit will display on GPIO[1] pin.	RW	0
16.8	GPIO[1] DIR	• Set to one then GPIO[1] pin is input. • Set to zero then GPIO[1] pin is an output.	RW	1
16.7	GPIO[0] Data	When GPIO[0] DIR (Reg. 16.6) bit is set to one, this bit value reflects the signal of GPIO[0] pin. When GPIO[0] DIR bit is set to 0, the value of this bit will display on GPIO[0] pin.	RW	0
16.6	GPIO[0] DIR	• Set to one then GPIO[0] pin is input. • Set to zero then GPIO[0] pin is an output.	RW	1
16.5	Auto Polarity Disable	• 1 = Disable Auto Polarity detection/correction. • 0 = Enable Auto Polarity detection/correction.	RW	0
16.4	Reverse Polarity	• 1= Reverse Polarity when Reg. 16.5 = 0. • 0= Normal Polarity when Reg. 16.5 = 0. If Reg. 16.5 is set to 1, writing a one to this bit will reverse the polarity of the transmitter.	RW	0
16.[3:1]	Reserved		RO	000
16.0	Receive Clock Control	Writing a one to this bit will shut off RX_CLK when incoming data is not present. RX_CLK will resume 1 clock cycle prior to RX_DV going high, and shut off 64 clock cycles after RX_DV goes low. No action when in Loopback or PCS Bypassed modes.	RW	0

REGISTER 17: INTERRUPT CONTROL/STATUS REGISTER

Table 23: Register 17: Interrupt Control/Status Register

Reg.bit	Name	Description	Mode	Default
17.15	Jabber_IE	Jabber Interrupt Enable.	RW	0
17.14	Rx_Er_IE	Receive Error Interrupt Enable.	RW	0
17.13	Page_Rx_IE	Page Received Interrupt Enable.	RW	0
17.12	PD_Fault_IE	Parallel Detection Fault Interrupt Enable.	RW	0
17.11	LP_Ack_IE	Link Partner Acknowledge Interrupt Enable.	RW	0
17.10	Link_Not_OK _ IE	Link Status Not OK Interrupt Enable.	RW	0
17.9	R_Fault_IE	Remote Fault Interrupt Enable.	RW	0
17.8	ANeg_Comp _IE	Auto-Negotiation Complete Interrupt Enable.	RW	0
17.7	Jabber_Int	This bit is set when a jabber event is detected.	RC	0
17.6	Rx_Er_Int	This bit is set when RX_ER transitions high.	RC	0
17.5	Page_Rx_Int	This bit is set when a new page is received during ANeg.	RC	0
17.4	PD_Fault_Int	This bit is set when parallel detect fault is detected.	RC	0
17.3	LP_Ack_Int	This bit is set when the FLP with acknowledge bit set is received.	RC	0
17.2	Link_Not_OK Int	This bit is set when link status switches from OK status to Non-OK status (Fail or Ready).	RC	0
17.1	R_Fault_Int	This bit is set when remote fault is detected.	RC	0
17.0	ANeg _Comp Int	This bit is set when ANeg is complete.	RC	0

REGISTER 18: DIAGNOSTIC REGISTER

Table 24: Register 18: Diagnostic Register

Reg.bit	Name	Description	Mode	Default
18.[15:12]	Reserved		RO	0000
18.11	DPLX	The result of Auto-Negotiation is Full-duplex =1, Half-duplex =0	RO	0
18.10	Speed	The result of the Auto-Neg. is 100BASE-TX = 1, 10BASE-T = 0	RO	0
18.9	RX_PASS	• In 10BT mode, this bit indicates that Manchester data has been detected. • In 100BT mode, it indicates valid signal has been received but not necessarily locked on to.	RO	0
18.8	RX_LOCK	Indicates the receive PLL has locked onto the received signal for the selected speed of operation (10BASE-T or 100BASE-TX). This bit is set whenever a cycle-slip occurs and will remain set until it is read.	RO/RC	0

Table 24: Register 18: Diagnostic Register (Cont.)

Reg.bit	Name	Description	Mode	Default
18.[7:0]	Reserved		RO	0

REGISTER 19: POWER/LOOPBACK REGISTER

Table 25: Register 19: Power/Loopback Register

Reg.bit	Name	Description	Mode	Default
19.[14:7]	Reserved	Reserved	RW	00
19.6	TP125	Transmit transformer ratio selection. • 1 = 1.25:1 • 0 = 1:1 The default value of this bit is controlled by TP125 pin (see ”Control and Status Pins” on page 14).	RW	0
19.5	Low Power Mode	• 1 = Enable advanced power saving mode. • 0 = Disable advanced power saving mode.	RW	1
19.4	Test Loopback	• 1 = Enable test loopback. (MII through clock recovery to MII) • 0 = Normal operation.	RW	0
19.3	Digital loopback	• 1 = Enable loopback. • 0 = Normal operation.	RW	0
19.2	LP_LPBK	• 1 = Enable link pulse loopback. • 0 = Normal operation.	RW	0
19.1	NLP Link Integrity Test	• 1 = In ANeg test mode, send NLP instead of FLP in order to test NLP receive integrity. • 0 = Sending FLP in ANeg test mode.	RW	0
19.0	Reduce Timer	• 1= Reduce time constant for ANeg timer. • 0 = Normal operation.	R	0

REGISTER 20: CABLE MEASUREMENT REGISTER

Table 26: Register 20: Cable Measurement Register

Reg.bit	Name	Description	Mode	Default
20.[15:8]	Reserved		RO	0
20.[7:4]	Cable measurement capability	These bits can be used as cable length indicator. The bits are incremented from 0000 to 1111, with an increment of approximately 10 meters. The equivalent is 0 to 32 dB with an increment of 2 dB at 100 MHz. The value is a read back from the equalizer, and the measured value is not absolute.	RO	0
20.[3:0]	Reserved		RO	0

REGISTER 21: MODE CONTROL REGISTER

Table 27: Register 21: Mode Control Register

Reg.bit	Name	Description	Mode	Default
21.15	Reserved		RO	0
21.14	NLP Disable	• 1 = Force 10B-T link up without checking NLP. • 0 = Normal Operation.	RW	0
21.13	Force_link_up	• 1 = Ignore link in 100BASE-TX and transmit data. ANeg must be disabled at this time (ANEGA pin tied low). • 0 = Normal Operation.	RW	0
21.12	Jabber Disable	• 1 = Disable Jabber function in PHY. • 0 = Enable Jabber function in PHY.	RW	0
21.11	10BT_Sel	• 1 = Enable 7-wire interface for 10BASE-T operation. • 0 = Normal operation. (Not valid in PCS Bypass mode.)	RW	0
21.10	Conf_ALED	• 1 = Activity LED only responds to receive operation. • 0 = Activity LED responds to receive and transmit. This bit should be ignored when Reg. 0.8 (see ”Register 0: Control Register” on page 24) is set or in the repeater mode.	RW	0
21.9	LED_Sel	• 1 = Use the LED configuration which is compatible with TSC78Q2120. • 0 = Select LED selection (see ”Advanced LED Selections” on page 19).	RW	Set by LED_RX/ LEDSEL
21.8	FEF_Disable	• 1 = Disable Far End Fault Insertion. • 0 = Enable Far End Fault Insertion and detection function. This bit valid when FX mode is enabled.	RW	Set by TECH, FX_DIS, ANEGA
21.7	Force FEF Transmit	• 1 = Force transmission of Far End Fault Insertion pattern. • 0 = Normal operation.	RW	0
21.6	Rx_Er_Cnt Full	• 1 = Receive Error Counter full. • 0 = Receive Error Counter not full.	RO/ RC	0
21.5	Disable Rx_Er_Cnt	• 1 = Disable Receive Error Counter. • 0 = Enable Receive Error Counter.	RW	0
21.4	Dis_WDT	• 1 = Disable the watchdog timer in the decipher. • 0 = Enable watchdog timer.	RW	0
21.3	En_RPBK	• 1 = Enable remote loopback. • 0 = Disable remote loopback.	RW	0
21.2	Dis_Scrm	• 1 = Enable 100M data scrambling. • 0 = Disable 100M data scrambling. When FX mode is selected, this bit will be forced to zero.	RW	Set by LED_COL/ SCRAM_EN
21.1	PCSBP	• 1 = Bypass PCS. Disable 4b/5b and scrambler in 100B-TX mode. • 0 = Enable PCS. Enable 4b/5b and scrambler in 100B-TX mode.	RW	Set by PCSBP

Table 27: Register 21: Mode Control Register (Cont.)

Reg.bit	Name	Description	Mode	Default
21.0	FX_SEL	• 1 = FX mode selected. • 0 = Disable FX mode.	RW	Set by FX_DIS

REGISTER 24: RECEIVE ERROR COUNTER REGISTER

Table 28: Register 24: Receive Error Counter Register

Reg.bit	Name	Description	Mode	Default
24.[15:0]	RX_ER counter	Count receive error events.	RW	0000

4B/5B CODE-GROUP TABLE

Table 29: 4B/5B Code-Group Table

PCS Code Group [4 3 2 1 0]	SYMBOL Name	MII (TXD/RXD [3:0]) [3 2 1 0]	Description
11110	0	0000	Data 0
01001	1	0001	Data 1
10100	2	0010	Data 2
10101	3	0011	Data 3
01010	4	0100	Data 4
01011	5	0101	Data 5
01110	6	0110	Data 6
01111	7	0111	Data 7
10010	8	1000	Data 8
10011	9	1001	Data 9
10110	A	1010	Data A
10111	B	1011	Data B
11010	C	1100	Data C
11011	D	1101	Data D
11100	E	1110	Data E
11101	F	1111	Data F
Idle and Control Code			
11111	I	0000	Inter-Packet Idle; used as inter-stream fill code.
11000	J	0101	Start of stream delimiter, part 1 of 2; always use in pair with K symbol.

Table 29: 4B/5B Code-Group Table (Cont.)

PCS Code Group [4 3 2 1 0]	SYMBOL Name	MII (TXD/RXD [3:0]) [3 2 1 0]	Description
10001	K	0101	Start of stream delimiter, part 2 of 2; always use in pair with J symbol.
01101	T	Undefined	End of stream delimiter, part 1 of 2; always use in pair with R symbol.
00111	R	Undefined	End of stream delimiter, part 2 of 2; always use in pair with T symbol.
Invalid Code			
00100	H	Undefined	Transmit Error; used to send HALT code-group
00000	V	Undefined	Invalid code
00001	V	Undefined	Invalid code
00010	V	Undefined	Invalid code
00011	V	Undefined	Invalid code
00101	V	Undefined	Invalid code
00110	V	Undefined	Invalid code
01000	V	Undefined	Invalid code
01100	V	Undefined	Invalid code
10000	V	Undefined	Invalid code
11001	V	Undefined	Invalid code

SMI READ/WRITE SEQUENCE

Table 30: SMI Read/Write Sequence

	Pream (32 bits)	Start (2 bits)	OpCode (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	TurnAround (2 bits)	Data (16 bits)	Idle
Read	1…1	01	10	AAAAA	RRRRR	Z0	D…D	Z
Write	1…1	01	01	AAAAA	RRRRR	10	D…D	Z

Section 5: Electrical Characteristics

Note **The following electrical characteristics are design goals rather than characterized numbers.**

OPERATING RANGE

- Operating Temperature (Ta) -40°C to +85°C
- Vcc Supply Voltage Range (Vcc) 2.97V to 3.63V
- TTL I/O interface operate in 3.3V or 5V

TOTAL POWER CONSUMPTION

Table 31: Total Power Consumption

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Supply Current	Icc	10BASE-T, Idle		25	30	mA
		10BASE-T, Normal activity		41	75	mA
		100BASE-TX		85	100	mA
		100BASE-FX		30	40	mA
		10/100BASE-TX, low power without cable		12	15	mA
		Power down			1	mA

TTL I/O CHARACTERISTICS

Table 32: TTL I/O Characteristics

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Input Voltage High	Vih		2.0			V
Input Voltage Low	Vil				0.8	V
Input Current	Ii		-8		8	mA
Output Voltage High	Voh		VCC-0.4			V
Output Voltage Low	Vol				0.4	V
Output Current High	Ioh				8	mA
Output Current Low	Iol		2			mA
Input Capacitance	Ci			10		pF
Output Transition Time		3.15V < VCC < 3.45V		5		ns
Tristate Leakage Current	|Ioz|				10	uA

REFCLK AND XTAL PIN CHARACTERISTICS

Table 33: REFCLK and XTAL Pin Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Low	Vil				0.8	V
Input Voltage High	Vih		2.0			V
Input Clock Frequency Tolerance	F				±50	ppm
Input Clock Duty Cycle	Tdc		40		60	%
Input Capacitance	Cin			3.0		pF

I/O CHARACTERISTICS – LED/CFG PIN CHARACTERISTICS

Table 34: I/O Characteristics – LED/CFG Pin Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Low Voltage	Vol				0.4	V
Output High Voltage	Voh		2.4			V
Input Current	Ii		8		8	µA
Output Current	Io		-10		10	mA

100BASE-TX TRANSCEIVER CHARACTERISTICS

Table 35: 100BASE-TX Transceiver Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Peak to Peak Differential Output Voltage	Vp	Note 1	1.9	2.0	2.1	V
Output Voltage Symmetry	Vss	Note 1	.98		1.02	mV
Signal Rise/Fall Time	Trf	Note 1	3.0		5.0	ns
Rise/Fall Time Symmetry	Trfs	Note 1	3	4	4	ns
Duty Cycle Distortion	Dcd				+250	ps
Overshoot/Undershoot	Vos				5	%
Output Jitter		Scrambled Idle			1.4	ns
Receive Jitter Tolerance					4	ns
Output Current High	Ioh	1:1 Transformer			40	mA
Output Current High	Ioh	1.25:1 Transformer			32	mA
Note 1: 50Ω (± 1%) resistor to VCC on each output.						

Table 35: 100BASE-TX Transceiver Characteristics (Cont.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Common Mode Input Voltage				1.8		V
Common Mode Input Current					10	uA
Differential Input Resistance				5		KΩ
Note 1: 50Ω (± 1%) resistor to VCC on each output.						

10BASE-T TRANSCEIVER CHARACTERISTICS

Table 36: 10BASE-T Transceiver Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Peak to Peak Differential Output Voltage	Vop	Note 1	4.5	5	5.5	V
Signal Rise/Fall Time			1		4	ns
Output Current Sink				15	16	mA
Output Current High	Ioh	1:1 Transformer			100	mA
Output Current High	Ioh	1.25:1 Transformer			80	mA
Start of Idle Pulse Width			300		350	ns
Output Jitter					1.4	ns
Receive Jitter Tolerance					32	ns
Receive Input Impedance	Zin		3.6			KΩ
Differential Squelch Threshold	Vds		300	400	500	mV
Common Mode Rejection				25		V
Differential Input Resistance			25			KΩ
Note 1: 50Ω (± 1%) resistor to VCC on each output.						

100BASE-FX TRANSCEIVER CHARACTERISTICS

Table 37: 100BASE-FX Transceiver Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage High	Voh	Note 1	2.2		2.5	V
Note 1: 69Ω to 3.3V VCC and 183Ω to ground.						

Table 37: 100BASE-FX Transceiver Characteristics (Cont.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage Low	Vol	Note 1	1.4		1.7	V
Signal Rise/Fall Time			1		4	ns
Output Jitter					1.4	ns
Differential Output Voltage High	Vih		2.1		2.4	V
Differential Output Voltage Low	Vil		1.5		1.8	V
Output Current Sink				15	16	mA
Note 1: 69Ω to 3.3V VCC and 183Ω to ground.						

10BASE-T LINK INTEGRITY TIMING CHARACTERISTICS

Table 38:

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Time Link Loss Receiver			50		150	ms
Link Pulse			2		7	Link Pulses
Link Min Receive Timer			2		7	ms
Link Max Receive Timer			50		150	ms
Link Transmit Period			8		24	ms
Link Pulse Width			60		150	ns

Section 6: Timing and AC Characteristics

DIGITAL TIMING CHARACTERISTICS

POWER ON RESET TIMING

Table 39: Power On Reset Timing

Parameter	*SYM*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
RST* Low Period	tRST		150	-	-	µs
Configuration	tCONF		100	-	-	ns

Figure 6: Power-on Reset Timing

MANAGEMENT DATA INTERFACE TIMING

Table 40: Management Data Interface Timing

Parameter	*SYM*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Mgt CLOCK	tMDCL		20	-	-	ns
Mgt CLOCK	tMDCH		20	-	-	ns
MDIO Setup	tMS	Setup on Read/Write Cycle	10	-	-	ns
MDIO Hold	tMH	Hold on Read/Write Cycle	10			ns

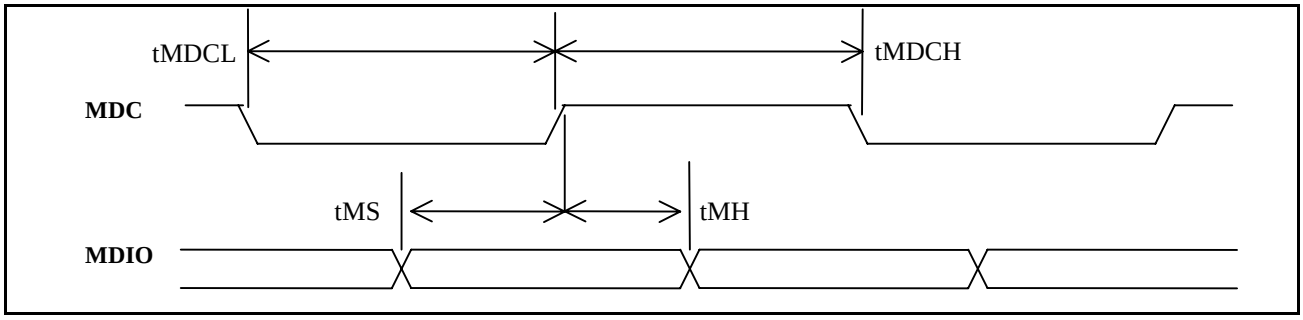

Figure 7: Management Data Interface Timing

100BASE-TX/FX MII TRANSMIT SYSTEM TIMING

Table 41: 100BASE-TX/FX MII Transmit System Timing

Parameter	*SYM*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
TX_CLK period	tCK		39.998	40.000	40.002	ns
TX_CLK High period	tCKH		18.000	20.000	22.000	ns
TX_CLK Low period	tCKL		18.000	20.000	22.000	ns
TX_EN to /J/	tTJ		-	40	180	ns
TX_EN sampled to CRS	tCSA	RPTR is logic low	-	40	180	ns
TX_EN sampled to COL	tCLA	RPTR is logic low	-	40	180	ns
!TX_EN to /T/	tTT		-	40	180	ns
!TX_EN sampled to !CRS	tCSD	RPTR is logic low	-	40	180	ns
!TX_EN sampled to !COL	tCLD	RPTR is logic low	-	40	180	ns
TX Propagation Delay	tTJ	From TXD[3:0] to TXOP/N(FXTP/N)	-	40	180	ns
TXD[3:0], TX_EN, TX_ER Setup	tTXS	From rising edge of TX_CLK	10	-	-	ns
TXD[3:0], TX_EN, TX_ER Hold	tTXH	From rising edge of TX_CLK	0	-	-	ns
!TX_EN to TX_EN	tTX_TX		120	-	-	ns

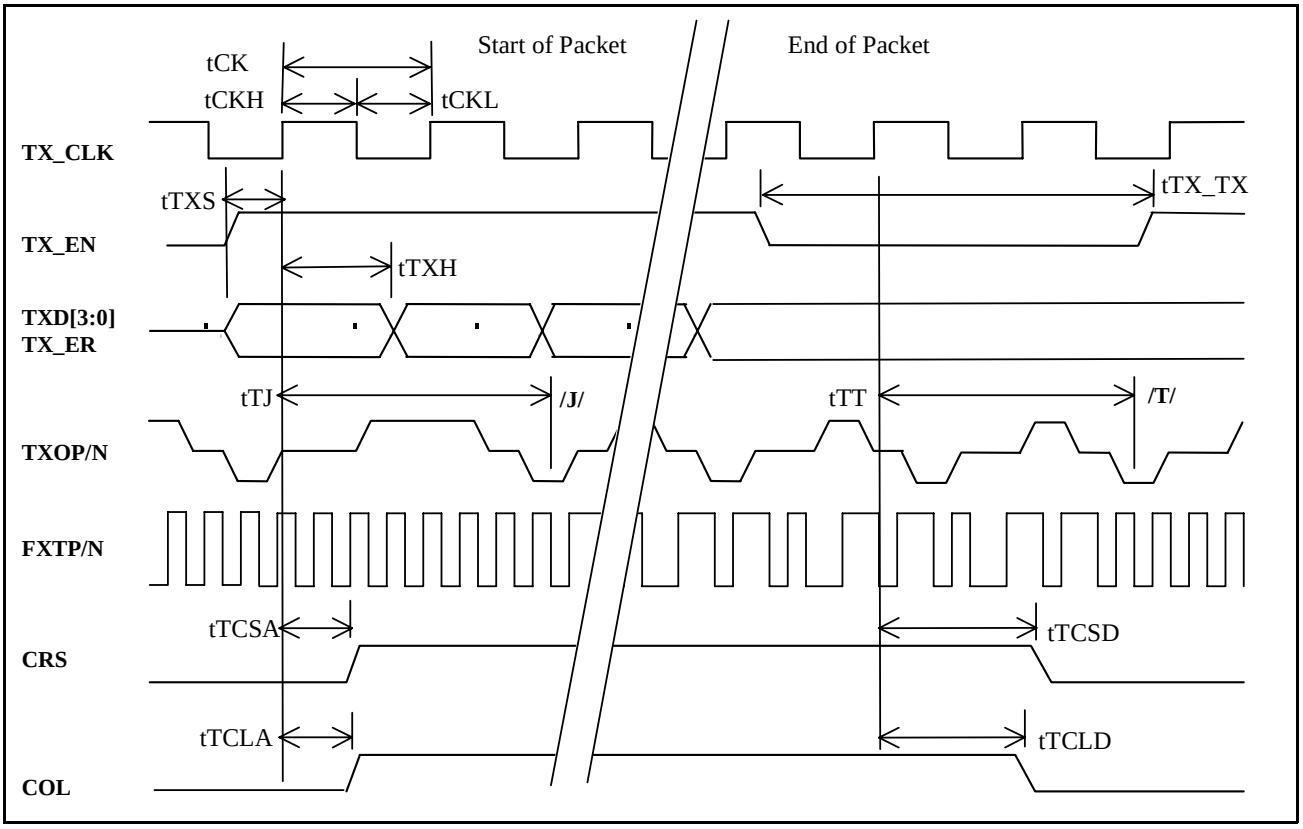

Figure 8: 100BASE-TX/FX MII Transmit Timing

100BASE-TX/FX MII RECEIVE SYSTEM TIMING

Table 42: 100BASE-TX/FX MII Receive System Timing

Parameter	*SYM*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
RX_CLK period	tCK		39.998	40.000	40.002	ns
RX_CLK High period	tCKH		18.000	20.000	22.000	ns
RX_CLK Low period	tCKL		18.000	20.000	22.000	ns
/J/K to RX_DV assert	tRDVA		-	40	180	ns
/J/K to CRS assert	tRCSA		-	40	180	ns
/J/K to COL assert	tRCLA	RPTR is logic low	-	40	180	ns
/T/R to !RX_DV	tRDVD	RPTR is logic low	-	40	180	ns
/T/R to !CRS	tRCSD	RPTR is logic low	-	40	180	ns
/T/R to !COL	tRCLD	RPTR is logic low	-	40	180	ns
RX Propagation Delay	tRDVA	From RXIP/N(FXRP/N) to RXD[3:0]	-	40	180	ns
RXD[3:0], RX_DV, RX_ER Setup	tRXS	From rising edge of RX_CLK	10	-	-	ns

Table 42: 100BASE-TX/FX MII Receive System Timing (Cont.)

Parameter	SYM	Conditions	Min	Typ	Max	Units
RXD[3:0], RX_DV, RX_ER Hold	tRXH	From rising edge of RX_CLK	10	-	-	ns

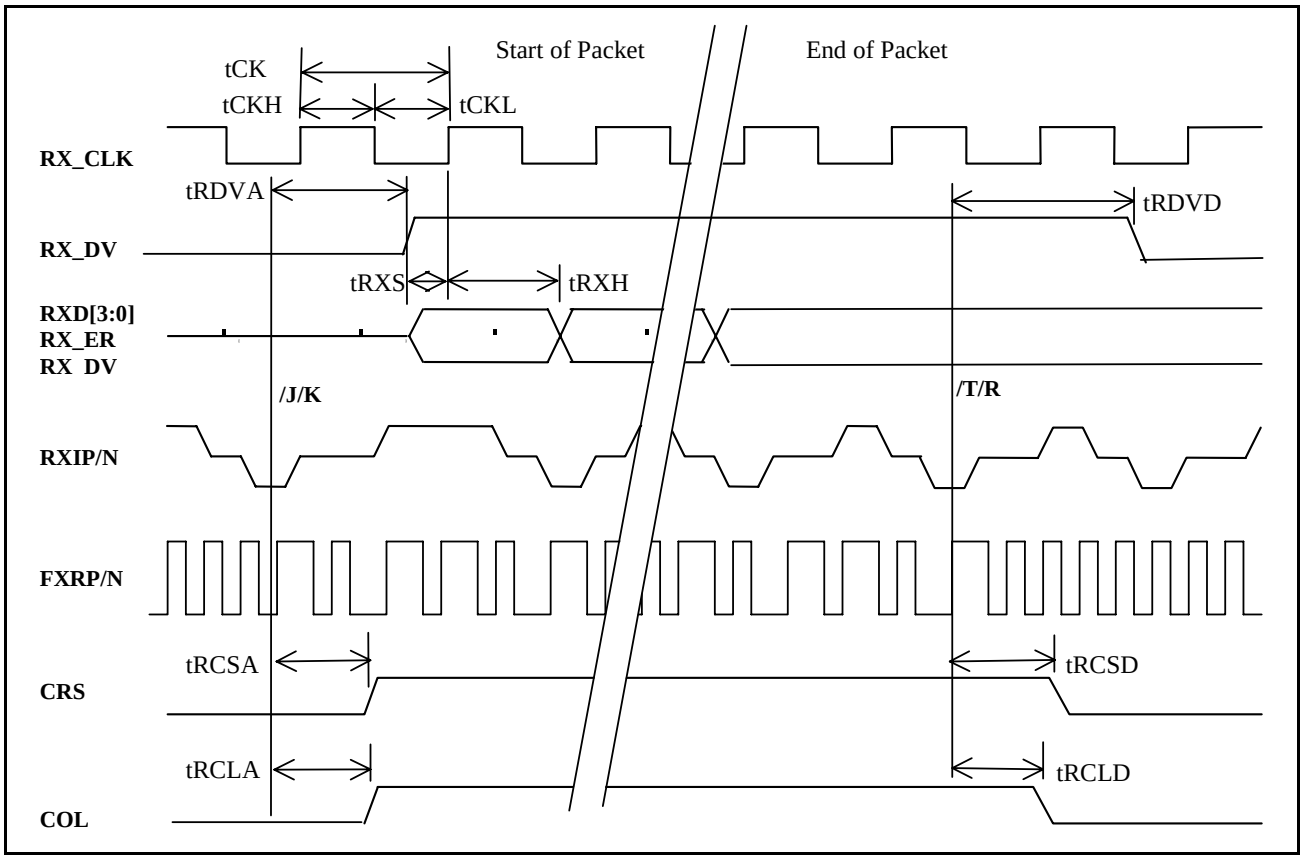

Figure 9: 100BASE-TX/FX MII Receive Timing

10BASE-T MII TRANSMIT SYSTEM TIMING

Table 43: 10BASE-T MII Transmit System Timing

Parameter	SYM	Conditions	Min	Typ	Max	Units
TX_CLK period	tCK		399.98	400.00	400.02	ns
TX_CLK High period	tCKH		180.00	200.00	220.00	ns
TX_CLK Low period	tCKL		180.00	200.00	220.00	ns
TX_EN to SOP	tTJ		240	-	360	ns
TX_EN sampled to CRS	tTCSA	RPTR is logic low	-	-	130	ns

Table 43: 10BASE-T MII Transmit System Timing (Cont.)

Parameter	SYM	Conditions	Min	Typ	Max	Units
TX_EN sampled to COL	tTCLA	RPTR is logic low	-	-	300	ns
!TX_EN to EOP	tTJ		240	-	360	ns
!TX_EN sampled to !CRS	tTCSD	RPTR is logic low	-	-	130	ns
!TX_EN sampled to !COL	tTCLD	RPTR is logic low	-	-	300	ns
TX Propagation Delay	tTJ	From TXD[3:0] to TXOP/N	240	-	360	ns
TXD[3:0], TX_EN, TX_ER Setup	tTXS	From rising edge of TX_CLK	10	-	-	ns
TXD[3:0], TX_EN, TX_ER Hold	tTXH	From rising edge of TX_CLK	0	-	-	ns
!TX_EN to TX_EN	tTX_TX		300	-	-	ns

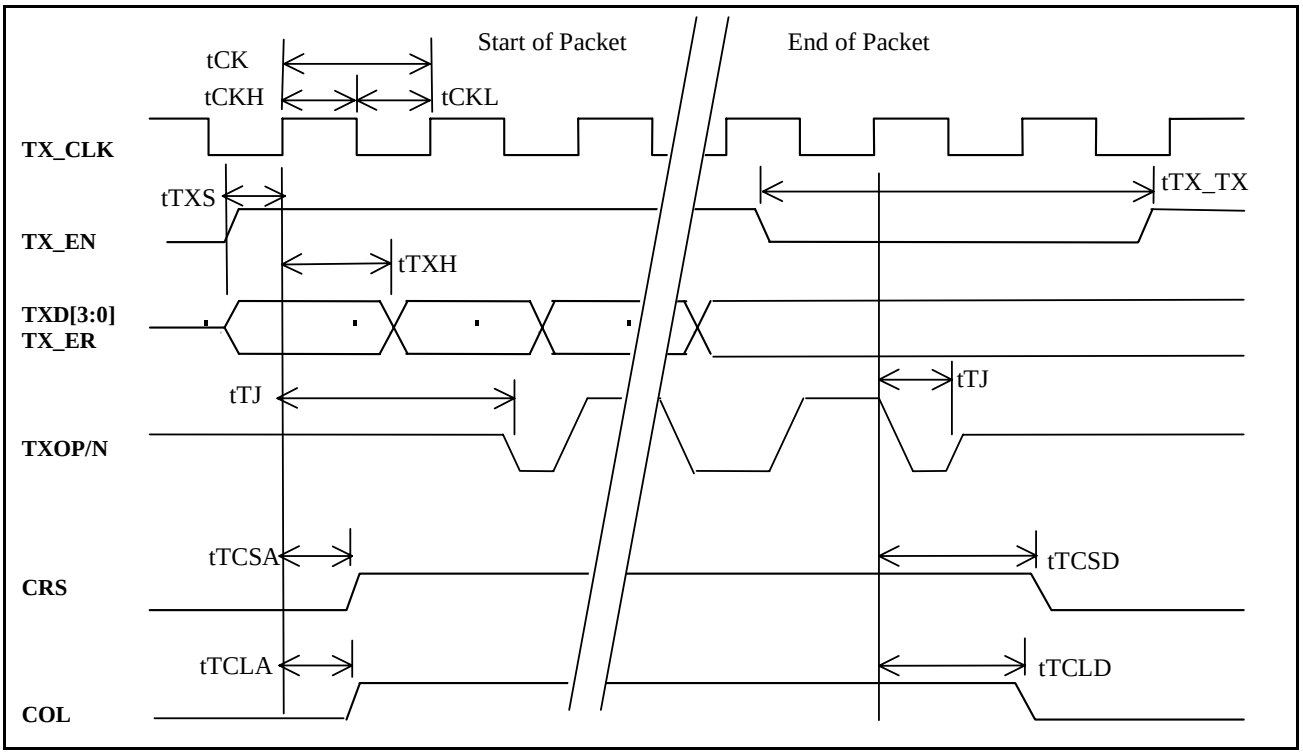

Figure 10: 10BASE-T MII Transmit Timing

10BASE-T MII RECEIVE SYSTEM TIMING

Table 44: 10BASE-T MII Receive System Timing

Parameter	SYM	Conditions	Min	Typ	Max	Units
RX_CLK period	tCK		399.98	400.00	400.02	ns
RX_CLK High period	tCKH		180.00	200.00	220.00	ns
RX_CLK Low period	tCKL		180.00	200.00	220.00	ns
CRS to RX_DV	tRDVA		100	100	100	ns
SOP to CRS	tRCSA		80	-	150	ns
SOP to COL	tRCLA	RPTR is logic low	80	-	150	ns
EOP to !RX_DV	tRDVD	RPTR is logic low	120	-	140	ns
EOP to !CRS	tRCSD	RPTR is logic low	130	-	190	ns
EOP to !COL	tRCLD	RPTR is logic low	125	-	185	ns
RX Propagation Delay	tRDVA	From RXIP/N to RXD[3:0]	180	-	250	ns
RXD[3:0], RX_DV, RX_ER Setup	tRXS	From rising edge of RX_CLK	16	-	-	ns
RXD[3:0], RX_DV, RX_ER Hold	tRXH	From rising edge of RX_CLK	12	-	-	ns

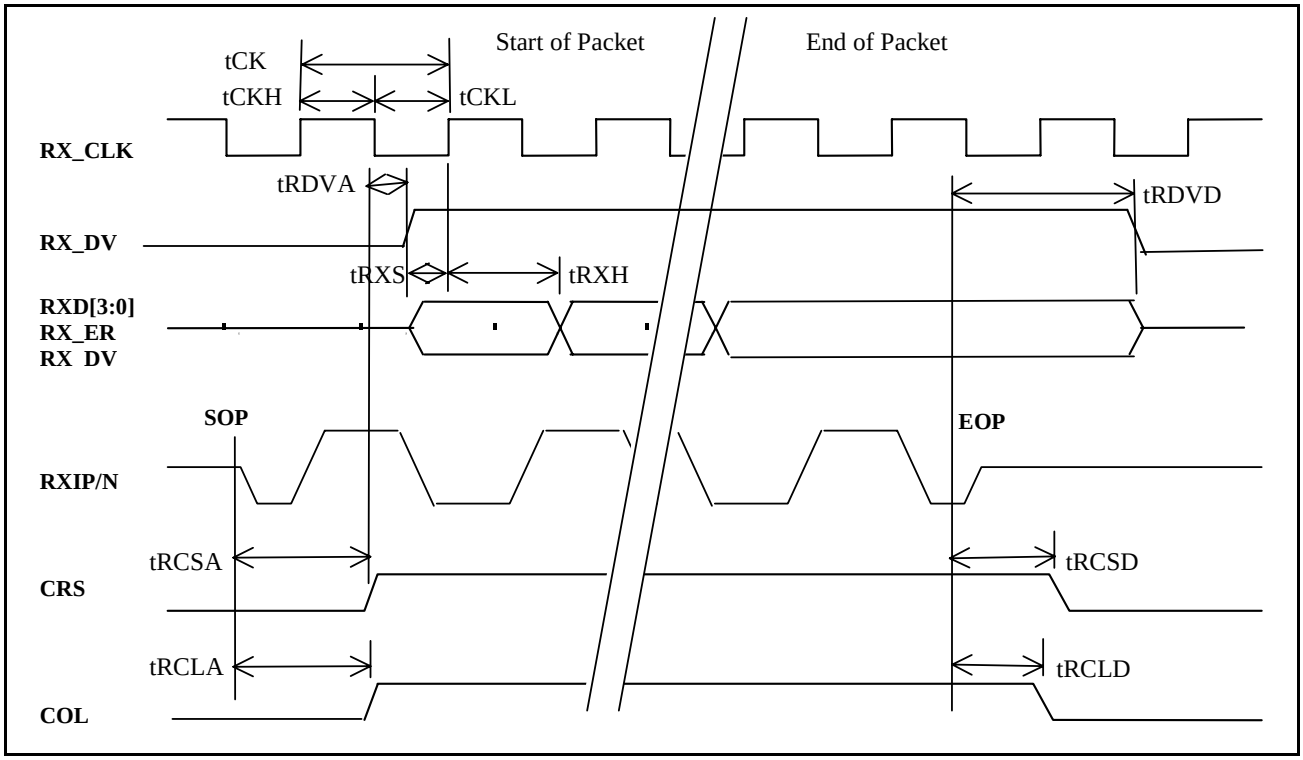

Figure 11: 10BASE-T MII Receive Timing

10BASE-T 7-WIRE TRANSMIT SYSTEM TIMING

Table 45: 10BASE-T 7-Wire Transmit System Timing

Parameter	SYM	Conditions	Min	Typ	Max	Units
10TCLK period	tCK		99.995	100.00	100.005	ns
10TCLK High period	tCKH		45.00	50.00	55.00	ns
10TCLK Low period	tCKL		45.00	50.00	55.00	ns
10TXEN to SOP	tTJ		240	-	360	ns
10TXEN sampled to 10CRS	tTCSA	RPTR is logic low	-	-	130	ns
!10TXEN to EOP	tTJ		240	-	360	ns
!10TXEN sampled to !10CRS	tTCSD	RPTR is logic low	-	-	130	ns
TX Propagation Delay	tTJ	From TXD[3:0] to TXOP/N	240	-	360	ns
10TD Setup	tTXS	From rising edge of 10TCLK	20	-	-	ns
10TD Hold	tTXH	From rising edge of 10TCLK	20	-	-	ns
! 10TXEN to 10TXEN	tTX_TX		300	-	-	ns

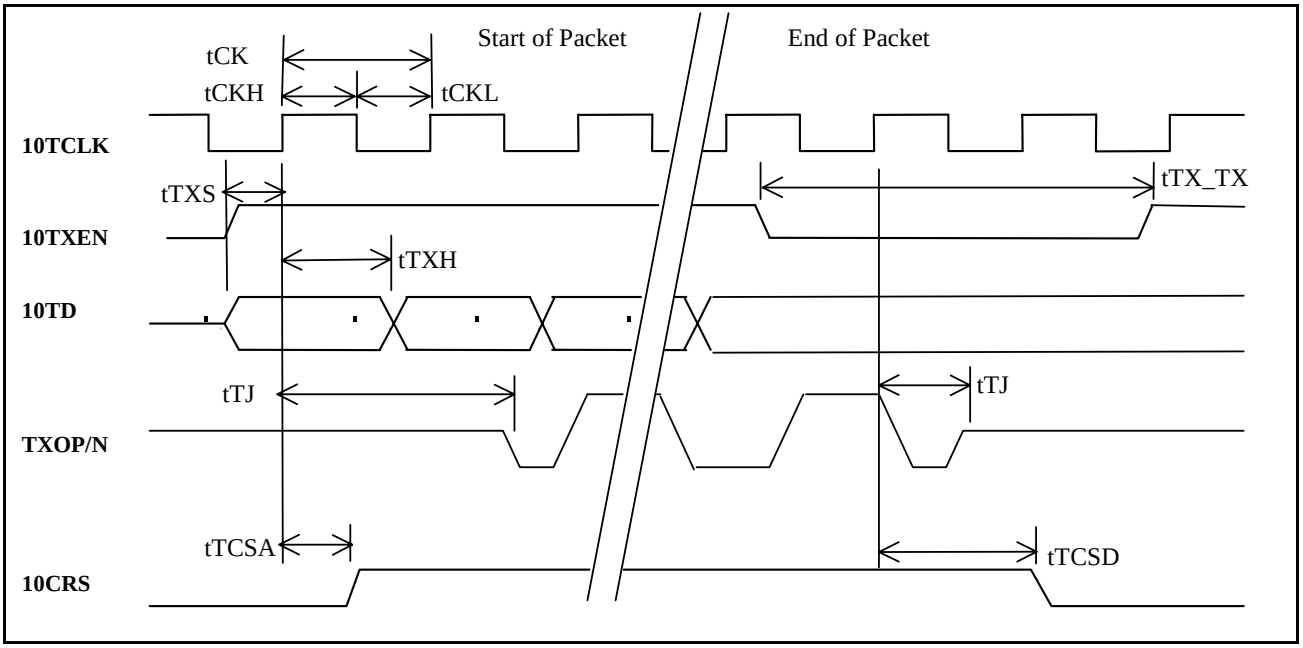

Figure 12: 10BASE-T 7-WireTransmit Timing

10BASE-T 7-WIRE RECEIVE SYSTEM TIMING

Table 46: 10BASE-T 7-Wire Receive System Timing

Parameter	SYM	Conditions	Min	Typ	Max	Units
10RCLK period	tCK		99.995	100.00	100.005	ns
10RCLK High period	tCKH		45.00	50.00	55.00	ns
10RCLK Low period	tCKL		45.00	50.00	55.00	ns
SOP to 10CRS	tRCSA		750	-	850	ns
10CRS to 10RD	tRDVA		750	-	850	ns
EOP to !10CRS	tRCSD		750	-	850	ns
RX Propagation Delay	tRDVD	From RXOP/N to 10RD	1500	-	1700	ns
10RD Setup	tRXS	From rising edge of 10RCLK	20	-	-	ns
10RD Hold	tRXH	From rising edge of 10RCLK	20	-	-	ns

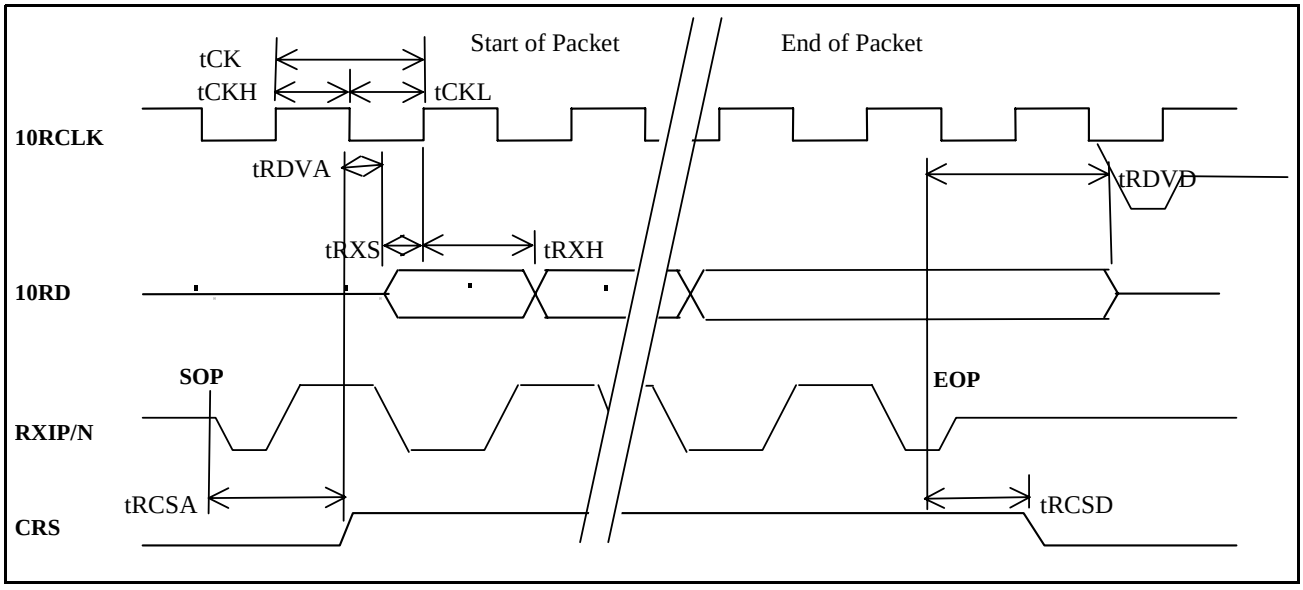

Figure 13: 10BASE-T 7-Wire Receive Timing

10BASE-T 7-WIRE COLLISION TIMING

Table 47: 10BASE-T 7-Wire Collision Timing

Parameter	SYM	Conditions	Min	Typ	Max	Units
Collision to 10COL	tCCA		80	-	150	ns
!Collision to !10COL	tCCD		125	-	185	ns

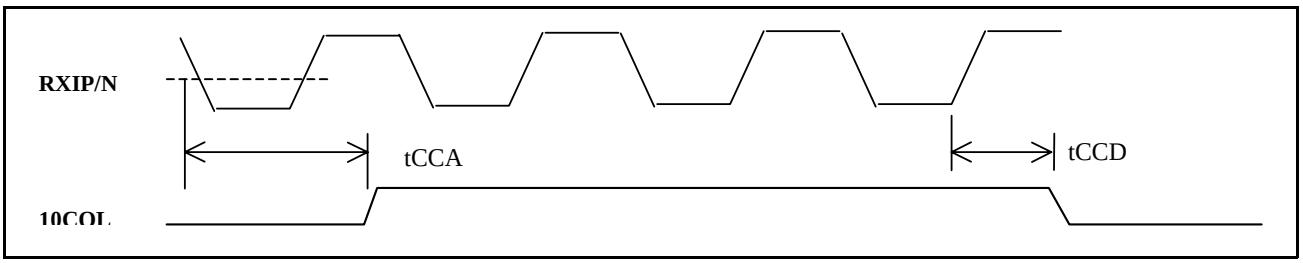

Figure 14: 10BASE-T 7-Wire Collision Timing

RECOMMENDED BOARD CIRCUITRY

TX APPLICATION TERMINATION

Please contact Altima Communications Inc. for the latest component value recommendation.

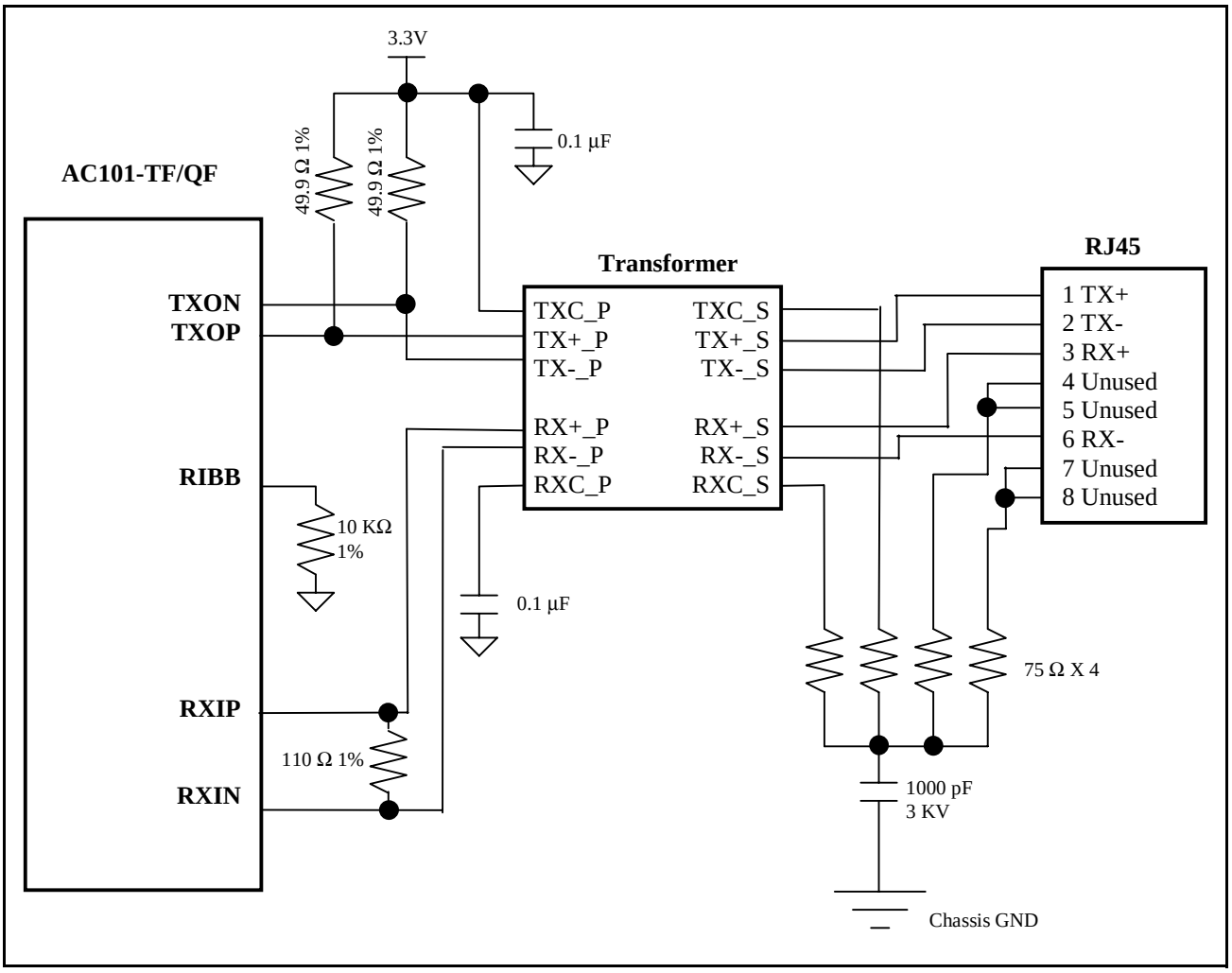

Figure 15: TX Application Termination Circuit

FX APPLICATION TERMINATION

Please contact Altima Communications Inc. for the latest component value recommendation.

To enable the FX mode, FX_DIS pin (see ”LED Indicators Pins” on page 16) must be pulled low by a 1 kilohm resistor.

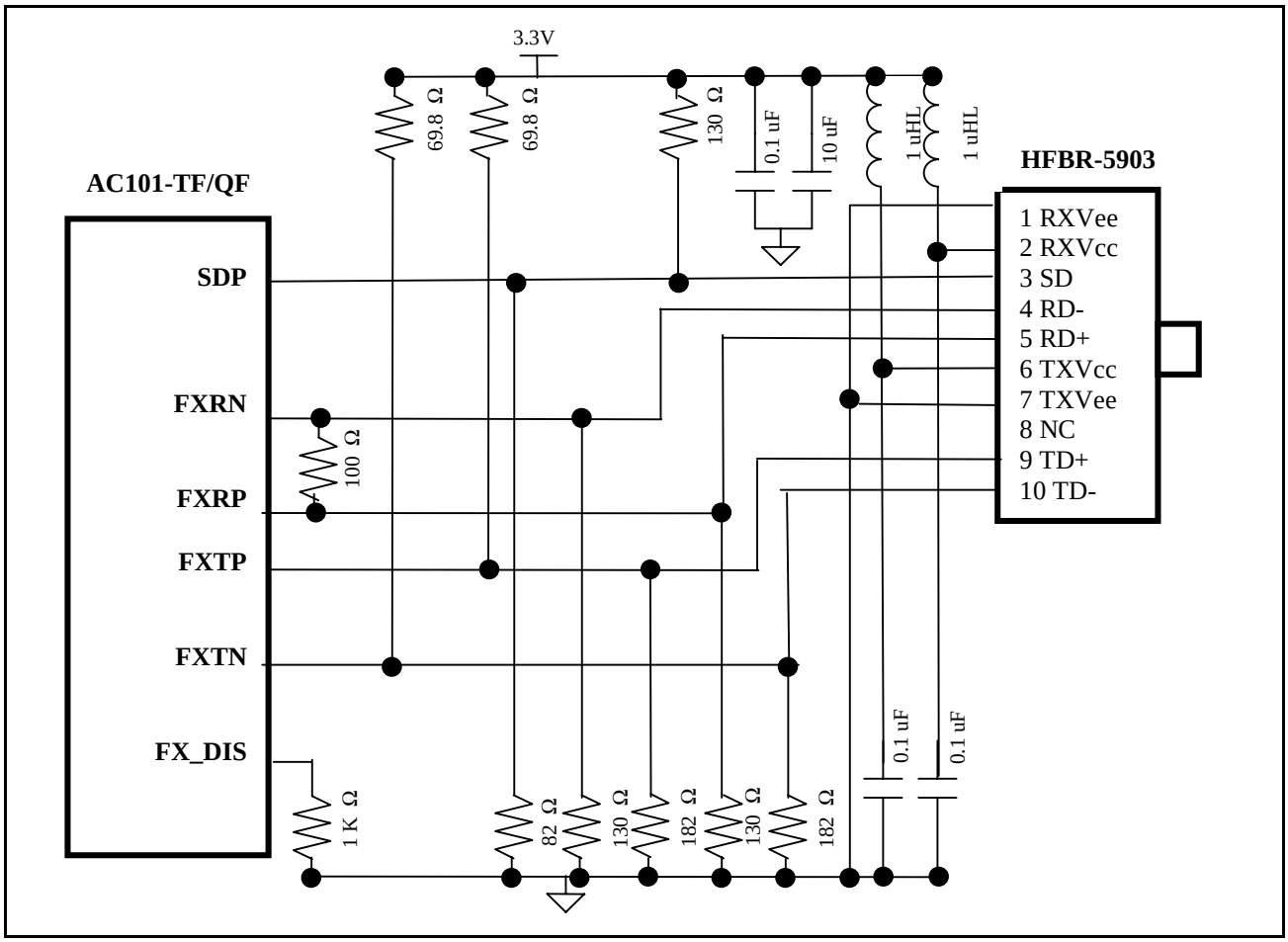

Figure 16: FX Application Termination Circuit

Power and Ground Filtering for AC101QF

Please contact Altima Communications Inc. for the latest component value recommendation.

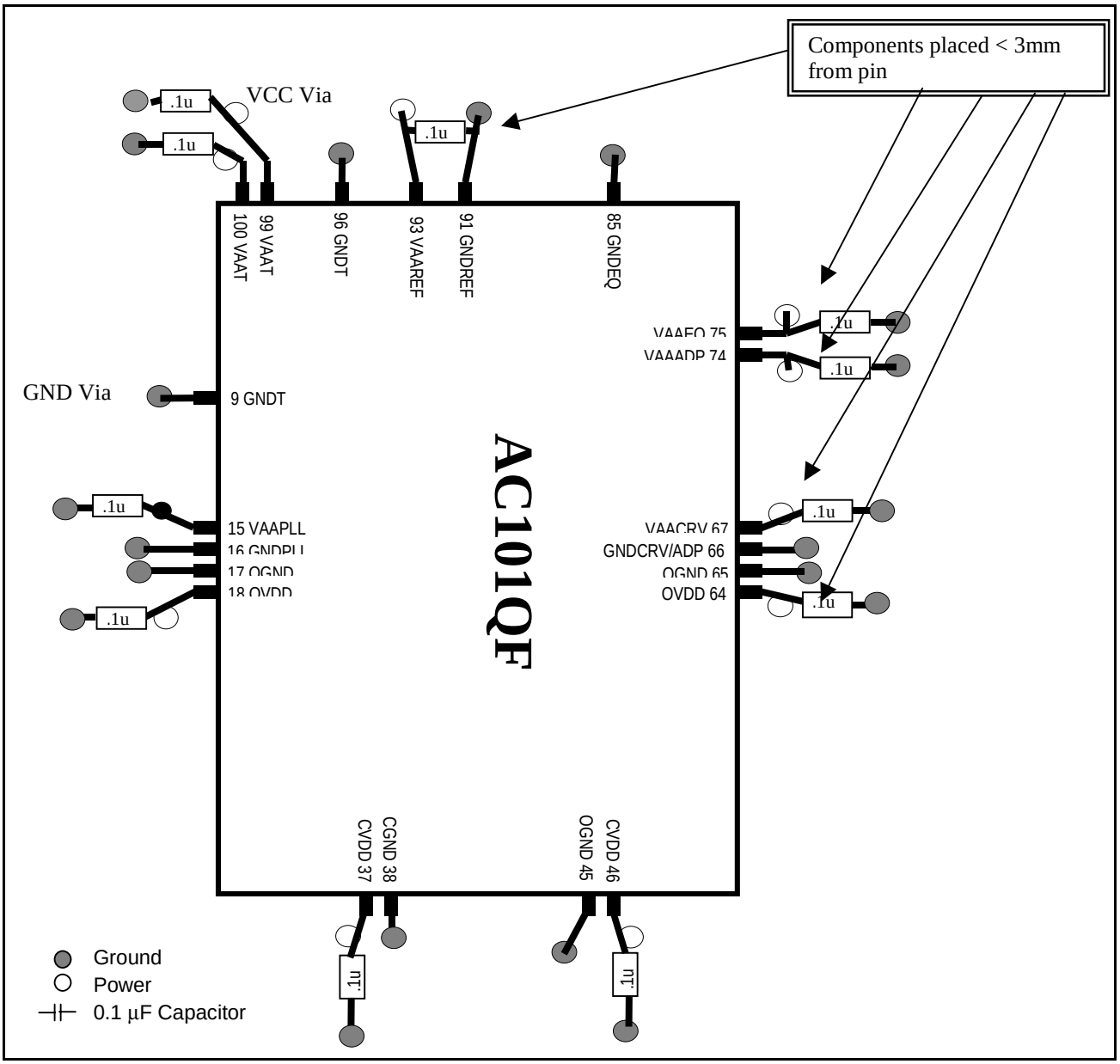

Figure 17: Power and Ground Filtering for the AC101QF

POWER AND GROUND FILTERING FOR AC101TF

Please contact Altima Communications Inc. for the latest component value recommendations.

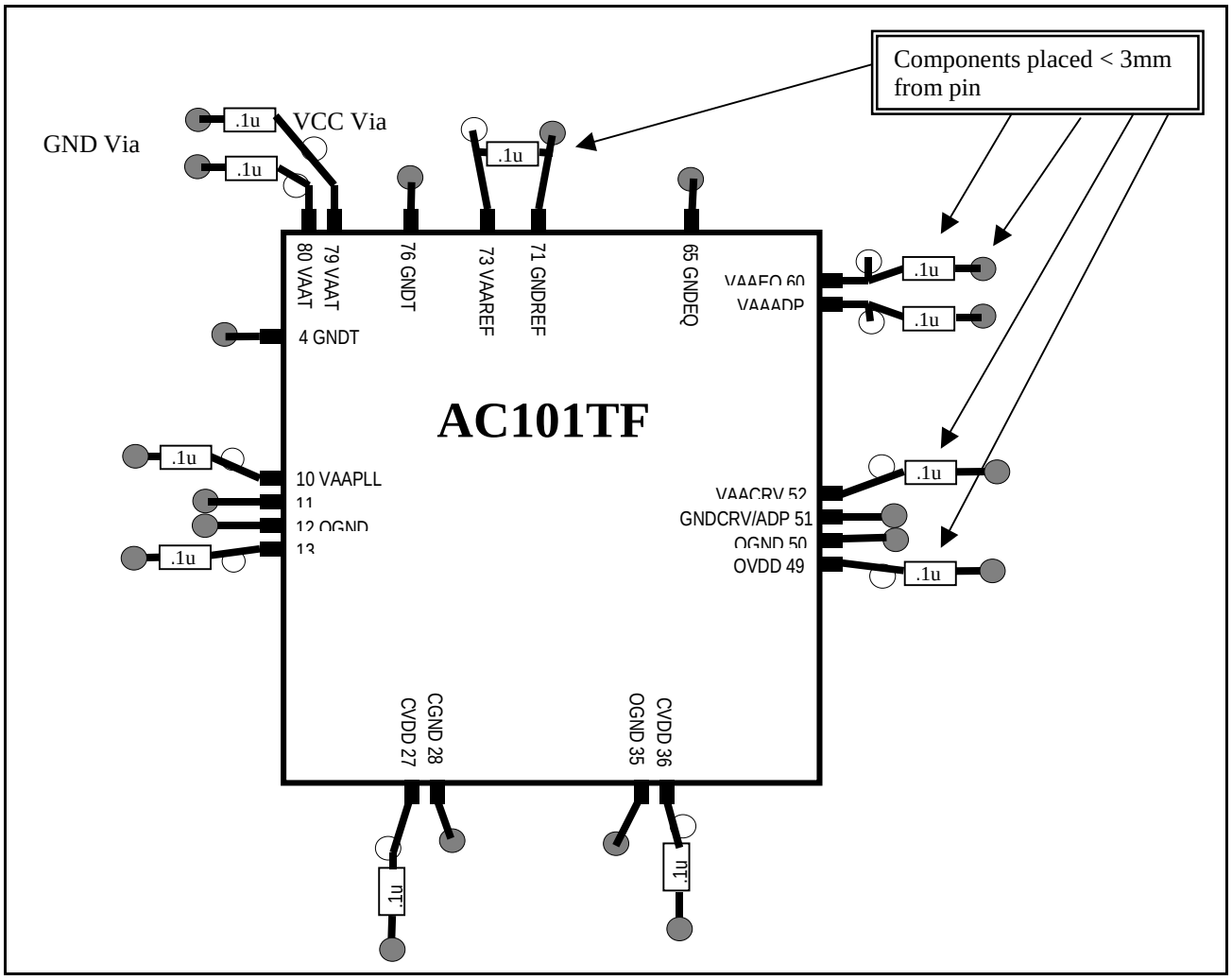

Figure 18: Power and Ground Filtering for the AC101TF

Section 7: Mechanical Information

PACKAGE DIMENSIONS FOR AC101QF (100 PIN PQFP)

Table 48: Quad Flat Pack Outline: 20 x 14 mm

N	A	A1	A2	B	D	D1	E	E1	e	L	L1
100	3.40 Max	0.25 Min	2.70 ± 0.2	0.3 ± 0.1	23.20± 0.25	20.00± 0.10	17.20± 0.25	14.00± 0.10	0.65	0.88 ± 0.2	1.60 ± 0.12

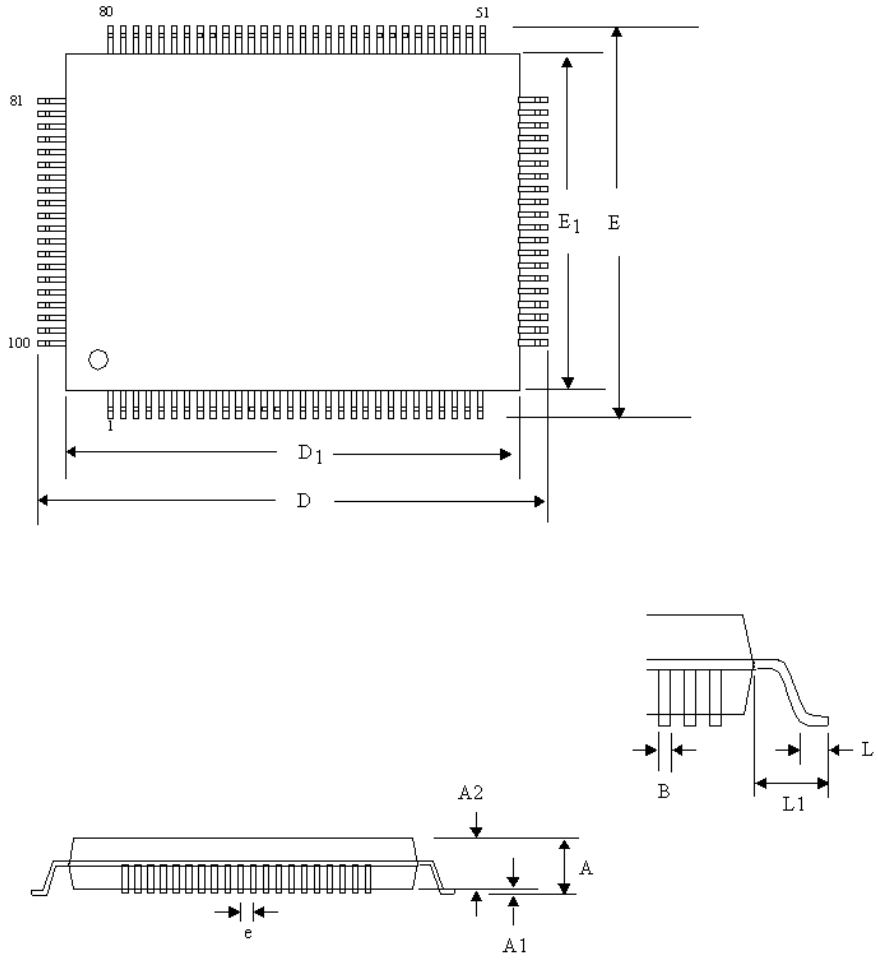

Figure 19: Package Dimensions for AC101QF (100 pin PQFP)

PACKAGE DIMENSIONS FOR AC101TF (80 PIN TQFP)

Table 49: Quad Flat Pack Outline: 12 x 12 mm

N	A	A1	A2	B	D	D1	E	E1	e	L	L1
80	1.20 Max	0.05 Min 0.15 Max	1.00 ± 0.05	0.22 ± 0.05	14.20± 0.25	12.00± 0.10	14.20± 0.25	12.00± 0.10	0.50	0.60 ± 0.15	1.00 ± 0.12

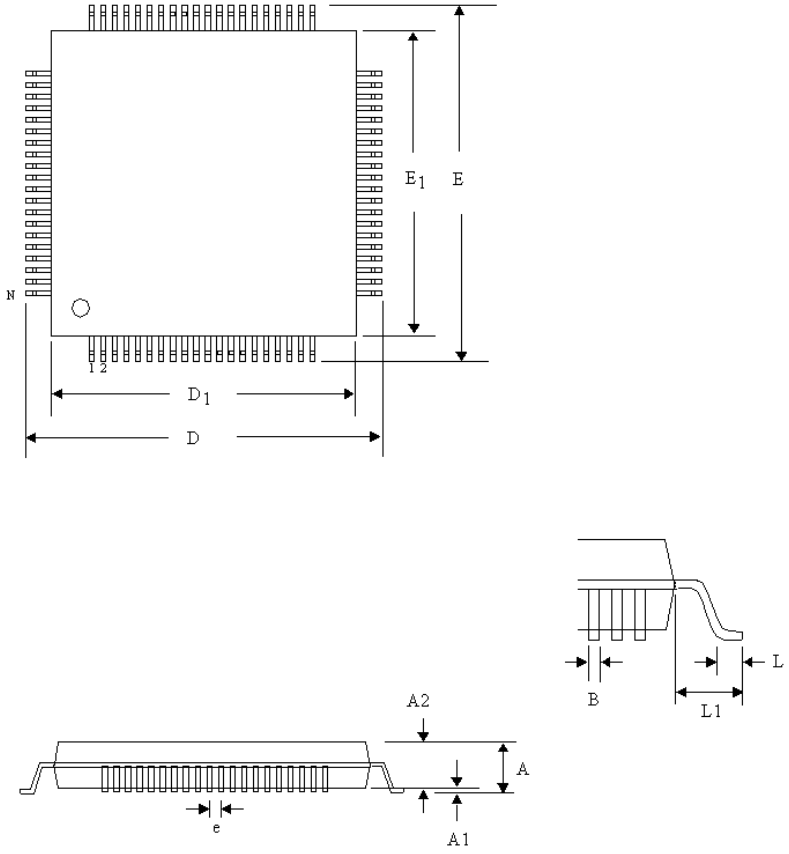

Figure 20: Package Dimensions for AC101TF (80 pin TQFP)

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