BROADCOM®

Data Sheet

BCM957452M4520C

Single-Port 1G/10G/25G/40G/50G Ethernet and Multi-Host PCI Express 3.0 x8 OCP 2.0 Mezzanine Card

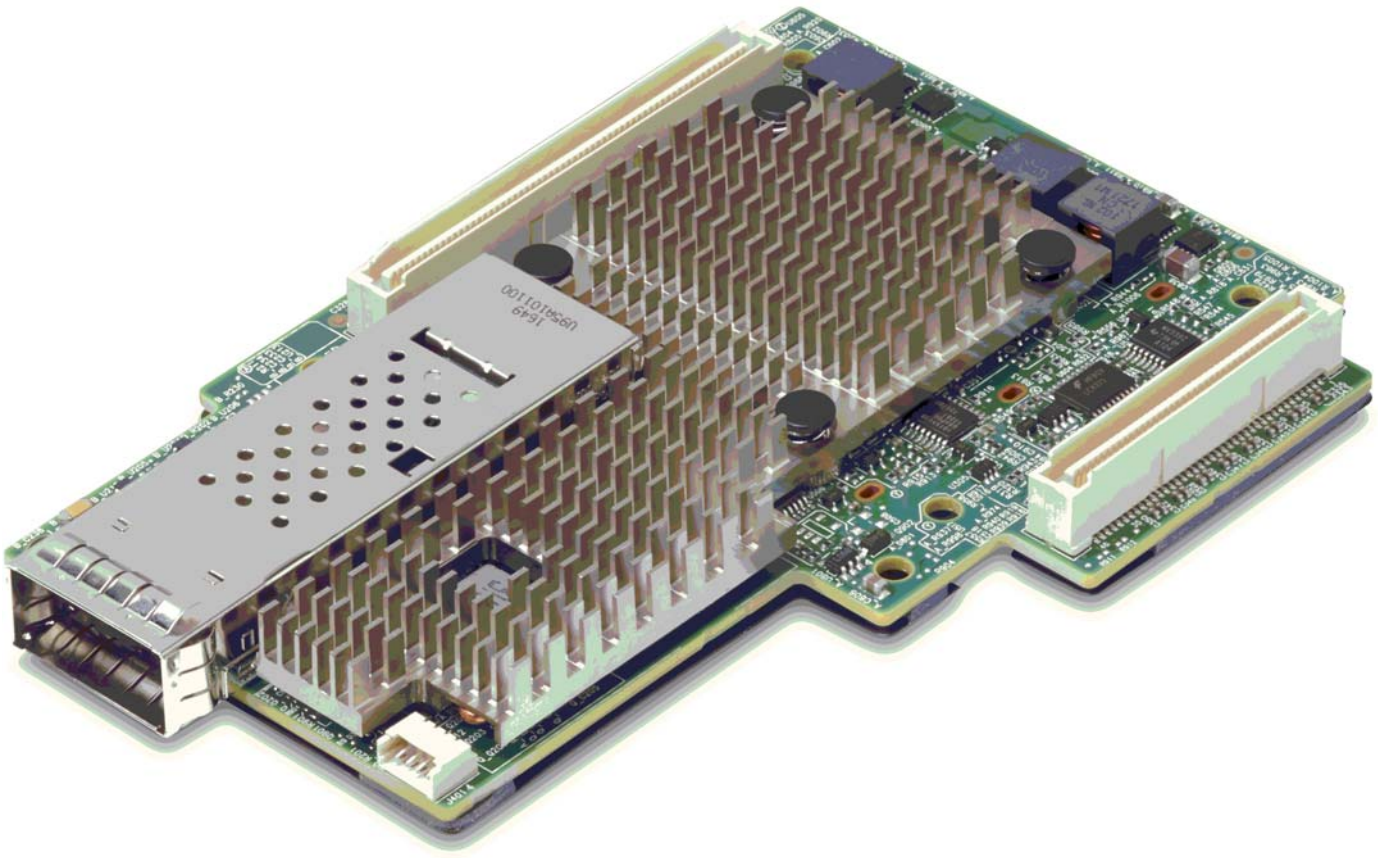
Overview

The Broadcom® BCM957452M4520C is a single-port 1G/10G/25G/40G/50G Ethernet, RoCE, SR-IOV, and multi-host PCI Express 3.0 x8 OCP mezzanine card designed to the Open Compute Project (OCP) mezzanine card specification with a QSFP28 network connector. The adapter is designed to the OCP Mezzanine v2.0 specification as a Type 2 adapter with the board outline adhering to the original v0.5 dimensions. The adapter supports both QSFP28/QSFP+ optical modules and copper direct-attach cables.

Features

- Single-port pluggable media interface, which may be equipped with 50 Gb/s or 40 Gb/s QSFP28/QSFP+ optical transceiver or with copper direct-attach cable.
- Fully compliant with the SFF-8665 standard.
- 8-lane PCI Express host interface that is designed to operate to the PCI Express v3.0 specifications. Support for up to four external hosts (for example, it has four PCIe endpoints) multiplexed through the MHB.
- SR-IOV with up to 1K virtual functions (VFs).
- RDMA over Converged Ethernet (RoCE).
- Function-Level Reset (FLR) support.
- TruFlow™ flow processing engine.
- Virtual Network Termination – XVXLAN, NVGRE, Geneve, GRE encap/decap.
- Switch acceleration.
- Tunnel-aware stateless offloads.
- DCB support: PFC, ETS, QCN, DCBx.
- TruManage™ integrated BMC.
- Network Controller Sideband Interface (NC-SI).
- SMBus 2.0.
- MCTP over SMBus.
- PCIe-based UART and KCS.
- Jumbo frames up to 9 KB.
- Advanced Congestion Avoidance.
- Multiqueue, NetQueue, and VMQ.
- IPv4 and IPv6 offloads.
- TCP, UDP, and IP checksum offloads.
- Large Send Offload (LSO).
- Large Receive Offload (LRO).
- TCP Segmentation Offload (TSO).
- Receive-side Scaling (RSS).
- Transmit-side Scaling (TSS).
- VLAN insertion/removal.
- Interrupt coalescing.
- Network boot – XPXE, UEFI.
- iSCSI boot.
- Wake-on-LAN (WOL).
- MSI and MSI.X.
- Conforms to the OCP Mezzanine Card Design Specification v2.0 Type 2.
- Single-port 50-Gigabit or 40-Gigabit Ethernet adapter for Open Compute Platform systems.

Figure 1: BCM957452M4520C OCP Mezzanine Card



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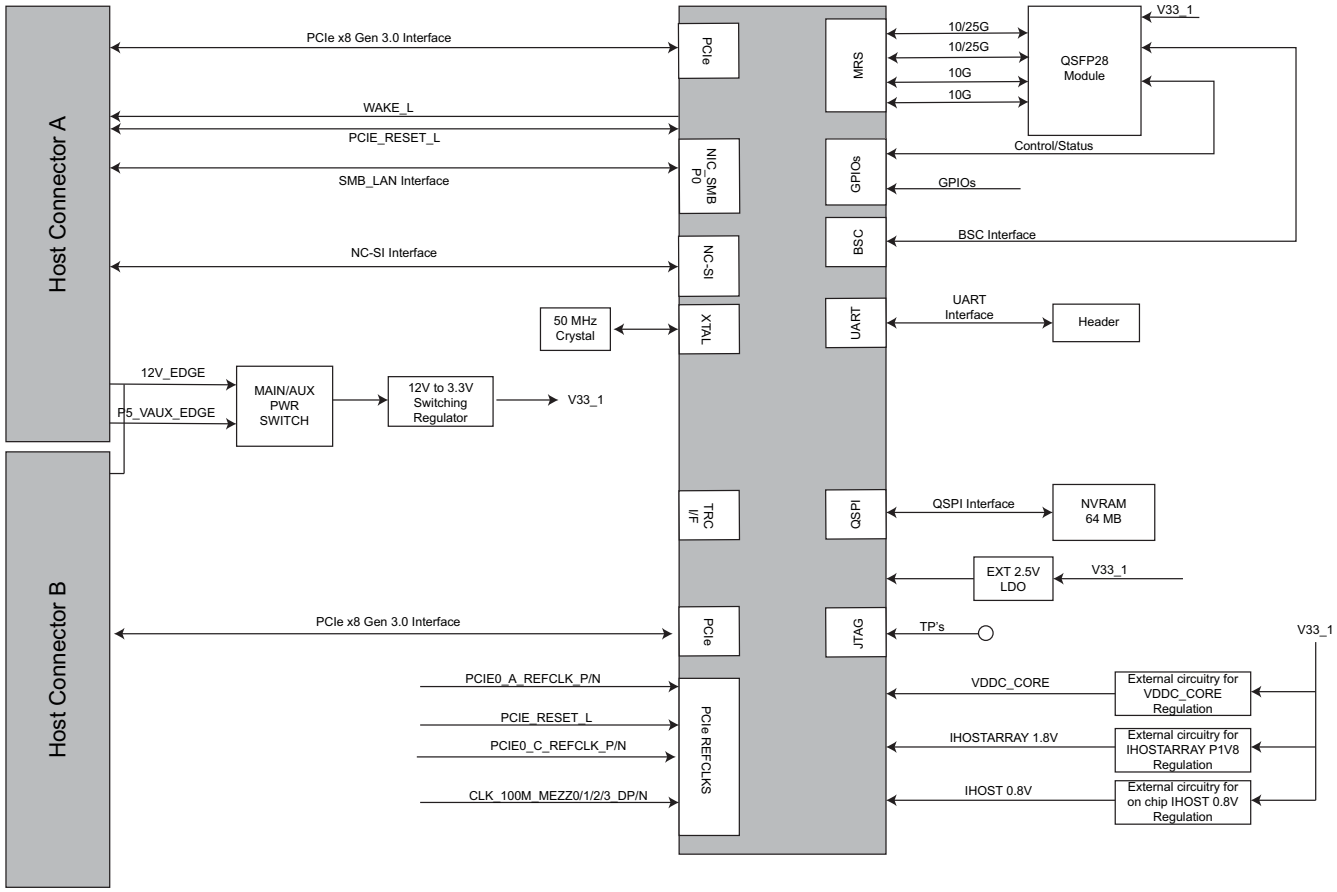
Chapter 1: Functional Description

Figure 2 shows the main functional blocks on the BCM957452M4520C OCP mezzanine card.

Figure 2: BCM957452M4520C Block Diagram



1.1 Host Interface Connectors

The BCM957452M4520C OCP mezzanine card interfaces with the system baseboard via two vertical-stacked card-to-card connectors. The PCIe bus, NC-SI bus, SMBus interface, various other sideband signals, and power are assigned to these two connectors. The pinout complies with that of Connector A and Connector B as described in the OCP Mezzanine Card 2.0 Design Specification. The following tables show the signal pinout for both connectors per the specification. Definitions of the signals at this connector are provided in the OCP Mezzanine Card Specification.

Table 1: Connector A

Pin	Signal
A1	MEZZ_PRSNTA1_N/BASEBOARD_A_ID
A2	P5V_AUX
A3	P5V_AUX
A4	P5V_AUX
A5	GND
A6	GND
A7	P3V3_AUX
A8	GND
A9	GND
A10	P3V3
A11	P3V3
A12	P3V3
A13	P3V3
A14	NCSI_CRSDV
A15	NCSI_RCLK
A16	NCSI_TXEN
A17	PERST_N0
A18	MEZZ_SMCLK
A19	MEZZ_SMDATA
A20	GND
A21	GND
A22	NCSI_RXD0
A23	NCSI_RXD1
A24	GND
A25	GND
A26	CLK_100M_MEZZ1_DP
A27	CLK_100M_MEZZ1_DN
A28	GND
A29	GND
A30	MEZZ_RX_DP<0>
A31	MEZZ_RX_DN<0>
A32	GND
A33	GND
A34	MEZZ_RX_DP<1>
A35	MEZZ_RX_DN<1>
A36	GND

Pin	Signal
A37	GND
A38	MEZZ_RX_DP<2>
A39	MEZZ_RX_DN<2>
A40	GND
A41	GND
A42	MEZZ_RX_DP<3>
A43	MEZZ_RX_DN<3>
A44	GND
A45	GND
A46	MEZZ_RX_DP<4>
A47	MEZZ_RX_DN<4>
A48	GND
A49	GND
A50	MEZZ_RX_DP<5>
A51	MEZZ_RX_DN<5>
A52	GND
A53	GND
A54	MEZZ_RX_DP<6>
A55	MEZZ_RX_DN<6>
A56	GND
A57	GND
A58	MEZZ_RX_DP<7>
A59	MEZZ_RX_DN<7>
A60	GND
A61	P12V_AUX/P12V
A62	P12V_AUX/P12V
A63	P12V_AUX /P12V
A64	GND
A65	GND
A66	P3V3_AUX
A67	GND
A68	GND
A69	P3V3
A70	P3V3
A71	P3V3
A72	P3V3

Pin	Signal
A73	GND
A74	LAN_3V3STB_ALERT_N
A75	SMB_LAN_3V3STB_CLK
A76	SMB_LAN_3V3STB_DAT
A77	PCIE_WAKE_N
A78	NCSI_RXER
A79	GND
A80	NCSI_TXD0
A81	NCSI_TXD1
A82	GND
A83	GND
A84	CLK_100M_MEZZ0_DP
A85	CLK_100M_MEZZ0_DN
A86	GND
A87	GND
A88	MEZZ_TX_DP_C<0>
A89	MEZZ_TX_DN_C<0>
A90	GND
A91	GND
A92	MEZZ_TX_DP_C<1>
A93	MEZZ_TX_DN_C<1>
A94	GND
A95	GND
A96	MEZZ_TX_DP_C<2>
A97	MEZZ_TX_DN_C<2>
A98	GND
A99	GND
A100	MEZZ_TX_DP_C<3>
A101	MEZZ_TX_DN_C<3>
A102	GND
A103	GND
A104	MEZZ_TX_DP_C<4>
A105	MEZZ_TX_DN_C<4>
A106	GND
A107	GND
A108	MEZZ_TX_DP_C<5>
A109	MEZZ_TX_DN_C<5>
A110	GND
A111	GND
A112	MEZZ_TX_DP_C<6>
A113	MEZZ_TX_DN_C<6>
A114	GND
A115	GND
A116	MEZZ_TX_DP_C<7>

Pin	Signal
A117	MEZZ_TX_DN_C<7>
A118	GND
A119	GND
A120	MEZZ_PRSNTA2_N

Table 2: Connector B

Pin	Signal
B1	MEZZ_PRSNTB1_N/BASEBOARD_B_ID
B2	GND
B3	MEZZ_RX_DP<8>
B4	MEZZ_RX_DN<8>
B5	GND
B6	GND
B7	MEZZ_RX_DP<9>
B8	MEZZ_RX_DN<9>
B9	GND
B10	GND
B11	MEZZ_RX_DP<10>
B12	MEZZ_RX_DN<10>
B13	GND
B14	GND
B15	MEZZ_RX_DP<11>
B16	MEZZ_RX_DN<11>
B17	GND
B18	GND
B19	MEZZ_RX_DP<12>
B20	MEZZ_RX_DN<12>
B21	GND
B22	GND
B23	MEZZ_RX_DP<13>
B24	MEZZ_RX_DN<13>
B25	GND
B26	GND
B27	MEZZ_RX_DP<14>
B28	MEZZ_RX_DN<14>
B29	GND
B30	GND
B31	MEZZ_RX_DP<15>
B32	MEZZ_RX_DN<15>
B33	GND
B34	GND
B35	CLK_100M_MEZZ2_DP
B36	CLK_100M_MEZZ2_DN
B37	GND
B38	PERST_N1
B39	PERST_N2
B40	PERST_N3
B41	P12V_AUX/P12V
B42	P12V_AUX/P12V
B43	RSVD

Pin	Signal
B44	GND
B45	MEZZ_TX_DP<8>
B46	MEZZ_TX_DN<8>
B47	GND
B48	GND
B49	MEZZ_TX_DP<9>
B50	MEZZ_TX_DN<9>
B51	GND
B52	GND
B53	MEZZ_TX_DP<10>
B54	MEZZ_TX_DN<10>
B55	GND
B56	GND
B57	MEZZ_TX_DP<11>
B58	MEZZ_TX_DN<11>
B59	GND
B60	GND
B61	MEZZ_TX_DP<12>
B62	MEZZ_TX_DN<12>
B63	GND
B64	GND
B65	MEZZ_TX_DP<13>
B66	MEZZ_TX_DN<13>
B67	GND
B68	GND
B69	MEZZ_TX_DP<14>
B70	MEZZ_TX_DN<14>
B71	GND
B72	GND
B73	MEZZ_TX_DP<15>
B74	MEZZ_TX_DN<15>
B75	GND
B76	GND
B77	CLK_100M_MEZZ3_DP
B78	CLK_100M_MEZZ3_DN
B79	GND
B80	MEZZ_PRSNTB2_N

1.2 BCM57452

The BCM57452 Ethernet controller is configured as a single-port 50 Gb/s MAC with integrated QSFP28 optical interface to the line side and x8 PCI Express v3.0 interface to the system host.

1.3 Clock Requirements

The BCM57452 has an integrated differential oscillator circuit that operates from an external 50 MHz crystal.

1.4 PCI Express Interface

PCIe is a high-bandwidth serial bus providing a low pin-count interface as an alternative to parallel PCI. It is part of the Host Interface Connector. The BCM57452 complies with the PCI Express Base Specification Revision 3.0, and supports an eight-lane PCIe v3.0 interface via the host interface connector. The BCM57452 supports up to four external hosts (that is, it has four PCIe endpoints) multiplexed through the Multi Host Bridge (MHB).

1.5 NC-SI Interface

The BCM57452 Ethernet controller supports the NC-SI specification, version 1.1.0. The NC-SI provides a standardized interface between the system BMC and the integrated NC-SI module of the BCM57452.

1.6 SMBus Interface

The BCM57452 Ethernet controller SMB interface supports serial communications between the BCM57452 and the system. The interface allows the Ethernet Controller to act as an SMBus master or a slave device.

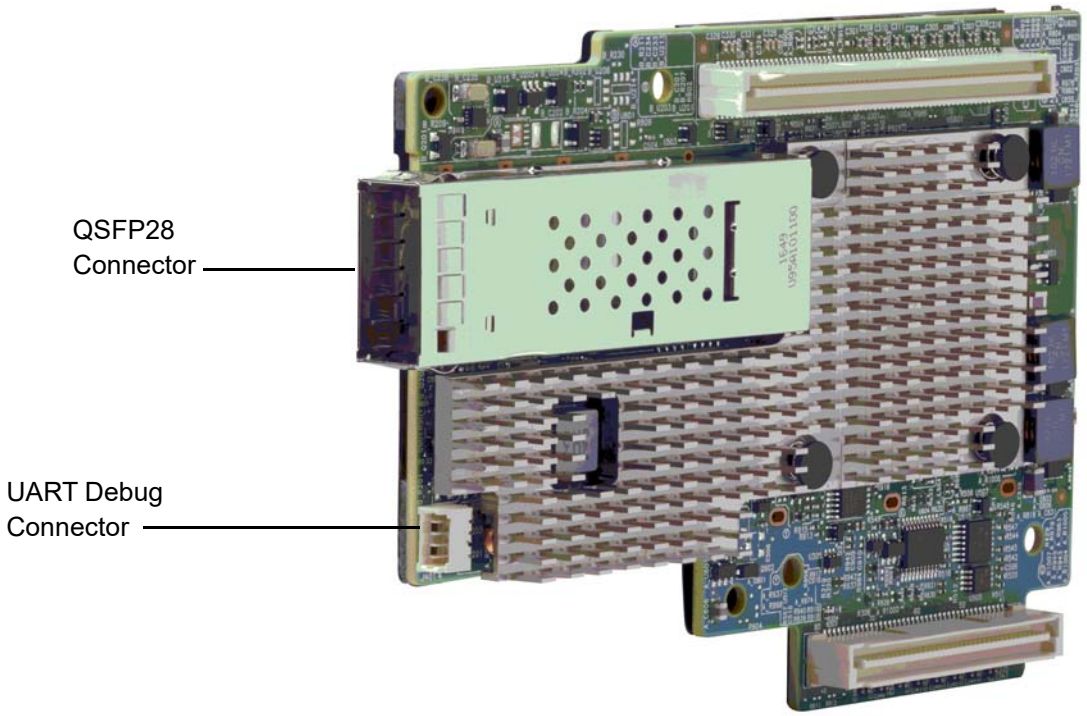
1.7 UART Interface

The BCM57452 Ethernet controller has an integrated UART interface that supports external access to its registers. The UART signals are brought out to the 4-pin header for connecting a remote access host. The UART debug connector is placed near the I/O connector to be accessible from outside, for ease of in-system debug.

Table 3: UART Connector Pinout

Pin	Signal
1	UART_TXD
2	UART_RXD
3	V33
4	GND

Figure 3: UART Debug Connector



1.8 Non-volatile RAM

The BCM57452 ethernet controller requires a non-volatile serial flash memory (NVRAM) to store the device firmware, PCI configuration space settings (for example, device ID, vendor ID), MAC address, and so on. After power-up, the firmware is downloaded into the device memory and executed by the on-chip processor. A 64 Mb flash is recommended for NVRAM.

1.9 Heat Sink

The passive heat sink is attached to the Ethernet controller using four spring-loaded push pins that insert into four mounting holes.

To prevent damage to the Ethernet Controller in the event of a missing heat sink, the mezzanine card is not allowed to power up. However, the FRU remains accessible.

1.10 DC/DC Regulators

The on-board voltage regulators use the 12V edge main power and 5V auxiliary supply from the host interface connector to derive the necessary power rails for different circuits and components on the board.

1.11 Power Supplies

All power is derived from the mezzanine card host interface connector 12V/5V supply pins. These voltage supply pins feed on-board regulators that provide the necessary power to the various components on the card. The mezzanine card has switching power supplies that power the card's various power rails.

1.12 LED Functions and Locations

The QSFP28 port supports two LEDs to indicate traffic activities and link speed. The LEDs are visible on the bottom side as shown in Figure 4 on page 11. Their locations and form factors conform to the OCP mezzanine card specification.

Figure 4: Activity and Link LED Locations

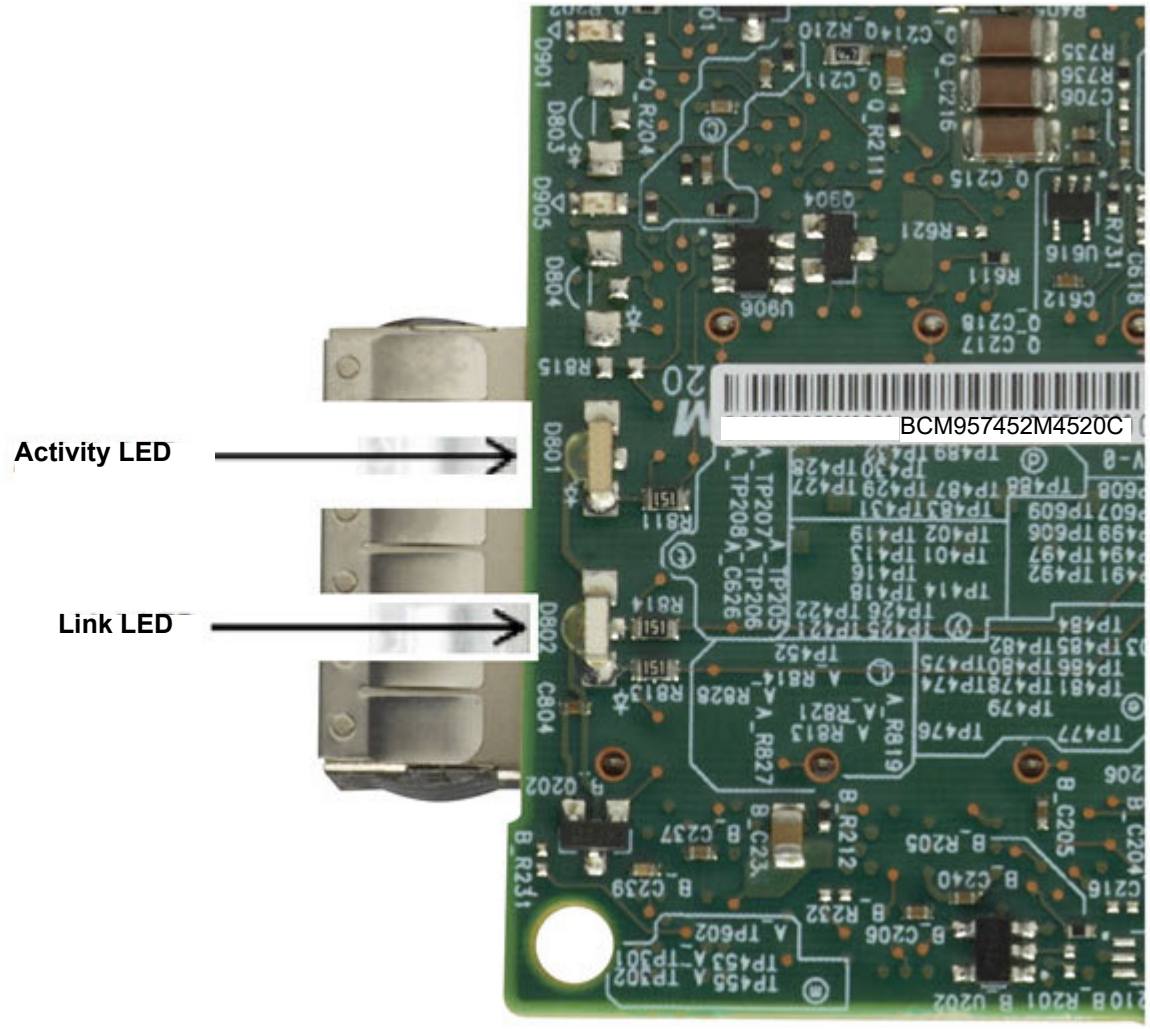


Table 4: LED Functions

NVRAM Manufacturer	Device	Mbit
Activity	Off	No activity
	Green blinking	Traffic flowing activity
Link	Off	No link
	Green	50G or 40G
	Yellow	25G or 10G

Chapter 2: Regulatory and Safety Approvals

The following sections detail the regulatory, safety, electromagnetic compatibility (EMC), and electrostatic discharge (ESD) compliance for the BCM957452M4520C OCP mezzanine card.

2.1 Regulatory

Table 5: Regulatory Approvals

Item	Applicable Standard	Approval (A)/Certificate (C)
CE/European Union	EN 62368-1:2014	CB report and certificate
UL/USA	IEC 62368-1 (ed. 2)	CB report and certificate

2.2 Safety

Table 6: Safety Approvals

Country	Certification Type/Standard	Compliance
International	CB Scheme ICES 003—Digital Device UL 1977 (connector safety) UL 796 (PCB wiring safety) UL 94 (flammability of parts)	Yes

2.3 Electromagnetic Compatibility (EMC)

Table 7: Electromagnetic Compatibility

Standard/Country	Certification Type	Compliance
CE/European Union	EN 55032:2012/AC:2013 Class A EN 55024:2010 EN 61000-3-2:2014 EN 61000-3-3:2013	CE report and CE DoC
FCC/USA	CFR47 Part 15 Subpart B Class A	FCC/IC DoC and EMC report referencing FCC and IC standards
IC/Canada	ICES-003 Class A	FCC/IC DoC and report referencing FCC and IC standards
ACA/Australia, New Zealand	AS/NZS CISPR 22:2009 +A1:2010	ACA certificate RCM mark
BSMI/Taiwan	CNS 13438 (2006) Class A	BSMI certificate
BSMI/Taiwan	CNS 15663	BSMI certificate/RoHS table
MIC/South Korea	KN32 Class A KN35	Korea certificate R Mark
VCCI/Japan	VCCI V-3 (2015-04)	Copy of VCCI online certificate

2.4 Electrostatic Discharge (ESD) Compliance

Table 8: ESD Compliance Summary

Standard	Certification Type	Compliance
EN 55024:2010 (EN 61000-4-2)	Air/Direct discharge	Yes

2.5 FCC Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Consult the dealer or an experienced radio/TV technician for help.

NOTE: Changes or modifications not expressly approved by the manufacture responsible for compliance could void the user's authority to operate the equipment.

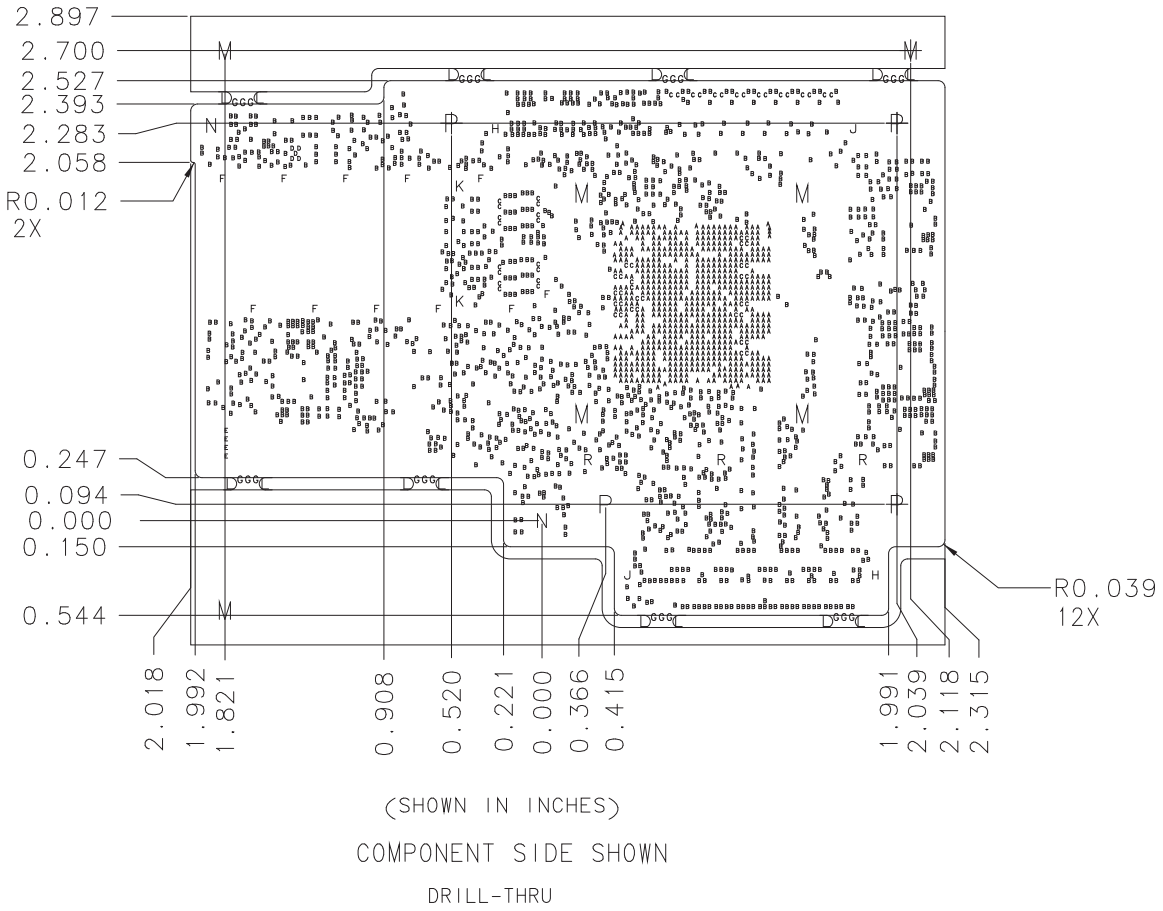
Chapter 3: Physical and Environmental Specifications

This section outlines the mechanicals of the BCM957452M4520C OCP mezzanine card as well as the environmental specifications.

3.1 Board Physical Dimensions

The BCM957452M4520C board dimensions are shown in Figure 5. The dimensions are in inches with a tolerance of ±0.005.

Figure 5: Board Physical Dimensions



3.2 Environment Specifications

The mezzanine card meets the same environmental requirements specified in the OCP systems.

Table 9: Environment Specifications

Parameter	Condition
Storage temperature	–40°C to +70°C

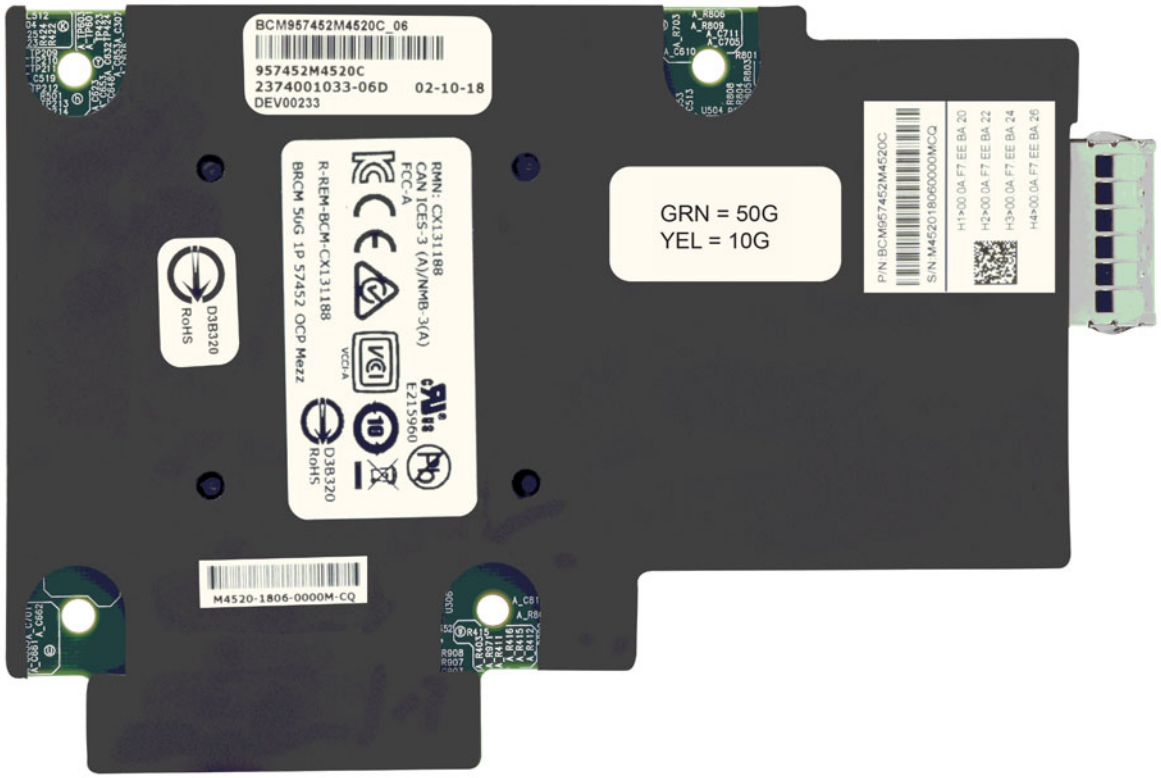
Table 9: Environment Specifications (Continued)

Parameter	Condition
Storage humidity	5% to 95% non-condensing
Vibration and shock	IEC78-2-(*) and IEC721-3-(*)

3.3 Label Information

This section provides the label information of the BCM957452M4520C OCP mezzanine card. Figure 6 outlines the label and corresponding locations.

Figure 6: Label Overview



3.3.1 MAC Address Label

In the example shown in Figure 7, the BCM957452M4520C is the part number with a 1D bar code for Broadcom serial number M452018060000MCQ. The 2D bar code is the MAC address. For example, 00.0A.F7.EE.BA.20 is the MAC address of host network interface for the base host (H1) and the MAC addresses of the subsequent hosts (H2, H3, and H4) are shown in order below.

Figure 7: MAC Address Label

Chapter 4: Ordering Information

Table 10: Ordering Information

Part Number	Description
BCM957452M4520C	Single-Port 1G/10G/25G/40G/50G Ethernet PCI Express 3.0 x8 OCP Mezzanine Card; RoHS-compliant

Revision History

957452M4520C-DS106; October 29, 2019

Updated:

- BCM957452M4520C Block Diagram – Updated block diagram.
- LED Functions – Updated link status.
- Label Overview – Updated link color status.
- Ordering Information – Updated part description.

957452M4520C-DS105; July 18, 2018

Updated:

- Host Interface Connectors

957452M4520C-DS104; June 6, 2018

Updated:

- Figure 1, BCM957452M4520C OCP Mezzanine Card
- Figure 4, Activity and Link LED Locations
- Table 4, LED Functions
- Figure 6, Label Overview
- MAC Address Label

957452M4520C-DS103; April 10, 2018

Updated:

- Figure 5, Board Physical Dimensions

957452M4520C-DS102; March 14, 2018

Updated:

- Figure 1, BCM957452M4520C OCP Mezzanine Card
- Figure 3, UART Debug Connector
- Board Physical Dimensions
- Figure 6, Label Overview
- MAC Address Label

957452M4520C-DS101; December 27, 2017

Updated:

- Section 2: “Regulatory and Safety Approvals,” on page 13

957452M4520C-DS100; January 31, 2017

Initial release.