

BCM89083

Automotive Ethernet Low-Latency Camera MCU

Overview

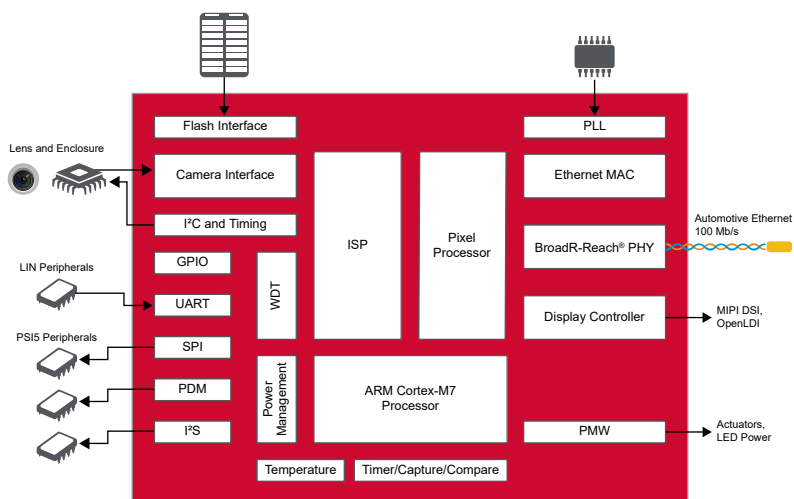
The Broadcom® BCM89083 is a fully integrated BroadR-Reach® camera endpoint microcontroller for automotive rear-view camera and side-view camera applications. The Arm Cortex-M7 supports low-latency interrupt processing through the use of Real-time Operating System (RTOS), runs an Ethernet Audio Video Broadcast (AVB) stack, and processes the housekeeping tasks for the various peripherals. The enhanced cache architecture provides increased system performance.

The CMOS image sensor interface supports two-lane MIPI CSI-2 interfaces. The ISP supports black-level adjustment, lens-shading correction, 2D adaptive noise filtering, defective pixel compensation, white-balance adjustment, color-crosstalk compensation, edge sharpening, demosaicing, color correction and gamma correction, falsecolor suppression, hue and saturation control, and adaptive local tone mapping in the hardware pipeline.

The display controller can directly drive two- or four-lane OpenLDI and MIPI DSI displays and can be connected to external LVDS serializers. A graphics plane overlay with alpha blending allows superimposing of driving trajectories, gauges, or other visual elements before encoding the video and streaming it over the BroadR-Reach Ethernet.

The device also supports IEEE 802.1as and IEEE 802.1Q AVB bridging standards for clock synchronization and video streaming. The BCM89083 integrates several I/O controllers, including SPI, QSPI, I2S/TDM, I2C, UART/LIN, PDM, and GPIO. The BCM89083 also contains on-chip switching regulators and FETs to simplify power-supply design.

Camera Platform Solution Functional Block Diagram



Key Features

- Integrated BroadR-Reach 100BASE-T1 PHY
- AECQ-100 qualified
- Flexible camera interface (MIPI CSI-2) to a wide range of camera sensors
- Flexible display interfaces (OpenLDI and MIPI DSI) to a wide range of displays and LVDS serializers
- High-performance, programmable SIMD Pixel processor/DSP cores for H264 Video encoding and implementation of video algorithms
- Low-latency encoder for encoding and transmission of 1.3-MP resolution video at 30 fps
- Integrated HDR-capable line-based ISP further reduces BOM cost
- Arm Cortex-M7 core running at 400 MHz
- Integrated 1.0V voltage regulator reduces the need for expensive external power management circuitry
- Support for gPTP time synchronization per IEEE 1588 and IEEE 1722a
- Low power and space optimized solution for rear view and surround view camera applications
- 7 mm x 7 mm, 81-pin FBGA package

Applications

- Automotive rear view camera
- Automotive surround view camera
- Automotive displays